Surface Treatments to Reduce Leakage Current in Homojunction In$_{0.53}$Ga$_{0.47}$As PIN Diodes for TFET Applications

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Surface Treatments to Reduce Leakage Current in Homojunction $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ PIN Diodes for TFET Applications

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Rochester Institute of Technology
Surface Treatments to Reduce Leakage Current in Homojunction In$_{0.53}$Ga$_{0.47}$As PIN Diodes for TFET Applications

Abhinav Gaur

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In Partial Fulfillment
Of the Requirements for the Degree of
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In
Microelectronic Engineering

Approved By:

Prof. Dr. Sean Rommel Advisor

Prof. Dr. Santosh Kurinec Committee Member

Prof. Dr. Karl Hirschman Committee Member

Rochester Institute of Technology
September 25, 2014
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Abhinav Gaur

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I would like to express my most sincere gratitude to my advisor and mentor, Prof. Sean L. Rommel for providing me the opportunity to work on this project. Being an international student, a lot of legal hurdles had to be overcome in getting me access to the group’s work. His determination to get me on board strengthened my resolve to continue this research further. It was a great experience learning from and working with him.

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I would like to thank my friends for making my time in Rochester enjoyable. I am deeply indebted to my family and friends back home for their love and unwavering support.
To my biggest pillars of support, my grandparents,

Jagdishwar Nath and Rajesh Gaur.
Abstract

In the field of low-power electronics, Tunnel field-effect transistors (TFETs) are gaining momentum due to aggressive voltage scaling. To enable scaling of power supply while maintaining a high $I_{on}$, a steep subthreshold slope and low $I_0$ are required. A TFET operates as a gated PIN diode under reverse bias with the intrinsic region as the channel.

This study focuses on minimizing $I_0$ in a III-V homojunction PIN diode. $I_0$ or leakage current is the current flowing in a PIN diode under reverse bias, that forms the off-state current ($V_{gate} = 0 \, \text{V}$) in a TFET.

![Figure 1: Overview of the impact of different surface treatments on $I_0$.](image)

Various surface treatment combinations were performed to study surface leakage, of which, BCB and HCl were the most effective passivation and clean, respectively. For the first time, in this study, electrical characterization of sub-micron PIN diodes was performed.
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<th>Term</th>
<th>Description</th>
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<tr>
<td>$C$</td>
<td>Load capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C'_D$</td>
<td>Depletion region capacitance per unit area</td>
<td>F/cm²</td>
</tr>
<tr>
<td>$C'_{ox}$</td>
<td>Oxide capacitance per unit area</td>
<td>F/cm²</td>
</tr>
<tr>
<td>$E_c/E_v$</td>
<td>Energy at the conduction/valence band edge</td>
<td>eV</td>
</tr>
<tr>
<td>$E_F$</td>
<td>Fermi level</td>
<td>eV</td>
</tr>
<tr>
<td>$E_g$</td>
<td>Energy band gap</td>
<td>eV</td>
</tr>
<tr>
<td>$f$</td>
<td>Frequency of operation</td>
<td>Hz</td>
</tr>
<tr>
<td>$I_{DS}$</td>
<td>Drain to Source current in a MOSFET</td>
<td>A/µm</td>
</tr>
<tr>
<td>$I_0$</td>
<td>Off-state current in a transistor</td>
<td>A/µm</td>
</tr>
<tr>
<td>$J_0/J_b$</td>
<td>Current per unit area/ Bulk Current Density</td>
<td>A/cm²</td>
</tr>
<tr>
<td>$J_1/J_s$</td>
<td>Current per unit perimeter/ Surface Current Density</td>
<td>A/cm</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann’s constant</td>
<td>$8.617 \times 10^{-5}$ eV/K</td>
</tr>
<tr>
<td>$n_i$</td>
<td>Intrinsic carrier concentration</td>
<td>cm⁻³</td>
</tr>
<tr>
<td>$n/p$</td>
<td>Electron/Hole concentration</td>
<td>cm⁻³</td>
</tr>
<tr>
<td>$N_{A}/N_D$</td>
<td>Acceptor/Donor concentration</td>
<td>cm⁻³</td>
</tr>
<tr>
<td>$q$</td>
<td>Elementary charge</td>
<td>$1.602 \times 10^{-19}$ C</td>
</tr>
<tr>
<td>$S$</td>
<td>Subthreshold swing</td>
<td>V/dec</td>
</tr>
<tr>
<td>$T$</td>
<td>Temperature</td>
<td>K</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>Supply voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>Drain–Source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate voltage</td>
<td>V</td>
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<tr>
<td>AFS</td>
<td>Automatic Focus System</td>
</tr>
<tr>
<td>BCB</td>
<td>divinylsiloxane-\textit{bis-benzocyclobutene}</td>
</tr>
<tr>
<td>BTBT</td>
<td>Band-to-Band Tunneling</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>DI</td>
<td>De-Ionized Water</td>
</tr>
<tr>
<td>DIBL</td>
<td>Drain Induced Barrier Lowering</td>
</tr>
<tr>
<td>EOT</td>
<td>Effective Oxide Thickness</td>
</tr>
<tr>
<td>ETD</td>
<td>Esaki Tunnel Diode</td>
</tr>
<tr>
<td>G-R</td>
<td>Generation and Recombination</td>
</tr>
<tr>
<td>GIDL</td>
<td>Gate Induced Drain Leakage</td>
</tr>
<tr>
<td>ILD</td>
<td>Inter-Level Dielectric</td>
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<tr>
<td>IQR</td>
<td>Inter-Quartile Range</td>
</tr>
<tr>
<td>IR</td>
<td>Infrared Light</td>
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<tr>
<td>LG</td>
<td>Linearly Graded</td>
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<tr>
<td>LM</td>
<td>Lattice Matched</td>
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<tr>
<td>LOR</td>
<td>Liftoff Resist</td>
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<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>NPGS</td>
<td>Nanometer Pattern Generation System</td>
</tr>
<tr>
<td>PAB</td>
<td>Post Application Bake</td>
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<tr>
<td>PEB</td>
<td>Post Exposure Bake</td>
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<tr>
<td>Term</td>
<td>Description</td>
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<tr>
<td>RIE</td>
<td>Reactive Ion Etch</td>
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<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
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<tr>
<td>SG</td>
<td>Step Graded</td>
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<tr>
<td>SIMS</td>
<td>Secondary Ion Mass Spectroscopy</td>
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<tr>
<td>SRH</td>
<td>Shockley-Read-Hall</td>
</tr>
<tr>
<td>TAT</td>
<td>Trap-Assisted Tunneling</td>
</tr>
<tr>
<td>TFET</td>
<td>Tunneling Field-Effect Transistor</td>
</tr>
<tr>
<td>TOF</td>
<td>Time-of-Flight</td>
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<td>WD</td>
<td>Working Distance</td>
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Chapter 1

Introduction and Motivation

The purpose of this thesis is the development and electrical characterization of epitaxially grown homojunction In$_{0.53}$Ga$_{0.47}$As PIN diodes for implementation in a Tunneling Field-Effect Transistor (TFET) in the area of low-power electronics.

With the advancement in the mobile electronics industry in the past decade, there is a drive to minimize power consumption to increase battery life while maintaining the high performance. As CMOS devices are being scaled down, there has come a time when dynamic and static power for a particular device are comparable. When a transistor is turned on, the dynamic power is given by $C_f V_{dd}^2$ [1] where $C$ denotes the load capacitance, $f$ is the clock frequency and $V_{dd}$ is the supply voltage at which the device is operating. The biggest factor in the load capacitance is the gate capacitance which has been constantly increasing with the scaling down of the dielectric. With the incorporation of high-$\kappa$ dielectrics, this factor has seen some relaxation as the EOT (effective oxide thickness) has increased but maintaining the same level of gate control.

In the past, the industry has been fighting power dissipation by reducing $V_{dd}$ while increasing clock speeds to boost performance of the chip [2]. As clock speeds have reached a saturation, the focus has again shifted to scaling the power supply, which would have the biggest impact on reducing dynamic power.

Static power constitutes gate leakage and subthreshold conduction. Gate leakage
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is tunneling of carriers through the dielectric to/from the channel. Subthreshold conduction, which is the major portion of leakage current, is the sum of reverse bias p-n current flow, drain induced barrier lowering (DIBL), punchthrough and and gate induced drain leakage (GIDL) at the gate-drain overlap. Of the two, gate leakage can be minimized by controlling the dielectric thickness.

![Image of MOSFET and leakage mechanisms]

**Figure 1.1:** (a) Leakage mechanisms in a MOSFET, (b) Increase in static power consumption with advancing technology node. (c) Comparison of dynamic and leakage power as with decreasing supply voltage (d) Gate leakage in a TFET architecture [3].

A MOSFET is characterized by (i) a high on-state current, $I_{DS}$, in order to drive other transistors, (ii) a low leakage floor, $I_{off}$, to minimize power consumption in the off-state, as a result a high on-off ratio, and (iii) fast switching between the two states denoted by a steep subthreshold swing, $S$, as has been shown in Eq. 1.1 where $V_{GS}$
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Figure 1.2: (a) Energy band diagram of an nMOSFET showing the lowering of the source-channel barrier with increasing gate bias. (b) Source electron carrier distribution showing the Fermi tail that results in a 60 mV/dec subthreshold slope [1].

is the gate bias.

\[ S = \ln(10) \left( \frac{d \ln(I_{DS})}{dV_{GS}} \right)^{-1} \]  

(1.1)

Constant field scaling necessitates \( V_{dd} \) scaling in every generation [4]. With the scaling of the power supply, the threshold voltage needs to be scaled as well. The carrier transport mechanism in a MOSFET is thermionic emission, in which the energy in the channel region is lowered by applying a bias, which allows carriers to flow from the source to the drain. Fermi-Dirac statistics that defines the curve of the carrier population in the source region limit the subthreshold swing to a theoretical value of 60 mV/decade at room temperature.

In a MOSFET, \( S \) is given by [5],

\[ S = \frac{kT}{q} \frac{C_{ox} + C_D}{C_{ox}} \ln(10) \]  

(1.2)
In Eq. 1.2, $C_{ox}$ is the oxide capacitance, $C_D$ is the depletion capacitance in the semiconductor channel, $T$ is absolute temperature, $k$ is Boltzmann constant, and $q$ is the electronic charge. Consider a thin dielectric thickness and a thick depletion region width, $C_{ox} \gg C_D$. In this case, $S$ limits to the simple form showed in Eq. 1.3.

$$S = \frac{kT}{q} \ln(10) \quad (1.3)$$

Subthreshold swing has a direct dependence on temperature. At room temperature, $S$ has a limit of 60 mV/decade. As the temperature of operation is higher than 300 K and since parasitic capacitances play a major role in the load capacitance of a device, the practical limitation of $S$ is 75 mV/decade.

The motivation of this work is to engineer the off current of a TFET device that enables MOSFET-like on-current with a low off-state to minimize leakage and faster switching between the two states.

### 1.1 TFET Background

In a TFET, instead of hopping over a barrier, as in a MOSFET (thermionic emission), the carriers are transported though a mechanism of quantum mechanical band-to-band tunneling (BTBT). This does not limit the subthreshold swing to 60 mV/decade and theoretically makes it independent of temperature. The steeper the subthreshold slope, the lower can be the supply voltage. The concern in this new geometry of devices is the leakage current.

A TFET is commonly realized by gating the i-region of a PIN diode. A PIN diode is an intrinsic semiconductor region between a p-doped and an n-doped semiconductor. Novel materials like III-V (InGaAs, InAs/GaSb) and 2-D semiconductors such as graphene have shown higher drive-currents than Si because of smaller band gaps and increased carrier mobilities [6]. However, devices made with these materials suffer in
switching and off-state because of defects in the bulk and surface trap states.

1.2 Organization of the Document

The remainder of the document is comprised of five chapters. Chapter 2 provides an overview of a PIN diode, major forms of dark current reported and their dependence on physical factors such as temperature, different starting substrates and layer structures and electrical factors such as voltage bias and gating practices.

Chapter 3 reports the fabrication details for the experiments performed. Also, the process developments done to improve and make the process cost and time-efficient are discussed in detail in this chapter. Chapter 4 reports the variation in leakage current of a device by changing intrinsic layer dimensions. Chapter 5 distinguishes bulk and surface leakage in a device and looks into various surface cleaning and passivation techniques that lower the dark current in the device.

Chapter 6 summarizes electrical results and analysis of successful and investigations of undesirable results and provides a scope of future improvements and suggestions for further analysis of certain concepts that this study did not address.
This chapter details the working of a PIN diode, its earlier applications in the field of optoelectronics, and the recent developments to implement a III-V TFET. Origin of dark currents are explained, and with the help of experimental and simulation data from literature, dependence of leakage current on (i) temperature, (ii) doping variations, (iii) layer compositions and thicknesses and (iv) improper gating have been analyzed.

2.1 PIN Diode Overview

A PIN diode is a p-n junction with an intrinsic region between the p-layer and the n-layer. Traditionally, it has been used in microwave circuits and as a photodetector because of its thick i-region that ensures a constant and low capacitance and a high breakdown voltage in the reverse bias [7].

In the forward bias regime, the diode acts as a current-controlled variable resistor. In this bias range, electrons and holes are injected into the i-region from the n-side and the p-side respectively. In this high-injection condition, there is always a finite number of charge carriers stored in the i-region, thereby reducing the resistivity of that region. Beyond a certain concentration of carriers, recombination current kicks in. In RF applications, it is used as a switch and an attenuator as it controls the
signal without adding much distortion to it.

![Typical I-V curve of a PIN Diode. High injection mode in the forward bias. Current blocking mode in the reverse bias][8]

By adjusting the cross-sectional area and thickness of the PIN diode, it is possible to create diodes with similar forward resistance and capacitance. The one with a thicker i-region, however, will show a higher breakdown voltage and low leakage, whereas, the thinner i-region device would show faster switching.

In the reverse bias regime, a PIN diode has wide applications in the field of optoelectronics as infra-red photodetectors. Photons strike at the i-region, creating electron-hole pairs that are swept by the electric field, causing current to flow. A thicker intrinsic region increases the number of photons absorbed and increases quantum efficiency, but increases the transit time.

Photodetectors can be broadly classified into three main categories based on their principle of operation: (i) PIN diodes, (ii) MSM (Metal-Semiconductor-Metal) Schottky junctions, and (iii) Avalanche photodiodes. This study is focused on the electrical performance of PIN diodes. Avalanche photodiodes [9] operate in the avalanche breakdown regime which increases the quantum efficiency but suffers due to a high dark current density, which is undesirable in electrical circuits.
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Figure 2.2: Energy band diagrams of (a) a tunnel diode operating under reverse bias, (b) a TFET in the OFF state, (c) a TFET in the ON state [5].

Recently, PIN diodes have found applications in low power electronics as a TFET [5]. The degenerately doped p-side and n-side act as Source and Drain respectively in the case of an n-TFET. The opposite nomenclature holds for the p-TFET. In both cases, the i-region is gated. In the case of an n-TFET, it is used to modulate the conduction band edge, so that when the device is ON, electrons tunnel from the valence of the p-type source to the conduction band of the i-region and are then swept to the drain by the lateral field.

Earlier work on TFETs was focused on Si and Ge but they exhibited lower on-state currents (Fig. 2.3) because of a high tunneling barrier [3,6]. With the incorporation of high-mobility, small and direct bandgap materials such as InGaAs, InAs, GaSb in the channel region, the drive current increased significantly, but this also resulted in a troublesome rise in the off-state current. The highest reported drive current in a 100 nm long TFET device is $720 \, \mu A/\mu m$ at $V_{GS} = 2.5 \, V$ and $V_{DS} = 0.5 \, V$ [10] which is still less than half of what was reported in a 65-nm technology node MOSFET ($1600 \, \mu A/\mu m$ with $S = 105 \, mV/\text{dec}$ at $V_{GS} = V_{DS} = 1.2 \, V$) [11]. However, the subthreshold slope and leakage currents have not been reported by [10], which may mean that those values are not comparable to the ones found in the literature.
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Figure 2.3: $I_D - V_{GS}$ of 100 nm long In$_{0.53}$Ga$_{0.47}$As TFET benchmarked against Si and Ge TFETs [3].

The key outstanding issues in a PIN that greatly affect the performance of a TFET are dark current and device breakdown. Sections 2.2 and 2.5 provide an overview of these mechanisms.

2.2 Dark Current

In optoelectronics, dark current is the current flowing through a photo-detector PIN in the absence of light. In electrical terms, dark current can be analogously defined as leakage current in a PIN diode at zero gate bias, i.e., in off mode.

In a diode, leakage current can either flow in the bulk of the device, which means it is dependent on the cross-sectional area of the structure, or it could be a surface dominant leakage, which would imply that it would scale with the perimeter of the device.

In Fig. 2.4 the band structure of the intrinsic region of a PIN diode is depicted with $E_C$ and $E_V$ as the conduction band minimum and the valence band maximum for a particular material, respectively. The energy trap level, $E_t$ has been defined as a discrete energy level close to the middle of the forbidden gap [12]. Physically, a
trap may be a foreign atom in the lattice, an interstitial, a vacancy or any other line or stacking faults caused by lattice mismatch.

At any surface, as the solid terminates abruptly, there are unsatisfied covalent bonds that also occupy energy states in the forbidden region. They are called Tamm-Shockley states and lead to surface current. [13,14]

Current flows in a diode because of the free moving electrons in the conduction band. Carriers require energy in terms of thermal excitation and/or electric field to cross-over from valence band to the conduction band. Mid-gap trap states provide an additional step between $E_V$ and $E_C$ that reduces the amount of energy required to jump from one band to the other — resulting in undesirable current flow called dark current.

Dark current in a PIN can be attributed to four main mechanisms: Shockley-Read-Hall Generation and Recombination (Fig. 2.4a), direct band-to-band tunneling (Fig. 2.4c), trap-assisted tunneling (Fig. 2.4d) and Poole-Frenkel current (Fig. 2.4b). While the former two are majorly present in the bulk, trap-assisted tunneling and Poole-Frenkel current contribute to surface leakage. The curved arrows in Fig. 2.4 represent a temperature dependent process and the straight arrows represent tunneling processes that are temperature independent.

Each mechanism is explained in further detail in Sec. 2.3.1, 2.3.2 and 2.4. Since dark current scaled linearly with area [15,16], the authors attributed bulk leakage as the main source of dark current and surface leakage as the less dominant factor.

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Figure 2.4: Leakage mechanisms in a PIN diode

(a) SRH G-R  (b) Poole-Frenkel  (c) BTBT  (d) TAT
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Figure 2.5: Dark current vs. Area for a lattice matched structure and a strain compensated structure at a bias -0.5 V at 290 K [15].

2.3 Bulk Leakage

A bulk leakage mechanism consists of three main models: (i) generation and recombination (G-R), (ii) band-to-band tunneling (BTBT) and (iii) trap-assisted tunneling (TAT) [15,16].

2.3.1 Bulk Leakage: Generation Recombination

As was seen from Fig. 2.6, G-R currents increased linearly with rise in temperature [15]. Performance of InGaAs/GaAsSb [15] PINs are dominated by G-R at small reverse bias and by trap assisted tunneling thereafter at room temperature. Shockley-Read-Hall Generation-Recombination (G-R) currents [12] are based on the model that recombination or generation occurs through the mechanism of trapping. Consider a deep level impurity $E_t$ with trap density $N_t$ cm$^{-3}$. A recombination process is defined by capture of an electron from the conduction band (Fig. 2.7a) and a capture of a hole from the valence band (Fig. 2.7c). In this process the carriers lose energy in the form of photon and more dominantly, phonon discharge. A generation process can be seen as an electron capture from the valence band (Fig. 2.7d) followed by an excitation to the conduction band (Fig. 2.7b). This process requires energy
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Figure 2.6: Measured and simulated current-voltage characteristics considering diffusion, G-R and tunneling currents for lattice matched InGaAs-GaAsSb at (a) $T = 290$ K, (b) $T = 260$ K, (c) $T = 230$ K, (d) $T = 200$ K [15].

Figure 2.7: Electron energy-band diagram for a semiconductor with deep-level impurities. (a) electron capture (b) electron emission (c) hole capture and (d) hole emission [17].
from the system that is provided in terms of heat and light.

G-R is maximized when $E_t$ is close to the intrinsic energy level of a material, indicating that only the trap levels near the mid-gap are effective G-R centers [5]. If the energy level of a defect is close to one of the band-edges, it acts as a trap with either processes (a) followed by (b), or (c) followed by (d). Generally, G-R processes take place to restore equilibrium in the system. In the case when the electron and hole concentration ($n$ and $p$ respectively) are much higher than the intrinsic concentration ($n_i$), i.e., $n_i^2 \ll np$, recombination takes place. In the opposite case, when in a certain bias condition a region is depleted of carriers, $n_i^2 \gg np$, generation kicks in.

### 2.3.1.1 Substrate impact on Dark Current

Jang [18] and Ishimura [19] presented In$_{0.53}$Ga$_{0.47}$As photodiodes on InP, GaAs and Si substrates. The dark current measured at similar physical conditions for the three devices showed a jump of almost three orders of magnitude in the case of GaAs and Si when compared to the control device on an InP substrate. This increase is attributed to lattice-mismatch dislocations that act either as generation centers to increase the dark current or as recombination traps that reduce the diffusion length of the carrier.

Jang [18] used dark current in an In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As PIN as a metric to compare different buffer layer qualities –mainly step graded and linearly graded buffers on GaAs and compared that to lattice matched InP substrate. As expected, the lattice matched (LM) sample showed lowest leakage current, followed by linearly graded (LG). Step graded (SG) samples showed maximum leakage as finite number of defects may be propagating from each step of the metamorphic buffer layer.

As seen in Fig. 2.8, dark current scales with area showing that bulk leakage is dominant. The authors have used polyimide for surface passivation, because of which they assume negligible surface leakage.

The strained sample in Fig. 2.5 showed higher leakage than the lattice-matched...
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Figure 2.8: Area scaled dark current of In$_{0.53}$Ga$_{0.47}$As-In$_{0.52}$Al$_{0.48}$As photodiodes on lattice matched (LM) InP substrate and on GaAs substrates with a linearly graded (LG) buffer layer and a step-graded (SG) buffer layer [18].

sample, due to dislocations, which were attributed to G-R currents because of the temperature dependence [15].

2.3.2 Bulk Leakage: Tunneling

As mentioned in Sec. 1.1, tunneling of carriers from the valence band through a region of higher energy (forbidden gap) to the conduction band is a quantum mechanical phenomenon called band-to-band tunneling (BTBT). Fig. 2.4c and Fig. 2.4d are the two mechanisms of leakage current due to tunneling called direct tunneling (BTBT) and trap-assisted tunneling (TAT), respectively.

BTBT, as observed in the forward regime of an Esaki tunnel diode (ETD) [20], has temperature independent peak-current values (Fig. 2.9c). An ETD consists of an abrupt p-n junction with both sides degenerately doped (Fig. 2.9a), i.e., the Fermi levels are placed in the valence band and the conduction band on the p-side and n-side respectively, as shown in Fig. 2.9a. In the forward bias, as the band overlap of the
electrons on the n-side and empty states on the p-side grows, BTBT across the thin barrier takes place, as shown in Fig. 2.9d, reaching a peak current when the overlap is maximum.

<table>
<thead>
<tr>
<th>60 nm</th>
<th>S.C.</th>
<th>(N_D^{++})</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 nm</td>
<td>S.C.</td>
<td>(i)-layer</td>
</tr>
<tr>
<td>300 nm</td>
<td>S.C.</td>
<td>(N_A^{++})</td>
</tr>
</tbody>
</table>

| Substrate |

(a) ETD layer structure. SC (Semiconductor material) like \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) [21].

(c) Same peak current of ETD for a temperature range showing that BTBT is temperature independent [11]. EBD of ETD at (b) thermal equilibrium, (d) peak voltage in forward bias.

Figure 2.9: (a) ETD layer structure. SC (Semiconductor material) like \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) [21]. (c) Same peak current of ETD for a temperature range showing that BTBT is temperature independent [11]. EBD of ETD at (b) thermal equilibrium, (d) peak voltage in forward bias.

Chen et al. [15] simulated BTBT and TAT (Fig. 2.6) that were comparable to experimentally measured data. Trap-assisted tunneling (TAT) is the mechanism of carrier hopping over the barrier assisted by a mid-gap trap state (Fig. 2.10a). Trap-assisted tunneling, although a bulk-dominated mechanism, is also a cause for surface leakage [16]. It shows a weak direct dependence on temperature (Fig. 2.6).

A study of quaternary InGaAsP and ternary InGaAs diodes was done by Tabatabaie et al. [22] to determine the nature of the tunneling process. Using temperature as the main factor, it was determined that the reverse tunneling current in InGaAsP is defect-dominated rather than being BTBT dominated. In defect-tunneling, a smaller tunneling barrier leads to a high current density at lower fields, whereas at higher fields, a small density of states value limits the current. Therefore, while defect-
assisted tunneling dominates leakage at a low bias, BTBT takes over at higher values of reverse bias.

![Diagram](image)

Figure 2.10: (a) Midgap defect-tunneling and BTBT in a PIN diode. (b) BTBT dominating over defect-tunneling at high fields. Dotted extension - predicted value of current flowing in the case of defect-tunneling. (c) Temp-independent nature of BTBT. (d) Leakage mechanisms in a device - G/R at low bias, defect-assisted tunneling at medium bias, BTBT at high bias and ultimately avalanche breakdown [22].

2.4 Surface Leakage Mechanisms

Surface traps and dangling bonds can occupy a discrete level or a band of trap states in the energy gap. If it traps a high number of carriers, then the Fermi level at the surface would be insensitive to gate modulation as there would always be an inversion
layer present at the interface. This has been observed in experimental demonstration of III-V MOSFETs [23–25]. This is called *Fermi level pinning* and is an extreme case of surface leakage.

![Figure 2.11:](a) Temperature dependence of off-current and subthreshold slope [16] (b) Frenkel-Poole Mechanism [26] (c) Interface state density profile on n-type In$_{0.53}$Ga$_{0.47}$As using split C-V measurement [16] (d) EBD showcasing the impact of no $D_{it}$ (left) and with $D_{it}$

A common problem in all TFET demonstrations is that the subthreshold slope is limited by parallel conduction paths (high surface leakage) between source and drain. These surface currents are dominated by the Poole-Frenkel mechanism [16] as mentioned earlier and represented graphically in Fig. 2.4b.

In the Poole-Frenkel mechanism [27–29], carriers within the trap states in the bandgap are thermally excited to the conduction band in the presence of a field, as shown in Fig. 2.11b. Thermal barrier height for traps was extracted from the temper-
ature sweep of $I_{DS-VGS}$ and split $C-V$ measurements to extract $D_{it}$. It showed that the interface states were essentially mid-gap which explained carrier tunneling into the mid-gap state and then the thermal excitation in the conduction band [16]. It was observed that current lowered with lowering the temperature. This is demonstrated in Fig. 2.11a. This process is responsible for the thermal dilution of the subthreshold swing. In the presence of high electric fields, current varies exponentially with the square root of the field [7].

2.4.1 Gate Experiment

Studies done by Lin et al. [30] have shown that upon application of a negative gate bias on the intrinsic region of an unpassivated InAs PIN, electrons are repelled from the substrate reducing the leakage current from 9.55 A/cm$^2$ at zero bias to 0.64 A/cm$^2$ at a $-40$ V bias, after which applying more gate bias did not have any significant change on the leakage current. This suggests that there was no leakage from the surface of the diode.

Table 2.1: Leakage current (A/cm$^2$) variation with variation in gate bias (V) and temperature (K) [30].

<table>
<thead>
<tr>
<th>Bias (V)</th>
<th>$T = 300$ K</th>
<th>$T = 77$ K</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>9.55</td>
<td>8.28</td>
</tr>
<tr>
<td>$-40$</td>
<td>0.64</td>
<td>$2.23 \times 10^{-5}$</td>
</tr>
</tbody>
</table>

Low temperature measurements on the same study showed that dark current went from 8.28 A/cm$^2$ at zero bias to 2.23 $\mu$A/cm$^2$ at a $-40$ V bias. This, along with no current modulation at zero bias when going from 300 K to 77 K, is an indication that surface leakage through an unpassivated surface is the major component of dark current. Whereas at $-40$ V there is presumably no surface leakage, the current reduced five orders of magnitude from 300 K to 77 K, in accord with Mohata et al. [31,32] referring to temperature-dependent SRH traps and TAT in the bulk.
2.4.2 In-rich and Ga-rich surfaces

Surface states due to material and process related issues may cause a shunt leakage current for InSb and InAs photodiodes [33, 34]. This increases the leakage floor of the devices and decreases sensitivity of the detector. In an unpassivated device, an inversion layer is formed on the surface of the p-type InAs layer, also known as Fermi level pinning. The bulk Fermi level penetrates into the conduction band at the surface causing the electrons to occupy quantized states. This inversion layer has an ohmic contact to the n-type substrate and forms a sidewall p-n junction at the p^{++}/i interface. Tunneling occurs when the p-side is heavily doped and the energy of electrons in the p-side overlaps the empty states in the conduction band of the n-region causing a shunt path for leakage current without any gate bias [35].

Figure 2.12: Peak current density vs. effective doping plot of different material systems with varying Indium concentrations [21]. SG –Staggered Gap (Type II heterojunction) and BG –Broken Gap (Type III heterojunction) [7].

Unless properly passivated, a rise in drive current also leads to an increase in leak-
age current, as can be seen from Fig. 2.3. Fig. 2.12 shows the variation of peak current density in an ETD with respect to reduced effective doping, \( N^* = \frac{N_A N_D}{N_A + N_D} \), as the Indium concentrations in different materials is changed. As the In-concentration in a material increases, the current density increases. The Zener current follows a similar trend with peak current density in an ETD. This brings forth an important point for passivating Indium rich surfaces to reduce leakage.

\[ \text{Figure 2.13: TOF-SIMS intensities of In and P in dielectric at different PDA temperatures and different surface cleaning methods [36].} \]

A study done by Chee et al. [36] looks at surface cleaning methods reported results of Time-of-Flight Secondary Ion Mass Spectroscopy (TOF-SIMS) on an InP substrate. In Fig. 2.13, it can be seen that even after an HF clean and post sulfide treatment, the In concentration at the surface was almost an order of magnitude higher than concentration of phosphorus and PO\(_2\).

For GaSb surfaces [25, 37] it was observed using SRXPS (Spin-Resolved X-ray Photoelectron Spectroscopy) that Sb\(_2\)O\(_3\) reacts with Ga on the surface to form Sb and Ga\(_2\)O\(_3\) at a temperature higher than 250 °C, which is a main cause for high interface states. It can be removed by an HCl clean follows by a vacuum anneal at 300 °C. Experiments done in this study will be focused the area dependence of leakage current in sub-micron PIN diodes. Whether bulk dark current still dominates, or does surface leakage take over at small dimensions is expected to be understood from this study.
### 2.5 Breakdown

In the reverse-bias operation of a PIN diode, the two modes of breakdown are Zener tunneling (soft breakdown) [38,39] and impact ionization [38]. Current-Voltage (I-V) plots of PIN structures fabricated on GaAs show the transition of Zener tunneling to impact ionization as a function of i-layer thickness. It was observed that as the nominal thickness was reduced from 68 nm to 10 nm, the reverse bias characteristics resemble those of an Esaki diode.

![Figure 2.14: Current Density-Voltage characteristics for GaAs PINs with varying i-layer thickness. (a) Experimental data. (b) Dots –Measured data, solid line –Modified Kane model [38].](image)

Using Kane’s tunneling model [40] and modifying it with Krieger’s four-band effective mass parameter [41], Fig. 2.14b shows Monte Carlo simulations that agree with experimental data. For an i-layer thickness of 100 nm in a GaAs PIN, breakdown by impact ionization occurs beyond 6 V. When extended to an In$_{0.53}$Ga$_{0.47}$As system, this value will vary a little — but the operating voltage of a TFET would be very small when compared to the avalanche breakdown voltage.
### Table 2.2: Homo junction PINs in literature.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Material</th>
<th>i-region length [µm]</th>
<th>( I_0 ) ( \frac{A}{cm^2} )</th>
<th>Temp [K]</th>
<th>Bias [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[16]</td>
<td>In(<em>{0.53})Ga(</em>{0.47})As on InP</td>
<td>0.1</td>
<td>( 4 \times 10^{-4} )</td>
<td>300</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td>( In_{0.53}Ga_{0.47}As-In_{0.52}Al_{0.48}As ) on InP</td>
<td>1</td>
<td>( 4 \times 10^{-5} )</td>
<td>300</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>( In_{0.53}Ga_{0.47}As-In_{0.52}Al_{0.48}As ) on GaAs (LG)</td>
<td>1</td>
<td>( 1.1 \times 10^{-4} )</td>
<td>300</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>( In_{0.53}Ga_{0.47}As-In_{0.52}Al_{0.48}As ) on GaAs (SG)</td>
<td>1</td>
<td>( 4 \times 10^{-3} )</td>
<td>300</td>
<td>5</td>
</tr>
<tr>
<td>[19]</td>
<td>In(<em>{0.53})Ga(</em>{0.47})As on GaAs</td>
<td>3</td>
<td>( 3.8 \times 10^{-4} )</td>
<td>448</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>In(<em>{0.53})Ga(</em>{0.47})As on InP</td>
<td>3</td>
<td>( 3.8 \times 10^{-7} )</td>
<td>448</td>
<td>10</td>
</tr>
<tr>
<td>[35]</td>
<td>InAs</td>
<td>0</td>
<td>( 1.6 \times 10^{-2} )</td>
<td>77</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.3</td>
<td>( 2.2 \times 10^{-4} )</td>
<td>77</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.72</td>
<td>( 3.18 \times 10^{-5} )</td>
<td>77</td>
<td>0.5</td>
</tr>
</tbody>
</table>

### 2.6 Pocket-doping or Hetero-integration

Dewey et al. [42] demonstrated a 100 nm channel length TFET that had a room temperature \( I_0 \) of \( 8 \times 10^{-11} \) A/µm at a drain bias of 0.5 V. To increase the drive-current and improve the subthreshold swing from 77 mV/dec to 60 mV/dec, a pocket of 6 nm intrinsic In\(_{0.7}\)Ga\(_{0.3}\)As was added at the source-channel interface. This increased the drive current by a factor of three, because of a decreased source-channel barrier height. However, for the same reason, this led to an increase in leakage current by almost an order of magnitude. The unpassivated surface of the pocket may lead to a higher number of surface states because of an increase in the In-concentration.

The electron BTBT generation profiles of the different TFETs in [31] have a
Table 2.3: Homojunction TFETs in literature. ‘*’ - In$_{0.7}$Ga$_{0.3}$As pocket at tunnel junction. ‘$\Delta$’ - Higher doping at interface. Wherever the value of $I_{off}$ has not been specifically mentioned in the paper, it was extracted from the $I_D-V_{DS}$ curve.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Mole Frac.</th>
<th>Source [nm]</th>
<th>Channel [nm]</th>
<th>Drain [nm]</th>
<th>$I_{off}$ [$\mu A/\mu m$]</th>
<th>$V_{ds}$ [V]</th>
<th>$I_{on}$ [$\mu A/\mu m$]</th>
<th>SS [mV/dec]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3]</td>
<td>0.53</td>
<td>60</td>
<td>100</td>
<td>300</td>
<td>$6 \times 10^{-9}$</td>
<td>0.75</td>
<td>20</td>
<td>-</td>
</tr>
<tr>
<td>[6]$^\Delta$</td>
<td>0.7</td>
<td>300</td>
<td>6 ($p^+$) + 6 ($n^+$) + 100</td>
<td>30 (n) + 150</td>
<td>$1 \times 10^{-7}$</td>
<td>0.05</td>
<td>0.6</td>
<td>84</td>
</tr>
<tr>
<td>[11]*</td>
<td>0.53</td>
<td>300</td>
<td>6 ($p^+$ <em>)+6 ($i^</em>$)+100</td>
<td>30 (n) + 100</td>
<td>$2 \times 10^{-9}$</td>
<td>0.5</td>
<td>50</td>
<td>86</td>
</tr>
<tr>
<td>[16]</td>
<td>0.53</td>
<td>60</td>
<td>100</td>
<td>-</td>
<td>$8 \times 10^{-10}$</td>
<td>0.6</td>
<td>0.1</td>
<td>-</td>
</tr>
<tr>
<td>[30]</td>
<td>1</td>
<td>100</td>
<td>700</td>
<td>200</td>
<td>$6 \times 10^{-5}$</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>[31]</td>
<td>0.53</td>
<td>60</td>
<td>-</td>
<td>300</td>
<td>$4 \times 10^{-8}$</td>
<td>0.75</td>
<td>23</td>
<td>200</td>
</tr>
<tr>
<td>[31]$^\Delta$</td>
<td>0.53</td>
<td>60</td>
<td>3($n^+$)+100</td>
<td>300</td>
<td>$1 \times 10^{-9}$</td>
<td>0.75</td>
<td>46</td>
<td>200</td>
</tr>
<tr>
<td>[32]</td>
<td>0.7</td>
<td>300</td>
<td>150</td>
<td>200</td>
<td>$1 \times 10^{-9}$</td>
<td>0.5</td>
<td>100</td>
<td>200</td>
</tr>
<tr>
<td>[42]</td>
<td>0.53</td>
<td>60</td>
<td>100</td>
<td>40</td>
<td>$8 \times 10^{-11}$</td>
<td>0.7</td>
<td>1</td>
<td>77</td>
</tr>
<tr>
<td>[42]*</td>
<td>0.53</td>
<td>60</td>
<td>6 (*)+100</td>
<td>40</td>
<td>$1 \times 10^{-10}$</td>
<td>0.5</td>
<td>2</td>
<td>60</td>
</tr>
</tbody>
</table>

direct correlation with the current flowing through a device. Also, as the energy gap decreases from a homojunction device to a $\delta$-doped device to a heterojunction TFET, the population of electrons increases, causing a rise in the drive-current. However, the distance of the electron profile from the metallurgical junction which is 10.3 nm in In$_{0.53}$Ga$_{0.47}$As homojunction versus 1.85 nm in a highly-staggered heterojunction leads to a rise in the dark current as shown in Fig. 2.16 for the TFETs at two distinct gate lengths.

Figure 2.15: Variation in band-gap at the tunneling interface and corresponding distance of the peak of $e^-$ BTBT generation rate for a homojunction, $\delta$-doped, moderately staggered and highly staggered TFET [31].
Chapter 2. Background Review

Figure 2.16: $I_D-V_{GS}$ for different channel lengths for a homojunction, $\delta$-doped, moderately staggered and highly staggered TFET [31]. The figure also demonstrates experimentally that over a wide range of materials chosen, a smaller gate length has a higher off-state current.

TFET performance comparisons upon inclusion of an In-rich layer at the tunneling interface have been done by Zhao et al. [11]. The layer structures implemented are in Fig. 2.17 which varies the $p^+/undoped\ In_{0.7}Ga_{0.3}As$ layer thickness at the tunneling interface.

![Layer Structures](image)

(a) \hspace{2cm} (b) \hspace{2cm} (c)

Figure 2.17: Layer structures used for TFET fabrication in [11].

It has been observed experimentally that a smaller band-gap and a smaller electron mass shows higher drive currents [11,43] and at the same time, higher leakage as well. Another TFET [6] reported using an Esaki diode ($p^+/n^+$) at the $p^+/i$ tunnel interface
to enhance the drive current by 50% by improving tunneling. However, above $8 \times 10^{18}$ cm$^{-3}$ doping level in the n$^+$ region, the $I_0$ increased by several orders of magnitude.

### 2.7 Variation in intrinsic region length

Results reported by Ray-Ming et al. [35] talk about the dependence of leakage current as a function of intrinsic-layer thickness done at 77 K, also shown in Table 2.2. The leakage currents for structures with undoped layer thicknesses of 0 µm, 0.3 µm and 0.72 µm are 16 mA/cm$^2$ 0.22 mA/cm$^2$ and 31.8 µA/cm$^2$ respectively at a reverse bias of 0.5 V. A small tunneling peak below 80 K in the forward bias of the PIN with no intrinsic layer is an indication of surface pinning, which is independent of temperature.

With the increase of i-layer thickness, there was no indication of tunneling current leading to the assertion that insertion of an undoped layer reduces the surface pinning effect. The veracity of this statement has been looked into detail in Chapter 4.

### 2.8 Temperature Analysis

The activation energy extracted for $I_0$ was between 0.29 eV and 0 eV — close to middle of the forbidden region in the In$_{0.53}$Ga$_{0.47}$As system suggesting SRH G-R currents and

![Figure 2.18](image)

**Figure 2.18:** (a) $I_D - V_G$ and (b) $I_D - V_D$ of an In$_{0.7}$Ga$_{0.3}$As TFET using p$^{++}$/i and p$^{++}$/n$^+$ tunneling junctions. (c) $I_D - V_G$ of In$_{0.7}$Ga$_{0.3}$As TFET using p$^{++}$/n$^+$ tunneling junctions and varying the doping concentration on the n$^+$ side [6].
Figure 2.19: Temperature dependent I-V characteristics of unpassivated InAs PINs with varying i-layer thickness [35].

tunneling currents. A subthreshold swing improvement at 150 K is indicative of a reduced interface trap response which means that interface trap-assisted-tunneling is also temperature dependent [11, 43]. Temperature analysis done by [16] showed that bulk leakage is dominated by SRH G-R currents, which increases exponentially with rising temperature.

Figure 2.20: (a) Temperature dependence of I-V characteristics of ungated In$_{0.53}$Ga$_{0.47}$As PIN [16] (b) Temperature dependent sub-threshold leakage (c) $I_0^{-1}/T$ plot of In$_{0.7}$Ga$_{0.3}$As TFET with different thicknesses of dielectrics [11].

The activation energy extracted in [35] at 160 K and higher is 0.33 eV which is comparable to the bandgap of InAs - indicating that bulk diffusion current dominates the transport mechanism in this temperature range. A similar extraction at 77 K gave an activation energy of 2.8 meV — much lower than the bandgap — implying
that surface leakage current is dominant (Fig. 2.10).

## 2.9 Gate Placement

![Gate Placement Diagrams](image)

**Figure 2.21:** Effect of gate placement on device characteristics [8]. The tunnel junction is at p/i interface.

Proper gating of the channel region is of utmost importance to maximize drive current and, in some cases, minimize surface leakage [8]. In the ideal case of gate placement (Fig. 2.21a), only the energy band in the intrinsic region is modulated as shown and explained in Fig. 2.2. Fig. 2.21b shows incomplete gating of the i-region, as a result the gate is not able to control the tunnel junction properly. In the case of overlapping the gate, the source gets depleted of carriers, reducing the drive current. Zhao et al. [11] have concluded that over-gating the vertical profile at the p⁺-side has resulted in a decrease in the ON-current because of a lesser tunneling field as a result of the increased gate influence at the interface. Finally, Fig. 2.21d shows a scenario where the i-region is not completely gated leaving an ungated region at the drain end. This would add a potential barrier to carriers, and the distance of the underlap
would greatly affect the drive current.

In this section, dark current has been broken down into bulk and surface leakage. Parametric relationships of G-R, Poole-Frenkel and tunneling have also been studied. The following chapter will explain the standard fabrication procedure to realize PIN diodes and the rationale behind moving towards a new mask set.
Chapter 3

Process Development

This chapter details the processing conditions used in this thesis and is divided into four sections. Sec. 3.1 outlines the recipes used in different steps, broadly classified by the process type (metallization, exposure, etch etc.). Sec. 3.2 describes the process details used for fabrication of ETDs in a chronological order. Sec. 3.3 looks at process modifications namely incorporating GCA lithography for PIN and TFET fabrication. Sec. 3.4 describes the new process flow and introduces a new mask set that incorporates the new process developments.

3.1 Standard Processing

3.1.1 Metallization

The devices used in this work were grown using Molecular Beam Epitaxy (MBE) with in-situ doping. Following growth, the samples were initially cleaned to remove native oxides that form on the surface of the sample. This was performed by dipping the sample in a 10:1 DI H$_2$O:HCl solution for 15 s and then rinsing with DI to remove excess HCl from the surface.

Next, the samples were loaded into a DC Sputter system to deposit 200 nm Mo using an 8-inch Mo target. The chamber with the samples loaded is pumped overnight to reach base pressures of $2 - 4 \times 10^{-7}$ Torr. Since the tool is not a load-lock system,
a pre-sputter was performed to remove any oxides/residue that may have formed on
the platen during sample loading. This was accomplished by using a shield to cover
the sample. The pre-sputter was done using an Ar plasma (2.2 mTorr, 18 sccm) at
1000 W for 120 s. For the actual deposition, the power was reduced to 200 W and
the run-time was 420 s.

The metallization process was used for top and bottom metal deposition and
probe pad deposition in PIN fabrication and drain, source and gate and probe metal
deposition in TFET fabrication.

3.1.2 Lithography

While a majority of the lithography steps in past studies involved EBL because of
sub-micron patterns, this study has shifted to optical lithography, with the intent of
leaving the SEM for inspection and analysis. For EBL, the samples used the SEM
controlled by the Nanometer Pattern Generation System (NPGS).

3.1.2.1 Resist Processing Parameters

Following a DI H$_2$O rinse and dehydration bake at 110°C, resist was spun on the
sample using a spin coater, which involves a 500 rpm step for 2 s followed by a 4 s
ramp up to the resist-specific spin speed (Table 3.1) which runs for 45 s followed by
a 4 s ramp down.

Dilute n-LOF (n-LOF 2020 diluted with PMGEA) is a negative tone optical resist
used to pattern mesas onto the Mo layer. n-LOF 2020 has a high sensitivity and
excellent etch resistance making it the ideal choice to transfer the resist pattern onto
the Mo.

Positive tone resist ARCH 8250 was used along with LOR 5A as a double resist
stack to deposit probe pad metal. Mo in excess areas is lifted off in a Remover
PG chemistry heated at 75 °C. The sample is kept in the solution for 20 minutes,
while stirring the solution every 2 – 3 minutes to avoid lifted-off Mo “flakes” from re- 
depositing on the sample and creating electrical shorts between pads. Dilute n-LOF and ARCH 8250 were used for e-beam patterning.

HPR 504 is a positive tone g-line (436 nm) resist used for optical lithography on the GCA \(5 \times \) stepper. Work done previously on the GCA \cite{8,44} has involved patterning alignment marks, grids and big features like probe pads for certain layouts. This study further increases the scope of the GCA by using it to pattern mesas in the surface treatment experiments and also improving it further to develop a new mask set, which has been further discussed in Section 3.3.2.

The details of resist processing parameters and their usage have been given in Table 3.1.

<table>
<thead>
<tr>
<th>Resist Tone</th>
<th>Dilute n-LOF</th>
<th>ARCH 8250</th>
<th>LOR 5A</th>
<th>HPR 504</th>
</tr>
</thead>
<tbody>
<tr>
<td>Purpose</td>
<td>Negative</td>
<td>Positive</td>
<td>Liftoff Resist</td>
<td>Positive</td>
</tr>
<tr>
<td>Spin [rpm]</td>
<td>3500</td>
<td>3000</td>
<td>3000</td>
<td>3000</td>
</tr>
<tr>
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<td>60</td>
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<tr>
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<td>110</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PEB Time [s]</td>
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<td>-</td>
</tr>
<tr>
<td>Developer</td>
<td>CD-26</td>
<td>CD-26</td>
<td>Remover PG</td>
<td>CD-26</td>
</tr>
<tr>
<td>Develop time [s]</td>
<td>30</td>
<td>60</td>
<td>1800</td>
<td>40</td>
</tr>
</tbody>
</table>

3.1.3 Exposure

For EBL, samples coated with resist were loaded onto the stage and transported to the SEM in a dark box. The Faraday cup was used to set up the beam current to 200 pA at 20 kV using the probe current which was set to \( \sim \)100 pA (depending on the displacement of the filament with respect to aperture). Setting the WD to 6 mm, the gold standard (a piece of gold metal attached to the stage) was used to focus
the beam and adjust the astigmatism. Scratch marks on the edges of the sample or alignment marks from previous patterning steps are used to generate a focus matrix which is used by the NPGS software while patterning.

Each pattern gets written serially and the total time (set-up and run-time) of the tool ranges from 2–4 hours depending on the size of the pattern in the CAD file and the beam current used to do the write. The mesa patterns were written at a dose of 30–35 $\mu$C/cm$^2$. Post exposure, the e-beam resists require a PEB at 110 °C for 60 s, after which the sample was developed in a CD-26 basic solution for resist-specific durations specified in Table 3.1 and later rinsed with DI H$_2$O.

In the case of a positive tone resist (both EBL and GCA), the pattern that is exposed to e-beam or light becomes an acid that can be dissolved by a base. In the case of a negative tone resist, the exposed area crosslinks and the unexposed resist can be dissolved in the CD-26 chemistry.

For the GCA, the resist coated sample was loaded onto the piece-parts paddle with the bottom edge of the sample touching the alignment screws. The run time of the tool ranges from 5–10 minutes per sample. Post exposure, the GCA resist does not require any bake. It was developed in a CD-26 solution and rinsed with DI H$_2$O.

### 3.1.4 Metal Etch

For mesa formation, the resist pattern was transferred to the top Mo layer using the Drytek Quad RIE system that uses an SF$_6$ plasma to anisotropically etch the metal. Chamber 2 was used for Mo etch on the system, which was prepared by running an O$_2$ clean (280 W, 180 s, 1000 sccm O$_2$ at 300 mTorr) prior to carrier introduction in the chamber.

It was followed by a 5 min carrier season with the Mo etch recipe (150 W, 125 sccm SF$_6$ at 125 mTorr) followed by a 2 min, 10 s metal etch at 60 °C.

Previous work had shown incomplete etching of the metal leaving pieces of metal
in the field, because of which the chamber temperature was increased from 48°C to 60°C and the etch time increased from 120 s to 130 s. A possible explanation could be etch residue along the walls of the chamber because of excessive tool usage. Alternatively, another theory put forward was that because of the rough topology of certain samples, localized electric fields were getting generated that etch some areas faster/slower than the rest.

### 3.1.5 Mesa Etch

The InGaAs layers are etched in a citric acid based chemistry that has an etch rate of 1.1 nm/s for a 20:1 citric acid:H$_2$O$_2$ solution [45].

Fig. 2.21 shows how improper gating can lead to a significant reduction of tunneling at the $p^{++}/i$ interface, so it is critical that the etch should be stopped as soon as the i-layer in the field is etched. The etch time can be determined by $(t_{\text{etch}} = t_{n+} + t_{i})/1.1$ s, where $t_{n+}$ and $t_{i}$ denote the thickness in nanometers of the n-type and the thickness of the intrinsic layer respectively.

The samples were introduced into the solution for $t_{\text{etch}}$ seconds and chemistry was
stirred every 10–15 s, as this is a diffusion limited reaction. III-V etching proceeds with an oxidation-reduction reaction at the surface, which is done by \( \text{H}_2\text{O}_2 \) in this case, followed by the removal of oxide from the surface, done by citric acid. Agitation is important when the oxidized layer is unable to diffuse out into the solution to give way for the peroxide to oxidize the next layer. This was followed by a quick rinse in DI \( \text{H}_2\text{O} \). The citric acid etch is highly selective and provides an etch stop at InP and GaSb.

3.1.6 Area Analysis

![SEM images showing device sizes in different rows.](image)

**Figure 3.2:** SEM images of device sizes in different rows. (LtoR) Top - Row 3, Row 4 and Row 7 Devices. Bottom - Row 8, Row 9, Row 10. Edge roughness is increasingly visible as edge length reduces. All SEM images were taken at an accelerating voltage of 20 KV and a filament current of 1.95 A.

Variation in dose during EBL because of beam drifting and patterning small sizes (100 nm) were two main reasons that the patterns lose the square shape as given in the CAD file. It gets worsened by a dry etch of the top metal that thins the resist causing roughness on the edges. Looking from a top-down SEM view of the devices (Fig. 3.2), the roughness is clearly much more visible in the Row 3 devices, as compared to the Row 10 devices.
A MATLAB script developed by [8, 44] analyses the top-down SEM images of devices which calculates the number of pixels occupied by the device in the image, which based on the magnification gives a physical unit of measurement of the edge (µm). A cross-sectional analysis of the device at 84° tilt gives additional undercut that takes place during the citric acid mesa etch. The etch is crystallographic in one orientation and nearly anisotropic in the other.

### 3.1.7 BCB Processing and Planarization

Divinylsiloxane-\textit{bis}-benzocyclobutene, BCB (Dow Chemicals, Cyclotene 3022) is a spin-on polymer resin used in the industry as a planarizing material and a low-κ ILD.

The sample was coated with a BCB adhesion promoter, AP-3000, using the SCS Manual Coater at 3000 rpm for 45 s, following which it was coated with BCB using the same recipe. It was followed by a PAB at 140 °C for 5 min. The sample was then transported to a nitrogen ambient oven and the temperature was ramped up from 140 °C to 250 °C. BCB was cured at 250 °C for 60 min.

After curing, BCB was etched back so that the surface of the top metal was exposed for probe pad lithography. It was done in a load-lock plasma etch tool, LAM 490, which uses a combination of O\textsubscript{2}/SF\textsubscript{6}/He (80 sccm/20 sccm/100 sccm respectively) to ash and etch BCB in an isotropic manner.

The recipe was first run with a carrier wafer for 5 minutes to season the carrier and the chamber. The recipe uses 25 W RF power with a 1.65 cm distance between the two electrodes at 300 mTorr.

After the season, the sample was etched for an initial step of 5 minutes. It was observed that the reflected power given by the system was significantly high (6 W for a 25 W forward power), because of which the etch rate reduced notably.

After the first etch, the sample was visually inspected under an optical microscope
to see whether the grid metal or the big devices started clearing or they still have residual BCB on them. The etch process was repeated for smaller intervals of time (1 min, 30 s, 15 s etc.) until a qualitative assessment that the BCB has been significantly etched back was made.

The BCB etchback process is still immature and needs to be fully developed as there is non-uniformity in the etch and visual inspection is required which usually results in a large range of devices that are open circuits. If the BCB has not been fully etched back, the probe pad does not contact the top metal, resulting in an open or a highly resistive circuit. On the other hand, if the BCB is overetched, the probe pad may not be on a planar surface and may develop a crack during probing.

### 3.2 Esaki Tunnel Diode Fabrication

The section outlines the steps followed in sequence to fabricate Esaki Tunnel Diodes (ETD) in a process developed by Pawlik [44]. Each step has been discussed in detail in Sec. 3.1.

The samples were prepared by cleaving 10 mm×10 mm pieces from InP wafers with In_{0.53}Ga_{0.47}As layers grown by MBE. The thickness and doping concentration of the layers vary in each sample.

The sample was cleaned in a 10:1 DI H₂O:HCl solution for 15 s to remove native oxides and particulates from the surface. 200 nm of Mo was deposited as top metal in a DC sputter tool. The same procedure was then followed to contact the bottom substrate using Mo.

The mesas were patterned using a negative tone chemically amplified resist, n-LOF 2020 (diluted with PMGEA), by e-beam lithography (Sec. 3.1.2) using the “battleship-game” grid pattern shown in Fig. 3.4. The layout has previously been used at RIT for fabrication of tunnel diodes, and has carried on for PIN fabrication. The top metal of the vertically grown diodes was patterned using EBL (Fig. 3.4-2).
Chapter 3. Process Development

The resist pattern was transferred to the Mo layer by a SF$_6$ plasma in a RIE chamber. The Mo was used as a hard mask to etch mesas in a 20:1 citric acid:H$_2$O$_2$ chemistry. The sample was then coated with BCB and it was cured in a N$_2$ ambient at 250 °C for 60 min. It was subsequently etched back until the top metal was exposed for Level 2 probe pad lithography. The probe pads (Fig. 3.4-4) were defined using EBL using a double resist stack of positive tone resist ARCH-8250 on liftoff resist LOR-5A. After the lithography step, 200 nm of Mo was deposited using a similar process as used for top and bottom metal, after which it was lifted off in a Remover PG solution heated at 75 °C.

The ETD pattern, used in Chapter 4, has been illustrated in Fig. 3.4. The 10×10 matrix has device sizes increasing from top to bottom. The first row consists of square devices 500 nm long, followed by 600 nm, 700 nm and 800 nm in the second, third and fourth rows, respectively. The first half of row 7 consists of 1 µm diodes and the second half has of 1.2 µm diodes. Rows 8, 9 and 10 follow a similar trend of increasing the edge length by 0.2 µm. The biggest devices in row 10 are 2.4 µm×2.4 µm in size.

The big devices (4×4 µm, 5×5 µm, 10×10 µm and 20×20 µm) in rows 5 and 6 are used for Level 1 electrical testing. The grid in the pattern is used as the second electrode when testing tunnel diodes.

Figure 3.3: Esaki Tunnel Diode Process Flow
3.3 Process Modifications for PINs and Semi-insulating Substrates

Semi-insulating substrates or insulating buffer layers containing Al do not allow the standard bottom electrode definition by contacting the substrate using metal. Esaki diode use the grid in the ETD pattern (Fig. 3.4) as the anode contact in the reverse-biased mode to create a virtual short. In PIN diodes, since the intrinsic layer is a mobile carrier free region in the reverse bias, current flow is limited — eliminating the possibility of a reverse tunneling junction contact.

A new process flow was developed as a part of this study to fabricate PIN diodes and modify the existing TFET process developed by Romanczyk [8]. The main motivation was to develop a methodology to directly contact the p$^+$ layer in PIN structures. The incorporation of optical lithography in the new process was of prime
importance to replace EBL that helped reduce the set-up and run-time of patterning steps. This initiated the development of a new layout, which integrated GCA lithography and the shadowed metal deposition process.

A comparison of the ETD and the new process has been shown in Fig. 3.5 with key improvements shown in Table 3.2.

![Figure 3.5: Set-up time (blue) and Run Time (orange) for (a) Old ETD Process, and (b) New Process.](image)

<table>
<thead>
<tr>
<th>Variable</th>
<th>ETD Process</th>
<th>New Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contacts</td>
<td>One top, one bottom</td>
<td>Two top side contacts</td>
</tr>
<tr>
<td>Number of steps</td>
<td>11</td>
<td>15</td>
</tr>
<tr>
<td>Number of hours</td>
<td>65 (4 lab days)</td>
<td>47 (3 lab days)</td>
</tr>
<tr>
<td>Lithography steps</td>
<td>2 (Both EBL)</td>
<td>4 (1 EBL, 3 GCA)</td>
</tr>
<tr>
<td>Overnight pumpdowns</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

The three metal deposition steps in the ETD process, top metal, bottom metal and probe pad, used overnight pumpdowns of the sputter chamber, which was improved...
to two overnight pumpdowns — top metal and probe pad, and an e-beam line-of-sight deposition for contacting the bottom p+ layer. Although number of steps increased from 11 to 15, the processing time was cut down by 18 hours.

### 3.3.1 Reducing Number of EBL Steps

This section gives a brief overview of how the scanning electron microscope is used for e-beam lithography, the setup time and run time of the tool, and the rationale to shift to optical lithography for certain patterning steps.

EBL at RIT utilizes the Zeiss LEO EVO 50 SEM with an attached Nanometer Pattern Generation Software (NPGS) from JC Nabity Lithography Systems to control the electron beam during the exposure.

The SEM column houses a LaB$_6$ filament at the top that emits electrons thermionically and has an acceleration voltage of 20 kV. The electron beam is first focused by condenser lenses and then rastered using scanning coils along the walls of the column before reaching the sample. The sample is coated with resist and loaded into the SEM chamber and the chamber is pumped down from atmospheric pressure, which takes 3–4 minutes. The column is not vented while loading the sample in the system. Typical column and chamber pressures before the beginning of the e-beam write are $2.1–2.5 \times 10^{-7}$ Torr and $2–4 \times 10^{-6}$ Torr respectively.

Once the chamber has been pumped down, the beam is warmed up and the current is stabilized, which roughly takes up to 30 minutes. A focus matrix is then prepared by focusing on scratch marks or alignment marks from previous level writes to fix for a tilted stage or sample. The control is then passed on to the NPGS system that patterns the layout on the sample.

The setup beginning from the resist coat to the focus matrix typically takes 60 minutes. The time duration of the write depends on the dose used for the pattern — which depends on the beam current specified in the job file. Also, it depends on the
size of the pattern as the beam rasters in the x-y axes. Mesa squares, which range from 500 nm to 2 \( \mu \text{m} \), have relatively short write times than the grid pattern and row, column and die identifiers which take up 95% of the actual pattern time. The first lithography pattern in the ETD process commonly finishes in 30 minutes.

The second lithography step for patterning probe pads has a similar set-up time but a much longer run-time because of defining probe pads over mesas that are 15 \( \mu \text{m} \) in diameter.

The GCA, on the other hand, does not require a low pressure environment and all the dies in the sample can be exposed simultaneously, cutting down tremendously on tool operating time. The disadvantage of optical lithography has been a minimum half-pitch limitation of 500 nm because of the operating wavelength of 436 nm. The electron beam, depending on the filament position in the column and condensor lenses, can theoretically be focused down to a minimum of 4–8 nm.

Table 3.3: Optical lithography vs. E-Beam Lithography

<table>
<thead>
<tr>
<th>Parameter</th>
<th>GCA</th>
<th>EBL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td>10 min</td>
<td>90 - 120 min</td>
</tr>
<tr>
<td>Min CD</td>
<td>500 nm</td>
<td>50 - 100 nm</td>
</tr>
<tr>
<td>Mask Set</td>
<td>Fixed</td>
<td>Can be modified at every run</td>
</tr>
<tr>
<td>Exposure</td>
<td>Whole mask patterned in one exposure</td>
<td>Beam rastering writes each pattern serially</td>
</tr>
</tbody>
</table>

A disadvantage of EBL is that each die is exposed serially. The GCA, on the other hand, exposes all the dies simultaneously (one GCA die contains 16 e-beam dies), having a higher throughput. As shown in Fig. 3.5, EBL took an average time of two hours, whereas a GCA exposure (including set-up time) takes 10 minutes.

Another disadvantage of EBL is possible damage to active regions of devices in patterning steps that follow mesa etch. This is not a point of worry for Esaki Diodes, but is a pressing concern for TFETs and PIN diodes that require a low off-state current.
The design file in EBL can be modified for each run to accommodate for different samples that have varying layer thicknesses. This is not possible in the case of optical lithography.

Because of SEM inspection steps for area analysis and process developments for shadowed metal depositon, EBL had become a bottleneck when working with a high volume of samples. The new layout that has been developed is a combination of optical lithography for alignment marks, probe pads and big features, and EBL to pattern mesa structures.

### 3.3.2 GCA Lithography Using Piece-Parts Paddle

The reasons for moving towards optical lithography were outlined in Section 3.3.1—namely less setup and run time and simultaneous exposure of multiple dies. The GCA was operated manually for the samples using a piece-parts paddle, represented in Fig. 3.6.

This work was performed with $11 \times 11 \text{ mm}^2$ Si samples that were used to analyze the focus issues faced in previous studies [8]. The sample were loaded onto the piece-parts paddle with the bottom edge touching the two sample stops at the bottom. This was done to minimize rotational misalignment in subsequent runs. The third stop (left) was used in the case of samples with horizontal dimensions larger than 15 mm.

The lower right corner (usually the reference corner of the sample) was aligned with the right alignment objective of the GCA. The amount of distance to move in the x and y axes for the center of the right alignment die was calculated using Eq. (3.1) and Eq. (3.2)

$$x = \frac{L - x_{\text{Step}}(n_{\text{Col}} - 1)}{2}$$  \hspace{1cm} (3.1)
Figure 3.6: Piece-parts paddle used for exposing 11×11 mm pieces for optical lithography on GCA. The sample stops are used to reduce rotational misalignment between multiple GCA levels. The vacuum hole is used to keep the sample in position throughout the exposure [8].

\[
y = \frac{W - y_{Step}(n_{Row} - 1)}{2} \tag{3.2}
\]

where \( L \) and \( W \) are the horizontal and vertical dimensions (in mm) of the sample respectively. \( x_{Step} \) and \( y_{Step} \) are the step distance between contiguous dies. The step distance is the sum of die width and the distance between neighboring dies. The number of rows and columns are given by \( n_{Row} \) and \( n_{Col} \). \( x_{Step}, y_{Step}, n_{Row} \) and \( n_{Col} \) are entered into the job-file in the GCA. The stage was moved manually using a joystick to the desired coordinates and exposed.

The automatic focus system (AFS) [46] determines an optimum focus setting that varies for different runs. Once achieved for a particular run, it is maintained during the entire exposure. It compensates the wafer flatness error by adjusting the elevation
of the reduction lens system. The upper-limit of the wafer flatness error that the AFS can accommodate is 2.5 \( \mu \text{m} \) for every 2.5 cm. The Receiver Assembly receives IR signals reflected from the surface of the wafer from the transmitter assembly. In Fig. 3.7, the surface of the wafer would be the image plane at the optical axis. The optical axis is an imaginary line that defines the path along with light propagates in the system. In the stepper, the optical axis passes through the center of curvature of each lens in the system. It passes through the center of the reticle and at the image plane, it is assumed to cross the wafer/sample.

**Figure 3.7**: GCA Auto-Focus System. The setup consists of a transmitter assembly that shines an IR light on the image plane at the optical axis through a series of a reticle, mirror and a condensing lens. The light was then collected through a collector lens and a mirror by a photodiode in the receiver assembly that converted the light to an electrical signal. The amount of illumination sensed by the receiver (the amplitude of the electrical signal) is used to drive a linear motor that drives a dogleg assembly that controls the movement of the microreduction printer tube (that houses the reduction lens assembly) in the z-axis. [46]

Work done previously on the GCA [8] used quadrant mask plates (four masks on one 5×5 inch glass reticle). This arrangement was preferred because the small
die size and it was cost-effective. The disadvantage of having multiple masks in one reticle is that the center of the quadrant mask is different from the optical axis. In the case when the sample is small enough that the optical axis and the light passing through the quadrant mask are not on the same plane, the micoreduction printer tube is unable to adjust the height of the reduction lens to focus correctly, resulting in out-of-focus features. In the z axis, the difference between the two planes would be the thickness of the sample (≈300 µm), much higher than the upper limit of the focus correction of 2.5 µm leading to out-of-focus patterns on the sample.

It can be rectified by (i) using full plate masks (one mask on one reticle) that would ensure that the light passes through the optical axis in which case samples as small as 10×10 mm$^2$ may be used, or (ii) using samples of larger dimensions so that when using a quadrant mask, the optical axis and the light would fall on the sample (same image plane).

### 3.3.3 Shadowed Metal Deposition

For the second top contact to the p$^+$ layer, 50 nm of Mo was deposited using a shadowed metal deposition process in the CHA e-beam evaporator. In the CHA, the sample was taped to a glass slide, which in turn was attached to a stationary mount that could be fixed onto the metal ring that supports the lower part of the planetary in the tool. Mo pellets placed at the bottom of the chamber in a crucible are evaporated by an electron beam in the vacuum chamber, depositing on the sample.

By angling the mount orthogonally to the flow of Mo atoms in the system, a line-of-sight deposition was achieved that contacted the p$^+$ layer. The Mo layer was aligned extremely close to the mesa, without shorting to either the top Mo because of the vertical etch depth (approximately twice or thrice the thickness of bottom Mo) or to the i-layer because of the crystallographic nature of the citric etch that leaves Mo extending off the edge of the mesa, shielding the sidewall, as shown in the SEM.
image in Fig. 3.8.

The prime improvement of defining the bottom contact in close proximity to the mesa is minimization of series resistance. Although not a direct advantage for this study of off-state in PINs, it will be of advantage in a TFET architecture where series resistance on on-state current is undesirable. For Esaki diodes fabricated using the ETD pattern in Fig. 3.4, the grid served as the anode contact and probe pad was the cathode contact. In the case of high current density samples, the 20 µm distance from the mesa to the grid was the cause of series resistance at higher values of forward bias.

The other advantage of the shadowed metal deposition process was electrical isolation of the two metal contacts without implementing a pattern and etch step cutting down on tool usage and process run-time.
3.4 New Mask Set

Figure 3.9: The zero-th level of the new layout. (1) - GCA alignment marks for subsequent optical lithography steps. The mask contains 9 GCA alignment marks - 4 in the corners, 1 in the center, and 4 at the center of each outer edge of the GCA die. (2) - e-beam alignment marks for each e-beam die. 16 e-beam dies, present on one GCA die, are patterned simultaneously. (3) - The die identifier has been incorporated in the GCA step to reduce EBL time. (4) - Row/column identifiers in each e-beam die. (5) - Alignment verniers for subsequent GCA lithography steps.

In the new process, 200 nm of Mo was deposited by DC sputter as top metal. It was followed by a zero-th level optical lithography step that defined GCA alignment marks (Fig. 3.9-1) and e-beam alignment marks for 16 dies (Fig. 3.9-2). The mask plate contains 16 e-beam dies that can be patterned simultaneously to cut down on runtime, which by EBL would have taken much more time. For the same reason, e-beam die identifiers and row/column numbers (Fig. 3.9-3,4) have been incorporated in the zero-th level. For subsequent GCA lithography steps, alignment verniers have also been added (Fig. 3.9-5).

Using a positive resist and a dark field mask for the zero-th level, the top metal was exposed in the patterns showed in Fig. 3.9. It was followed by a RIE etch of Mo in SF$_6$ chemistry for 2 min, 10 sec. To provide further contrast between the alignment pits and the surface—higher contrast results in better e-beam alignment—the exposed
semiconductor in the pit was etched for 4 minutes in a 20:1 citric acid:H\(_2\)O\(_2\) chemistry. The samples were coated with dilute n-LOF 2020 and mesas were patterned by e-beam using the SEM and NPGS software. After the mesa lithography, the top metal was etched using the same recipe that was used for the zero-th level Mo etch. The semiconductor was etched for \(t_{n^{+}i}/1.1\) s, where \(t_{n^{+}i}\) is the combined thickness of the n\(^+\) and intrinsic region in nanometers.

![Image](image_url)

**Figure 3.10:** The pattern in the figure represents one e-beam die. There are 16 e-beam dies in a 4x4 grid on a mask plate. (a) Vias (cyan-crosshatched) etched through BCB to contact the bottom metal using a dark field mask. Areas where the diodes are patterned by EBL shown in blue. (b) Probe pad lithography step using a clear field mask contacting the top of the mesa and the bottom metal through the via.

The bottom p\(^+\) layer was contacted by depositing 50 nm of Mo in the CVC e-beam evaporator using the shadowed metal deposition process. After the deposition, BCB coat, cure and etchback followed the same procedure as outlined in Sec. 3.2. The etchback was monitored after brief etch periods to ensure that only the top metal on the mesas was cleared. HPR-504 was then spun on the sample and vias were patterned in each of the 16 e-beam dies. The pattern was transferred to BCB using the BCB etchback recipe in the Drytek Quad RIE etch tool. The location of the vias in the die have been shown in Fig. 3.10a.
200 nm Mo was sputtered on the sample using CVC 601, followed by a GCA patterning step that defined the probe pads on the diodes and over the vias. The excess Mo was etched by the standard Mo etch recipe to electrically isolate the contacts.

This chapter explained the processing steps to fabricate $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ PIN diodes. A new layout was designed that enabled (i) optical lithography on piece-samples, and (ii) a shadowed metal deposition process using line-of-sight deposition for contacting the bottom layer of the structure. The new process designed was a significant improvement over the ETD process because it reduced processing time by 15 hours and minimized series resistance by defining electrical contacts closer to the mesa. Chapter 4 uses the ETD process to fabricate PIN diodes that assess variation in $I_0$ with change in i-layer thickness and cross-sectional area of a diode.
Chapter 4

Dark Current Variation by Changing Intrinsic Layer Dimensions

This chapter investigates the effect of thickness of the intrinsic layer on leakage current and breakdown voltage of a PIN diode. Electrical results are compared with dark currents of photodetectors investigated in literature. Also, the area dependence of leakage current is investigated. Sec. 4.1 contains layer structures of the PIN samples used in this thesis. Sec. 4.2 and Sec. 4.3 describe the fabrication and testing of the pieces and discuss the electrical behavior of different samples.

4.1 PIN Structures Used in the Study

This section provides details of the different PIN structures that have been used in this study. All the structures are vertically grown homojunction In$_{0.53}$Ga$_{0.47}$As PINs that were grown using Molecular Beam Epitaxy at Texas State University, San Marcos. The growth nomenclature, dopant type and density have been identified in Table 4.1.

All the samples were grown on a 3-inch lattice matched InP substrate. The n$^+$ and p$^+$ layers were degenerately doped with the dopants in all the structures being Si and Be, respectively. PIN1 had an i-layer thickness of 50 nm. The n$^+$ drain was 30 nm thick and doped with Si at $3 \times 10^{19}$ cm$^{-3}$. The p$^+$ source was 300 nm thick and doped with Be at $1 \times 10^{19}$ cm$^{-3}$. 
PIN2 had an i-layer thickness of 100 nm. The n\textsuperscript{+} drain was 30 nm thick and doped with Si at \(3 \times 10^{19}\) cm\textsuperscript{-3}. The p\textsuperscript{+} source was 300 nm thick and doped with Be at \(1 \times 10^{19}\) cm\textsuperscript{-3}. PIN1 and PIN2 were used for the studying the dependence of dark current on the i-layer thickness. PIN3 had an i-layer thickness of 100 nm. The n\textsuperscript{+} drain was 300 nm thick and doped with Si at \(1 \times 10^{19}\) cm\textsuperscript{-3}. The p\textsuperscript{+} source was 300 nm thick and doped with Be at \(1 \times 10^{19}\) cm\textsuperscript{-3}.

PIN4 had an i-layer thickness of 100 nm. The n\textsuperscript{+} drain was 30 nm thick and doped with Si at \(3 \times 10^{19}\) cm\textsuperscript{-3}. The p\textsuperscript{+} source was 30 nm thick and doped with Be at \(1 \times 10^{19}\) cm\textsuperscript{-3}. Various surface treatments and passivation techniques were performed on PIN4 to minimize surface leakage current and minimize overall \(I_0\).

<table>
<thead>
<tr>
<th>Document Name</th>
<th>Group Name</th>
<th>Growth Name</th>
<th>Layer Structure</th>
<th>Thickness [nm]</th>
<th>Dopant [cm\textsuperscript{-3}]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN1</td>
<td>PIN0-D</td>
<td>TSU 5-2560</td>
<td></td>
<td>30</td>
<td>Si</td>
</tr>
<tr>
<td></td>
<td></td>
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<td>300</td>
<td>Be</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>(1 \times 10^{19})</td>
<td></td>
</tr>
<tr>
<td>PIN2</td>
<td>PIN0-F</td>
<td>TSU 5-2562</td>
<td></td>
<td>30</td>
<td>Si</td>
</tr>
<tr>
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<td></td>
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<td></td>
<td>100</td>
<td>(3 \times 10^{19})</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>300</td>
<td>Be</td>
</tr>
<tr>
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<td></td>
<td>(1 \times 10^{19})</td>
<td></td>
</tr>
<tr>
<td>PIN3</td>
<td>PIN0-A</td>
<td>TSU 1474</td>
<td></td>
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</tr>
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<td>PIN4</td>
<td>PIN0-E</td>
<td>TSU 5-2561</td>
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<td>Si</td>
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<td>(3 \times 10^{19})</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>30</td>
<td>Be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(1 \times 10^{19})</td>
<td></td>
</tr>
</tbody>
</table>

### 4.2 Fabrication

PIN1 and PIN2 were used in the experiment to analyze the dependence of \(I_0\) on i-layer thickness. The two structures are In\textsubscript{0.53}Ga\textsubscript{0.47}As homojunction PINs that differ in the i-layer thickness—50 nm and 100 nm, respectively. Table 4.1 details the layer
Chapter 4. Dark Current Variation by Changing Intrinsic Layer Dimensions

thicknesses (nm), dopant type and density (cm$^{-3}$) in the PINs used for the study. The fabrication followed the standard ETD Fabrication process explained in Sec. 3.2. The diodes were square patterns in the e-beam layout with the edge length ranging from 500 nm in row 1 to 2.4 µm in row 10. The mesa in PIN1 was etched for 73 s to etch 80 nm In$_{0.53}$Ga$_{0.47}$As. The mesa etch for PIN2 was done for 118 s to etch 130 nm In$_{0.53}$Ga$_{0.47}$As.

To analyze area dependence of $I_0$, PIN1, PIN2 and PIN3 with layer structures as shown in Table 4.1 were used. The primary difference between the two layer structures was that the n$^+$-doped region was 30 nm in PIN2 and 300 nm in PIN3. A 100 nm i-layer thickness was similar for both the samples. The fabrication process outlined in Sec. 3.2 was used. PIN2 was etched for 118 s to remove 130 nm In$_{0.53}$Ga$_{0.47}$As and PIN3 was etched for 6 min, 4 s to create a 400 nm deep mesa.

Taking into consideration a large undercut—to the order of 250 nm in large devices to 450 nm in small devices—the mesa sizes for PIN3 were modified by increasing the edge length for devices of all rows by 1 µm.

4.3 Electrical Analysis

Electrical testing was done on the Keithley 4200 SCS parameter analyzer that performed force and sense measurements on the device. For testing, metal probes 2 µm in diameter were used to contact the top metal over the mesa, and the bottom of the sample was contacted using the chuck. Leakage current measurements of the reverse biased PINs are a function of proper grounding of the system, shielding of the test-setup and the system settling time.

In the Keithley, the test was performed in a metal enclosure (Fig. 4.1a) that eliminated RF interference from surrounding areas. The enclosure also ensured testing in a dark environment as light can strike the PIN generating $e^-\cdot h$ pairs disturbing the leakage floor. Cables are another likely source of noise in the measurements. A
general advice is to use triaxial cables and keeping them as short as possible.

Figure 4.1: (a) Keithley Test Setup showing an optical microscope on a probe station. The probes are connected to the parameter analyzer via triaxial cables. The whole testing equipment is shielded inside a metal enclosure. (b) $I - t$ plot [Keithley 4200 Manual] characterizing system settling time after application of a 10 V step voltage. Transient current immediately after the voltage step decays to steady current. The time constant is the time the current takes to settle down to $1/e$ of the initial value. Higher the dielectric absorption and/or resistivity of the material, higher is the settling time.

The system settling time (Fig. 4.1b) is the time that current takes to reach a steady state value and is mainly a function of the inherent capacitance in the switch relays. It is also a function of the resistivity of the material. If the measurement speed is higher than the system settling time, then the measured current is not the leakage current but the transient current leading to wide fluctuations and erroneous results.

On an average, 100–120 devices were tested for each sample to generate a dataset.
Because of a high settling time as a consequence of a highly resistive i-layer in the reverse bias, the time taken to perform one $I-V$ sweep ranged from 1.5 minutes for big devices (when currents were in the 10 $\mu$A range) to 5 minutes in the smallest devices (current in the 100 fA range). In the whole process, device testing had been most time-intensive part.

**Figure 4.2:** $I-V$ characteristics of PIN1 (50 nm i-region) and PIN2 (100 nm i-region). The curves compare devices of edge length 2 $\mu$m, 1.2 $\mu$m and 800 nm. In the forward bias (left half), the current in PIN1 is limited by series resistance. From -0.3 to 0 V, both devices show a similar trend dominated by carrier recombination in the i-region. Early on in the reverse bias (right half), PIN1 shows a higher leakage floor dominated by bulk SRH G-R which is taken over by mid-gap tunneling beyond 0.4 V.

Typical PIN $I-V$ characteristics have been shown in Fig. 4.2. The plots show forward bias on the left half and the reverse bias on the right half. The forward bias (left half) voltage is negative because of the way the SCS measured applied voltage.

Devices from Rows 10 (maximum current in the forward bias), Row 8 and Row 4 were tested from PIN1 and PIN2. The mask defined edge lengths for the devices are 2 $\mu$m, 1.2 $\mu$m and 800 nm respectively. The maximum current in the forward bias was seen in Row 10 devices, that have a mask defined edge length of 2 $\mu$m, followed by Row 8 devices (1.2 $\mu$m) and Row 4 devices (800 nm).
Forward current in Row 4 PIN1 devices is 2 orders lower when compared to PIN2 devices of the same size—much less than expected. This has been attributed to series resistance added by unetched BCB between the probe and top metal on the mesa.

A steady reverse bias current was observed for PIN2—10 pA for a 800 nm device at a bias point of 0.5 V, translating to a current density of $1 \times 10^{-4}$ A/cm$^2$. PIN1 showed exponentially increasing leakage (linear on a log scale) from 0.1 V, an indication of midgap tunneling and Poole-Frenkel mechanism as the field is not yet strong enough to tunnel carriers from the valence band to conduction band. Rows 8 and 4 have a similar curve as Fig. 2.10d, which characterizes the regions for SRH G-R, midgap tunneling and BTBT.

It was also observed that the off-current floor, defined by SRH Generation current, is higher in PIN1 that has a 50 nm i-layer by 1.5 orders of magnitude than PIN2 with a 100 nm i-layer. This could be because carriers, when generated, were carried away by the field across the intrinsic layer before they had time to recombine. In the case of PIN2, some electrons would have lost their energy as there would be a higher probability of scattering through the i-layer and recombine with holes to reduce the off-current in the particular device.

Because of a 50 nm i-layer, avalanche breakdown occurs at 0.8 – 0.9 V in PIN1 and 1.5 V in PIN2 (100 nm i-region). Contrasting with PIN devices used as photodetectors, avalanche breakdown occurs at a reverse bias of more than 40 V because of a wider intrinsic region ranging from 1 μm [18] to 10 μm. To further minimize $I_0$, i-region width can be increased, but that would mean (i) added series resistance in ON-state, and (ii) a high aspect ratio of the vertical PIN structure that can result in the devices with small cross-sectional area breaking off of the substrate during processing.

The plot in Fig. 4.3 compares $I_0$ normalized by area ($J_0$) of PIN1,2 and 3 with different vertically grown PINs in literature as a function of intrinsic layer thickness.
Chapter 4. Dark Current Variation by Changing Intrinsic Layer Dimensions

It was observed that $I_0$ dropped exponentially with an increase in i-layer thickness—almost 6 orders drop in current over 2 decades of i-layer thickness.

**Figure 4.3:** Comparison of $I_0$ normalized by area (A/cm$^2$) for the samples used in this experiment and in literature. The general trend predicted was that bulk leakage rises exponentially as the width of the i-region decreases. LM - Lattice Matched. LG - Linearly Graded. SG - Step Graded.

For the experimental data, current measurements were taken at room temperature and 0.5 V (reverse bias). The data points from literature have been taken over a wide range of temperatures (77 K to 448 K) and bias (0.5 V to 10 V). In addition, different substrates and materials were also used in the dataset obtained from literature. Ray-ming *et al.* [35] fabricated PIN diodes on InAs, whereas Jang *et al.* [18] fabricated In$_{0.53}$Ga$_{0.47}$As PIN diodes on a lattice matched (LM) InP substrate and on different substrates with a linearly graded (LG) buffer and a step graded (SG) buffer. Fig. 2.8 shows significant increase in $I_0$ as the substrates change from LM to LG to SG as a result of increasing defect density in the bulk of the device.

It was observed that PIN2, PIN3 and Mookerjea *et al.* [16] were slightly below the
trend-line because of certain surface passivations (discussed later in Chapter 5) and gate control over the i-region, respectively. This study reported a low current density of $3 \times 10^{-5}$ A/cm$^2$—an order of magnitude lower than [16], which had been used to realize a TFET.

Figure 4.4: Area dependence of current in PIN1 (square) and PIN2 (star). In a device, $I_0$ can be reduced by scaling the area of a device which reduces the bulk leakage current.

Fig. 4.4 depicts current scaling with area in PIN1 and PIN2. The current was obtained at a reverse bias of 0.5 V as current at this voltage is dominated by SRH G-R and TAT. Both the curves follow a linear trend that show an increasing current with an increase in area. The supports the argument that leakage current is a bulk phenomenon. Therefore to obtain a low leakage current in TFET devices, the first thing to be done should be reduction in the cross-sectional area of a PIN diode.

As a part of this study, for the first time, electrical characterization was performed
on sub-micron PIN diodes (devices with area less than $1 \times 10^{-8}$ cm$^2$ in Fig. 4.4). The smallest tested device in PIN1 had a mesa cross-sectional area of 0.05 µm$^2$.

However, as the cross sectional area was scaled down, the area to perimeter ratio reduced and the current did not follow the same linear trend that was being followed for large area diodes. It was observed that the perimeter of the device played an ever-increasing role in controlling the surface leakage component of $I_0$ in sub-micron PIN diodes. The origins of surface leakage and possible methods to reduce it have been discussed in Chapter 5.
Chapter 5

Surface Leakage and Treatments

Chapter 4 reported the impact of scaling the cross-sectional area and the i-layer thickness on $I_0$. For large area diodes, bulk leakage was established as the dominant factor in $I_0$. This chapter investigates different forms of leakage current caused by dangling bonds and surface oxidation in a sub-micron PIN diode. A theory has been proposed that could extract bulk leakage current and surface leakage current using a first-order mathematical approach. Sec. 5.1 investigates bulk and surface current using the ETD pattern and Sec. 5.2 looks at surface cleans and passivation techniques to reduce surface currents.

5.1 Surface Leakage vs. Bulk Leakage

5.1.1 Fabrication

Samples PIN1, PIN2 and PIN3 will be used to analyze different forms of leakage current—bulk leakage paths and surface trap states. The samples were fabricated using the ETD pattern with the steps detailed in Sec. 3.2. The mesas in PIN1, PIN2 and PIN3 were etched 80 nm, 130 nm and 430 nm deep, respectively.
5.1.2 Mathematical Model

As a part of this study, a theory was proposed that could extract surface leakage density \( (A/\mu m) \) and bulk leakage density \( (A/cm^2) \) mathematically from raw \( I-V \) data, standardizing the comparison between the surface cleans and passivation.

In this model, measured current can be represented as the sum of the cross-sectional area \( (A) \) times bulk current density \( (J_B) \) and perimeter \( (P) \) times surface current density \( (J_S) \).

\[
I = A \cdot J_B + P \cdot J_S \tag{5.1}
\]

Assuming a square device (edge length \( W \mu m \)), the equation can be represented as,

\[
I = W^2 \cdot J_B + 4W \cdot J_S \tag{5.2}
\]

Dividing both sides by \( W \),

\[
\frac{I}{W} = W \cdot J_B + 4 \cdot J_S \tag{5.3}
\]

This is the equation of a straight line where measured current per unit edge length, \( I/W \) can be plotted against edge length, \( W \) of the device. The slope of the line gives bulk current density and the y-intercept gives the surface current density. In the case of diodes with varying areas and perimeters, the above equation can be represented as,

\[
\frac{I}{P} = J_1 = J_S + \left( \frac{A}{P} \right) \cdot J_B \tag{5.4}
\]

where, \( J_1 \) is measured current per unit perimeter \( (A/cm) \). This equation for extraction of the different components of leakage current is a first order approximation that does not account for current mechanisms that are common to both the bulk and
the surface. Also, there may be bulk or surface dark currents that could be dependent on higher orders of area and perimeter. Due to time limits and non-availability of other methods of analysis of dark current, this study has tried to use the first-order approximation to characterize the different surface cleans and passivation in Sec. 5.2.

5.1.3 Electrical Analysis

Fig. 2.5 demonstrates current scaling with area which signifies that bulk current dominates dark current in the case of large sized devices where the area to perimeter ratio is high. In the case when the dimensions are scaled down to a couple of microns, the area to perimeter ratio reduces as shown in Fig. 5.1. The dominance of perimeter over area correlates to surface leakage being the dominating factor in dark current.

Fig. 5.2 plots current per unit perimeter, $J_1$, against edge length of the device for PIN1 and PIN2. Using Eq. (5.3), bulk and surface leakage can be defined by the slope and the y-intercept of the dataset. The primary observation was that the slopes of the two datasets were different, with PIN1 being higher than PIN2, and the y-intercepts of the two datasets were different—with the PIN1 intercept more than

Figure 5.1: Change in the area to perimeter ratio with scaling device dimensions. The impact of perimeter increases as the dimensions are scaled down. In a PIN diode, it means there is a greater impact of surface leakage on the total dark current.
Figure 5.2: $J_1$ vs. $W$ for PIN1 and PIN2 comparing bulk and surface leakage mechanisms in the two samples.

For smaller dimensions in PIN1 (with edge lengths less than $6 \times 10^{-5}$ cm), the curve leveled out and did not follow the standard current scaling as would be expected in a bulk leakage dominated device. This discrepancy was attributed to surface leakage caused by dangling bonds and surface oxidation. Had there been no surface impact on $I_0$, the curve for PIN1 would have intercepted the y-axis much lower—in the range...
of $1 \times 10^{-7}$ A/cm.

The leveling off of current was not clearly visible in PIN2, indicating that the dominance of surface leakage begins in a device of edge length 500-600 nm. At this size, the area to perimeter ratio is 0.125 ($\mu$m).

![Figure 5.3: $J_1$ vs. $W$ for PIN1 and PIN3 comparing bulk and surface leakage mechanisms in the two samples.](image)

Fig. 5.3 plots $J_1$ against edge length for PIN1 and PIN3. PIN3 with the 100 nm i-region showed a clear difference in slope from PIN1 and even showed lower bulk leakage than PIN2 (Fig. 5.2). It was hypothesized that the 300 nm thick top n$^+$ layer was more forgiving to the impact of DC sputter while depositing Mo. PIN2 showed a higher bulk leakage current which was attributed to lattice damage to the 30 nm n$^+$ layer at the top that went through to the i-layer possibly increasing the SRH G-R. The y-intercepts in Figs. 5.2 and 5.3 show that PIN2 and PIN3 had similar surface leakage current.
Chapter 5. Surface Leakage and Treatments

This experiment established the different nature of bulk and surface current and how it affects $I_0$ as a device is scaled. With surface leakage playing a major role in $I_0$ of sub-micron diodes at the operational bias of 0.5 V, it was of prime importance to minimize the dangling bonds and surface oxidation by various surface treatment techniques that have been discussed in Sec. 5.2.

5.2 Surface Treatments and Passivation Techniques

The primary objective of this study is to implement surface cleaning and surface passivation techniques that would ensure a low dark current density in diodes. In addition, the techniques will also address the problem of current spreading at high reverse bias. Issues like lattice damage, surface oxidation and dangling bonds contribute to surface leakage. While the former two are process-induced, the latter two are a function of the material at the surface.

In the process flow, as shown in Fig. 3.3, the mesa etch is followed by an area analysis step - in which the cross-sectional images are captured on the SEM, like the one showed in Fig. 3.8, to assess the undercut of the semiconductor. This subjects the active area of the diode to radiation, causing possible lattice damage. In addition, the surface of the mesa structure gets oxidized when exposed to air, which in the case of In$_{0.53}$Ga$_{0.47}$As is In$_x$O$_y$ and Ga$_x$O$_y$ that is conductive and creates a surface short.

The cleans used in this experiment were (i) an HCl based clean (10:1 DI H$_2$O:HCl) [37, 47] and (ii) Citric acid etch (20:1 Citric Acid:H$_2$O$_2$) [45]. Surface passivation is done to tie up the dangling bonds with other atoms. Passivation also helps in eliminating or reducing surface contact with oxidizing media. In this experiment, (i) an ammonium sulfide passivation treatment [48, 49], and (ii) BCB passivation have also been studied. BCB has been widely used in III-V devices for planarization [49] and this work explores its passivation properties.
5.2.1 Fabrication

The following section details the fabrication of PIN devices on sample PIN4. This study provides insight on the dependence of dark current on the area to perimeter ratio. Mo was deposited on the top and bottom of the sample to form cathode and anode, respectively. The overgrowth mask was patterned on HPR 504 using a GCA lithography step.

The Overgrowth GCA pattern was used for the fabrication in which the top half of the pattern varies the perimeter of the device but maintaining the same area for a given set of devices (Fig. 5.4a). The bottom half of the pattern maintains a constant perimeter but the area is varied (Fig. 5.4b).

The top metal was etched in the Drytek Quad using the standard recipe (see Sec. 3.1.4). The resist was stripped after a 30 s dip in acetone, followed by a quick rinse in IPA and water. The mesa etch was timed for 118 s to etch the top 130 nm, after which each iteration received separate treatments (Table 5.1).

PIN4(CONTROL) was tested directly after the etch.

PIN4(BCB-OVE) was coated with BCB and cured using standard recipe. Since the overgrowth pattern has small devices that are widely spaced with no grid, the
Table 5.1: Experiment Set - Surface Clean and Passivation. \( \Delta \) - Overetched BCB Sample. \( \Theta \) - Liftoff Sample.

<table>
<thead>
<tr>
<th>Sample</th>
<th>HCl Clean</th>
<th>Citric Etch</th>
<th>AP 3000</th>
<th>BCB</th>
<th>Sulfide</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(CONTROL)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PIN4(BCB-OVE)( \Delta )</td>
<td>-</td>
<td>-</td>
<td>Y</td>
<td>Y</td>
<td>-</td>
</tr>
<tr>
<td>PIN4(LIFT) ( \Theta )</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PIN4(BCB-LIFT) ( \Theta )</td>
<td>-</td>
<td>-</td>
<td>Y</td>
<td>Y</td>
<td>-</td>
</tr>
<tr>
<td>PIN4(HCL)</td>
<td>Y</td>
<td>-</td>
<td>Y</td>
<td>Y</td>
<td>-</td>
</tr>
<tr>
<td>PIN4(CITRIC)</td>
<td>-</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>-</td>
</tr>
<tr>
<td>PIN4(BCB)</td>
<td>Y</td>
<td>-</td>
<td>Y</td>
<td>Y</td>
<td>-</td>
</tr>
<tr>
<td>PIN4(BCB-NoAP)</td>
<td>Y</td>
<td>-</td>
<td>-</td>
<td>Y</td>
<td>-</td>
</tr>
<tr>
<td>PIN4(SULFIDE)</td>
<td>-</td>
<td>Y</td>
<td>-</td>
<td>-</td>
<td>Y</td>
</tr>
</tbody>
</table>

etchback did not progress as it had on previous samples. Visual inspections using an optical microscope after 3 min + 4 min + 3 min showed small sized devices still covered with BCB (unlike the usual 7 min etch for the “battleship-game” grid layout in previous experiments). After an additional 3 min etch, it was observed that the BCB had overetched from all the devices and the surrounding field, exposing the mesa sidewall to an \( \text{O}_2 \) plasma during the process.

PIN4(HCL) and PIN4(CITRIC) underwent the same treatment as PIN4(BCB-OVE). After the overetch, PIN4(HCL) was given a 60 s 10:1 DI \( \text{H}_2\text{O}:\text{HCl} \) dip and PIN4(CITRIC) was given a 15 s citric acid treatment (pure citric acid — no \( \text{H}_2\text{O}_2 \)). The devices were tested immediately after the treatments. After understanding the disadvantages of BCB overetch, a second set of PIN4 samples were processed.

Up to the mesa etch, the samples were processed similarly as their predecessors. After the citric etch and before BCB coat, PIN4(BCB) and PIN4(BCB-NoAP) were subjected to a 60 s HCl dip, with great emphasis on minimizing transit time between subsequent steps. In PIN4(BCB-NoAP), BCB was applied directly on the sample without priming it with AP 3000, to see if the mobile ions (\( \text{Na}^+ \), \( \text{K}^+ \)) in the adhesion promoter play a part in increasing the surface leakage of a PIN diode.

The BCB was etched for 3 min + 3 min + 2 min + 1.5 min + 0.5 min, with the color
of BCB on the metal dots closely monitored after every iteration. Still a thin coat was left on the devices, which could be removed during probing.

PIN4(SULFIDE) received sulfide treatment immediately after the citric acid etch. Sulfur in ammonium sulfide, \((\text{NH}_4)_2\text{S}\), is known to passivate dangling bonds at III-V surfaces [48,49]. The sample was dipped in the ammonium sulfide solution for 10 mins, followed by a quick rinse in IPA and water. The samples were tested immediately afterwards.

Because the initial version of the overgrowth mask was a dark field mask and only a positive tone g-line resist was available, PIN4(LIFT) and PIN4(BCB-LIFT) were prepared using liftoff. In this process, the bottom metal had been deposited on the sample, and a double resist stack of LOR 5A and HPR 504 was coated on the top surface of the sample. After the GCA exposure and a 45 s develop in CD-26, 200 nm Mo was sputtered on the sample. After the blanket deposition, the excess Mo was lifted off in Remover PG chemistry using the standard liftoff recipe detailed in Section 3.1.2. After the liftoff, the mesa was etched for 118 s to etch the n$^+$ doped and intrinsic In$_{0.53}$Ga$_{0.47}$As layers. PIN4(LIFT) was tested after the mesa etch and PIN4(BCB-LIFT) was given standard BCB treatment and etchback after which it was tested.

The samples were also tested four days and eight days after the fabrication process had been completed to further understand the effect of treatments on their performance.

For analysis and comparison of different treatments, a current reading at a reverse bias of 0.5 V was used. The reason for choosing the particular bias point is that $I_0$ in this region is dominated by TAT and BTBT. Since TAT is majorly a surface phenomenon, the effect of surface cleans and passivation would be clearly demonstrated.
5.2.2 Irregularities in Data

Before proceeding with the analysis, it would be helpful to underline some reasons for irregularities in obtaining data, which were mainly the technical limitations with the maskset, probing issues, BCB etchback and wearing out of top metal.

The overgrowth pattern had been written for a previous version of the GCA stepper, which necessitated fiducial marks in the middle of opposite edges of the mask plate, unlike the current GCA masks, where they are supposed to be slightly off-centered on the opposite edges. This makes it challenging to align multiple mask levels for this pattern.

Testing of devices on Keithley 4200 parameter analyzer was performed using probes that have a tip diameter of 2 $\mu$m. Testing devices that have the top metal pad in that range (2–4 $\mu$m) may result in metal peel-off or in extreme cases, device breaking off from the substrate. If the probe lands in the field, it scratches the BCB, which then sticks to the tip of the probe.

Underetched BCB has resulted in a plethora of problems related to the probes. In PIN4(BCB) and PIN4(BCB-NoAP), BCB was intentionally left on the top metal to ensure complete encapsulation of sidewall. To electrically test a device, a thin layer of BCB had to be scratched from the ensure a proper contact. The scratched BCB ended up sticking to the probes making it challenging to take further measurements because of (i) the inability to contact the top metal in some cases, and (ii) added series resistance when contact to the Mo was made, but with residual BCB on the probe tip. In some cases, when the BCB was scratched on Day 1, it was removed in flakes, accidentally exposing the sidewall and confounding the data when the devices were probed on subsequent days.

Probing a device multiple times led to damage and fracturing of the metal. Hence, a majority of Day 4 and Day 8 results have resulted in a large variation in collected data.
5.2.3 BCB Passivation

This section investigates the effectiveness of BCB passivation in reducing $I_0$ of a diode. BCB had been traditionally used as a planarizing material and as a low-$\kappa$ ILD to minimize parasitic capacitances in vertical devices. In this experiment, PIN4(CONTROL) and PIN4(BCB) were used. All the data points were obtained at a reverse bias of 0.5 V. PIN4(CONTROL) did not undergo any surface current reduction treatment and hence was chosen as the control sample. PIN4(BCB) was coated and cured with BCB (Table 5.1).

![Image of J1 vs. Area:Perimeter and a box plot](image)

(a) $J_1$ vs. Area:Perimeter. PIN4(BCB) - Red and PIN4(CONTROL) - Black

(b) Median represented by mid-line in the box. The box represents the middle 50% of the particular dataset.

**Figure 5.5:** BCB Treatment. Comparison of $J_1$ in a control sample with a sample treated with BCB. Current drops 4 orders of magnitude in PIN4(BCB).

<table>
<thead>
<tr>
<th>Sample</th>
<th>Sample Size</th>
<th>$J_1$ Median $\left[ \frac{A}{cm} \right]$</th>
<th>$J_1$ St. Dev. $\left[ \frac{A}{cm} \right]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(CONTROL)</td>
<td>97</td>
<td>$1.3 \times 10^{-4}$</td>
<td>$3.62 \times 10^{-4}$</td>
</tr>
<tr>
<td>PIN4(BCB)</td>
<td>74</td>
<td>$5.2 \times 10^{-8}$</td>
<td>$4.8 \times 10^{-7}$</td>
</tr>
</tbody>
</table>

**Table 5.2:** BCB Treatment. Comparison with Control.

Fig. 5.5 shows surface leakage current (A/cm) of the device that did not receive any treatment (PIN4(CONTROL) — black) and the device that received BCB passi-
viation (PIN4(BCB) — red). The sample size and variation in data has been reported in Table 5.2.

An even spread of data points was reported for PIN4(CONTROL) across three orders of magnitude in Fig. 5.5a, making it difficult to generate a trend. PIN4(BCB) shows a much more concise data set with a positive slope. The abscissa of Fig. 5.5a represents the area to perimeter ratio and the ordinate denotes measured current normalized by perimeter. Using Eq. (5.4), the y-intercept of the plot gives the surface leakage current density, $J_S$ (A/cm) and the slope of the plot gives the bulk current density, $J_B$ (A/cm$^2$). However, with the spread of the data because of the several issues outlined in Sec. 5.2.2, the theorized trend was not observed clearly.

It was observed from Fig. 5.5a that the distribution is much tighter in PIN4(BCB) (BCB) over a range of area perimeter ratios emphasizing the ill-effect of exposing the sidewall surface to atmosphere resulting in conductive oxides.

Qualitatively, it can be seen from Fig. 5.5a that as the area begins to dominate the perimeter (moving from left to right on the x-axis), the effectiveness of the clean was not that evident in PIN4(BCB) and the current was much closer to PIN4(CONTROL), suggesting bulk current domination which would be similar in both devices.

A box plot variation of the dataset has been shown in Fig. 5.5b in which the effectiveness of the passivation is shown by the dark current dropping 4 orders of magnitude—from $1.3 \times 10^{-4}$ A/cm in the control sample to $5.2 \times 10^{-8}$ A/cm in the sample passivated with BCB, PIN4(BCB). The midline in the box plot represents the median of the dataset and box represents the interquartile range (IQR) of the dataset that depicts the middle fifty percent of the data. The whiskers extending from the box represent the maximum and minimum of the dataset. In statistical analysis, the IQR is a better tool to analyze the spread of the data than the maximum-minimum range.
Fig. 5.6 compares the variation of off-current of the two samples over a period of time. In this study, $I-V$ data recorded on Day 1 (right after the fabrication), Day 4 and Day 8 to was compared to (a) assess surface oxidation over time, and (b) the effectiveness of passivation over time.

![Graph showing the comparison of current variation with time for PIN4(CONTROL) and PIN4(BCB).](image)

(a) No Treatment  
(b) BCB Treatment

**Figure 5.6:** Surface leakage current (A/cm) variation with time. While the control sample shows severe uniform degradation across all devices because of increased surface oxidation, the BCB sample shows a slightly dispersed spread but a lower median value of $J_1$.

**Table 5.3:** BCB Treatment. $J_1$ [A/cm] Degradation with time.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Day 1</th>
<th>Day 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(CONTROL)</td>
<td>$1.3 \times 10^{-4}$</td>
<td>$5.2 \times 10^{-8}$</td>
</tr>
<tr>
<td>PIN4(BCB)</td>
<td>$5.2 \times 10^{-8}$</td>
<td>$3.5 \times 10^{-8}$</td>
</tr>
</tbody>
</table>

From Day 1 to Day 4, $I_0$ increased from $4 \times 10^{-6}$ A/cm to $1 \times 10^{-4}$ A/cm indicating sidewall surface oxidation resulting in formation of conductive In$_x$O$_y$ and Ga$_x$O$_y$. The current spread was confined from 4 orders of magnitude on Day 1 to one order spread on Day 4. It was observed that the lower IQR has shifted by more than three orders from Day 1 to Day 4. All the devices in PIN4(CONTROL) performed worse on Day 4 than on Day 1. Day 8 measurements looked similar to Day 4 suggesting that there was little or no surface oxidation post Day 4.
In PIN4(BCB), it was observed that the variation in data increased from Day 1 to Day 4 but $I_0$ dropped (marginally). Because of the contrasting data, it cannot be said that BCB passivation improves over time, but it can be concluded that BCB passivation was successful in maintaining $I_0$ at a low value. Day 8 measurements on PIN4(BCB) gave confounding results since most resulted in open circuits. This cannot be a passivation phenomenon because carrier transport in the bulk of the device is not affected by the passivation. It could have happened if the Mo contact had been oxidized by BCB, adding a large (infinite) series/contact resistance in the device.

5.2.4 BCB Overetch

The benefits of BCB passivation have been reported in Sec. 5.2.3. This section investigates the effects of exposing the mesa sidewall to an oxygen plasma on $I_0$ of a diode by overetching the BCB layer. In this experiment, PIN4(CONTROL) and PIN4(BCB-OVE) were used. All the data points were obtained at a reverse bias of 0.5 V. PIN4(CONTROL) did not undergo any surface current reduction treatment and hence was chosen as the control sample. PIN4(BCB-OVE) was coated and cured with BCB, but etched back for 13 min using the standard recipe (3.1.7), exposing significant amount of mesa sidewall to an $O_2$ plasma (Table 5.1).

Fig. 5.7a shows a scatter plot of surface leakage current, $J_1$ (A/cm) that compares $I_0$ in the overetched BCB sample (PIN4(BCB-OVE)) to the control sample. In the graph, $J_1$ has been plotted against the ratio of area to perimeter to compare surface leakage in the two devices. A statistical comparison is shown in Table 5.4.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Sample Size</th>
<th>$J_1$ Median $\left[ \frac{A}{cm} \right]$</th>
<th>$J_1$ St. Dev. $\left[ \frac{A}{cm} \right]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(CONTROL)</td>
<td>97</td>
<td>$1.3 \times 10^{-4}$</td>
<td>$3.62 \times 10^{-4}$</td>
</tr>
<tr>
<td>PIN4(BCB-OVE)</td>
<td>107</td>
<td>$1.15 \times 10^{-2}$</td>
<td>$1.16 \times 10^{-2}$</td>
</tr>
</tbody>
</table>
Chapter 5. Surface Leakage and Treatments

Figure 5.7: Effect of O\textsubscript{2} plasma on mesa sidewall in a BCB etchback (red) process. Surface leakage increases by 2 orders of magnitude in PIN4(BCB-OVE).

An even spread of data points was reported for PIN4(CONTROL) across three orders of magnitude because of variation in the degree of surface oxidation of different diodes, making it difficult to generate a trend. PIN4(BCB-OVE) shows higher leakage than the control but a tighter distribution - suggesting further and more uniform oxidation of the mesa sidewalls in the O\textsubscript{2} plasma.

In comparison to the control, leakage in PIN4(BCB-OVE) increased by two orders of magnitude (Fig. 5.7b). The spread in both treatments looks similar - but while it is large due to a scattered dataset in PIN4(CONTROL), it is wide in PIN4(BCB-OVE) because of a linear trend as seen in Fig. 5.7a.

Qualitatively, it can be seen from Fig. 5.5a that as the area begins to dominate the perimeter (moving from left to right on the x-axis), the effect of the oxidized surface was not that evident in PIN4(BCB-OVE) and the current was much closer to PIN4(CONTROL), suggesting domination of bulk current - which would be similar in both devices.

As a part of this experiment, the thickness of BCB was co-related to the color...
observed during optical inspection, so as to have a fair idea on when to stop the BCB etchback process in samples that do not have big metal pads to inspect the clearing off of BCB.

After 13 mins (3+4+3+3) of BCB etchback, the thickness of BCB in areas that showed blue, pink and yellow colors (Fig. 5.8) were recorded using a Nanometrics 210 Spectrophotometer (Nanospec). The Nanospec shines light of different wavelengths on the sample and monitors the reflected light. The difference in the wavelength at which the first peak and the first valley occurs is used to give the film thickness. The Nanospec takes the refractive index of the material as the input. The refractive index of BCB is 1.54 [BCB Curing and RI] based on the BCB cure time and temperature. 5 – 7 points were measured for each color and the average thickness was recorded (Table 5.5).

![Figure 5.8: 20x photomicrograph showing different colors of BCB on sample PIN4(BCB-OVE). (L to R) Pink, Blue and Yellow. Devices denoted by white squares in the field.](image)

<table>
<thead>
<tr>
<th>Color</th>
<th>Avg. Thickness [Å]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pink</td>
<td>2470</td>
</tr>
<tr>
<td>Blue</td>
<td>1321</td>
</tr>
<tr>
<td>Yellow</td>
<td>&lt; 1000</td>
</tr>
</tbody>
</table>

Table 5.5: BCB Thickness Chart. Thickness should lie between 1300 Å(height of the mesa) and 3300 Å(height of mesa + top metal).

In order to passivate the structure and avoid additional series resistance during testing, the ideal thickness of the BCB layer should be between 1300 Å, which is the height of the mesa in PIN4 and 3300 Å, which is the sum of the height of the mesa and the thickness of the top metal. From Table 5.5, a BCB film with color ranging
between pink (2470 Å) and blue (1321 Å) should have the mesa encapsulated and the metal exposed (white when looked at under an optical microscope - 5.8). A major part of PIN4(BCB-OVE) had a BCB film that was yellow in color. The Nanospec readings ranged from 500 to 900 Å, clearly much thinner than the mesa. In these regions, the BCB had been overetched and the mesa had been exposed to an O\textsubscript{2} plasma, damaging and oxidizing the sidewall, and increasing the \( I_0 \) of the PIN.

### 5.2.5 Sulfide Treatment

This section reports sulfur passivation of mesa sidewall using ammonium sulfide \((\text{NH}_4)_2\text{S}\) chemistry. A lot of work has been done on passivating large area PIN diodes \([48,49]\). In this work, sulfur passivation has been reported on devices of varying perimeters and has been benchmarked against other surface treatments, such as BCB passivation, HCl clean and citric etch. Degradation of sulfur passivation over time has also been studied and compared with transient effects of BCB passivation. In this experiment, PIN4(CONTROL) and PIN4(SULFIDE) were used. The control sample did not undergo any surface treatment and the latter was soaked in a \((\text{NH}_4)_2\text{S}\) solution for 10 mins.

Fig. 5.9a shows a scatter plot of surface leakage current, \( J_1 \) (A/cm) that compares \( I_0 \) in the sulfide sample (PIN4(SULFIDE)) to the control sample. In the graph, \( J_1 \) has been plotted against the ratio of area to perimeter to compare surface leakage in the two devices. A statistical comparison is shown in Table 5.6.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Sample Size</th>
<th>( J_1 ) Median ( \frac{A}{cm^2} )</th>
<th>( J_1 ) St. Dev. ( \frac{A}{cm^2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(CONTROL)</td>
<td>97</td>
<td>1.3\times10^{-4}</td>
<td>3.62\times10^{-4}</td>
</tr>
<tr>
<td>PIN4(SULFIDE)</td>
<td>84</td>
<td>2.37\times10^{-7}</td>
<td>7.47\times10^{-7}</td>
</tr>
</tbody>
</table>

\( J_1 \) in the control sample spanned from 2\times10^{-6} to 2\times10^{-3} A/cm without a definite trend. In PIN4(SULFIDE), the scatter points remained random but scaled down two
Figure 5.9: Sulfide Treatment. Comparison of $J_1$ in a control sample with a sample treated with (NH$_4$)$_2$S. Current drops 3 orders of magnitude in PIN4(SULFIDE) but the distribution still remains large.

to three orders of magnitude — $1 \times 10^{-8}$ to $4 \times 10^{-6}$ A/cm. The median was recorded at $2.37 \times 10^{-7}$ A/cm and the standard deviation was $7.47 \times 10^{-7}$ A/cm — high compared to the median and considering there was no observable increasing/decreasing trend in Fig. 5.9a.

From Day 1 to Day 4 (Fig. 5.10a), $I_0$ increased from $4 \times 10^{-6}$ A/cm to $1 \times 10^{-4}$ A/cm indicating sidewall surface oxidation resulting in formation of conductive In$_x$O$_y$ and Ga$_x$O$_y$. The current spread was confined from 4 orders of magnitude on Day 1 to one order spread on Day 4. It was observed that the lower IQR has shifted by more than three orders from Day 1 to Day 4. All the devices in PIN4(CONTROL) performed worse on Day 4 than on Day 1. Day 8 measurements looked similar to Day 4 suggesting that there was little or no surface oxidation post Day 4.

In PIN4(SULFIDE), it was observed that on Day 1 the majority of the distribution was contained within $1 \times 10^{-7}$ A/cm and $1 \times 10^{-6}$ A/cm, with the median at $2.3 \times 10^{-7}$ A/cm (Fig. 5.10b). On subsequent days, although the median remained the same,
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**Figure 5.10:** Surface leakage current (A/cm) variation with time. While the control sample shows severe uniform degradation across all devices because of increased surface oxidation, the sulfide sample shows a large dispersion but a similar median value of \( J_1 \) from Day 1 to Day 4. Day 8 measurements were similar to Day 4 measurements indicating that the mesa surface did not deteriorate further after Day 4.

the spread increased from one order of magnitude (on Day 1) to four orders on Day 4 and Day 8. This could be attributed to the fact that sulfur passivation deteriorates over time. The sulfur atoms that tie up the dangling bonds at the mesa sidewall either diffuse out into the atmosphere creating dangling bonds or are replaced by oxygen atoms that react with the In and Ga atoms to form conductive oxides. Devices that have larger perimeters have a higher probability of sulfur escaping into the atmosphere. The serpentine patterns in the overgrowth mask have a very high perimeter to area ratio, which could be responsible for an increase in the spread. However, as the area to perimeter ratio increased (moving towards a square mesa), current levels on Day 4 were similar to those on Day 1 — hence the median remained constant.

**Table 5.7:** Sulfide Treatment. \( J_1 \) [A/cm] Degradation with time.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Day 1</th>
<th>Day 4</th>
<th>Day 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(CONTROL)</td>
<td>4×10^{-6}</td>
<td>2×10^{-4}</td>
<td>1×10^{-4}</td>
</tr>
<tr>
<td>PIN4(SULFIDE)</td>
<td>2.3×10^{-7}</td>
<td>3.5×10^{-7}</td>
<td>3.5×10^{-7}</td>
</tr>
</tbody>
</table>

Fig. 5.15a shows a scatter plot comparing BCB passivation with sulfur passivation.
While BCB (red) shows a concise dataset with an increasing trend and an a median surface leakage of $5.2 \times 10^{-8}$ A/cm, surface leakage current in the sulfur passivated sample (blue) is spread out evenly over an order of magnitude without showing any particular trend.

### 5.2.6 Overetched BCB vs. HCl Clean and Citric Etch

This section reports the effectiveness of two surface cleaning chemistries — (i) HCl clean, and (ii) Cirtic etch in reducing $I_0$ in a PIN diode. For this experiment, PIN4(HCL) and PIN4(CITRIC) were used. These samples were co-processed with the overetched BCB sample, PIN4(BCB-OVE). Post the 13 min overetch, PIN4(HCL) was treated with a 10:1 DI H$_2$O:HCl for 60 s and PIN4(CITRIC) received a 15 s dip in citric acid solution (no H$_2$O$_2$). The two cleans were performed after the overetch of BCB on the samples. To gauge the effectiveness of the cleans, PIN4(BCB-OVE) was chosen as the control sample.

Fig. 5.11a shows a scatter plot of surface leakage current, $J_1$ (A/cm) that compares $I_0$ in the overetched BCB sample (PIN4(BCB-OVE)) before and after HCl treatment. In the graph, $J_1$ has been plotted against the ratio of area to perimeter to compare surface leakage in the two devices. A statistical comparison is shown in Table 5.4.

PIN4(BCB-OVE) (red) shows high leakage and a tighter distribution - suggesting uniform oxidation of the mesa sidewalls across all devices in the O$_2$ plasma. Post HCl clean (purple), $I_0$ values dropped by 1.5 orders of magnitude to $5.5 \times 10^{-4}$ A/cm (Fig. 5.11b). In addition, there was a set of devices across the range of area and perimeter ratios that demonstrated leakage current one to two orders lower than the median of the dataset. A possible explanation for this phenomenon could be that HCl removes native oxides from the In$_x$Ga$_{1-x}$As surface but does not passivate any dangling bonds that resulted in a leaky distribution. In some devices where there were little or no In or Ga dangling bonds, $J_1$ was reported on the order of $1 \times 10^{-6}$ A/cm.
Chapter 5. Surface Leakage and Treatments

(a) $J_1$ vs. Area:Perimeter. PIN4(BCB-OVE) - Red and PIN4(HCl) - Purple

(b) Median represented by mid-line in the box. The box represents the middle 50 % of the particular dataset.

**Figure 5.11:** HCl Treatment. Comparison of $J_1$ (A/cm) in an overetched BCB sample before and after a 60 s HCl clean. Current drops 1.5 orders of magnitude in PIN4(HCL). It was hypothesized that HCl removes native oxides but does not passivate/clean any dangling bonds.

It was observed that as the area begins to dominate the perimeter (moving from left to right on the x-axis), the effect of the oxidized surface was not that evident in PIN4(BCB-OVE) and current levels were similar to PIN4(HCL), suggesting domination of bulk current - which would be similar in both devices.

Fig. 5.12 demonstrates the effect of an HCl clean in PIN3. The top layer in PIN3 is n+ doped 300 nm thick followed by a 100 nm thick intrinsic layer. The black curves represent $I-V$ data of a set of PIN3 devices before the HCl clean. The devices were fabricated using the ETD Fabrication process. After a 60 s clean in 10:1 DI H$_2$O:HCl, the same set of devices were tested that gave reduced $I_0$ throughout the range of reverse bias (blue).

It was observed that at early reverse bias voltages, pre-clean testing showed elevated $I_0$ characterized by midgap tunneling [22]. At higher values of reverse bias, $I_0$ increases sharply indicative of the onset of BTBT at voltages close to the the energy bandgap of In$_{0.53}$Ga$_{0.47}$As (0.74 eV). Post-clean, the surface oxides were removed and

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Figure 5.12: Comparison of $I_0$ in PIN3 before (black) and after (blue) a 60 s HCl clean. HCl treatment reduces surface oxides that result in reduction of $I_0$ in the form of mid-gap tunneling.

the current dropped by two orders of magnitude at 0.5 V reverse bias. It was understood that midgap tunneling in submicron PIN diodes is majorly a surface leakage phenomenon. The onset of BTBT was also delayed post-clean.

Fig. 5.13a compares $J_1$ in the overetched BCB sample before and after a 15 s citric etch. PIN4(CITRIC) (green) shows a wide range of surface leakage current from $2 \times 10^{-8} \text{A/cm}$ to $3 \times 10^{-3} \text{A/cm}$ — with a majority of the devices at the higher end of the distribution. The etch chemistry of H$_2$O$_2$ and citric acid was not used in this study because (i) citric acid is the component of the chemistry that etches In$_x$O$_y$ and Ga$_x$O$_y$. The purpose of H$_2$O$_2$ is to oxidize the surface, and (ii) the etch rate of the mesa etch chemistry (20:1 citric acid:H$_2$O$_2$) is high (1.1 nm/s). Any excess In$_{0.53}$Ga$_{0.47}$As etch would have reduced the cross sectional area of the device, thereby reducing the bulk current and surface currents, skewing the result and leading to erroneous conclusions. The spread in the sample (Fig. 5.13a—green) was hypothesized to be a function of an increased surface states due to citric etch.

Comparing the two cleans, HCl and Citric, it was observed that PIN4(CITRIC)
Figure 5.13: Citric Acid Treatment. Comparison of \( J_1 \) (A/cm) in an overetched BCB sample before and after a 20 s citric acid clean. Current drops 2 orders of magnitude but with an increase in dispersion in PIN4(CITRIC).

Table 5.8: HCl Clean and Citric Clean on overetched BCB sample.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Sample Size</th>
<th>( J_1 ) Median [A/cm]</th>
<th>( J_1 ) St. Dev. [A/cm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(BCB-OVE)</td>
<td>107</td>
<td>1.15\times 10^{-2}</td>
<td>1.16\times 10^{-2}</td>
</tr>
<tr>
<td>PIN4(HCL)</td>
<td>96</td>
<td>5.52\times 10^{-4}</td>
<td>7.97\times 10^{-4}</td>
</tr>
<tr>
<td>PIN4(CITRIC)</td>
<td>118</td>
<td>1.5\times 10^{-4}</td>
<td>5.46\times 10^{-4}</td>
</tr>
</tbody>
</table>

had a lower surface leakage current than PIN4(HCL) (Table 5.8). Because PIN4(HCL) showed a bidmodal distribution, standard deviation in PIN4(HCL) is higher than PIN4(CITRIC) despite the former being a much tighter distribution. In conclusion, since both cleans performed gave similar results, HCl treatment was given preference because in addition to removal of native oxides, it can also remove ionic contaminants from the surface of the material.

Both surface cleans do not address the passivation of surface states, and in order to reduce \( I_0 \), either BCB or sulfide encapsulation is essential.
5.2.7 Cleans versus Passivation

In this study, surface leakage current was compared for devices that have undergone (i) an HCl clean, and (ii) Sulfide passivation. The premise of this comparison was that a clean and a passivation affect the surface leakage current of a device differently. While one reduces leakage by removing surface oxides, the other passivates the dangling bonds at the air-material interface.

(a) $J_1$ vs. Area:Perimeter. PIN4(HCL) - Red and PIN4(SULFIDE) - Blue.

(b) Median represented by mid-line in the box. The box represents the middle 50% of the particular dataset.

**Figure 5.14:** Comparison of $J_1$ (A/cm) in a sample treated with HCl and a sample treated with ($\text{NH}_4)_2\text{S}$. Current drops around 3 orders of magnitude in PIN4(SULFIDE). The two treatments compare the impact of surface oxides (HCl) and dangling bonds (Sulfide) on $I_0$.

Fig. 5.14a shows a clear distinction between $J_1$ of PIN4(SULFIDE) (blue) and PIN4(HCL) (red). PIN4(HCL) with a median at $5.52 \times 10^{-4}$ A/cm showed removal of native oxides but severe leakage due to dangling bonds. Some devices in PIN4(HCL) that had a significantly lower concentration of dangling bonds had $I_0$ comparable to the surface leakage in PIN4(SULFIDE). In the sulfur passivated sample, sulfur atoms bond with In and Ga atoms at the surface filling the electron vacancies. Without proper encapsulation, sulfur atoms can diffuse into the ambient, creating the dangling bonds again. Sulfur does not reduce native oxides, which is the reason that there is a
reduction of surface leakage by an order of magnitude in PIN4(BCB), as can be seen in Fig. 5.15a. The BCB sample, in this case, had undergone an HCl clean that had removed the native oxides before BCB encapsulation.

Table 5.9: Comparison of HCl clean and Sulfide Passivation.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Sample Size</th>
<th>$J_1$ Median [$A/cm$]</th>
<th>$J_1$ St. Dev. [$A/cm$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(HCL)</td>
<td>96</td>
<td>$5.52 \times 10^{-4}$</td>
<td>$7.97 \times 10^{-4}$</td>
</tr>
<tr>
<td>PIN4(SULFIDE)</td>
<td>84</td>
<td>$2.37 \times 10^{-7}$</td>
<td>$7.47 \times 10^{-7}$</td>
</tr>
</tbody>
</table>

Fig. 5.15b shows transient nature of BCB passivation (red) and sulfur passivation (blue). It was observed that the sulfur escaped into the atmosphere from Day 1 to Day 4 increasing the variation surface leakage current across devices. In contrast, the median value of $J_1$ decreased from $5.2 \times 10^{-8}$ A/cm to $3.5 \times 10^{-8}$ A/cm from Day 1 to Day 8, with a slight increase in variation across the devices. This suggests that BCB is successful is passivating the dangling bonds at the In$_{0.53}$Ga$_{0.47}$As surface and is
successful in mesa encapsulation and preventing O$_2$ from oxidizing the surface. Comparing Day 4 leakage currents, PIN4(SULFIDE) had a much higher leakage current and variation than PIN4(BCB) suggesting that BCB is a better passivating material than (NH$_4$)$_2$S in terms of tying up dangling bonds and transient nature of the passivation.

5.2.8 BCB Adhesion Promoter — AP 3000

This experiment explores the impact of using the standard adhesion promoter for BCB, AP-3000 on the $I_0$ of a PIN diode. It was hypothesized that leakage should increase if AP-3000 was used, as the datasheet [50] reports traces of mobile ions (Na$^+$ and K$^+$) in the solution that could result in an increased surface leakage. For this experiment, PIN4(BCB) and PIN4(BCBnoAP) were used. Post the mesa etch and a 60 s HCl clean, adhesion promoter AP-3000 and BCB were spun on PIN4(BCB) and only BCB was spun on PIN4(BCBnoAP). Both the samples were cured at 250 °C for 60 min before being etched back for 9 min in the plasma etch chamber (Sec. 3.1.7).

It was observed that $J_1$ in PIN4(BCBnoAP) was constantly higher than PIN4(BCB) across the range of area to perimeter ratios (Fig. 5.16a). Fig. 5.16b shows that the distribution is much tighter in PIN4(BCB) than PIN4(BCBnoAP) with a surface leakage current of $5.2 \times 10^{-8}$ A/cm and $2.39 \times 10^{-6}$ A/cm, respectively. The experimental results were contrary to the hypothesis - which would mean that (i) mobile ions are in such a small concentration in the adhesion promoter that they do not have enough impact on the surface of the semiconductor, and (ii) without AP-3000, BCB does not adhere to the semiconductor surface properly, developing cracks to allow partial surface oxidation or unpassivated dangling bonds.

The second argument was emphasized again in Fig. 5.17b that shows an increase in surface leakage in PIN4(BCBnoAP) to $3.5 \times 10^{-5}$ A/cm from Day 1 to Day 4. This could be an effect of O$_2$ in the ambient oxidizing the mesa sidewall through the cracks.
Chapter 5. Surface Leakage and Treatments

(a) $J_1$ vs. Area:Perimeter. PIN4(BCB) - Red and PIN4(BCBnoAP) - Blue.

(b) Median represented by mid-line in the box. The box represents the middle 50% of the particular dataset.

Figure 5.16: Comparison of $J_1$ (A/cm) in two samples coated with BCB with and without the adhesion promoter, AP-3000. The sample with BCB directly on the surface showed $I_0$ for all area perimeter ratios than than sample with an AP-3000 coat before BCB application.

Table 5.10: Comparison of $J_1$ [A/cm] in PIN4(BCB) and PIN4(BCBnoAP).

<table>
<thead>
<tr>
<th>Sample</th>
<th>Sample Size</th>
<th>$J_1$ Median $\left[ \frac{A}{cm} \right]$</th>
<th>$J_1$ St. Dev. $\left[ \frac{A}{cm} \right]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(BCB)</td>
<td>74</td>
<td>$5.2 \times 10^{-8}$</td>
<td>$4.8 \times 10^{-7}$</td>
</tr>
<tr>
<td>PIN4(BCBnoAP)</td>
<td>60</td>
<td>$2.39 \times 10^{-6}$</td>
<td>$1.03 \times 10^{-5}$</td>
</tr>
</tbody>
</table>

Comparing that with PIN4(BCB), proper encapsulation of the sidewall resulted in no degradation of the surface.

Table 5.11 reports that on Day 4, there was a difference of three orders of magnitude between PIN4(BCB) ($3.5 \times 10^{-8}$ A/cm) and PIN4(BCBnoAP) ($3.5 \times 10^{-5}$ A/cm), accentuating the impact of using AP-3000 before BCB application in reducing $I_0$.

5.2.9 Metal Liftoff

Metal can be patterned on devices in two ways - etch and liftoff. All the samples used in the treatments above had metal pads patterned by dry etch of Mo. In this experiment, PIN4(BCB-LIFT) was compared with PIN4(BCB) to analyze the effect
Figure 5.17: Surface leakage current, $J_1$ (A/cm) variation with time. While the BCB with AP-3000 sample (red) shows a slightly dispersed spread but a lower median value of $J_1$, the BCB w/o AP-3000 sample (blue) shows an increase in $J_1$.

Table 5.11: BCB with and without AP-3000. Degradation with time.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Day 1 Median $J_1$ [A/cm$^2$]</th>
<th>Day 4 Median $J_1$ [A/cm$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN4(BCB)</td>
<td>$5.2 \times 10^{-8}$</td>
<td>$3.5 \times 10^{-8}$</td>
</tr>
<tr>
<td>PIN4(BCBnoAP)</td>
<td>$2.39 \times 10^{-6}$</td>
<td>$3.5 \times 10^{-5}$</td>
</tr>
</tbody>
</table>

of Mo etch vs. Mo liftoff. PIN4(BCB-LIFT) had liftoff Mo as the top contact and PIN4(BCB) had etched Mo as the top contact.

Fig. 5.18 shows that the liftoff sample, PIN4(BCB-LIFT) has leakage current ranging over 5 orders of magnitude without showing a specific trend, unlike PIN4(BCB) (Mo etch for top metal) that had a tight distribution for the whole range of area to perimeter ratios.

Liftoff of uniformly coated metal (sputter Mo coats conformally) results in fencing on the edges of a device. It may lead to a parallel path of conduction between the $p^+$ and the $n^+$ layer in the event that the metal fence falls during subsequent processing shunting the two layers — observed in the top range of the distribution. The devices in the lower end of the spectrum fall in the range of Mo etch suggesting no fall-off of fence.
Figure 5.18: Comparison of $J_1$ in PIN4(BCB) with a Mo liftoff sample treated with BCB, PIN4(BCB-LIFT). Current in the liftoff sample did not show any specific dependence of area and perimeter and ranged over 5 orders of magnitude.

In conclusion, a qualitative assessment of different surface cleans and passivation techniques was made. Fig. 5.19 gives an overview of the various treatments and their impact on $I_0$. It was observed that BCB was a better candidate for surface passivation than $(\text{NH}_4)_2\text{S}$ as it showed a lower surface leakage current (A/cm) and lesser degradation over time. Both the cleans removed surface oxides. The HCl clean in this case was given preference because in addition to etching III-V oxides, it also removes ionic contaminants from the surface.

It was also observed that dangling bonds on the surface have a greater impact on $I_0$ than surface oxides. It can be seen in Fig. 5.19 when comparing an HCl clean and a sulfide passivation where the former etches oxides and the latter ties up dangling bonds using sulfur, and while comparing sulfur treatment vs. BCB treatment where sulfur does not etch native oxides and on the other sample, BCB was applied post oxide removal.

In terms of surface leakage (normalized with perimeter), PIN4(BCB) showed an improvement over the TFET device reported by [42] by an order of magnitude. The $I_0$ extrapolated from [42] was $2.5 \times 10^{-11}$ A/µm and the one extracted in PIN4(BCB) was $4 \times 10^{-12}$ A/µm.
Figure 5.19: Overview of the impact of different surface treatments on $I_0$. BCB and HCl came out as the preferred passivation and cleaning chemistries. *’ - For the HCl clean and the Citric clean, the control piece was the Overetched BCB sample.
Chapter 6

Conclusions and Scope of Future Work

6.1 Concluding Remarks

In this study, a new fabrication process was developed to realize In$_{0.53}$Ga$_{0.47}$As homojunction PIN diodes. As a part of the new process, piece exposure using optical lithography was developed to improve the total processing time of a sample from 65 hours to 47 hours. A shadowed metal deposition process was also developed that enabled contacting the bottom layer to provide an electrical contact as close as possible to mesa, minimizing series resistance. It removed the problem of fencing caused by liftoff and saved a pattern-etch step generally used for isolating the two contacts.

Bulk and surface components of dark current were analyzed and different surface treatments were performed to minimize $I_0$. It was observed that Fermi level pinning caused by dangling bonds has a far greater impact on surface leakage than surface oxidation.

Of the various treatments, a combination of BCB passivation and HCl clean have been recommended to give lowest $I_0$ (normalized by perimeter) of $4 \times 10^{-12}$ A/$\mu$m. The closest TFET [42] reported an $I_0$ of $2.5 \times 10^{-11}$ A/$\mu$m.

This study has reported, for the first time, electrical characterization of sub-micron PIN diodes, in comparison to TFETs reported in literature that have mesa dimensions ranging from 5 $\mu$m to 20 $\mu$m.
6.2 Scope of Further Investigations

To expand further on surface treatments, materials like polyimide and nitride passivation layers, which have been standard passivation materials for photodetectors can be used. Further, cleaning treatments can be used along with high-$\kappa$ dielectrics, such as $\text{Al}_2\text{O}_3$ that have shown to consume surface oxides [51]. This process can be significantly beneficial when gating the PIN to realize a TFET. Further analyses need to be performed to better understand and isolate different surface leakage and bulk leakage mechanisms. Temperature analysis can be used to characterize SRH G-R leakage floor and separate it from TAT and BTBT. Material analysis such as Secondary Ion Mass Spectroscopy can be used to find out dopant density in the p$^+$ and n$^+$ regions and the actual width of the intrinsic region.

A new mask can be designed extend the perimeter analysis that utilizes EBL to fabricate sub-micron mesas and GCA to pattern probe pads. The absence of big metal pads in the Overgrowth mask was a severe disadvantage in terms of probing mesas directly and top metal degradation because of overuse. This will enable a cleaner dataset and provide more accurate results.

Further, this study can be expanded to different material systems such as homo-junction $\text{In}_{0.9}\text{Ga}_{0.1}\text{As}$ and $\text{InAs/GaSb}$ (Type III heterojunction) to enable a higher $I_{on}$ in TFETs and can be used to compare different buffer systems and starting substrates such as Silicon and GaSb.
Bibliography


[45] G. C. DeSalvo, W. F. Tseng, and J. Comas, “Etch rates and selectivities of citric acid hydrogen peroxide on GaAs, Al$_0.5$Ga$_0.7$As, In$_0.2$Ga$_0.8$As, In$_0.53$Ga$_0.47$As, In$_0.52$Al$_0.48$As and InP,” Journal of the Electrochemical Society, vol. 139, no. 3, pp. 831–5, 1992.


Appendix A

PIN Diode Process Flow

1. Metal 1 (Mo) deposition
   (a) Tool: CVC 601 DC Sputter.
   (b) 10:1 DI H₂O:HCl, DI H₂O rinse, dry.
   (c) Presputter: 1000 W, 120 s, 2.2 mT, 18 sccm Ar.
   (d) Sputter: 200 W, 420 s, 2.2 mT, 18 sccm Ar.

2. Resist coat: nLOF 2020
   (a) Tool: SCS spin coater.
   (b) DI H₂O rinse, dehydration bake @ 110°C, 60 s.
   (c) dilute nLOF coat @ 3500 rpm.
   (d) Post application bake @ 110°C, 60 s.

3. Level 1 exposure: e–beam lithography
   (a) Tool: LEO SEM, NPGS
   (b) Scratch for focus matrix and measure sample dimensions.
   (c) Load sample with minimum exposure to white light.
   (d) Using the faraday cup, set \( I_{\text{specimen}} \) to 300 pA (corresponding to \( I_{\text{probe}} = 100-105 \) pA).
   (e) Set WD = 6 mm and focus on the gold standard to check wobble and astigmatism.
   (f) Create label for new sample in CAD file. Convert to vector and move to layer 9.
   (g) Edit run file for initial/final stage moves based on the sample dimensions. Follows standard coordinate system. Units are \( \mu \text{m} \).
   (h) Verify the correct dose for each pattern in the NPGS file. Area dose = 30 nC/cm², Area dose = 20 nC/cm², Line dose = 1 nC/cm.
   (i) Open com port.
Appendix A. PIN Diode Process Flow

(j) Using the scratches, develop a focus matrix by moving the stage height to focus on the first scratch and afterwards using the working distance.

(k) Verify that \( I_{\text{specimen}} \) is in the range of 300 pA.

(l) Go to the reference point. Switch from SEM to NPGS mode before writing.

(m) Post exposure bake @ 110°C, 60 s.

(n) Develop — CD 26, 30 s, rinse in DI H\(_2\)O, dry.

4. Mo etch

(a) Tool: Drytek Quad Ch. 2.

(b) 3 min O\(_2\) clean — 280 W, 180 s, 300 mT, 100 sccm O\(_2\), 60°C.

(c) 3 min carrier season — 150 W, 180 s, 125 mT, 125 sccm SF\(_6\), 60°C.

(d) 2 min etch — 150 W, 125 mT, 125 sccm SF\(_6\), 60°C.

5. In\(_x\)Ga\(_{1-x}\)As etch

(a) 20:1 citric acid:H\(_2\)O\(_2\). Agitate every 15 s. Etch rate (\( x = 0.53 \)) = 1.1 nm/s.

(b) Quick rinse in DI H\(_2\)O with agitation.

(c) Long rinse in second DI H\(_2\)O, dry.

6. SEM inspection

(a) Observe undercuts of different metal and semiconductor layers at typical tilt angles of 75° and 84°.

7. BCB coat and cure

(a) Tool: SCS spin coater and Blue M Oven.

(b) DI H\(_2\)O rinse, dehydration bake.

(c) Coat with BCB adhesion promoter AP 3000.

(d) Coat with BCB (SCS standard recipe 2).

(e) Post application bake @ 140°C, 5 min.

(f) Place in oven pre-heated at 140°C. Ramp oven from 140°C to 250°C.

(g) Bake @ 250°C, 60 min.

8. BCB etchback

(a) Tool: LAM 490 plasma etch

(b) 5 min carrier wafer season — 25 W, 300 s, 300 mT, 80 sccm O\(_2\), 1000 sccm He, 20 sccm SF\(_6\), 1.65 cm (distance).

(c) 5 min etch.

(d) Inspect optically and/or using SEM.
Appendix A. PIN Diode Process Flow

(e) Etch for more time if pads not clear (bigger pads clear faster). Minimum etch time = 15 s.

9. Resist coat: LOR 5A
   (a) Tool: SCS spin coater.
   (b) Coat with LOR 5A (SCS standard recipe 2).
   (c) Post application bake @ 110°C, 5 min.
   (d) Coat with ARCH 8250 (SCS standard recipe 2).
   (e) Post application bake @ 110°C, 60 s.

10. Level 2 exposure: e–beam lithography
    (a) Tool: LEO SEM, NPGS.
    (b) Load sample with minimum exposure to white light. e-beam should not hit any device area when in SEM mode.
    (c) Using the faraday cup, set $I_{\text{specimen}}$ to 300 pA (corresponding to $I_{\text{probe}} = 100-105$ pA).
    (d) Set WD = 6 mm and focus on the gold standard to check wobble and astigmatism.
    (e) Edit initial/final stage moves based on Level 1 exposure.
    (f) Area dose = 30 nC/cm$^2$, Area dose = 20 nC/cm$^2$, Line dose = 1 nC/cm.
    (g) Open com port.
    (h) Rotation correction for alignment marks. Always move left.
        SEM x-y coordinate system opposite to conventional system. Units are mm.
        i. Align center mark to crosshairs using x–y joystick.
        iii. Move to rightmost mark. Align crosshairs.
        iv. Follow (ii) and (iii) till all three marks align to crosshairs.
    (i) Go to all pre-alignment marks to generate a focus matrix.
    (j) Verify that $I_{\text{specimen}}$ is in the range of 300 pA.
    (k) Go to the reference point. Switch from SEM to NPGS mode before writing.
    (l) Post exposure bake @ 110°C, 60 s.
    (m) Develop — CD 26, 30 s, rinse in DI H$_2$O, dry.

11. Metal 2 (Mo) deposition
    (a) Tool: CVC 601 DC Sputter.
    (b) 10:1 DI H$_2$O:HCl, DI H$_2$O rinse, dry.
    (c) Presputter: 1000 W, 120 s, 2.2 mT, 18 sccm Ar.
Appendix A. PIN Diode Process Flow

(d) Sputter: 200 W, 420 s, 2.2 mT, 18 sccm Ar.

12. Liftoff

(a) Samples in 100 mL Remover PG @ 150°C, 30 min.
(b) Keep agitating solution every 3–4 mins.
(c) Quick rinse in IPA, 1–2 mins.
(d) DI H$_2$O rinse, dry.
(e) Optical inspection. If required, repeat from (12a), 5 mins.