Modeling and fabrication of optically resonant periodic structures

Charles Faisst Jr.
Modeling and Fabrication of Optically Resonant Periodic Structures

By

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A Thesis Submitted in
Partial fulfillment
of the Requirements for the Degree of

Master of Science
In
Microelectronic Engineering

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October 2002
Preface

Dr. Louis Pasteur is quoted as saying “Chance favors the prepared mind.” I misquoted Dr. Pasteur once in a presentation as saying “Change favors the prepared mind.” After giving this error some thought, I realized how applicable that statement is to my professional career.

In life change is inevitable, especially in the world of technology. However, you can embrace change or be fearful of it. A prepared mind is often more capable of dealing with the changes life brings. Change then becomes a challenge and not a nightmare.

Those who prepare and plan for change position themselves to be successful. I am very fortunate to be associated with many people who prepare and plan for change and who have vision and leadership.

I would like to thank the Eastman Kodak Company for financially supporting my education at The Rochester Institute of Technology. I am especially thankful to one particular visionary, David R. Smith. David’s planning for future change has included preparing his employees through education. I would also like to thank Eric Leonard at Kodak who has been a big part of my career development path and who encouraged me to further my education. I also want to thank my immediate supervisor Bryan Beaman who kept encouraging me during the latter time of this research to “keep going and finish.”

Special thanks to my thesis advisor Dr. Karl D. Hirschman for his guidance and practical understanding of ORPEL structures from theory - to design - to processing - to testing. His encouragement during the times I did not understand “ORPEL” was uplifting. Karl has made the learning experience at RIT very rewarding. I would also like to thank Dr. Santosh Kurinec, Professor Dale Ewbanks, and Dr. Thomas Brown for their guidance, instruction and participation on my thesis committee. I would also like to thank the support staff (Tom, Chuck, Al, Scott, John, Rich, Bruce, and Sean) at the Semiconductor and Microsystems Fabrication Laboratory at RIT for keeping the systems up and running. Many thanks to the grads and undergrads that helped with the different process steps (Nate, Chris, Mike and Tina). A special thanks to Sara Widlund, the Department Senior Staff Assistant for the countless tasks she performed that helped to make my stay at RIT pleasant. I would like to thank Jason Neiser at The Institute of Optics at the University of Rochester for the discussions on ORPEL, for testing the devices in their labs, and for proofing my thesis.

A very special heartfelt thanks to my wife Peggy for her support, encouragement, and love. She has always been with me through the changes in my career with its many different “educational requirements.” I would not want to enjoy this life and the changes it brings with anyone else. To Jaci, Christine and Steven, I hope the visits to the “fab” and dressing in the “monkey suits” helped you to understand what Dad was trying to learn at school.

However, my thankfulness would not be complete if I did not take a moment and give thanks to my savior, my creator, my Lord - Jesus Christ. He has given me the gifts and talents to be the person that I am, and the person that I am going to be.
Modeling and Fabrication of Optically Resonant Periodic Structures
I, Charles F. Faisst Jr., hereby grant permission to the Wallace Memorial Library, of the Rochester Institute of Technology, to reproduce my thesis, in whole or in part, with the knowledge that any reproduction will not be for commercial use or profit.

Student ________________________
Charles F. Faisst Jr.
Abstract
Optically resonant periodic electrode (ORPEL) structures developed for use as an optical modulator at telecommunication wavelengths using standard microelectronic processes have been successfully fabricated. These structures combine passive optical components (i.e. waveguides, diffraction gratings) with optical and/or electrical excitation, which alters the optical properties of the device. Although the electro-optical effect in silicon is weak in comparison to III-V materials, a change in the free carrier concentration will cause a change in the effective index of refraction, and can alter the resonance wavelength. Optical test results have demonstrated resonance near 1550 nm on devices with grating pitches ranging from 0.68 to 1.08 μm. Parameters which are important to the electrical operation and optical performance of the devices have been investigated, both experimentally and using computer simulation. Simulation software has proven to be a very useful tool in structural and optical modeling of ORPEL devices; optical modeling predictions and experimental results for 0.70 μm pitch grating structures are in reasonable agreement. This work will present the theory of operation, device design, fabrication details, and electrical and optical measurements on ORPEL structures.
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1 Introduction

1.1 Background

Photonics is the science and technology of generating, manipulating, transmitting and detecting light\(^1\). This field includes many aspects of the physical sciences, engineering, and information science. Photonics encompasses optics, imaging, optoelectronics, optical information processing, quantum optics, lasers, materials science and their applications.

The data rate in the year 2001 for the conventional Internet backbone is one trillion (1E12) bits per second. One future requirement for the Internet is a data rate of 10 petabits (1E15 bits) a second\(^2\). This high data rate is attributed to applications requiring online virtual reality and sharing computing power across the network. The optical network is becoming faster than what conventional electronic switching technologies can handle. In order to meet the demand for higher data transfer rates it is more effective to switch light waves than to convert photons to electrons and be limited by electronic switches. Because of these requirements, the demand for optical wave manipulating devices has increased.

In 1994, the National Science Foundation (NSF) conducted a workshop on optical science and engineering\(^3\). During this workshop, it stated one of the NSF’s goals was “to stimulate the creation of the science and technology base required to realize the National Information Infrastructure.” The 1994 NSF report also stated that “the challenge is to increase the system performance and reduce the cost by using optics within the switches instead of converting to electronic switches...a key question is how to best combine the capabilities of optics and electronics to build networks that can be controlled, managed, and interconnected.\(^4,^5\)”

The integration of technologies associated with photonics and microelectronics has created a new breed of devices often identified as OPTO-Electronics, Optical-MEMS, or Micro-optical-electro-mechanical-systems (MOEMS)\(^6\). This new breed of devices can incorporate components from the field of optics, mechanics and electronics.
Designs include simple photonic integrated circuits, such as, the Interuniversity Microelectronics Center (IMEC) optical phase controller shown in Figure 1.

![Image of IMEC's Packaged Photonic Optical Phase Controller]

Figure 1 IMEC's Packaged Photonic Optical Phase Controller

MOEMS designs can also include complex systems, such as, Lucent Technologies silicon optical bench technology. The bench is used as a platform for attaching lasers, lenses, waveguides, detectors and support electronics. A picture of this type of device can be seen in Figure 2. This system requires complicated pick and place assembly equipment to assemble the bench.

The field of photonics, which includes manufacturing, is also an immature technology that suffers most importantly from high cost. The high cost of manufacturing photonic devices has inhibited the introduction of many of these devices into the market. There is also a need for improved manufacturability and yield to help drive cost down. Therefore, photonic devices that utilize existing microelectronic manufacturing processes will have an advantage over devices requiring new process technologies. The integration of microelectronics and photonics adds functionality to the device while maintaining a very small footprint and reduced cost.
1.2 Overview of Thesis Research

One method for creating data transmitters and receivers for optical communications wavelengths is using out-of-plane optical coupling geometry on silicon-on-insulator (SOI) technology\(^9\)\(^{,}10\). This study was carried out using SOI waveguides equipped with optically resonant periodic electrode (ORPEL) structures, developed using conventional microelectronic fabrication techniques. As a receiver, the periodic electrodes enable the device to selectively couple a narrow band of light energy into the waveguide structure. As a transmitter, data to be transmitted from the device is imposed on a reflected signal from an incident continuous-wave probe signal. Theoretically modulation is controlled by electronically altering the free-carrier density and/or distribution, thus altering the effective index of refraction of the waveguide core and coupling properties of the device. The device structures enable an integrated I/O interface between VLSI circuitry and off-chip optical signals.

This report will describe the structural design, the fabrication process, the reflection spectra simulation using rigorous coupled-wave analysis software\(^11\), process results, and electrical test results. Device characterization will include reflection spectra to verify optical resonance at a wavelength of 1550 nanometers. Measured data will be compared to both optical and process models.
2 Theory

2.1 ORPEL Structures

2.1.1 Description of ORPEL Structures

The ORPEL structure is an electrically controlled optical binary switch. A cross-section of the structure is shown in Figure 3. Light is either coupled into or reflected from the structure due to changes in the index of refraction of the silicon layer within the waveguide and the ability of the structure to optically resonate at a desired wavelength. The methods for controlling the change in refractive index include free-carrier effects, effects of composition variations, electric field effects and strain effects\textsuperscript{12}. Soref and Bennett have shown that the optical properties of silicon are strongly affected by injection of charge carriers into an undoped sample\textsuperscript{13}. The method used in controlling the change in the index of refraction in the ORPEL structures is by free-carrier effect. The following equation for determining the change in refraction due to free electrons and free holes for a homogenous material is as follows\textsuperscript{14}:

\[
\Delta n = -\left[\frac{e^2 \lambda^2}{8\pi^2 c^2 \varepsilon_0 n}\right] \times \left[\frac{\Delta N_e}{m_{ce}^*} + \frac{\Delta N_h}{m_{ch}^*}\right]
\]

Equation 1

Where \(e\) is the electronic charge, \(\varepsilon_0\) is the permittivity of free space, \(n\) is the unperturbed refractive index of single crystal silicon (c-Si) at wavelength, \(\lambda\), \(m_{ce}^*\) is the conductivity effective mass of electrons, \(m_{ch}^*\) is the conductivity effective mass of holes, \(c\) is the speed of light, \(\Delta N_e\) and \(\Delta N_h\) are the change in the number of free electrons and holes respectively. Optical wave guiding in semiconductor materials requires a controlled variation in the refractive index in the plane perpendicular to the direction of power flow\textsuperscript{15}. For wave guiding to occur in a semiconductor layer the surrounding layers must have a lower index of refraction.
Figure 3 Sketch of ORPEL Structure showing buried periodic electrodes and Light Propagation.

In order to get the optical wave into the waveguide a coupling mechanism is required. The coupling mechanism for the ORPEL structure is a buried diffraction grating in the amorphous silicon (a-Si) and crystalline silicon (c-Si) combined layers\textsuperscript{16}. Sankey, et. al., have shown that a first order approximation for coupling the incident light into the periodic structure is\textsuperscript{17}:

$$\frac{2\pi}{\lambda} \cdot n_{\text{eff}} = \frac{2\pi}{\lambda} \sin \theta + m \frac{2\pi}{\Lambda}$$

\textbf{Equation 2}

Where $\lambda$ is the wavelength of the incident light, $\Lambda$ is the grating period, $\theta$ is the coupling angle, $n_{\text{eff}}$ is the effective index of refraction, and $m$ is an integer corresponding to the mode number.

The combination of the optical medium and the periodic refractive index causes gaps to occur in the dispersion curve of the structure\textsuperscript{18}. Bieber, et. al., reports that the dispersion curve gaps correspond to frequency stop bands and are centered about the wavelengths that satisfy the Bragg condition. First order Bragg condition is given by Equation 3.
\[ \delta = \pi \left[ \frac{2n_{\text{eff}}}{\lambda} - \frac{1}{\Lambda} \right] \]

Equation 3

Where \( \delta \) is called the detuning factor, and satisfies the Bragg condition when \( \delta = 0 \), \( \Lambda \) is the grating period, and \( n_{\text{eff}} \) is the effective index of refraction. When the Bragg condition is satisfied an oscillating wave is established in the waveguide.

A portion of this wave is coupled back out of the waveguide and interferes either constructively or destructively with the specular reflection\(^1^9\). Without changing the structure layers tuning of the waveguide to a desired resonant frequency is accomplished by changing the electrode period, \( \Lambda \).

Modulation of the resonant frequency (thus the reflection intensity at the design frequency) can be accomplished by optical excitation\(^2^0\), or in principle by carrier injection. As was shown in optical experiments\(^2^1\), the carrier injection process should alter the effective index of refraction of the waveguide structure. A DC voltage applied across the buried grating will create an electric field between the electrodes. The presence of an electric field will cause a change in the number of carriers via injection of holes or electrons near the electrodes. The change in the carrier concentration will cause a change in the refractive index of the c-Si layer, which will cause a shift in the resonant frequency. Grating geometries are created using a metal-semiconductor (MS) contact configuration. MS contacts exhibit picosecond electrical switching characteristics\(^2^2\), and are therefore ideal for high-speed operation. An alternative method of electrically controlled modulation is through an electric field induced perturbation of optically generated electron-hole pairs. Carriers generated by a continuous wave source (above bandgap) incident on the ORPEL device can be rearranged by an external bias, which may cause the device to detune (\( \delta \neq 0 \)), and thus modulate the communication signal.

2.1.2 Design

An optical modulator should have a switching characteristic spectrum similar to that shown in Figure 4\(^2^3\). The reflection change should be defined at a specific wavelength and the amount of change should be maximum and definitive. In order to have a device that results in these switching characteristics the design of the waveguide structure is
The design of the structure includes the waveguide layer stack, the material of the layers, the optical properties the layers, and the design of the buried coupling electrodes. In addition the layers selected must be compatible with standard microelectronic processes.

In order to construct a waveguide in silicon the outer layer refractive indices must be lower than the silicon layer. This requirement is satisfied using silicon-on-insulator (SOI) substrates. Maszara et. al. and Evans et. al. have previously demonstrated the use of SOI substrate as waveguides. The SOI substrates are also compatible with microelectronic manufacturing tool sets. The top cladding layer of the waveguide structure is air and the lower cladding layer of the waveguide is a buried layer of silicon dioxide (SiO₂). Both surrounding layers have indices of refraction lower than that of silicon (n_air=1, n_SiO₂=1.45 at a wavelength of 1.55μm).

The periodic grating of the ORPEL structure is a patterned stack of titanium and aluminum on the surface of the top crystalline silicon layer. The titanium layer in conjunction with the silicon creates the MS contact. The aluminum layer is for optical reflection and electrical interconnect. The metal grating is covered with an a-Si layer to create the buried electrode structures. These layers are separated from the silicon substrate by the buried SiO₂ layer. The a-Si layer allows the metal grating to be buried within a nearly continuous semiconductor layer. The a-Si overcoat provides symmetry.
about the electrodes and increases the coupling efficiency\textsuperscript{26}. The a-Si feature defines the boundaries of the waveguide. The a-Si layer also provides physical protection of the metal gratings (prohibits electrical opens and shorts after electrodes are defined).

The target layer thickness and grating periods used for defining the ORPEL structures were determined by a design iteration procedure using rigorous couple-wave analysis software\textsuperscript{27} (refer to Section 2.1.3). The target layer thickness selected is listed in Table 1. The periodicity ($\Lambda$) of the gratings used range from 0.68 to 1.08\textmu m in 0.02\textmu m increments (refer to Figure 5). A grating pitch of 0.68\textmu m was selected as the smallest feature dimension because of resolution limitations of the available optical lithography equipment in Rochester Institute of Technology’s Semiconductor and Microsystems Fabrication Laboratory (0.34\textmu m, 365nm I-line stepper).

Figure 5 shows the various dimensions of the ORPEL layout. Parameter values used for device design, layout, and simulation are listed in Table 1 and Table 2. Design values for 0.68 and 1.08\textmu m grating pitch are listed in Table 2. Design values for other pitch structures fall within these design values.

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness (Angstrom)</th>
</tr>
</thead>
<tbody>
<tr>
<td>c-Si layer</td>
<td>12600</td>
</tr>
<tr>
<td>Ti layer</td>
<td>100</td>
</tr>
<tr>
<td>Al layer</td>
<td>400</td>
</tr>
<tr>
<td>a-Si layer</td>
<td>3900</td>
</tr>
</tbody>
</table>

Table 1 Target Layer Thickness

<table>
<thead>
<tr>
<th>Grating Length</th>
<th>a-Si Length</th>
<th>a-Si Width</th>
<th>Electrode Length</th>
<th>Electrode End Gap</th>
<th>Bus to Bus Spacing</th>
<th>Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>1003.3</td>
<td>990.4</td>
<td>133.1</td>
<td>146.7</td>
<td>3.4</td>
<td>150</td>
<td>0.68</td>
</tr>
<tr>
<td>1101</td>
<td>1080</td>
<td>135</td>
<td>156.6</td>
<td>5.38</td>
<td>162</td>
<td>1.08</td>
</tr>
</tbody>
</table>

Table 2 Range of ORPEL feature design values for 0.68 and 1.08\textmu m pitch structures (Units in microns).
Figure 5 Schematic for ORPEL buried gratings and Amorphous silicon features. Dimension 1 refers to the overall length of the grating for a specific period. Dimension 2 is the overall length of the a-Si feature. Dimension 3 is the width of the a-Si feature. Dimension 4 is the length of a single grating finger. Dimension 5 is the distance between the end of a single grating finger and the bus of the other grating fingers. Dimension 6 is the overall width of the grating structure. Dimension 7 is the grating pitch, A (Not to Scale).

2.1.3 Optical Modeling of ORPEL Structures

The rigorous coupled-wave analysis (RCWA) software was developed by the Institute of Optics at the University of Rochester\textsuperscript{28}. The software incorporates rigorous coupled-wave theory of 2-D diffraction gratings. The RCWA software was developed using differential methods and the use of Fourier expansion to accommodates the transition of the permittivity of the gratings\textsuperscript{29}. The RCWA software provides reflection, transmission, and absorption spectra for buried two-dimensional gratings. The software was used to model the optical response of an optimized design and an “as fabricated” ORPEL structure. Actual device dimensions are put into the model and compared to the optimized designed device structures for a specific grating period.
The design parameters of the optimized structure are listed in Table 3, Table 4, and Table 5. The material layers and their assigned thickness used in the optical model are listed in Table 3. The index of refraction for the semiconductor materials used in the modeling of the ORPEL structures is listed in Table 4. The index, \( n \) used by the software is in the complex form \( a-bi \), where \( a \) is the real part and \( b \) is the imaginary part. The index of refraction used in Equations 1 and 2 are not complex, and should not be confused with the index used in the software. Table 5 includes other parameters needed by the RCWA software, for example, incident angle of light. The structure used in the model is comprised of six different layers as shown in Figure 6.

![Figure 6 Rigorous Coupled-Wave Analysis structure layers](image)

**Figure 6** Rigorous Coupled-Wave Analysis structure layers: Layer 1 is a continuous layer of crystalline silicon, layer 2 is a combination of amorphous silicon and titanium, layer 3 is a combination of amorphous silicon and aluminum, layer 4 is a continuous layer of amorphous silicon, layer 5 is a combination of air and amorphous silicon, an layer 6 is a continuous layer of air.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide</td>
<td>3.0</td>
</tr>
<tr>
<td>Top c-Si</td>
<td>1.26</td>
</tr>
<tr>
<td>Titanium</td>
<td>0.01</td>
</tr>
<tr>
<td>Aluminum</td>
<td>0.04</td>
</tr>
<tr>
<td>a-Si</td>
<td>0.39</td>
</tr>
<tr>
<td>Sum of Al &amp; Ti</td>
<td>0.05</td>
</tr>
</tbody>
</table>

**Table 3 Optimized Optical Model Layer Thickness**
### Table 4 Optical Model Refractive Indices at $\lambda=1.55\mu m$.

<table>
<thead>
<tr>
<th>Material</th>
<th>Refractive Index, n</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide</td>
<td>$1.44 + 0i$</td>
</tr>
<tr>
<td>c-Si (top)</td>
<td>$3.476 +0i$</td>
</tr>
<tr>
<td>a-Si and Ti</td>
<td>$3.48, 2.22-4.073i$</td>
</tr>
<tr>
<td>Al layer with a-Si</td>
<td>$3.48, 1.44-16i$</td>
</tr>
<tr>
<td>All a-Si</td>
<td>$3.48 + 0i$</td>
</tr>
<tr>
<td>Air and a-Si</td>
<td>$1, 3.48+0i$</td>
</tr>
</tbody>
</table>

### Table 5 Optical Model Optical Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Index of Refraction of Incident Medium (air)</td>
<td>1</td>
</tr>
<tr>
<td>Index of Refraction of Substrate (c-Si)</td>
<td>3.45</td>
</tr>
<tr>
<td>High Index of Refraction of Grating (a-Si):</td>
<td>3.48</td>
</tr>
<tr>
<td>Low Index of Refraction of Grating (Al layer)</td>
<td>1.44-16i</td>
</tr>
<tr>
<td>Wavelength</td>
<td>1.55 $\mu m$</td>
</tr>
<tr>
<td>Grating period</td>
<td>0.78 $\mu m$</td>
</tr>
<tr>
<td>Depth</td>
<td>1</td>
</tr>
<tr>
<td>Duty Cycle of Grating (amount of grating occupied by space)</td>
<td>0.5</td>
</tr>
<tr>
<td>Incident Angle</td>
<td>0</td>
</tr>
<tr>
<td>Lower Limit of Diffraction Order</td>
<td>-5</td>
</tr>
<tr>
<td>( # of diffraction orders used for calculations)</td>
<td></td>
</tr>
<tr>
<td>Upper Limit of Diffraction Order</td>
<td>5</td>
</tr>
<tr>
<td>Angle psi (Electric field parallel to grating)</td>
<td>$90^\circ$ for TE</td>
</tr>
<tr>
<td>Angle psi (Magnetic field perpendicular to grating)</td>
<td>$0^\circ$ for TM</td>
</tr>
<tr>
<td>Angle delta (Incident wave perpendicular to grating)</td>
<td>$0^\circ$</td>
</tr>
</tbody>
</table>

#### 2.1.4 Rigorous Coupled Wave Analysis Results

All of the device parameters listed in Table 3, Table 4, and Table 5 are for an optimized structure with a grating pitch of 0.78$\mu m$. The result of the simulated "optimized" optical spectra is shown in Figure 7. The left chart shows the reflection and transmission spectra of a 2-D ORPEL structure. The right chart is the absorption spectrum of the metal layers. This design was chosen as the "optimum" because it resulted in the steepest transition in diffraction efficiency near the wavelength of 1.55$\mu m$. 

---

11
Figure 7 Diffraction efficiency curve for ORPEL structure with optimized structure components. Grating period: 0.78µm; c-Si layer thickness: 1.26µm; Titanium thickness: 100Å; Aluminum thickness: 400 Å; a-Si layer thickness: 3900Å; Refractive Index: 3.476; Wavelength: 1.55µm. Left Chart: Reflection and Transmission spectra. Right Chart: Metal absorption spectra.

It was decided to benchmark the reflectivity response of the optimum structure using a change in the index of 0.09% and 0.26% from the ideal index value of 3.476. It was assumed that these changes in the refractive index could be obtainable through carrier injection. The reflectivity chart in Figure 8 is the result of simulating the optimum structure with an ideal refractive index of 3.476. Detuning for this structure occurs around 1.554µm. Figure 8 shows the reflectivity for this same structure with a change in the index of refraction of 0.003 (0.09%). The model predicts that a change in the index of 0.003 will result in a change in reflectivity at the design wavelength of 30% by inducing a red shift in the resonance wavelength. This reflectivity change may not provide adequate optical switching characteristics, however an index change of 0.009 (0.26%) shows a change in reflectivity close to 70%.
2.2 Electrical Operation

Solid-state devices require electrical interconnects between the device and an electrical stimulus, such as, a DC voltage source. The metal-semiconductor (MS) contact is a fundamental electrical interconnect. The MS contact can be designed either as an ohmic or rectifying contact, and becomes the connection to this outside stimulus. The rectifying MS type contact is referred to as a Schottky diode or MS diode and is the type of contact that is utilized due to its injection efficiency and fast response.\textsuperscript{30,31}

Three assumptions are made when defining an “ideal” MS contact. The assumptions are 1) the metal and semiconductors are in intimate contact on an atomic scale, with no layers of any kind between the material, for example, oxide, 2) there is no intermixing or interdiffusion between the metal and semiconductor, and 3) there are no absorbed impurities or surface charges at the MS interface.\textsuperscript{32} The energy band diagram in Figure 9 shows the energy bands for a p-type MS contact where the metal work function ($\Phi_m$) is less than the work function of the semiconductor ($\Phi_S$). For this type of contact there is a barrier to hole flow in both directions under equilibrium conditions. To reduce the barrier to hole flow from the semiconductor to the metal the Fermi energy level in the metal must be raised upward relative to the Fermi energy level in the semiconductor. The resulting hole current from the semiconductor to the metal is expected to increase exponentially with increased difference between the Fermi levels.

Figure 8 A: Optimized Structure $n=3.476$; Resonance $\sim 1.554 \mu m$, B: Optimized Structure with $n=3.479$ (0.03%) change in refractive index; 20% Change in Reflection Response. C: Optimized Structure with $n=3.485$ (0.09%) change in refractive Index; 70% Change in Reflection Response.
In Figure 9, $E_o$ is the vacuum energy and represents the energy at which an electron can be free of the material. $\Phi_m$ is the metal work function, it is the voltage needed to remove an electron from the surface of the metal. $X$ is the electron affinity of the semiconductor, it is the voltage necessary to remove an electron from the conduction band of the semiconductor. The electron affinity is a material constant of silicon. $\Phi_s$ is the work function of the semiconductor and is dependent on the dopant levels. The Fermi energy ($E_F$) level is also dopant dependent. $\Phi_{bi}$ is called the built-in voltage, which is the voltage drop across the MS contact under equilibrium conditions. $\Phi_B$ is the surface potential-energy barrier encountered by holes. For an ideal MS p-type contact,

$$\Phi_B = E_G + X - \Phi_M$$  \hspace{1cm} \text{Equation 4}

$E_G$ is the energy gap for silicon.

![Figure 9 p-type MS Contact Energy Band Diagram](image)

**2.2.1 Schottky Diode Electrostatics**

The MS contact exhibits a built-in voltage under equilibrium conditions. The built-in voltage is the voltage dropped across the MS diode, $V_{bi}$ can be expressed by the following equation.

$$V_{bi} = \frac{1}{q} \left[ \Phi_B - (E_c - E_F)_{FB} \right]$$  \hspace{1cm} \text{Equation 5}
Where $\Phi_B$ is defined in equation 3, $q$ is the electronic charge, and $(E_c - E_F)_{FB}$ is the energy difference between $E_c$ (conduction energy level) and $E_F$ (Fermi energy level) under flat band or zero field conditions. The energy difference is a function of the semiconductor doping level.

**Charge Density**

Under equilibrium conditions a depletion region exists in the semiconductor. The depletion region can be viewed as a distance, $x_p$, into the semiconductor. A net negative charge, $\rho$, arises in the depletion region due to acceptors. There is no positive n-type donor charge to balance the p-type acceptor charge as seen in a $p$-$n$ diode. The charge, $\rho$, in the depletion region can be approximated by the following relationships.

$$
\rho \approx \begin{cases} 
qNa & \text{... } 0 \leq x \leq W \\
0 & \text{... } x > W 
\end{cases}
$$

Where Na is the total number of acceptors/cm$^3$, and W is the depletion width in microns.

**Electric Field**

On the semiconductor side of the MS contact, the electric field, $E$, and the charge density are related to Poisson’s equation:

$$
\frac{dE}{dx} = \frac{\rho}{K_s \varepsilon_0} \approx \frac{qNa}{K_s \varepsilon_0} ... 0 \leq x \leq W
$$

Equation 6

Where $K_s$ is the dielectric constant of silicon, and $\varepsilon_0$ is the permittivity of free space. Separating variables and integrating Equation 6 from an arbitrary point $x$ within the depletion region to where $x=W$ and $E=0$, the electric field, $E$ can be obtained as a function of $x$.

$$
E(x) = -\frac{qNa}{K_s \varepsilon_0} \cdot (W - x) ... 0 \leq x \leq W
$$

Equation 7
**Electrostatic Potential**

The electrostatic potential in the semiconductor can be derived by:

\[
\frac{dV}{dx} = -E = \frac{qN_a}{K_s \varepsilon_0} \cdot (W - x)
\]

Equation 8

Separating variables and integrating equation 8 over the depletion region from some arbitrary point x to x=W where the potential is set to zero, the electrostatic potential as a function of x can be written as:

\[
V(x) = -\frac{qN_a}{2K_s \varepsilon_0} \cdot (W - x)^2 \quad 0 \leq x \leq W
\]

Equation 9

**Depletion Width**

Under equilibrium conditions the potential drop across the depletion region is \(V_{bi}\), the built in voltage, at x=0. If a voltage is applied to the MS diode then \(V = -(V_{bi} - V_a)\) at x=0, where \(V_a\) is the applied voltage. Substituting these conditions into Equation 9 and solving for the depletion width, W:

\[
W = \left[ \frac{2K_s \varepsilon_0}{qN_a} \cdot (V_{bi} - V_a) \right]^{1/2}
\]

Equation 10

**2.2.2 Schottky Diode I-V Characteristics**

**Forward Bias Operation**

The current resulting from majority carrier hole injection over the potential barrier in an MS diode is referred to as the thermionic emission current\(^{33}\). The reverse-bias electron diffusion current and the recombination-generation current associated with carrier generation in the depletion region are negligible. The fact that MS contacts have little or no minority carrier charge storage causes the switching time to be reduced by a factor of ten when compared with a typical p-n junction\(^{34}\). It is this characteristic of the MS contact that will be utilized in the design of the ORPEL structures. The expression for the majority carrier current is:
\[ I = I_s \cdot \left( e^{\frac{qV_a}{k\cdot T}} - 1 \right) \]  \hspace{1cm} \text{(Amps)} \hspace{1cm} \text{Equation 11}

Where \( V_a \) is the applied voltage (Volts), \( k \) is Boltzmann constant \( (8.617 \times 10^{-5} \text{eV/K}) \), \( T \) is the temperature \( (300^\circ \text{Kelvin}) \). \( I_s \) is expressed by the following equation.

\[ I_s = AA^\ast \cdot T^2 \cdot e^{-\frac{\Phi_B}{kT}} \]  \hspace{1cm} \text{(Amps)} \hspace{1cm} \text{Equation 12}

Where \( A \) is the cross-sectional area \( (\text{cm}^2) \) of the contact, \( A^\ast \) is the product of the Richardson Constant and the effective hole mass, \( T \) is temperature \( (\text{Kelvin}) \), and \( \Phi_B \) is the surface potential energy barrier (Equation 3).

**ORPEL MS Contact Turn-on Voltage**

It would be useful from a design point of view to be able predict at what voltage the ORPEL structure will conduct. However, the structure is not a simple MS diode, rather it is back-to-back diodes created by the physical arrangement of the interdigitated fingers and the lack of an ohmic contact to set the potential of the silicon layer. At the onset of current flow, the depletion width is approximately equal the grating space. With the boron concentration in the silicon layer of \( 1 \times 10^{15} \text{atoms/cm}^3 \) Equation 10 predicts a turn-on voltage of less than 1 volt. Although this configuration (floating body) deviates from the ideal MS contact, the device characteristics should exhibit high speed and high injection efficiency.

**2.3 Test Chip Design**

The final test structure is a composite of RWCA, structural analysis, and process capability. The grating design is shown in Figure 5 and feature dimensions are listed in Table 2. The target thickness for each layer is listed in Table 1. A test chip was designed with these target design parameters. The test chip layout is shown in Figure 10. There are four regions on the test chip. Regions A and C are identical in design as are Regions B and D. Region A includes grating structures with pitch ranging from 0.68 to 0.86\( \mu \text{m} \), in 0.02-\( \mu \text{m} \) increments. Region B includes grating structures with pitch ranging from 0.88 to 1.08\( \mu \text{m} \), in 0.02-\( \mu \text{m} \) increments.
Titanium was selected as the electrode metal because previous work has shown that titanium ensures that a Schottky barrier is created at the metal-semiconductor interface. S. Alexandrou, et. al. have demonstrated that photodiodes fabricated using titanium have switching speeds in the 6-12 picosecond range\(^{35}\).

The structures were fabricated using 5 mask levels. The mask level, the mask manufacturer, and the feature defined by the mask are listed in Table 6.

<table>
<thead>
<tr>
<th>Mask</th>
<th>Manufacturer</th>
<th>Feature Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level 0</td>
<td>Canon</td>
<td>Alignment Marks</td>
</tr>
<tr>
<td>Level 1</td>
<td>Benchmark</td>
<td>Grating/Electrodes</td>
</tr>
<tr>
<td>Level 2</td>
<td>RIT</td>
<td>Contact Cut</td>
</tr>
<tr>
<td>Level 3</td>
<td>RIT</td>
<td>Metal 1</td>
</tr>
<tr>
<td>Level 4</td>
<td>RIT</td>
<td>a-Si Overcoat</td>
</tr>
</tbody>
</table>

Table 6 Mask Identification

![Figure 10 Test Chip Layout](image)

Figure 10 Test Chip Layout: Region A and C: Grating pitch range - 0.68\(\mu\)m to 0.86\(\mu\)m; Region B and D: Grating pitch range - 0.88\(\mu\)m to 1.08\(\mu\)m; 0.02\(\mu\)m increment in grating pitch for all 4 regions.
3 Device Fabrication

3.1 Introduction

The ORPEL structures are realized by the use of an optical lithography technique called "Lift-off". Lift-off is a relatively simple method for patterning films that are deposited. A pattern is defined on a substrate using photoresist. A metallic film is blanket-deposited over the substrate, covering the photoresist and areas in which the photoresist has been cleared. During the actual lifting-off, the photoresist under the metal film is removed with solvent, taking the metal film with it, and leaving only the metal film that was directly deposited on the substrate.

3.2 Fabrication Process

The fabrication of ORPEL structures consists of 26 sequential processing steps. Theses steps include thermal oxide growth, optical lithography, metal deposition, metal etching, a-Si deposition, silicon and a-Si etching, and cleaning procedures. Some of the process steps are repeated more than once during the fabrication process.

3.2.1 Substrate Preparation

The substrate used in the fabrication of the ORPEL structures is silicon on insulator (SOI). The UNIBOND® SOI wafer was purchased from SOITEC Incorporated, Peabody Massachusetts. UNIBOND® wafers uses both ion implantation and wafer bonding technologies to create the silicon-insulator-silicon substrate. Using two separate wafers, the silicon surface of one wafer is first oxidized to form what will become the buried oxide layer of the SOI structure. An ion implantation step, using hydrogen ions, is then executed through the oxide layer by a standard high-current ion implanter to form the Smart Cut® layer. The wafer is then separated at the layer created by the hydrogen implant, which is then annealed and polished. Figure 11 shows the cross-section of the SOI wafer. Table 7 lists the specifications of the SOI substrates used in the fabrication of the ORPEL structures. There are two different lots of SOI wafers identified as lot numbers 75578.2 and 24668.1. Lot 24668.1 has a resistivity of 13.5 to 22.5 ohm-cm as compared to lot 75578.2, which has a resistivity greater than 2000 ohm-cm.
number and identification number are scribed on the backside of the wafer with a diamond point marker.

![Diagram of Active Wafer and Buried Oxide Layer](image)

**Figure 11** SOI Substrate: Buried oxide layer 3μm thick, Active wafer 1.5μm thick, Handle wafer 620μm thick.

<table>
<thead>
<tr>
<th>Active Wafer</th>
<th>Thickness: 15000 Å</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dopant:</td>
<td>Boron</td>
</tr>
<tr>
<td>Crystal Growth:</td>
<td>Float Zone</td>
</tr>
<tr>
<td>Crystal Orientation</td>
<td>100</td>
</tr>
<tr>
<td>Resistivity (Lot 75578.2)</td>
<td>2000 ohm-cm</td>
</tr>
<tr>
<td>Resistivity (Lot 24668.1)</td>
<td>13.5 – 22.5 ohm-cm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Buried Oxide Layer</th>
<th>Thickness: 30000 Å</th>
</tr>
</thead>
<tbody>
<tr>
<td>Handle Wafer</td>
<td>Thickness: 675μm</td>
</tr>
<tr>
<td>Dopant:</td>
<td>Boron</td>
</tr>
<tr>
<td>Crystal Growth:</td>
<td>Czochralski Zone</td>
</tr>
<tr>
<td>Crystal Orientation</td>
<td>100</td>
</tr>
<tr>
<td>Resistivity:</td>
<td>14 - 22 ohm-cm</td>
</tr>
<tr>
<td>Flat</td>
<td>1 flat 55 - 60mm (long flat)</td>
</tr>
</tbody>
</table>

**Table 7** SOI Substrate Specifications

**RCA Clean**

The RCA clean process is a multi “dip and rinse” immersion process for cleaning the wafer surface. The RCA clean includes three specific cleaning baths. The wafers are immersed in the baths in sequential order. The first bath contains one part ammonium hydroxide, three parts hydrogen peroxide, and fifteen parts of distilled (DI) water. The wafers are immersed in the first bath for ten minutes at 75°C. This bath removes any organic materials. The wafers are then rinsed with DI water to remove any residue from the first bath. The wafers are then immersed in a 50:1 ratio of water to hydrofluoric acid bath for one minute to remove any chemically grown oxide layer. Wafers are then rinsed again in DI water to remove any residual acid. The wafers are then immersed in a bath of one part hydrochloric acid, three parts hydrogen peroxide and fifteen parts DI water for
ten minutes at 75°C. The final bath removes any trace metals on the wafer. The wafers are then rinsed in DI water and then spun dried.

**Oxidation**

The SOI wafers have an initial c-Si layer thickness of 15,000 angstroms (Å). The optimum design requires a c-Si layer thickness of 12,600 Å. The c-Si layer thickness was reduced by 2400 Å. The c-Si layer thinning was accomplished by thermally growing an oxide layer and then etching away the oxide layer using buffered hydrofluoric acid. During thermal oxidation of silicon the growing oxide consumes 44% of the silicon\(^{36}\). In order to remove 2,400Å of silicon an oxide layer of 5000Å is required.

Wafers are placed in a furnace under controlled ambient and thermal conditions. The wafers are loaded vertically in a quartz boat with other monitor wafers of the same type. Additional wafers are needed to insure a uniform gas flow across the wafers, which will result in a more uniform oxide thickness across the wafer surface. In order to reduce processing time two separate thermal cycles where performed to grow the required 5000Å thick oxide. After the first thermal cycle, the oxide thickness was measured on control wafers using a Nanospec Reflectance Spectrophotometer. The oxide was then removed using a buffered hydrofluoric acid. The same thermal process was then repeated using the same wafers. The oxide layer was then measured a second time to insure another 2500Å oxide was grown. If the total oxide grown was within 100Å of the total required oxide layer of 5000Å, the step was complete. The second oxide layer was not removed until after planarization. If the total oxide grown was not within 100Å a third thermal cycle was performed on the wafers. Once the final oxide thickness was achieved the oxide layer remained on the wafers through the planarization process. The process parameters used to thermally grow the oxide are listed in Table 8.
<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equipment</td>
<td>Bruce Furnace, Tube 4</td>
</tr>
<tr>
<td>Load Wafers at Temperature</td>
<td>800°C, N₂ ambient, 10 LPM</td>
</tr>
<tr>
<td>Push Rate</td>
<td>12 in/min, N₂ ambient, 10 LPM</td>
</tr>
<tr>
<td>Stabilize</td>
<td>15 minutes, N₂ ambient, 10 LPM</td>
</tr>
<tr>
<td>Ramp Up</td>
<td>1000°C, Dry O₂, 5 LPM, 20 minutes</td>
</tr>
<tr>
<td>Soak</td>
<td>1000°C, Dry O₂, 10 LPM, 590 minutes</td>
</tr>
<tr>
<td>Ramp Down</td>
<td>25°C, N₂, 10 LPM, 35 minutes</td>
</tr>
<tr>
<td>Pull Rate</td>
<td>12 in/min, N₂, 5 LPM</td>
</tr>
</tbody>
</table>

**Table 8 Oxide Growth Process Recipe**

Figure 12 shows a cross-section of the device structure after the oxide growth step. The figures shown in this section are not drawn to scale. The sketches are a graphical method to show how the additive and subtractive processes are used to build the device.

![Cross-section of wafer after Oxide Growth step. Oxide thickness: ~2500Å](image)

**Resist Mask**

A resist coating 0.8-1.0μm thick is applied to the surface of the wafer to protect the top surface of the wafer during etching and chemical mechanical planarization (CMP). The resist layer will be applied using an automated coating track.

Wafers are coated with Olin OIR-620-10 photoresist using the Semiconductor Systems Incorporated (SSI) wafer-coating track. The process begins with baking the wafer at 140°C for two minutes to remove any residual moisture from previous cleaning steps. The wafer is primed at this elevated temperature with a vapor of hexamethyldisilazane (HMDS) to improve photoresist adhesion. The wafer is then cooled to room temperature prior to photoresist coating. Photoresist is dispensed onto the wafer surface and spun at 3750 RPM to achieve the desired resist thickness. The wafer is then baked at 120°C for 120 seconds to remove 90-95% of the resist solvent and to cross link the resist. The cross-section after completion of this process step is shown in Figure 13.
Buffered Oxide Etch (BOE)

The oxide on the backside of the wafer is removed prior to CMP to decrease process time. The etch rate for the BOE is 800-1000Å/ min. The wafer with photoresist on the top surface is submersed in a buffered hydrofluoric acid bath for five minutes to remove the SiO_2 layer. The etch process is followed by a DI rinse and spin-drying. Figure 14 shows the layer structure upon completion of this step.

Chemical Mechanical Planarization (CMP)

Chemical mechanical planarization (CMP) is a process that planarizes the wafer surface to a flat, uniform finish. CMP tools use an abrasive suspended in a chemical slurry. The slurry is applied between the wafer surface and a rotating pad. The slurry is Ferro 888-G, manufactured by Ferro Corporation. Table 9 lists the process settings used for this step. The wafers are kept in a bath of distilled water until the resist can be removed. Allowing the wafers to dry after CMP will create a slurry residue on the wafer surface.
SOI wafers are backside polished for light transmission measurement purposes only. This step is not required for the operation of the ORPEL structures. Planarization of the backside of the wafer minimizes light transmission distortions caused by surface aberrations.

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equipment</td>
<td>Westech 372</td>
</tr>
<tr>
<td>Slurry</td>
<td>Ferro 888-G</td>
</tr>
<tr>
<td>Program Recipe</td>
<td>BACKSIDE6IN</td>
</tr>
<tr>
<td>Platen Speed</td>
<td>50 RPM</td>
</tr>
<tr>
<td>Carrier Speed</td>
<td>47 RPM</td>
</tr>
<tr>
<td>Pad Temperature</td>
<td>80°F</td>
</tr>
<tr>
<td>Polish Time</td>
<td>55 min</td>
</tr>
<tr>
<td>Wafer Pressure</td>
<td>1.1 psi</td>
</tr>
</tbody>
</table>

Table 9 CMP Process Recipe

**Resist Strip**

The wafer is removed from the distilled water bath and immediately soaked in acetone to remove the resist layer. The wafer is submerged in the acetone for 30 seconds. The wafer is then rinsed with DI water and spun dry. Figure 15 shows the cross-section of the device upon completion of this step.

![Figure 15 Wafer Layer Stack after O2 Plasma Ash](image)

**RCA Clean and BOE**

Since the wafers were removed from the clean room to access the CMP process equipment and the inherent contamination issues with the CMP process itself, it was necessary to clean the wafer surface before proceeding.

This RCA cleaning step is the same as described in section 3.2.1 (*RCA Clean*). However, instead of a 50:1 HF:DI water solution, a buffered oxide etch bath is used to etch the oxide layer. The wafers are etched in BOE for 5 minutes followed by a cascade rinse for 2 minutes and a spin-rinse-dry cycle.
The purpose of this step is to remove the front side oxide layer and to minimize contamination on the wafer surface prior to the Level 0 lithography process. The final c-Si thickness will be created after this step is complete.

3.2.2 ORPEL Electrode Definition

Alignment Mark Lithography – Level 0

Alignment marks will be placed in the wafer by a combination of lithography and etching processes. The alignment marks will be used to align the different layer masks during subsequent lithography steps.

Wafers are coated with Olin OIR-620-10 photoresist using the SSI wafer-coating track. The process begins with baking the wafers at 140°C for two minutes to remove moisture from previous cleaning steps. The wafers are primed at this elevated temperature with a vapor of hexamethyldisilazane (HMDS) to improve photoresist adhesion. Photoresist is dispensed onto the wafer surface and spun at 3750 RPM to achieve a resist thickness of approximately 1 μm. The wafer is then baked at 110°C for 60 seconds. Wafers are exposed in the Canon FPA 2000 i1 stepper, and then developed on the SSI wafer track. The process parameters are listed in Table 10.

The wafer alignment marks to be etched into the silicon surface are shown in Figure 16. Subsequent lithography steps will use the small “cross-in-box” feature to align the different device layers. Figure 17 is a cross-section of the device after completion of this process step.
### Process Parameter Setting

**Resist Coating**
- **Equipment**: SSI Wafer Track
- **Program**: COAT
- **Dehydration Bake**: 140°C, 2 minutes
- **Surface Prime**: HMDS
- **Resist**: Olin OIR-620-10
- **Spin Speed**: 3750 RPM
- **Soft Bake**: 110°C, 60 seconds

**Exposure**
- **Equipment**: Canon I-line Stepper
- **Program**: ORPEL1 L0
- **Dose**: 140 mJ/cm²
- **Focus**: 0.0μm
- **Mask**: Canon N0-365 Calibration

**Develop**
- **Equipment**: SSI Wafer Track
- **Program**: DEVELOP
- **Post Exposure Bake**: 110°C, 60 seconds
- **Developer**: Shipley CD-26
- **Develop Time**: 60 seconds
- **DI Rinse**: 20 seconds, followed by a spin dry for 30 seconds at 3750 RPM
- **Hard Bake**: 120°C, 60 seconds

---

### Table 10 Photolithography Level 0 Process Recipe

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Size (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>60</td>
</tr>
<tr>
<td>B</td>
<td>40</td>
</tr>
<tr>
<td>C</td>
<td>100</td>
</tr>
<tr>
<td>W</td>
<td>6</td>
</tr>
</tbody>
</table>

---

### Figure 16 Wafer Alignment Marks
Silicon Etching

Alignment marks for subsequent lithography steps are etched into the wafer surface by reactive ion etching using sulfur hexafluoride (SF₆). The LAM 490 Dry Etch system is used to etch the silicon surface. Previous experience has shown that the etch rate is approximately 0.6μm per minute. The dry etch process parameters are listed in Table 11. Figure 18 shows the cross-section of the alignment marks in the top silicon surface after completion of this step.

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equipment</td>
<td>LAM 490</td>
</tr>
<tr>
<td>Program</td>
<td>POLY</td>
</tr>
<tr>
<td>Etch Time</td>
<td>30 seconds with 15% over-etch</td>
</tr>
<tr>
<td>Base Pressure</td>
<td>0.320 Torr</td>
</tr>
<tr>
<td>Gas</td>
<td>SF₆</td>
</tr>
<tr>
<td>Gas Flow</td>
<td>150 sccm</td>
</tr>
<tr>
<td>Forward Power</td>
<td>140 Watts</td>
</tr>
<tr>
<td>Reflected Power</td>
<td>4 Watts</td>
</tr>
<tr>
<td>Electrode Gap</td>
<td>0.9 cm</td>
</tr>
</tbody>
</table>

Table 11 Silicon Reactive Ion Etching Recipe

Figure 18 Cross-section of wafer after Si Etching. Wafer alignment marks etched in surface of silicon, ~0.5μm down into silicon.
Ash Resist

Upon completion of a photolithography, etching, or deposition step, the photoresist layer used as a mask during these steps is removed by oxygen plasma. This step is performed at various steps throughout the fabrication procedure. Subsequent ashing resist steps will refer to this section for process parameter definition.

The wafer is placed in a vacuum chamber where 4000 standard cubic centimeter per minute (sccm) of oxygen and an RF-energy of 500 watts is used to create the plasma. Wafers are ashed for three minutes. Figure 19 shows the layer stack upon completion of this step.

![Alignment marks in Si](image)

**Figure 19 Cross-section of alignment marks after resist removal**

**Level 1 Lithography**

The level 1 lithography step is performed to define the reverse image of the grating fingers (also called electrodes) in the negative resist layer. This lithography steps includes three processes; coating the wafer surface with negative resist, exposing the resist to a 365 nm ultraviolet radiation source, and developing the resist.

The wafers are coated with Clariant AZ-nLOF-2010 negative photoresist using the SSI wafer track. The program recipe allows for hand dispensing of the photoresist onto the wafer surface. The program recipe is listed in Table 12.

The next step is to expose the resist coated wafers with 365nm ultraviolet radiation. The wafers were exposed using a Canon FPA-2000 i1 stepper. A focus exposure matrix was performed on control wafers and it was found that an exposure of 58 mJ/cm² and a focus of 0.0μm was the optimal setting for the nLOF resist and the mask.

The mask used for defining the electrodes was designed at RIT, but purchased from Benchmark Technologies of Lynnfield Massachusetts. The mask is a 5x, chrome on glass
reticle with pellicles on both sides to minimize defects caused by airborne particles. The smallest feature on this mask is 1.7\(\mu\)m lines and spaces.

After exposure, the wafers were developed on the SSI wafer track. The develop process includes a post exposure bake at 110\(^\circ\) C for 60 seconds, followed by a puddle spray of Shipley CD-26 developer for 50 seconds. The developer is removed by a DI water rinse and spin dry sequence. The process recipes for each step are listed in Table 12.

Figure 20 shows the cross-section of the image of the electrodes in the resist layer. The resist over the wafer alignment marks conforms to the depth of the marks, but is not shown in the sketch.

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resist Coating</td>
<td></td>
</tr>
<tr>
<td>Equipment</td>
<td>SSI Wafer Track</td>
</tr>
<tr>
<td>Program</td>
<td>ORPEL1</td>
</tr>
<tr>
<td>Dehydration Bake</td>
<td>140(^\circ) C, 2 minutes</td>
</tr>
<tr>
<td>Surface Prime</td>
<td>HMDS</td>
</tr>
<tr>
<td>Resist</td>
<td>Clariant nLOF-2010</td>
</tr>
<tr>
<td>Spin Speed</td>
<td>3750 RPM</td>
</tr>
<tr>
<td>Soft Bake</td>
<td>110(^\circ) C, 60 seconds</td>
</tr>
<tr>
<td>Exposure</td>
<td></td>
</tr>
<tr>
<td>Equipment</td>
<td>Canon I-Line Stepper</td>
</tr>
<tr>
<td>Program</td>
<td>ORPEL1_L1</td>
</tr>
<tr>
<td>Dose</td>
<td>58 mJ/cm(^2)</td>
</tr>
<tr>
<td>Focus</td>
<td>0.0(\mu)m</td>
</tr>
<tr>
<td>Mask</td>
<td>Benchmark</td>
</tr>
<tr>
<td>Develop</td>
<td></td>
</tr>
<tr>
<td>Equipment</td>
<td>SSI Wafer Track</td>
</tr>
<tr>
<td>Program</td>
<td>DEVORPEL</td>
</tr>
<tr>
<td>Post Exposure Bake</td>
<td>110(^\circ) C, 60 seconds</td>
</tr>
<tr>
<td>Developer</td>
<td>Shipley CD-26</td>
</tr>
<tr>
<td>Develop Time</td>
<td>50 seconds</td>
</tr>
<tr>
<td>DI Rinse</td>
<td>20 seconds, followed by a spin dry for 30 seconds at 3750 RPM</td>
</tr>
<tr>
<td>Hard Bake</td>
<td>None</td>
</tr>
</tbody>
</table>

Table 12 Level 1 Lithography Recipe for Clariant nLOF 2010 negative resist.
Metal Deposition

The electrodes will be formed using a metal lift-off process. Metal lift-off requires that the sidewalls of the sacrificial layer must be accessible by the solvents used during dissolution of the sacrificial layer. Therefore, an evaporation process was chosen to insure that no or minimal material is deposited on the sidewalls of the sacrificial layer.

The electrodes comprise two different metal layers. The first layer is titanium, and the purpose of the titanium is to insure that a metal-semiconductor (MS) contact is formed. The target thickness for the titanium layer is 100 Å. The aluminum layer is used to provide the electrical connectivity from the MS contact to the electrical test equipment. The target thickness of this aluminum layer is 400 Å. Both layers are deposited under a vacuum of approximately 3×10⁻⁶ Torr, however, vacuum is broken between depositions to reposition the wafer. The titanium source is a solid wound coil of titanium. A direct current of 42 amps is applied across the coil causing the temperature of the coil to increase. Titanium atoms are released from the source and deposited on the wafers surface. A pre-evaporation is executed to minimize transfer of surface impurities from the titanium source to the wafer surface. A shutter is placed over the source during pre-heating and pre-evaporation. The shutter is moved from over the source allowing the evaporated metal to deposit on the wafer surface. The wafers are mounted in the system’s planetary holders and rotated at a speed of approximately 15 RPM.

A quartz crystal resonator sensor mounted inside of the deposition chamber monitors the film thickness. Electrical signals from the sensor are recorded and displayed on the front panel of the Infinicon measurement system. The shutter is repositioned over the source once the target thickness is attained on the sensor display.
The aluminum source is an aluminum pellet weighing approximately 0.55 grams, and is manufactured by Materials Research Corporation. The aluminum pellet is placed in a coil wound tungsten basket. A DC current is applied to the basket causing the aluminum pellet to heat and melt. Once the aluminum is molten, a pre-evaporation of 30 seconds is performed before a shutter is opened exposing the wafer to the evaporated aluminum. The thickness of the deposited metal is also monitored using the quartz crystal sensor. The shutter is positioned over the source when the target thickness is shown on the sensor display panel. The process parameters for both the titanium and aluminum evaporation are listed in Table 13. The aluminum is deposited on wafers that are oriented perpendicular to the source, located 11.5 inches from the source, and are stationary during deposition. Figure 21 shows the cross-section after completion of the evaporation process.

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Aluminum Deposition</strong></td>
<td></td>
</tr>
<tr>
<td>Equipment</td>
<td>CHA Industries Evaporator</td>
</tr>
<tr>
<td>Source</td>
<td>Aluminum Pellet, Lot No. Q46-0068</td>
</tr>
<tr>
<td>Basket</td>
<td>Tungsten, multiple strand</td>
</tr>
<tr>
<td>Base Pressure</td>
<td>3·10⁻⁶ Torr</td>
</tr>
<tr>
<td>Pre-Heat Current</td>
<td>30 amps</td>
</tr>
<tr>
<td>Pre-Heat Time</td>
<td>Until molten (~ 2-3 minutes)</td>
</tr>
<tr>
<td>Pre-Evaporation Current</td>
<td>40 amps</td>
</tr>
<tr>
<td>Pre-Evaporation Time</td>
<td>30 seconds</td>
</tr>
<tr>
<td>Evaporation Current</td>
<td>40-42 amps</td>
</tr>
<tr>
<td><strong>Titanium Deposition</strong></td>
<td></td>
</tr>
<tr>
<td>Equipment</td>
<td>CHA Industries Evaporator</td>
</tr>
<tr>
<td>Source</td>
<td>99% Solid Titanium Coil</td>
</tr>
<tr>
<td>Base Pressure</td>
<td>3·10⁻⁶ Torr</td>
</tr>
<tr>
<td>Pre-Heat Current</td>
<td>40 amps</td>
</tr>
<tr>
<td>Pre-Heat Time</td>
<td>60 seconds</td>
</tr>
<tr>
<td>Pre-Evaporation Current</td>
<td>46 amps</td>
</tr>
<tr>
<td>Pre-Evaporation Time</td>
<td>60 seconds</td>
</tr>
<tr>
<td>Evaporation Current</td>
<td>46 amps</td>
</tr>
</tbody>
</table>

Table 13 Al and Ti Evaporation Process Recipe.
Metal Lift-Off

Dissolving the underlying resist layer with a resist solvent lifts off the aluminum and titanium. The metal that is deposited directly onto the substrate will not be lifted off. The metalized electrode pattern is formed upon completion of this step.

The wafer is submersed in a bath of Clariant AZ-300T resist solvent. The solvent in AZ-300T is N-Methyl-2-pyrrolidone (NMP). The wafer is submersed in NMP at 70°C for 10-15 minutes and slightly agitated. The wafer is then rinsed in DI water for 5 minutes and then placed in a spin rinse dryer. The wafer is then heated to 140°C for four minutes to remove any moisture from the wafer surface.

Figure 22 shows the cross-section of the electrodes and substrate after lift-off is complete.

3.2.3 Amorphous Silicon Overcoat

The a-Si layer is deposited using the Perkin-Elmer 2400 sputtering system. The 2400 is direct-current plasma sputtering vacuum system. An 8” silicon target was used at a power of 1000 watts using a 250K Hz DC pulsed signal. The target had a series of magnets mounted on the backside to increase plasma density.
The base pressure used in this process step ranged from $1.5 \cdot 10^{-7}$ Torr. A pre-sputter of 5 minutes at 1000 watts was performed prior to exposing the substrates to the plasma to remove any oxide on the target surface. Table 14 lists the typical process parameters for all depositions. The argon flow was adjusted to get a sputter pressure between $8 \cdot 10^{-3}$ Torr. The substrate was rotated at a speed of 2 RPM through the plasma. Figure 23 shows the cross-section after deposition. The a-Si layer is conformal to the underlying topography, but is not shown in cross-section.

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Pressure</td>
<td>$3-6 \cdot 10^{-7}$ Torr</td>
</tr>
<tr>
<td>Argon Flow</td>
<td>28 sccm</td>
</tr>
<tr>
<td>Sputter Pressure</td>
<td>$7-9 \cdot 10^{-3}$ Torr</td>
</tr>
<tr>
<td>DC Power</td>
<td>1000 Watt</td>
</tr>
<tr>
<td>DC Voltage</td>
<td>350 Volts</td>
</tr>
<tr>
<td>DC Current</td>
<td>2.86 Amps</td>
</tr>
<tr>
<td>Frequency</td>
<td>250 k Hz, pulsed</td>
</tr>
<tr>
<td>Substrate to Target Distance</td>
<td>~1.5 inches</td>
</tr>
<tr>
<td>Sputter Time</td>
<td>23 minutes</td>
</tr>
<tr>
<td>Target</td>
<td>99.9999% pure, 100 orientation, Boron Doped 9 ohm cm, 0.25” thick</td>
</tr>
</tbody>
</table>

Table 14 PE2400B a-Si Process Recipe

![Amorphous silicon layer](image)

**Figure 23 Cross-section after a-Si Deposition**

**Level 2 Lithography – Contact Cut Definition**

The level 2 lithography defines the opening that will provide electrical interconnect from the grating fingers to the electrical circuitry. Level 2 lithography utilizes the same process as defined in Section 3.2.2 (see Table 10), except the mask used is identified, as Level 2 and the exposure program is ORPEL1_L2. This lithography step will create an
opening in the resist over the electrode contact pad. The resulting cross-section after completion of this step is shown in Figure 24.

![Diagram](image.png)

**Figure 24 Level 2 Lithography: Contact Cut**

**Amorphous Silicon Etching**

The contact opening created in the previous step has exposed the a-Si layer covering the underlying aluminum contact pad. The a-Si layer is removed since it is not a good conductor in its present state. The underlying pad is used to electrically connect the electrodes during testing. The amorphous silicon that is covering the aluminum contact pad is removed by reactive ion etching. The etching process is the same as described in Section 3.2.2 (Silicon Etching). The cross-section of the device is shown in Figure 25 after the completion of this step.

![Diagram](image.png)

**Figure 25 Cross-sectioning after RIE of a-Si layer.**

**Ash Resist**

The resist mask is removed by placing the wafer in oxygen plasma. The same process is used as described in Section 3.2.2 (Ash Resist). The cross-section of the device is shown in Figure 26 after the completion of this step.
3.2.4 Contact Pad Definition

A layer of aluminum is evaporated onto the a-Si layer. This layer was patterned to create the interconnect layer between the electrodes and the electrical test circuitry. The aluminum thickness is approximately 6000Å. The aluminum was deposited using the CHA Evaporator System as described in Section 3.2.2 (Metal Deposition). The difference in this step as compared to Section 3.2.2 is the substrate is located 8 inches from the source. Three tungsten baskets mounted in parallel with a single aluminum pellet in each basket are used as the source. The quartz crystal sensor located in position two monitors the aluminum thickness. The process is halted when the desired thickness is displayed. Figure 27 shows the cross-section after evaporation has been completed.

Level 3 Lithography Metal Pattern

The level 3 lithography defines the electrical interconnect circuitry from the contact cut to the external stimulus. Level 3 lithography utilizes the same process as defined in Section 3.2.2 (see Table 10), except the mask used is identified as Level 3. The exposure program used is ORPEL1_L2. The resulting cross-section after completion of level 3 lithography is shown in Figure 28.
Aluminum Etch

The wafer is submersed in a bath of aluminum etchant solution until the aluminum defining the metal pattern remains. The etchant is comprised of a mixture of phosphoric, acetic, and nitric acids. The immersion time will be determined by the final thickness of the aluminum layer. The etch rate of the aluminum etchant is 100Å/sec at 50°C. The wafers are then rinsed in DI water and spun dry. The resulting cross-section of the layers after completion of this process step is shown in Figure 29.

Ash Resist

The resist mask is removed by placing the wafer in oxygen plasma. The same process used is described in Section 3.2.2 (Ash Resist). Upon completion of this step the layer stack resembles the sketch shown in Figure 30.
3.2.5 Overcoat Etch for Waveguide Confinement

The a-Si area over the metal electrodes is defined in this lithography step. The a-Si area completes the layer stack for defining the ORPEL structure. The same process steps described in Section 3.2.2 (see Table 10), are used to coat resist, expose and develop to get the desired geometry for the a-Si area. The mask used in this process step is identified as Level 4. The exposure program is ORPEL1_L2.

Etch a-Silicon Layer

The a-Si feature defines the waveguide cavity. The a-Si layer that is not used in defining the waveguide is removed using dry etching as described in Section 3.2.2 (Silicon Etch). Figure 32 shows the cross-section of the layers upon completion of the a-Si etching step.
Ash Resist

The resist mask is removed by placing the wafer in oxygen plasma. The same process used is described in Section 3.2.2 (*Ash Resist*). The fabrication of the ORPEL structure is completed after the conclusion of this processing step. Upon completion of this step the layer stack resembles the sketch shown in Figure 33. The ORPEL structure is defined between the top a-Si layer and the bottom of the top c-Si layer. The devices are now ready to be singulated and tested.

3.3 Processing Summary

Introduction

Results for each processing step are not included in this Section. For example, the buffered oxide etch process is an established process and the results are similar to those previously reported. Only process steps that had not been previously characterized or that encountered problems are reported in this Section.
Chemical Mechanical Planarization

CMP of both control and SOI wafers resulted in unsatisfactory surface planarity. The available slurry used during planarization was not optimized for silicon. Only portions of the backside of the wafer were planarized. Process changes to time (1 to 3 hours), platen speed (50-65 rpm), carrier speed (47-55 rpm), and wafer pressure (1.0 to 1.4 psi) were tried to planarize the backside of the wafer. Control wafer C2 was polished for 50 minutes, wafer pressure 1.0 psi, platen speed of 50 rpm and carrier speed of 47 rpm and was 90% planarized. The same process parameters except wafer pressure (1.4psi instead of 1.0psi) were used on device wafer 75578.4. A 40% planarization was achieved on this wafer. The front surface of this wafer was beginning to show wear on the outside perimeter of the wafer. It was decided not to continue planarization this wafer due to the fact that the top surface was also being polished. Device wafer 24668.1-4 was polished using the same parameters as control wafer C2, except the polish time was extended to 3 hours. The surface planarity was checked at the end of the 2nd and 3rd hours. Approximately 40% of the surface was planarized at the end of the 3rd hour. The front surface was beginning to show wear around an area inside the perimeter of approximately 0.5 inches. It was decided not to continue with planarization due to the fact that the top surface was being polished. The concern is that the c-Si layer was being thinned, which could affect the operation of the device.

Metal Deposition

Titanium and aluminum thickness after deposition are measured using the Tencor Model P2 Profilometer. Heat resistance tape was placed across control wafers in a cross pattern. After deposition the tape was removed and metal thickness was measured at nine to ten locations across the wafer. The metal thickness results are tabulated in Table 15.

The measured thickness results are compared to the readings displayed on the Infinicon measurement panel used during deposition. There are two mounting positions for the Infinicon sensor. Position one is located near the top of the planetary tooling. The second sensor position is beneath the planetary track. Titanium deposition was monitored using the sensor located in position one. Aluminum deposition was monitored using the sensor located in position two.
Evaporation of titanium resulted in a mean thickness of 108Å. The Infinicon system displayed 105Å at the end of the deposition cycle for these measured thickness values. Multiple process characterization runs resulted in a uniform titanium thickness when the wafers were mounted in the system’s planetary holders and rotated during evaporation. It was also determined that the Infinicon measurement gauge tooling factor of 100% was the appropriate setting for monitoring titanium deposition. The tooling factor is used by the Infinicon measurement system to compensate for differences in the way the tooling is configured inside the chamber. The tooling includes, the source material, the source holder, the physical location of the source, source resistance, wafer location, and rotation speed of wafer holder. The tooling configuration used for titanium included source #1, a titanium coil, an evaporation current of 42-44 amps, and the wafers rotated in the planetary at a speed of approximately 15 RPM.

The mean aluminum deposition thickness is 411Å. The Infinicon gauge displayed 426Å at the end of deposition. The aluminum is deposited on wafers that are oriented perpendicular to the source, located 11.5 inches from the source, and are stationary during deposition. A tooling factor of 70% was determined to be the best setting for a specific tooling configuration. The tooling configuration for aluminum deposition includes source #2, a multi-wire wound tungsten basket, a single aluminum pellet, and an evaporation current of 42-44 amps.

<table>
<thead>
<tr>
<th>Statistic</th>
<th>Ti Thickness (Å)</th>
<th>Al thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>108</td>
<td>411</td>
</tr>
<tr>
<td>Standard Deviation</td>
<td>8.5</td>
<td>21</td>
</tr>
<tr>
<td>Range</td>
<td>21</td>
<td>61</td>
</tr>
</tbody>
</table>

Table 15 Titanium and Aluminum Thickness Statistics. Thickness measured with profilometer across the wafer surface (ten measurements minimum).

**Level 1 Lithography – Electrode Definition**

The result of 0.68μm pitch electrode definition in negative photoresist is shown in Figure 34. The dark area in the Figure is the space between the resist lines. The dark area will become the metal line after lift-off has been completed. The clear areas indicated in Figure 34 are the resist lines and will become the space between the electrodes after lift-off. The width of the lines and spaces were measured using a Hitachi CD Scanning Electron Microscope. Five measurements were taken for both line and space dimensions.
The average space width is 0.45\(\mu\)m and the average line width is 0.23\(\mu\)m. The target width for both lines and spaces is 0.34\(\mu\)m for the 0.68\(\mu\)m grating pitch.

The electrode image in photoresist is at an exposure dose of 58 mJ/cm\(^2\). The width of the lines and spaces could be adjusted by changing the exposure dose. Keeping in mind that the resist is negative acting (the resist that is exposed remains after developing). Reducing the dose would decrease the resist dimension, the space becomes wider, and therefore the metal width increases. Increasing the exposure dose would increase the resist dimension, the space becomes narrower, and therefore the metal width decreases.

![Figure 34 Electrode Definition in Resist (0.68\(\mu\)m Pitch device). Dark area is cleared, light area resist (where noted).](PICTURES\68PITCH.TIF)

<table>
<thead>
<tr>
<th>Lines ((\mu)m)</th>
<th>Spaces ((\mu)m)</th>
<th>Pitch ((\mu)m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>Mean</td>
<td>Mean</td>
</tr>
<tr>
<td>0.227</td>
<td>0.457</td>
<td>0.683</td>
</tr>
<tr>
<td>Standard Deviation</td>
<td>Standard Deviation</td>
<td>Standard Deviation</td>
</tr>
<tr>
<td>0.010</td>
<td>0.019</td>
<td>0.022</td>
</tr>
<tr>
<td>Range</td>
<td>Range</td>
<td>Range</td>
</tr>
<tr>
<td>0.030</td>
<td>0.04</td>
<td>0.06</td>
</tr>
</tbody>
</table>

Table 16 Measurement results for 0.68\(\mu\)m Pitch Line/Space electrodes. Sample size: three chips across the wafer with five measurements per chip.

An image of the 0.70\(\mu\)m metal lines after lift-off is shown in Figure 35. The metal line and space dimension are measured using the Hitachi CD SEM. The average pitch is
0.704\(\mu m\) with a standard deviation of 0.007\(\mu m\). The average space width is 0.206\(\mu m\) with a standard deviation of 0.008\(\mu m\) (refer to Table 17).

The duty cycle is defined as the ratio of the space width to the pitch. The duty cycle is used by the RCWA software to determine reflection response behavior. For example, a pitch of 0.70\(\mu m\) with a space width of 0.35\(\mu m\) would have a duty cycle of 50%. The duty cycle of the device measured in Figure 35 is 29%. A duty cycle of 29% was entered into the model and the results of the model are shown in Section 4.2.

![Figure 35 0.70 um Metal Electrodes](PICTURES\070PITCH.TIF)

<table>
<thead>
<tr>
<th>Pitch ((\mu m))</th>
<th>Spaces ((\mu m))</th>
<th>Lines ((\mu m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>0.704</td>
<td>Mean</td>
</tr>
<tr>
<td>Standard Deviation</td>
<td>0.007</td>
<td>Standard Deviation</td>
</tr>
<tr>
<td>Range</td>
<td>0.02</td>
<td>Range</td>
</tr>
</tbody>
</table>

Table 17 Measured Metal Lines/Space Widths for 0.70\(\mu m\) structure. Sample size: three chips across the wafer, five measurements per chip.

**Amorphous Silicon Sputtering**

The amorphous silicon thickness varied across the wafer. The thickness was measured on a control wafer that was included in the chamber during the device deposition. Amorphous silicon thickness was measured using the Tencor Model P2 Profilometer. Heat resistant tape was placed across control wafers in a cross pattern. After deposition the tape was removed and a-Si thickness was measured at nine to ten
locations across the wafer. The a-Si thickness ranged from 1500Å to 2100Å. Previous process characterization runs resulted in a-Si thickness ranging from 3800Å to 5900Å for the same process recipe.

The reason for the film non-uniformity on the wafers from both the process characterization runs and the device run is due to the wafer path through the plasma. The wafer rotates angularly through the plasma; the angular velocity is slower toward the center of the chamber keeping part of the wafer in a denser plasma longer. This was verified by profilometry measurements across the surface of test wafers. This also became apparent during silicon etch characterization experiments done on the Lam 490. The area of the wafer that was located in the sputtering chamber toward the center took longer to clear during etching.

The a-Si thickness range variability between the device wafers and the process characterization wafers may be due to moisture in the argon gas line. The a-Si layer on the device wafers appeared bluish in color. Typical a-Si film has a silvery gray appearance. The blue color of the a-Si layer indicates that oxygen has been entrapped in the film during sputtering. This would explain the color variation across the wafer surface.

The sputtering process also produced considerable debris on the wafer surface. Flaking created on the target surface was noticeable after 20-25 minutes of sputtering. It is not clear as to why the surface of the target created the flakes. The surface was cleaned with acetone and isopropyl alcohol prior to sputtering. A static five minute pre-sputter was also performed prior to rotating the device wafers into the plasma.

After subsequent process steps, some areas of the wafer showed considerable metal to a-Si separation, which caused metal to peel. The unwanted metal caused the resist coating to be non-uniform across the wafer. It is speculated that the surface became contaminated or the resist layer was not thoroughly removed during ashing and prior to deposition.

It was discovered during electrical testing that the interconnect between the top metal layer and the grating metal layer was electrically open. Further analysis showed that the a-Si layer was not etched through to the electrode metal layer. Further process characterization is required insure the a-Si is etched completely.
Wafer Dicing

Finished wafers are singulated using a K&S 780 6" Dicing Saw. A diamond blade was used to perform the dicing operation. The process parameters used for the dicing operation are listed in Table 18. A wafer was mounted to the mounting ring with a laminate film on both sides to protect the structures during dicing.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equipment</td>
<td>K&amp;S 780 Saw</td>
</tr>
<tr>
<td>Program</td>
<td>ORPEL1</td>
</tr>
<tr>
<td>Blade Rotational Speed</td>
<td>20,000 RPM</td>
</tr>
<tr>
<td>Blade</td>
<td>Diamond Resinoid</td>
</tr>
<tr>
<td></td>
<td>p/n 7777-7006-008</td>
</tr>
<tr>
<td>Blade Kerf</td>
<td>0.008 inches</td>
</tr>
<tr>
<td>1st Cut Index</td>
<td>-2.6575 inches</td>
</tr>
<tr>
<td>Y-Index</td>
<td>0.5315 inches</td>
</tr>
</tbody>
</table>

Table 18 K&S Wafer Dicing Process Recipe

It was determined during preliminary dicing characterization that a protective coating other than the laminate film would be required to protect the device during dicing. It was found that peeling the laminate film would lift off the ORPEL structures from the surface of the wafer.

Control wafer, C2, was coated with resist and hard baked for two minutes at 140°C. No laminate film was applied to C2. Results of dicing C2 showed that the resist was partially removed during the dicing operation. However, structures were not damaged on wafer C2.

In order to insure that the ORPEL structures are protected during dicing, device wafers were coated with resist and hard baked prior to dicing, and a dicing laminate film was applied on top of the resist. The combinations of resist coating and laminate film provided adequate protection for the device structures during dicing. The resist and laminate film were removed by soaking the chip in acetone. Peeling the laminate film off of the device even with the additional resist layer lifted the structures from the chip. Soaking the chip in acetone dissolved the resist layer and released the laminate film without damaging the ORPEL structures.
4 Optical and Electrical Characterization

4.1 Device Reflection Spectrum

The ORPEL structure is subject to a normally incident laser beam that is swept from 1510 to 1590 nm in 0.2nm increments. The measurement setup is shown in Figure 36. The tunable distributed feedback laser source generates a laser radiation that is swept between 1510 and 1590nm. The incident beam is split 50/50 by a 3dB fiber splitter. Fifty percent of the light is linearly polarized and then coupled out of the fiber via a collimator and then focused by a cylindrical lens on to a device structure. The reflected signal is collected by the same fiber and split 50/50 on the way back through the fiber, of which an Indium Gallium Arsenide detector collects half. The other half of the reflected signal is blocked by an optical isolator to keep the signal from returning to the source.

A wavelength sweep between 1510 and 1590nm is performed on each structure on the chip. The reflected power is collected by the sensor and stored in a computer for analysis. A plot of the reflection power spectrum for structures with electrode pitches from 0.68 to 0.76μm on device 5-8 are shown in Figure 37 through Figure 41. The minimum reflected power shows the resonant frequency of the device for a specific electrode pitch.

Figure 36 Reflection Measurement Configuration

The 0.72μm power curve shows two resonant wavelengths (one near 1530 and 1570 nm). This can be attributed to three possible individual variances in the device film layers.
or a combination of 2 or more of these variances. Any variance in the grating duty cycle, the a-Si layer thickness, or the index of refraction of the a-Si layer causes the resonance to shift or produce multi-resonant behavior. Figure 37 through Figure 41 show the shift in the resonance due to change in grating pitch. The resonant wavelength for the 0.68\(\mu\)m device is near 1530nm (Figure 37), where the resonant wavelength for the 0.76\(\mu\)m structure is 1570nm (Figure 41).

![Figure 37 Reflection Spectrum for 0.68 um ORPEL device](image1)

![Figure 38 Reflection Spectrum for 0.70 um ORPEL device](image2)
Figure 39 Reflection Spectrum for 0.72 um ORPEL device

Figure 40 Reflection Spectrum for 0.74 um ORPEL device
4.2 Optical Model Adjustments

The power reflection spectrum for the 0.70 μm structure on chip 5-8 is shown in Figure 42 along with the model prediction. The ordinate axis units are arbitrary in order to overlay the experimental data and the model data. The actual reflected power of the device ranges between $3 \times 10^{-5}$ to $1 \times 10^{-4}$ watts (refer to Figure 38).

Different device components, for example, metal and a-Si layer thickness and grating duty cycle have been measured on a control wafer processed along with device 5-8. The average measured electrode pitch is 0.704 μm (see Table 17), the a-Si layer thickness ranged between 1500-1600 Å, and the duty cycle is 29%. The only unknown component of this device is the index of refraction of the a-Si layer.

The a-Si layer deposited during sputtering ranged between 1500 Å and 2100 Å instead of the required thickness of 3900 Å. The majority of the a-Si film had a bluish tint color in appearance, and this was not consistent across the wafer surface. It is speculated that the argon gas feed line was not purged entirely of oxygen (possibly due to moisture) before sputtering resulting in a film of SiOx, where $x$ is between 0 and 2. The film’s index of refraction would be less than the index of amorphous silicon ($n_{\text{a-Si}} \approx 3.45$). The only unknown input parameter for the model is the refractive index of the a-Si layer.
value for the index was selected by trial and error to be around 3.0 to fit the model to the experimental results. The model shows that an index greater than 3.3 and less than 2.8 would shift the resonance beyond the tested range of 1510 nm to 1590 nm. Assuming that the a-Si layer has an index of 3.0, the model and experimental data match relatively well. Both the model and the experimental results show a resonance near 1550 nm.

![Reflection Spectrum of 0.70 um Pitch Structure](image)

**Figure 42 Reflection Spectrum of 0.70 um Structure with Model Prediction**

### 4.3 Electrical Testing

ORPEL structures were electrically tested using a micro-probe station and an HP4145 analyzer. A probe was contacted to the aluminum contact pad connecting the grating structure. A voltage between 0 and -30 volts was applied to the structure and current was measured. A representative I-V characteristic for a 0.70μm ORPEL structure is shown in Figure 43. The result shows that the ORPEL structure conducts at a low bias, with an abrupt discontinuity current compliance at ~27 volts. It is important to note that this "breakdown-like" effect is non-destructive, repeatable, and observed using both forward and reverse voltage sweeps. However, there were subtle shifts in the I-V curve.
during repeat scans, possibly due to interface trap charges and release of carriers. A temperature study would be required to investigate charge trapping.

An ideal MS contact assumes that the layers are in atomic intimate contact, with no layers in between. However, there is a native oxide layer between the silicon surface and the titanium layer because of the delay between wafer cleaning step and metal deposition. There is also a titanium oxide layer between the titanium and aluminum layer due to processing. The vacuum chamber was vented to atmosphere between the titanium and aluminum deposition cycles to reposition the wafers. It is also assumed that there are no impurities or surface charges at the MS interface. In reality impurities could have been introduced during CMP processing due to any residual slurry material on the wafer surface. Multiple cleaning cycles were required during fabrication. The first metal deposition for the electrode definition on device wafer 24668.1 did not adhere to the substrate. The wafers had to be cleaned an additional time using the RCA process before the metal would adhere to the substrate. Oxide layers between silicon and titanium and between titanium and aluminum in conjunction with impurities introduced during CMP processing could account for the higher turn on voltage that is seen in IV curve of the device in Figure 43.

![Figure 43 IV Curve for a 0.70 um Pitch ORPEL Structure](image_url)

Figure 43 IV Curve for a 0.70 um Pitch ORPEL Structure
MS diodes were fabricated using the same processing steps used in fabricating ORPEL devices. The diodes were electrically tested using the same procedure as the ORPEL device. Figure 45 and Figure 44 shows the I-V response for the MS diode. The forward bias IV curve shows the diode turns on around 0.25 volts. These results correlate very closely to the predicted turn on voltage for an MS contact. The reverse breakdown voltage for these diodes is around -85 volts.

**Figure 44** Forward Bias IV Characteristic for a MS diode.

**Figure 45** Reverse Bias IV Characteristic for a MS diode.
4.4 Conclusions

4.4.1 Summary of Work

Optically resonant periodic electrode structures using standard microelectronic processes (optical lithography versus electron beam direct write systems) have been successfully fabricated and tested. Testing included both reflectivity spectra and I-V characterization.

Devices with grating pitches from 0.68 to 1.08μm have show resonance near the 1550 nm wavelength. Shifting in resonance due to the grating pitch has also been demonstrated. Increase in grating pitch caused the resonance wavelength to red shift, thus confirming the first order Bragg condition for buried grating structures. When the Bragg condition is satisfied a standing wave is established in the waveguide at the resonant frequency.

Optical modeling predictions and experimental results for 0.70μm devices are in good agreement. The model software is a very useful tool in predicting device resonance due to changes in the structure caused by process variances.

Electrical testing results shows that the ORPEL structure conducts at a low bias, with an abrupt onset to current compliance at ~27 volts. Although the MS contact performance of the ORPEL structure may be poor for electrical injection, it may be sufficient for electrical control of optically generated carriers. The addition of an ohmic contact to the body (similar to a base connection in a bi-polar junction transistor) would allow direct control of the bias configuration. This could be accomplished by a change to the Level 0 Mask that would provide an open area to implant boron or phosphorus to create an ohmic contact.

4.4.2 Future Work

Processing

Planarization of the backside of the wafers was inconsistent and somewhat unsuccessful. More characterization of the CMP process is required to insure 100% planarization of the backside of the wafer. Some of the devices that were planarized on the backside of the device exhibited high noise levels in the reflection spectra. Discussions with Dr. Tom Brown at the University of Rochester indicated that possible
sources of noise in the reflection spectra were caused by the backside surface to air interface. Dr. Brown suggested coating the backside of the wafer after planarization with silicon nitride or other material to minimize reflection distortion caused at the silicon-air interface.

The duty cycle of the grating electrodes is around 30% for the devices tested. A 50% grating would remove one of the variances that affect resonance. The lithography step was optimized at 58 mJ/cm² using visual inspection with an optical microscope. This proved to be an inefficient method for measuring line and width dimensions. Further lithography optimization should be done using a CD SEM to verify line and space dimensions and to insure that the resist image will produce a grating duty cycle of 50%. Changes to the exposure dose and focus should be attempted in order to reach a grating duty cycle of 50%.

Metal adhesion to large a-Si areas was problematic. The aluminum deposited for defining the electrical interconnect circuitry separated from the a-Si layer causing resist coating problems during subsequent lithography steps. Whether this was a cleanliness issue, a process related issue or a shear stress problem caused by dissimilar materials is unknown at this time. This will require further process characterization to determine cause of aluminum separation.

Layer thickness is critical to the performance of the ORPEL structure. Resonance of the device is affected by layer thickness. The exact thickness of the SOI c-Si layer could not be determined with existing measurement techniques. Therefore, the exact thickness of the c-Si layer could only be estimated from oxide growth equations. Techniques should be investigated for measuring the top silicon layer of an SOI substrate to verify final thickness.

The electrical performance of the MS contact for the ORPEL structure was poor. Contamination between metal layers, metal oxidation, and a low purity titanium source may be responsible for creating interfacial trap charges. Changes to the metal deposition process would eliminate the oxide layer between the aluminum and titanium layers. Etching the wafers in a dilute hydrofluoric acid to remove the native oxide on the silicon prior to metal deposition would improve the MS contact.
Device Testing

The electro-optical effect due to carrier charge injection was not verified due to the poor performance of the MS contact. SOI wafers with different resistivity where processed simultaneously, however due to a mishap during processing wafers with lower resistivity were not tested (electrically or optically). The electro-optical effect is highly influenced by the substrate impurity level. Substrate impurity levels between $1 \times 10^{18}$ to $1 \times 10^{19}$ atoms/cm$^3$ would provide greater changes in the index of refraction while maintaining an MS contact. Different impurities levels could be investigated to determine an optimum level of impurities to obtain maximum reflection changes while still maintaining an MS contact configuration.

Device Design

The location of the electrical interconnects pads inhibited simultaneous access of the optical and electrical test probes. A change to the metal mask would alleviate this problem. In order to bias the device a change in mask level 3 will be required to relocate the metal interconnect pads. The change in the mask will make it easier to access the interconnect pads for packaging. It is recommended that the chip be packaged so that the optical testing and electrical biasing fixturing have access to the chip simultaneously.

The c-Si layer above the buried SiO$_2$ layer electrically floats on the existing design. An addition of an ohmic contact to the body of the device would allow for different bias configurations.
5 References


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