IC Design for the TV Receiver

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IC DESIGN FOR TV RECEIVER

by

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CHAPTER I INTRODUCTION

Many novel circuit designs could have not been applied to consumer electronics because of the complexity and cost. Modern semiconductor technology removes the obstacles by allowing the use of the monolithic integrated circuit.

Integrated circuits create the possibility for new system approaches to consumer electronics as well as new circuit design techniques. This thesis discusses a horizontal and signal processing IC that is employed in color TV receivers. It is integrated with monolithic bi-polar processes.

The purpose of this thesis is not only to disclose the original concept that was employed in the circuit design, but to assist those who wish to design an integrated circuit. It also should serve the purpose for those who wish to understand the designing of an integrated circuit.

The basic color TV receiver system, signal processing system, horizontal system, integrated circuit approach, integrated circuit design, and integrated circuit testing are discussed. The integrated circuit layout, mask, diffusion process, and metallization are excluded from the discussion.
FIGURE 2-1
BASIC COLOR T.V. RECEIVER BLOCK DIAGRAM
FIGURE 2-2

COMPOSITE VIDEO SIGNAL WITH NEGATIVE GOING SYNC.
CHAPTER II BASIC COLOR TV RECEIVER SYSTEM

The TV transmission is a vestigial side band signal with a bandwidth of 6 MHz. The frequency ranges are 54 MHz to 88 MHz for the channels 2 to 6, 174 MHz to 216 MHz for the channels 7 to 13, and 470 MHz to 890 MHz for the channels 14 to 83. The picture signal is transmitted by the amplitude modulation. The channel 4, for example, is from 66 MHz to 72 MHz. It has the picture carrier at 67.25 MHz, the chroma carrier at 70.83 MHz and the sound carrier at 71.75 MHz.

The RF signal, which appears at the antenna in the block diagram Fig. 2-1, is amplified by the RF amplifier and mixed with a local RF oscillator in the tuner. The local oscillator is at 113 MHz for the channel 4. The RF amplifier stage should provide a low signal to noise ratio for the amplified RF signal, coupled to the mixer stage, for minimum snow in the picture.

The tuner output has the difference signals between the RF signal and local RF oscillator, but practically all the receiver gain and selectivity is obtained in the IF amplifiers. The vestigial side band transmission is compensated in the receiver by the frequency response of the IF stages. On the IF response curve, the picture, chroma, and sound carriers are located at 45.75 MHz, 42.17 MHz, and 41.25 MHz, respectively. In the IF stage, two traps are recommended for the lower adjacent sound carrier at 47.25 MHz and the upper adjacent picture carrier at 39.75 MHz.

The video detector is the second detector for the modulated picture carrier signal, following the last IF stage. Since the AM
picture signal is peak detected in the video detector stage, its output corresponds to the modulation envelope of the IF input signal. This envelope is the original composite video signal containing sound, luminance, chroma, and synchronizing signals.

Since the sound signal, whose carrier frequency is at 4.5 MHz with ± 25 KHz frequency deviation, is a narrow band signal, a resonant circuit can be used as a wave trap to filter out the sound signal from the composite video signal. The sound signal is limited by the sound IF limiter stages and demodulated by an FM discriminator. The audio signal is amplified by the sound amplifier stage.

The luminance signal has a band width up to 4.2 MHz. This signal requires a high frequency boost to overcome the frequency roll-off in the tuner and IF stages. It also requires the 3.58 MHz trap to eliminate the chroma (color) carrier signal and 4.5 MHz trap to eliminate the sound carrier. The luminance signal is amplified with the above requirements and applied to the picture tube.

The chroma signal has its carrier at 3.58 MHz with "I" and "Q" sideband signals. The "I" signal has a sideband of +500 KHz and -1.5 MHz. The "Q" signal has a sideband of ± 500 KHz. The "I" and "Q" signals are multiplexed with 90 degree phase difference at 3.58 MHz. The chroma signal is bandpassed to eliminate the luminance and sound signals. The output amplitude of the chroma amplifier stage is kept fairly constant by the ACC (automatic chroma control).

The chroma burst signal is applied to the chroma reference oscillator to lock the oscillator frequency to the input carrier frequency. An injection lock or PLL (phase lock loop) system is used with the crystal controlled oscillator. Two oscillator output signals, with
90 degree phase difference, are applied to the chroma demodulator.

The chroma demodulator is a coherent demodulator that requires a carrier signal. Two oscillator output signals are applied to the demodulator in order to demodulate the input chroma signal. The demodulator provides two demodulated output signals, B-Y, and R-Y. The third color signal G-Y is obtained by the proper matrix with B-Y and R-Y signals. These three signals, whose bandwidths are about 500 KHz, are applied to the picture tube.

The synchronizing signal includes horizontal and vertical sync. signals. In order to extract the sync. signal from the composite video signal, first the random noise pulses must be suppressed. This noise suppression of the composite video signal is accomplished in the noise inverter stage. The noise suppressed composite signal is applied to the sync. separator stage, which is basically a peak clamping circuit. The sync. separator output is called the composite sync. signal, since it includes the horizontal and vertical sync. signals.

The horizontal sync. signal and F.B. (Fly-Back) pulse are properly combined in the horizontal AFC (automatic frequency control) stage. A DC control voltage is provided by the AFC stage to synchronize the horizontal oscillator to the incoming sync. signal. The horizontal oscillator runs at 15.75 KHz. The horizontal output stage generates the high voltage (approximately 25 KV) and deflection current for the horizontal yoke.

The composite sync. signal is integrated with a RC time constant of 0.3 m sec. This integration extracts the vertical sync.
pulses from the composite sync. signal. The vertical sync. pulses trigger the vertical oscillator whose free running frequency is about 48 hz to 60 hz. The vertical output stage drives the vertical deflection yoke. There are basically two types of driving systems. The first is a voltage drive system and the second is a current drive system. The second system is preferred since it eliminates the nonlinearity, caused by the yoke resistance variation due to changes in temperature.

The noise suppressed composite video signal is applied to the AGC gate stage which is gated by the F.B. pulse. This stage provides a control voltage to keep the peak video signal amplitude constant while the RF signal strength varies. The AGC signal is applied to the tuner and IF stages to control the gain.
FIGURE 3-1

VIDEO SIGNAL WITH IMPULSE NOISE

FIGURE 3-2

VIDEO SIGNAL WITH SUPPRESSED IMPULSE NOISE
CHAPTER III  DESCRIPTION OF THE INTEGRATED SYSTEM

(A-1) Impulse noise clipping and amplification

The video signal sometimes contains man-made impulse noise that is higher in amplitude than the sync. signals as shown in Fig. 3-1. If the impulse noise is not suppressed, the noise pulses are separated by the sync. separator. Then the noise pulses interrupt the horizontal or vertical synchronization. In order to prevent the interruption by the noise, the noise suppression circuit is employed before sync. separation.

The impulse noise clipping level is set just above the tip of the sync. pulses as in Fig. 3-1. Any noise pulse above the clipping level is amplified and inverted by the noise amplifier. The inverted noise pulse is added to the original composite video signal, then the impulse noise is suppressed or inverted as shown in Fig. 3-2.
Impulse noise AC couple requirement

If the inverted noise pulses are added to the original composite video signal by DC coupling, a variation in the RF signal strength may develop an AGC lock-up. When a channel is changed from a weak station to a strong station, the AGC voltage is not able to change fast because of a moderately long time constant (0.1 second). The tuner and IF gain is still high, providing an unusually high video detector output signal.

The excessively high video signals go higher than the noise clipping level. The noise amplifier amplifies the sync. and video signals. The amplified signal is inverted and added to the original composite video signal. This results in a smaller composite video signal for the AGC gate stage. The smaller signal forces the AGC to increase the tuner and IF gains further, causing an even smaller composite video signal. This process continues until there is almost no video signal. It is called an AGC Lock-up.

Even when AC coupling is employed between the impulse noise amplifier and the noise suppression stage, the AGC lock-up still occurs, but only temporarily. After the AGC lock-up occurs, the AC coupling capacitor charges up and no inverted signal can transfer through the capacitor. If no inverted signal is added to the original composite video signal, then the high amplitude composite signal will appear at the AGC gate stage. Consequently the AGC system takes over and reduces the tuner and IF gains. In this way, the composite video signal amplitude is returned to normal.
(A-3) Synchronizing pulse separation

The sync separator circuit separates the synchronizing information from the composite video signal. It should function properly during reception of weak signals and particularly in the presence of impulse noise.

The reaction of the sync. separator circuit to impulse noise is extremely important in the performance of the deflection oscillators. Impulse noise has two important effects on synchronization: (1) the presence of a noise burst in the separator output represents misinformation which can cause erratic oscillator operation; (2) the nature of the peak-clamping process makes it possible for a single noise burst to "block" the sync. separator and remove sync information for a considerable period.

The various techniques for handling impulse noise are employed before sync separation. Many forms of noise clipping or inversion are encountered most commonly in circuits.

Noise upset can be considerably reduced by limiting peak noise amplitude. An ideal limiter would clip noise pulses at sync tip level. It should not clip sync amplitude enough to impair sync separation. The clipping level itself must be immune to noise.

The IC employs the impulse noise suppression or inversion and clipping circuits. Since these cannot be perfect, some small noise signals will come out of the circuits. To prevent interference by this remaining noise, a double time constant network is used for the sync. separator.
FIGURE 3-3.
HORIZONTAL LOOP BLOCK DIAGRAM
CHAPTER III DESCRIPTION OF THE INTEGRATED SYSTEM

(B-1) Transfer function

An elementary horizontal loop consisting of a phase detector, a low pass loop filter, and a voltage controlled oscillator (VCO) as shown in Fig. 3-3. The input horizontal sync signal has a phase of \( \theta_i(t) \), and the VCO output has a phase \( \theta_o(t) \). If the loop is locked, and the phase detector is linear, the phase detector output voltage is,

\[
V_d = K_d (\theta_i - \theta_o)
\]

Where \( K_d \) is called the "phase detector gain factor" and has dimensions of volts per radian. The loop filter transfer function is given by \( F(S) \).

Frequency of the voltage controlled oscillator (VCO) is controlled by the filtered error voltage \( V_2 \). Deviation of the VCO from its center frequency is \( \Delta \nu = K_o V_2 \), where \( K_o \) is the VCO gain constant and has dimensions of radians per second per volt. Since the frequency is the derivative of phase, the VCO operation may be described as \( d\theta_o/dt = K_o V_2 \).

By using Laplace notation the following equations are applicable:

\[
\begin{align*}
V_d(S) &= K_d [\theta_i(S) - \theta_o(S)] \\
V_2(S) &= F(S) V_d(S) \\
\theta_o(S) &= K_o V_2(S)/S
\end{align*}
\]

Combination of these equations results in the basic loop equation.

\[
\frac{\theta_i(S) - \theta_o(S)}{\theta_i(S)} = \frac{\theta_e(S)}{\theta_i(S)} = \frac{S}{S + K_o K_d F(S)} \quad --- \text{eq. (3-1)}
\]
$V_d(s)$ $R_1$ $V_2(s)$

$R_1 = 6.2K$ ohms \hspace{1cm} C_1 = 2 \mu f$

$R_2 = 510$ ohms \hspace{1cm} C_2 = 0.1 \mu f$

FIGURE 3-4.

HORIZONTAL LOOP FILTER
(B-2) Loop Characteristic

In a phase lock loop, the loop filter is between the phase detector and VCO. It filters the phase detector output voltage by averaging for a long period of time, thereby eliminating noise that could be very large. The filtered voltage is then applied to the VCO. The input to the loop is a noisy signal, whereas the output of the VCO is a cleaned-up version of the input. Two important characteristics of the filter are that the bandwidth can be very small and the filter automatically tracks the input signal frequency.

A widely used horizontal loop filter is shown in Figure 3-4. The loop filter transfer function is

\[ F_1(S) = \frac{V_2(S)}{V_d(S)} = \frac{R_2C_1 + 1}{R_1R_2C_1C_2S^2 + R_1C_2S + R_1C_1S + R_2C_1S + 1} \]  
\[ = \frac{1}{(1.02 \times 10^{-3} S + 1)} \]  
\[ = \frac{1}{(S + 22.13 \times 10^3) (S + 90)} \]  
\[ \text{eq. (3-2)} \]  
\[ \text{eq. (3-3)} \]

The equation 3-3 shows a zero at 156 hz and two poles at 14 hz and 3,500 hz. It is clear that the capacitor \( C_2 \) is used for high frequency filter. When the loop frequency is less than 3 KHz, the capacitor \( C_2 \) is not much effective, and the loop filter transfer function can be approximately simplified. The simple loop filter transfer function is

\[ F_2(S) = \frac{R_2C_1S + 1}{R_1C_1S + R_2C_1S + 1} \]  
\[ = \frac{S\tau_2 + 1}{S (\tau_1 + \tau_2) + 1} \]  
\[ \text{--- eq. (3-4)} \]

Where \( \tau_1 = R_1C_1 \quad \tau_2 = R_2C_1 \)
The equation (3-4) is substituted into the basic loop equation (3-1), then the second order loop will be established. The loop transfer function is

\[
\frac{\theta_e(S)}{\theta_i(S)} = \frac{S [S + 1/(\tau_1 + \tau_2)]}{S^2 + S (1 + KoKd\tau_2)/(\tau_1 + \tau_2) + KoKd/(\tau_1 + \tau_2)}
\]

----eq. (3-5)

The transfer function may be rewritten as

\[
\frac{\theta_e(S)}{\theta_i(S)} = \frac{S (S + Wn^2/KoKd)}{S^2 + 2\zeta WnS + Wn^2}
\]

----eq. (3-6)

Where \(Wn\) is the "natural frequency" of the loop and \(\zeta\) is the "damping factor". Therefore,

\[
Wn = \left( \frac{KoKd}{\tau_1 + \tau_2} \right)^{1/2}
\]

----eq. (3-7)

\[
\zeta = \left( \frac{1}{2} \right) \left( \frac{KoKd}{\tau_1 + \tau_2} \right)^{1/2} \left( \frac{1}{\tau_2 + \frac{1}{KoKd}} \right)
\]

----eq. (3-8)

The factor KoKd is known as the "loop gain"; it has the dimensions of frequency.
Static Phase Error

The phase detector compares the phase of a periodic input sync. signal against the phase of the VCO. Output of the phase detector is a measure of the phase difference between its two inputs. A small phase difference or error is usually desired. Phase error is investigated because there is no average frequency error in a locked loop.

Phase error is given by the equation (3-1) as

\[ \theta_e(S) = \frac{S\theta_i(S)}{S + KoKdF(S)} \quad \text{---eq. (3-9)} \]

The final value theorem of Laplace transforms states

\[ \lim_{t \to \infty} y(t) = \lim_{s \to 0} sY(S) \]

Application of the final value theorem to the phase error equation (3-9) yields

\[ \lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} \frac{s^2\theta_i(S)}{S + KoKdF(S)} \quad \text{---eq. (3-10)} \]

When there is a step change of frequency of magnitude \( \Delta W \), \( \theta_i(S) = \frac{\Delta W}{s^2} \). Substitution of this value \( \theta_i \) into eq. (3-10) results in

\[ \lim_{s \to 0} \frac{\Delta W}{S + KoKdF(S)} = \frac{\Delta W}{KoKdF(0)} \]

The product \( KoKdF(0) \) is called the "DC loop gain" and is denoted by the symbol \( Kv \). Therefore, the static phase error is given by

\[ \theta_v = \frac{\Delta W}{Kv} \quad \text{---eq. (3-11)} \]
Hold-in and Pull-in Ranges

The preceding investigation of phase error is based on the assumption that the phase error is sufficiently small, thus allowing the loop to be considered linear in its operation. The assumption becomes progressively worse as the error increases until, finally, the loop drops out of lock.

The phase-lock loop, employed in the horizontal IC, has a "DC loop gain", \( K_v \), defined as

\[
K_v = KoKdF(0) \quad \text{--- eq. (3-12)}
\]

The DC loop gain is the maximum feedback gain that the phase-lock loop can provide. This means that the loop gain \( KoKdF(0) \) represents the maximum possible frequency difference with which the system could hold-in. Therefore, the hold-in range of the loop is

\[
\Delta \omega_H = KoKd \quad \text{--- eq. (3-13)}
\]

when \( F(0) = 1 \) and the loop is already locked.

When a frequency offset between the VCO and input signal is lower than 3 KHz, the AC gain of the loop filter is \( \tau_2/(\tau_1 + \tau_2) \). The pull-in frequency is equal to the dynamic loop gain. Therefore, the pull-in range is

\[
\Delta \omega_p = \frac{KoKd \tau_2}{\tau_1 + \tau_2} \quad \text{--- eq. (3-14)}
\]
CHAPTER IV INTEGRATED CIRCUIT APPROACH

(A) Integrated circuit requirements

Integrated circuit requirements have to be satisfied in order to obtain a reliable, economical and well performing circuit.

For reliable integrated circuits, the maximum power dissipation of an IC package should not exceed 500 m watts in free air. The well designed IC should not dissipate more than 350 m watts. The lower the power dissipation is, the higher the reliability is. When a transistor or resistor is over-stressed in an IC, it will be a less reliable chip, even if the total power dissipation is low.

For economical integrated circuits, the total chip area should be small. Several years ago a chip area of 1,000 sq. mils was considered as a small chip, but now 3,000 sq. mils is considered as a small area. As time goes by, the small chip area will increase, since its yield is increasing with the better technology. The number of transistors and resistors should be minimized. The smaller geometry transistors and less total resistances are recommended. More functions should be integrated in one chip if possible. The standard IC package has 14 or 16 pin leads. The less pins the IC requires, the less expensive it is to produce.

For excellent performance, the IC designer should know the limitations of the integrated devices. The NPN transistors in the monolithic IC are not much different than the discrete NPN transistors, but the breakdown voltages should not be higher than 30 volts. The lateral PNP has low Beta, current and $f_T$. The substrate or
vertical PNP transistors are a little better than the lateral PNP transistor, but still far inferior to NPN transistors. The PNP transistors are discussed in detail in Chapter V.

The base diffusion resistors are most commonly used. Its resistance is 50 ohms to 25K ohms with ± 25% tolerance. The resistance matching can be 2.5%. In normal practice, 10K ohms is the maximum resistance. There are other types of resistors such as epitaxial, emitter diffusion, ion implantation and pinch resistors. The pinch resistor has specific design applications which will be explained in Chapter V. Use of capacitors is not recommended, but, if necessary, the capacitance must not exceed 30 pf.
(B) Integrated circuit design procedure

Various IC design procedures are employed by designers, but there are not many deviations from the basic rules. A designer should adopt a logical procedure that meets the fundamental requirements of the desired system and integrated circuit. The most common procedure, adopted by many companies, is discussed.

(1) System partition

An integrable system is partitioned from the main system with full knowledge of the desired system requirements and capabilities of an integrated circuit. Limitations of an integrated circuit, such as power, operating voltage, poor PNP transistor design, too high a resistance tolerance, frequency response, and noise figures, are variable as the process technology improves. A designer should be well informed about recent developments. The interface problem between the main system and partitioned integrable system has to be considered.

(2) Subsystems

The subsystems of the integrable system are designed with discrete devices. Some integrated components can be used if available. The subsystems are evaluated individually by the designer.

(3) Complete system evaluation

When all the subsystems are satisfactory, these subsystems are put into a breadboard, and evaluated as one system. The breadboard circuit is incorporated into the main system, and the complete system is evaluated.

(4) Conversion of discrete to IC design
The breadboard circuit with discrete components should be converted to a circuit configuration identical to what will be used in the IC. Current sources are recommended, wherever applicable, to reduce power consumption and chip area. It should be noted that one $V_{BE}$ voltage is about 0.6 volts at $I_C = 1$ ma in the discrete design, but it is 0.75 volts at $I_C = 1$ ma in the IC design.

The circuit must go through a major redesign to reduce the number of the internal components and required external components. High reliability can be gained by not over-stressing a single internal component. The number of pins could be reduced with novel circuit design techniques. These techniques are demonstrated in the horizontal and signal processing IC at pin #2 and 11.

Next, the final circuit diagram is drawn.

5) IC breadboard

A final breadboard is built with all the IC components except resistors. The IC breadboard is also incorporated into the main system, and evaluated extensively.

6) Mask layout

The circuit designer should be involved in the mask layout by determining: (a) the transistor sizes; (b) type of transistors for a given function since a transistor in the IC can be made for the specific requirement, such as high Beta, low saturation resistance, or high $V_{BE}$ drop; (c) type of diode such as base -- emitter junction or collector -- base junction diode; (d) Transistor matching; (e) resistance matching; (f) location of transistors to eliminate the possibility of parasitic oscillation.
FIG. 5-1

DC BIAS CIRCUIT
Chapter V Circuit Design

(A) DC Bias Network

The purpose of the DC bias network is to provide several constant DC sources. The emitter follower configuration is commonly used for a low AC impedance source. Transistor Q_{40} serves as a current source for Q_{41} as shown in Figure 5-1. A voltage of 5V_{BE} is provided at the emitter of Q_{41}, which also serves as a current source for Q_{42}. A voltage of (6.8 + 5V_{BE}) is provided at the emitter of Q_{42}. The emitter of Q_{46} has a potential of V_{CC} - (V_{BE} \cdot \text{NPN} + V_{BE} \cdot \text{PNP}). This arrangement is discussed in the section of the AC coupling of impulse noise.

One V_{BE} \cdot \text{NPN} = 0.75 volts at I_c = 1 ma and 25 degree C. One V_{BE} \cdot \text{PNP} = 0.70 volts at I_c = 0.2 ma and 25 degree C. These V_{BE} voltages change with transistor sizes. If a transistor size is increased by four times, the V_{BE} voltage is lowered by approximately 38 m volts. The following equation applies:

\[ \Delta V_{BE} = V_{BE1} - V_{BE2} = (KT/q) \ln \left( \frac{\text{size 2}}{\text{size 1}} \right) \]

As a reference point, an NPN transistor with an isolation area of 3.2 x 5 square mil and an emitter area of 0.5 square mil has a V_{BE} voltage of about 0.75 volts at I_c = 1 ma.

The preceding DC sources are immune to the supply voltage fluctuation, but temperature coefficients of V_{BE} and zener voltage should be considered. The temperature coefficient of a V_{BE} drop, at current density of 10 amperes/cm², is -2mv/degree C. The coefficient of a zener diode is approximately +2.5mv/degree C at 1 ma, with a breakdown voltage of 6.8 volts. The zener breakdown voltage
varies widely from 6.0 volts to 9.0 volts depending on the IC process.

One $V_{BE}$ reference voltage is generated in an IC by use of a base-emitter junction or base-collector junction. The base-emitter junction with the collector shorted to the base is commonly used, since the $V_{BE}$ voltage can be predicted very accurately. When the base-emitter junction is employed as a diode, its reverse breakdown voltage is only about 6.8 volts. To get a high reverse breakdown voltage, a collector-base junction with the emitter shorted to the base is employed. The junction, however, creates a parasitic PNP transistor, when the junction is forward biased. The effect of the parasitic PNP transistor can be minimized by a buried layer underneath the collector. In this case, the parasitic PNP transistor has a current gain of about 0.1. The base of the NPN diode serves as the emitter of the parasitic PNP, the collector of the NPN diode serves as the base of the parasitic PNP, and the substrate serves as the collector of the parasitic PNP.

The IC diode is made with a transistor, but it takes less area than a regular transistor. When the collector is shorted to the base, the collector terminal N+ can come very close to the base diffusion or even slightly overlap the base diffusion. One contact terminal is opened between the base and collector, instead of two contact terminals, one each for the base and collector. In this way, the distance between the base and collector is reduced. Consequently the total isolation area of a diode is smaller than that of a transistor.

A zener diode in an IC utilizes a base-emitter reverse breakdown voltage. The collector is shorted to the emitter. A zener
diode occupies the same area as a transistor, since all three contact terminals should be brought out to allow shorting the emitter and collector, and utilizing the other terminal as an anode.
FIGURE 5-2
SIGNAL PROCESSING CIRCUIT
(B) Video Amplifier

A negative going sync. video signal is applied to the base of transistor \( Q_1 \) of Figure 5-2. The signal is amplified by \( Q_1 \), and applied to an emitter follower, transistor \( Q_2 \). Transistor \( Q_3 \) provides a constant current to \( Q_2 \) in normal operation, except when impulse noise is detected. The positive going video signal at the emitter of \( Q_2 \) is applied to a darlington emitter follower, \( Q_{12} \) and \( Q_{13} \). The video output at pin #4 therefore has a very low AC impedance. Resistor \( R_{12} \) is used for current limiting, in case pin #4 is shorted to ground accidentally. Transistor \( Q_{11} \) serves as a constant current source for the darlington.

It is a general practice to employ current sources in an IC design in order to reduce the chip area and its power dissipation. For an example, the average voltage at the emitter of transistor \( Q_{13} \) is approximately 15 volts. If a 2K ohm resistor is used instead of the current source \( Q_{11} \), a 7.5 ma current flows through the resistor. The chip dissipates 150 m watts due to only one resistor when \( V_{CC} = 20 \) volts. To reduce the power dissipation, a high impedance resistor, such as 20K ohms, can be used. Then the chip dissipates only 15 m watts.

A lower resistance resistor reduces the chip area, but increases the power dissipation. A higher impedance resistor reduces the power dissipation, but increases the chip area. When transistor \( Q_{11} \) and resistor \( R_{13} \) are used as a current source, the area occupied by these two components is approximately equivalent to a 2K ohm resistor. Now the chip dissipates only 15 m watts. This proves that current sources should be employed in an IC design as a common design practice.
Transistor $Q_{10}$ and resistor $R_{14}$ are used for a current mirror function, so these should not be included in the above current source discussion.

A substrate PNP, such as transistor $Q_2$ of Figure 5-2, has a Beta of about 10 at $I_c = 1\, \text{ma}$ and $f_T = 25\, \text{MHz}$. A lateral PNP, such as transistor $Q_3$ has a Beta of about 10 at $I_c = 0.01\, \text{ma}$ to $0.1\, \text{ma}$ and $f_T = 4\, \text{MHz}$. A Beta of a lateral PNP at $I_c = 1\, \text{ma}$ is approximately one. A substrate or vertical PNP is a far better transistor than a lateral PNP. A substrate PNP, however, can be used only as an emitter follower, since its collector is the substrate of the IC. It cannot have a collector load resistor.
(C) Impulse noise clipping and amplification

A negative going composite video signal, shown in Figure 2-2, is applied at the emitter of transistor Q7 in Figure 5-2. The base of transistor Q7 is connected to an external DC reference voltage that is approximately 0.5 volts higher than the tip of the input sync. signal. Normally transistors Q7, Q4, Q5, Q6, and Q8 are in the non-conduction mode except when impulse noises are detected.

Any impulse noise, going 0.25 volts below the sync. tip, is clipped off by the transistor Q7 emitter. The clipped-off portion of the impulse noise is amplified by transistors Q5 and Q6. The amplified impulse noise signal brings up the base of transistor Q8 from ground level to 6.8 volts.

Resistors R6 and R8 are current limiting resistors, protecting transistors Q7 and Q6 from overstress. Resistor R5 is a 50K ohms pinch resistor to ensure that transistor Q5 would not be turned on by a leakage current of transistor Q7. Resistor R7 is also a pinch resistor. It ensures that transistor Q6 is turned off when transistor Q5 is off.

A pinch resistor is employed in monolithic circuits to provide large value resistors while keeping the required resistor area down. A pinch resistor structure is formed by placing an N+ type emitter diffusion over the P type base diffused resistor. The N+ type region should be connected to the positive voltage side of the resistor for normal operation.

The resistance value of a pinch resistor is 5K ohms to 250K ohms. Its absolute value tolerance is -50% and +100%, and its resistance ratio tolerance is 10%. Application of a pinch resistor is quite
limited not only due to the tremendous tolerance, but its low breakdown voltage. A pinch resistor has a breakdown voltage of 6.8 volts, since it is formed in the base and emitter regions. A pinch resistor should not be employed where the potential drop across the resistor is higher than 5 volts. An equivalent circuit for a pinch resistor is a conventional resistor in parallel with a zener diode. A 20K pinch resistor may require the same area as a 2K base diffusion resistor.

At the base of transistor Qg, there are two components, a pinch resistor and zener diode as shown in Figure 5-2. The actual IC layout has only one component, pinch resistor Rg, since the zener diode function is replaced by the pinch resistor breakdown voltage.
(D) Impulse noise AC coupling and suppression

It is established in the preceding discussion that transistors Q8 is "off" in normal operation before impulse noises are detected. And transistor Q4 is "off" since the base is biased one $V_{BE}$ lower than the emitter. The amplified impulse noise signal is applied to the base of transistor Q8, raising the base up to 6.8 volts from the ground potential. This noise signal transient generates about 6 mA of AC collector current through transistor Q8. Pin #2 or collector of transistor Q9 is normally close to ground potential. The AC current, of course, saturates transistor Q8, lowering its collector to near 6 volts. The maximum collector current of Q8 is about 1 mA, supplied by transistor Q3. This is how the impulse noise is suppressed at the emitter of transistor Q2, as shown in Figure 3-2.

When an AGC lock-up occurs, transistor Q8 stays in saturation for some time. Then the one microfarad capacitor at pin #2 is charged up to 6 volts. Therefore the AC noise current is no longer available to transistor Q8. The base of transistor Q8 is still at 6.8 volts. The emitter and collector currents are supplied by the constant current sources Q9 and Q3, respectively.

It should be noted that one $V_{BE}$ · NPN drop is across resistor R3, as emphasized in previous discussions. And one $V_{BE}$ · NPN drop is also across resistors $R_{13}$ plus $R_{14}$. The current of transistors Q9 is the same as transistor Q10. Therefore, the current ratio of the collector and emitter in transistor Q8 is inversely proportional to the resistor ratio of resistors $R_3$ and ($R_{13}$ + $R_{14}$), $750/(1K + 220)$. By the resistor ratio it is ensured that the collector DC current is
always more than the emitter DC current in transistor Q₈. This forces transistor Q₈ to come out of saturation and its collector to return to the original quiescent level, emitter potential of transistor Q₂. Now the impulse noise suppression is no longer possible and the AGC lock-up is released.

If the DC collector current of transistor Q₈ was less than the DC emitter current, transistor Q₈ would never come out of saturation. In this manner the AGC lock-up would continue indefinitely. Therefore, it is very important for the impulse noise signal to be AC coupled and for the collector current to be less than the emitter DC current in transistor Q₈.

Once the one microfarad capacitor at pin #2 is charged up to 6 volts, and the AGC lock-up is released. Then the capacitor would be discharged through the current source transistor Q₉ near to ground potential. In normal operation, the capacitor would be charged very little by the impulse noise signals. Each impulse noise duration is short and the capacitor is always discharged in the absence of noise.
(E) Sync. separator

The output of the video amplifier at pin #4 is a positive going sync. video signal. Approximately 90% of the impulse noise is eliminated from the video signal by the noise suppression circuit. The remainder of the noise amplitude is clipped off by the noise clipping network, transistor Q7.

The video signal is clamped at pin #5 through a double time constant network to provide a high degree of immunity from impulse noise. The two time constants are \( R_{15}C_1 = 0.032 \) seconds, and \( R_{17}C_2 = 32 \) \( \mu \) seconds. The video signal is filtered by a low pass filter \( L_1R_{18} \).

When a disturbing pulse is received, such as a noise burst, the change in voltage across the two capacitors is inversely proportional to their capacitances. A short pulse through \( R_{16} \) will change \( C_2 \) to a voltage about 10 times as fast as \( C_1 \). This prevents \( C_1 \) from being charged up first and discharges with the short time constant. Capacitor \( C_1 \) will be charged up during a sync. pulse period, and discharged with the long time constant during a trace period.

When the base-emitter junction of the transistor \( Q_{14} \) is used as a diode clamp, the amplified sync. pulses will appear at the collector of \( Q_{14} \). Transistor \( Q_{16} \) is a constant current source, serving as an active load for \( Q_{14} \). A diode is placed between the emitter of \( Q_{14} \) and ground, to protect the base and emitter junction from breaking down. Negative going sync. pulses appear at the collector of \( Q_{14} \).

An additional advantage of using the double time constant network is for the vertical sync. pulse interval. The vertical sync. pulses have long clamping periods and very short discharge periods. The short time constant is very effective in allowing fast discharge during the vertical sync. period.
FIG. 5-3

HORIZONTAL PHASE DETECTOR CIRCUIT
FIGURE 5-4

(a) F.B. PULSE
(b) AMPLIFIED F.B. PULSE
(c) SAW-TOOTH VOLTAGE AT PIN #7
(d) HORIZONTAL SYNC. PULSE
(e) PHASE DETECTOR OUTPUT CURRENT
(F) Horizontal AFC Detector

A position going F.B. pulse, generated in the horizontal output stage, is applied to pin #8 in Figure 5-3. The pulse is amplified by transistor Q20. Transistor Q27 is an active load for Q20. The collector of Q20 will have a waveform as shown in Figure 5-4b. A sawtooth waveform as shown in Figure 5-4c is generated at pin #7 by use of R23C4 low pass network. This sawtooth is filtered again by R31C5 low pass network, and applied to pin #9. The filtered voltage is almost a DC voltage, whose value is at the center of the sawtooth voltage.

At the junction of Q21 collector and Q23 base, a horizontal sync. pulse appears as shown in Figure 5-4d, therefore a sync. pulse of amplitude 3VBE is developed across resistor R32. A sync. signal current, 3VBE/R32, is applied to transistors Q24 and Q25 only during a sync. pulse interval. When the sawtooth voltage at pin #7 is higher than the DC voltage of pin #9, the sync. signal current goes through Q24, and composite PNP (Q29 and Q30). The same current will go through composite PNP (Q31 and Q32), and appears at the phase detector output pin #11. When the sawtooth voltage at pin #7 is lower than pin #9, the sync. signal current goes through Q25, and appears at pin #11. The phase detector output current is shown in Figure 5-4e. The output current should be equal in amplitude for both the positive and negative positions. Then it is considered to be a balanced phase detector.

Depending on arrival time of a sync. pulse signal compared with the F.B. pulse signal, the detector output current will be more positive or negative. The minimum output is zero when the positive and
negative portions are equal. The maximum output is

\[ V_{d. \ max.} = R_{44} \left( \frac{3V_{BE}}{R_{32}} \right) \left( \frac{T_s}{T_h} \right) \]  

\[ = 2.16 \text{ volts} \]  

Where \( T_s \) is a sync. pulse duration (5 u sec.), and \( T_h \) is a sync. pulse period (63.5 u sec.). The equation 5-1 shows the use of resistance ratio \( (R_{44}/R_{32}) \) rather than its absolute value. Therefore, the detector output voltage is very predictable.

The phase detector gain factor is

\[ K_d = \frac{\Delta V_d}{\Delta t} = \frac{2.16}{(T_s/2)} \]  

\[ = 0.865 \text{ v/u sec.} \]

or 8.74 v/rad.
FIG. 5-5

HORIZONTAL VCO CIRCUIT
FIGURE 5-6
EQUIVALENT CIRCUIT FOR OSCILLATOR

\[ R_{L2} = 750 \text{ ohms (DC Resistance of } L2) \]
\[ i_{C38} = h_{FE38} i_{b38} \]
\[ i_{C38} = i_{C35} + i_{C36} \]
\( (h_{ie37} + h_{ie38}) \gg R_{40} \)
FIGURE 5-7
SIMPLIFIED EQUIVALENT CIRCUIT FOR OSCILLATOR

When
(1) $i_{c35} = i_{c36}$
(2) $h_{ie37} = h_{ie38}$
(3) $R_{38} = R_{42} \parallel (R_{40} + R_{L2})$
(4) $wL_2 = 1/\omega C_8$
(G-1). Oscillator loop gain

Two conditions of an LC oscillator are that there has to be a positive feedback and the loop gain should be greater than one. The positive feedback is provided with transistors Q₃₇, Q₃₈, Q₃₅, and Q₃₆ in Figure 5-5. An input signal at pin #14 is amplified by a differential amplifier (Q₃₇ and Q₃₈). The collector signal of Q₃₈ is in phase with the input. This signal is applied to a differential amplifier (Q₃₅ and Q₃₆), and amplified by Q₃₅ and Q₃₆ without phase inversion. The phase of pin #13 signal is same as the input signal at pin #14. An LC tank circuit, which is tuned in series, is provided between pins #13 and 14. This meets the positive feedback requirement. In oscillator circuit discussion, the base voltages of Q₃₅ and Q₃₆ are assumed to be equal. Transistors Q₃₅ and Q₃₆ are employed in the phase shift network, and discussed in the next section.

When transistors Q₃₇ and Q₃₈ are in oscillation, a 50-50 duty cycle current is going through Q₃₇. This current is applied alternately to Q₃₄, then Q₃₅. The oscillator output with a 50-50 duty cycle is provided at the collector of Q₃₃.

Using equivalent circuits of Figure 5-6 and 5-7, a total loop gain of approximately 2 is calculated. In the equivalent circuits, V₃₇ is an input voltage for Q₃₇, and V₃₆ is the collector voltage of Q₃₆.
\[
\frac{V_{36}}{V_{37}} = \frac{I_c \cdot R_{38}}{2 h_{fe} \cdot I_b \cdot R_{38}} \quad \cdots \text{eq. (5-3)}
\]

\[
= \frac{h_{fe} \cdot I_b \cdot R_{38}}{4 h_{fe} \cdot I_b \cdot R_{38}}
\]

\[
= \frac{h_{fe} \cdot R_{38}}{4 h_{fe} \times 0.025} = 7.65
\]

\[
\frac{V_{37}'}{V_{36}} = \frac{R_{40}}{R_{L2} + R_{40}} = \frac{240}{750 + 240} \quad \cdots \text{eq. (5-4)}
\]

Combining eq. 5-3 and 5-4 produces

the total loop gain \( T \) of the oscillator.

\[
T = \frac{V_{37}'}{V_{37}}
\]

\[
= \frac{V_{36}}{V_{37}'} \cdot \frac{V_{37}}{V_{36}} \approx 1.9 \quad \cdots \text{eq. (5-5)}
\]
FIGURE 5-8

EQUIVALENT CIRCUIT OF PHASE SHIFT NETWORK WHEN TRANSISTOR Q35 IS NOT CONDUCTING.
G-2) Phase shift network

The purpose of the phase shift network is to make a voltage controlled oscillator out of a regular oscillator. Transistors Q35 and Q36 are a current sharing network. Transistor Q38 is treated as a constant current source during the one half of an oscillation period.

A change of the phase detector output voltage at the base of Q35, compared to the base of Q36, produces current differences in Q35 and Q36. The current difference provides a phase change at pin #13. If the currents through Q35 and Q36 are equal, and resistors \( R_{38} = R_{42}/(R_{L2} + R_L) \), then the signals at pin #12 and #13 are equal. At this time capacitor Cg is not effective. There is no phase shift in the tuned circuit \( L_2C_8 \). The tuned frequency \( f_0 \) is 31.8 KHz.

The current sharing differential amplifier (Q35 and Q36) gain is

\[
\frac{I_{c35} - I_{c36}}{V_d} = \frac{1}{R_{39} + R_{43}}
\]

\[
= \frac{1}{480} \text{ amp/v.}
\]

\[
= 2.08 \text{ ma/v.} \quad \text{--- eq. (5-6)}
\]

An equivalent circuit for the phase shift network when transistor Q35 is not operating at all, is shown in Figure 5-8. Equation 5-8 is derived from the equivalent circuit. To provide no phase shift between the collector current of Q36 and the input signal at pin 14, the sum of all the "jw" components should be zero. This results in a new oscillator frequency \( f_{36} \). Combining equation 5-6 and 5-10 produces the VCO gain constant \( K_0 \).

\[
K_0 = 2.08 \times 667 = 1,387 \text{ hz/v} \quad \text{--- eq. (5-7)}
\]

at 31.5 KHz
\[ Z_1 = \frac{R_{42} \left( R_{38} + \frac{1}{j \omega C_9} \right)}{R_{42} + \left( R_{38} + \frac{1}{j \omega C_9} \right)} = |Z_1| |\phi_{Z1}| \]

\[ Z_2 = (R_{40} + R_{L2}) + j \omega L_2 + \frac{1}{j \omega C_3} = |Z_2| |\phi_{Z2}| \]

when \( \phi_{Z1} = -\phi_{Z2} \)

\[
\frac{510 - j \frac{10^8}{\omega}}{1.5 \times 10^3 - j \frac{10^8}{\omega}} = 10^3 - j \omega \times 25 \times 10^{-3} + j \frac{10^9}{\omega} \quad \text{eq. (5-8)}
\]

Let \( Z_j \omega = 0 \)

\[ f_{36} = 30.8 \text{ kHz.} \quad \text{eq. (5-9)} \]

The phase shift network gain factor \( K_p \) is

\[
\frac{f_0 - f_{36}}{\frac{2V_{BE}}{R_{42}} \cdot \frac{1}{2}} = \frac{(31.8 - 30.8) \times 10^3}{1.5 \text{ mA}} = 667 \text{ h}_3/\text{mA}
\]
CHAPTER VI  RESULTS

Hold-in Range

\[ \Delta W_H = K_v = K_0 K_d F(o) \] from eq. 3-13

\[ K_d = 8.74 \text{ V/rad.} \] from eq. 5-2

\[ K_0 = 1,387 \text{ hz/v} \] from eq. 5-7

\[ \Delta W_H = 2\pi \times 1,387 \times 8.74 \]

Hold-in frequency

\[ \Delta f_H = \pm 12,122 \text{ hz} \]  --- eq. 5-11

at \( f_{osc} = 31.5 \text{ KHz} \)

Hold-in frequency

\[ \Delta f_{H1} = \pm 6,061 \text{ hz} \]

at \( f_{osc} = 15.75 \text{ KHz} \)

The above hold-in range is calculated assuming that the VCO constant \( K_0 \) is linear within that range. In reality, the maximum frequency change provided by the phase shift network is 1 KHz \((31.8 \text{ KHz} - 30.8 \text{ KHz})\) from equation 5-10. Therefore, the actual hold-in range with the VCO is \( \pm 500 \text{ hz} \) at \( f_{osc} = 15.75 \text{ KHz} \).

Pull-in Range

\[ \Delta W_P = K_v \tau_2/(\tau_1 + \tau_2) \] from eq. 3-14

\[ K_v = 2\pi \times 12,122 \] from eq. 5-11

\[ \tau_1 = 6.2K \times 2 \times 10^{-6} \text{ from the loop filter} \]

\[ \tau_2 = 510 \times 2 \times 10^{-6} \text{ from the loop filter} \]

\[ \Delta W_P = 2\pi \times 921 \]  ---eq. 5-12

Pull-in frequency

\[ \Delta f_H = \pm 921 \text{ hz} \]

at \( f_{osc} = 31.5 \text{ KHz} \)

Pull-in frequency

\[ \Delta f_{H1} = \pm 460 \text{ hz} \]

at \( f_{osc} = 15.75 \text{ KHz} \)

Static phase error

\[ \phi_v = \Delta W/K_v \] from eq. 3-11
Static phase error within the pull in range is

$$\theta_V = \frac{\Delta W_p}{K_V}$$

$$\Delta W_p = 2\pi \times 921 \text{ from eq. 5-12}$$

$$K_V = 2\pi \times 12,122 \text{ from eq. 5-11}$$

$$\theta_V = 75.90 \times 10^{-3} \text{ rad.}$$

Time error is

$$t_e = 0.384 \text{ u sec. at 31.5 Khz}$$

Time error constant is

$$2 \times 0.384 \text{ u sec/460 hz} = 0.166 \text{ u sec/100 hz at 15.75 Khz}$$

Damping factor

$$\zeta = \frac{1}{2} \left( \frac{k_o k_d}{\tau_1 + \tau_2} \right)^{1/2} \left( \frac{\tau_2 + 1}{K_o K_d} \right) \text{ from eq. 3-8}$$

$$K_d = 8.74 \text{ v/rad. from eq. 5-2}$$

$$K_o = 2\pi \times 693 \text{ rad./v at 15.75 Khz from eq. 5-7}$$

$$\tau_1 = 6.2K \times 2 \times 10^{-6} \text{ from the loop filter}$$

$$\tau_2 = 510 \times 2 \times 10^{-6} \text{ from the loop filter}$$

$$\zeta = 0.84$$

Natural frequency

$$W_n = \left( \frac{k_o k_d}{\tau_1 + \tau_2} \right)^{1/2} \text{ from eq. 3-7}$$

$$W_n = 1.635 \times 10^3$$

$$f_n = 261 \text{ hz}$$

Noise clipping, inversion and sync separator

There is no practical way to obtain and indicate the performance of these functions by a numerical value. The relative comparison demonstrated excellent performance.
Chapter VII Integrated Circuit Test

The integrated circuit is designed and processed on a silicon wafer. After the metallization step, the completed IC chips on the wafer should be tested thoroughly to sort out good chips. This test (probing) determines the wafer yield. The average wafer yield is approximately 40% to 50% with 60 x 60 mil chips. It has been a common practice to process two inch diameter wafers. However, many IC manufacturers are starting to process three inch diameter wafers to increase the total number of chips on a diffusion process, and thus increase the total yield.

The probing process is the first test of the chips after all the diffusion processes are completed. It, however, can not be regarded as a preliminary rough test. The average cost of a chip on a wafer is about 7¢ and the packaging cost of an IC is about 40¢ for a 14 pin plastic package. If the probing process was not thorough, the bad chips could be packaged and the unit IC price would be increased. Therefore, any chip with a marginal test result should be rejected in the probing process. If this is done, when the chips are packaged, the marginal units in the final test may be considered as good units.

The probing and final test methods, and expected results, are generated by the circuit designer. All the tests should be performed within 200 m sec. per chip for mass production. An automated computer program is utilized for fast measurement and decision. DC tests instead of AC tests are strongly recommended.

Some parasitic oscillations may occur in the wafer probing process due to the long interconnecting wires. Even if the wafer probing stage
and the computer are located near by each other, the interconnecting wires are approximately 6 ft. To prevent the parasitic oscillation, every pin of the chip is by-passed with a capacitor. Therefore, AC tests are not possible under this type of environment, unless the test frequency is within a low audio range.

High frequency test equipment is available, but if the AC tests are required, the unit IC cost will increase tremendously. The $f_T$ of an IC transistor does not vary much since the same diffusion process is employed. The stray capacitances and inductances due to interconnections in the IC remain constant from chip to chip. For this reason, 100% DC tests with the AC tests on a sample basis should be sufficient testing to meet all the requirements in the analog circuits. The digital circuits are tested at a low frequency toggling rate (not higher than 50 Khz), in addition to the DC tests.

Three of the horizontal and signal processing IC parameter distributions are illustrated on Figures 7-1, 2 and 3. These are the computer read-outs for 194 units in the probing stage. In the figures, the two columns at the extreme left are ranges of voltage or current distribution. The first column at the extreme right is the number of chips per range (or cell). The second column from the right is the accumulated percentage of the chips from the low voltage or current range. The third column from the right is the independent percentage in each cell.

Figure 7-1 shows the current drain distribution of the IC when the supply voltage is +30V. The IC operates at about +22 volts in the actual application, but it is tested at +30V to simulate the worst case
condition for a supply voltage transient. The units between 15.0 ma and 25 ma are acceptable.

Figure 7-2 shows the video amplifier gain distribution at pin #4 when +2 volts DC is applied to pin #1. The acceptable voltage range is 23.5 volts to 25.5 volts.

Figure 7-3 shows the DC bias voltage distribution for the phase shift transistors Q35 and Q36 at pin #11. This test also allows determination of the horizontal phase detector network leakage current effect. The acceptable voltage range is 10.25 volts to 12.00 volts. Seven units above 15.00 volts indicate the effect of a strong leakage current in the phase detector.
Chapter VIII Conclusion

A horizontal and signal process IC has been designed for a color TV receiver, following the discussed IC design procedure and method. Excellent results have been obtained with the IC. The use of novel circuit design techniques was incorporated. There was no discrepancy between the theoretically expected results and actual performance. This demonstrates that the discussed design procedure and method can be recommended for future IC design exercises.

The integrated circuit provided excellent noise clipping, noise suppression (or inversion), and sync separator functions. It also provided; (1) a stable horizontal oscillator with a frequency deviation of less than 60 hz from the desired 31.5 Khz. This deviation is true for a temperature range of 0 degree C to +55 degree C. (2) a balanced phase detector that improves impulse noise immunity. (3) a small static phase error of (0.166) u sec/100 hz compared with the conventional phase error of a 0.3 u sec/100 hz. (4) a wide pull-in range of ± 490 Hz compared with ± 180 hz at 15.75 Khz. (5) a wide hold-in range of ± 500 hz compared with 220 hz. This performance resulted in elimination of the horizontal hold control on a TV receiver.

It is recommended that the horizontal and signal process IC includes the AGC function for a perfect system partition. This recommendation is because the design of the sync, separator, noise inversion, and horizontal AFC is intimately related to the AGC. Therefore these should be regarded as a system problem.
REFERENCES


