Optimal design of a 2.4 GHz CMOS low noise amplifier

Sharmila Sridharan

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Optimal Design of a 2.4 GHz CMOS Low Noise Amplifier

by

Sharmila Sridharan

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In

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Abstract

In most RF receivers, the Low Noise Amplifier (LNA) is normally the first component, whose performance is very critical. For the LNA architecture that uses source degeneration inductors and cascode topology, the performance depends largely on the performance of the inductors. All the parasitics associated with the inductors should be thoroughly analyzed and taken into consideration while designing the LNA. The work presented in this thesis can be broadly classified as follows: optimization of the LNA design with respect to all the parasitics associated with the on-chip spiral inductors, modeling high performance inductors, which are embedded in the silicon substrate and analysis of parasitic effects from the Electro Static Discharge (ESD) protection circuitry on the performance of the LNA. A methodology has been developed such that the LNA design can be optimized in the presence of an ESD protection circuitry in order to achieve the required input impedance match. This optimization procedure is presented for all possible placements of the ESD protection circuitry at the input of the LNA, that is, with respect to the gate inductor being realized on-chip or off-chip or a combination of on-chip and off-chip inductors. The thesis presents the procedure to vary the source inductance and gate inductance values in the presence of parasitic ESD capacitance in order to optimize LNA design such that the required input impedance match is maintained.
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CHAPTER 1

Introduction

1.1 Background

The low noise amplifier (LNA) is one of the first blocks and an important component in the receive path of most wireless receivers. The block diagram of a radio frequency (RF) receiver using heterodyne architecture is as shown [1]:

![Heterodyne receiver block diagram](image)

**Fig. 1.1.** Heterodyne receiver block diagram

BPF1 is a bandpass filter also called the band selection filter since it is used to select the band of interest of the received signal. The next stage is the LNA, which is used to amplify the signal with minimal additional noise by the amplifier. The next stage is another bandpass filter (BPF2) called the anti-image filter followed by the mixer. Here a variable local oscillator (LO) frequency is used and the mixer is followed by a bandpass
filter BPF3 also called the channel filter. This channel filter is then followed by an intermediate frequency (IF) amplifier. The output of this amplifier is then demodulated using a demodulator.

Since the signal at the input of the LNA is normally a very weak signal, the LNA should provide good gain and noise performance. Also, in the receiver, the noise figure of the LNA is very critical. This can be illustrated using Frii’s formula [2] as follows:

\[
NF_{\text{tot}} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{G_1} + \ldots + \frac{NF_m - 1}{G_1 \ldots G_{(m-1)}}
\]  

(1.1)

where \(NF_1 \ldots m\) is the noise figure of the respective stages, \(NF_{\text{tot}}\) is the total noise figure and \(G_1 \ldots (m-1)\) is the gain of the respective stages. It is evident from the above equation that the noise contributed by each stage decreases when the gain of the preceding stage increases. Hence the noise figure of the first few stages in a cascade is very critical.

Next, the definition of some of the terms commonly used in RF circuits is provided [2].

(i) **Harmonics**: When a sinusoid is applied to a nonlinear system, the output contains frequency components that are integer multiples of input frequency. An
expression can be obtained in which the term with the input frequency is called the "fundamental" and the higher order terms are called "harmonics".

(ii) Gain Compression: The gain varies with the variation of the signal amplitude. In most circuits of interest the gain approaches zero for sufficiently high input levels. This is because the output is a compressive or saturating function of the input. In RF circuits, the "1-dB compression point" quantifies this effect. It is defined as the input signal level that causes the small signal gain to drop by 1 dB.

(iii) Desensitization and Blocking: Since a large signal tends to reduce the average gain of the circuit, the weak signal may experience a vanishingly small gain. This is called "desensitization". In RF design, the term "blocking signal" usually refers to interferers that desensitize a circuit even if the gain does not fall to zero.

(iv) Cross Modulation: The transfer of noise or modulation on the amplitude of the interferer to the amplitude of the weak signal is referred to as cross modulation. This occurs when a strong interferer and a weak signal pass through a nonlinear system.

(v) Intermodulation: This phenomenon arises as a result of the mixing of two signals and when their sum is raised to a power greater than unity. The output generally contains components that are not harmonics of the input frequencies.
1.2 Thesis Outline

The thesis presented here can be divided into three main areas of focus. The first part of the work consists of designing a fully integrated CMOS LNA for radio frequency (RF) applications. The inductors in the LNA design are all on-chip spirals built on the top-most metal layer. The second part of the work consists of modeling high quality factor embedded inductors for RF applications. A thorough analysis and comparison of parasitics associated with on-chip spirals and embedded inductors is done. No previous work has been reported with inductors being constructed in the silicon substrate to achieve high quality factor. The third portion of the work consists of the analysis of ESD parasitic effects on the performance of the LNA. Previous work has only considered the analysis of CMOS LNA with ESD protection only for the case when off-chip inductors are used to realize the gate inductor [3]. Here, a thorough analysis of the input impedance of the LNA with respect to the placement of ESD parasitic capacitance is illustrated for the following cases:

(i) when the gate inductor is realized completely on-chip;
(ii) when the gate inductor is realized completely off-chip;
(iii) when the gate inductor is realized as a combination of on-chip and off-chip inductors.

For the first case, the placement of the ESD parasitic capacitance is between the input pad and the gate inductor. In the second case, the placement of the ESD parasitic
capacitance is between the input pad and the gate of the input transistor. In the third case, the placement of the parasitic capacitance is between the off-chip and on-chip inductors. A procedure to obtain input match in the presence of ESD parasitics for all the above cases is also presented.

1.3 Organization

In the second chapter, the design procedure for a fully integrated narrowband CMOS LNA is presented. Since the LNA is fully integrated, its performance depends largely on the performance of the on-chip spirals. The on-chip spirals are normally built on the topmost metal layer in order to keep them far away from the substrate. The chapter also discusses the modeling of these inductors. A CAD tool called ASITIC (Analysis and Simulation of Inductors and Transformers for Integrated Circuits) [4] is used to model inductors for the LNA design.

The third chapter illustrates a novel fabrication technique called the Integrated Materials Wafer (IMW). Using this technique embedded inductors are constructed and these inductors were also modeled. In this technique the inductor is placed in the substrate, but isolated from the substrate using an insulative layer. This isolation results in avoiding most of the parasitics associated with on-chip spirals. The simulation results are also presented which show the improvement in the performance of embedded inductors over the on-chip spirals made on the top-most metal layer.
In chapter four, the types of ESD events, importance of using ESD protection circuits and commonly used ESD protection circuits are presented. Simulation results for the performance of the LNA with ESD circuits is presented. Theoretical analysis and procedure to obtain input impedance matching when the ESD protection circuitry is included is also illustrated. The analysis is done with respect to fully integrated LNA wherein the placement of ESD capacitance is between the input pad and the gate inductor. The importance of designing the LNA by taking the ESD parasitic effect into account is highlighted.

Chapter five discusses the theoretical analysis and procedure to obtain input match in the presence of ESD circuits for the following two cases wherein:

(i) the gate inductor is completely off-chip and

(ii) the gate inductor is a combination of on-chip and off-chip inductors.

The last chapter summarizes the results. The chapter also discusses future work that can be done.
CHAPTER 2
LNA Design in 0.25 um CMOS Technology

This chapter discusses the design procedure of a fully integrated narrowband CMOS LNA. The specifications and the reason for the choosing inductive degeneration and cascode topology are first discussed. The formulas used in the design process are then provided along with the design procedure. The trade-offs in the design are also presented. The performance of this LNA is found to depend to a large extent on the quality of inductors used. Since the design is fully integrated, all inductors used are on-chip.

The range of inductance values that are available in the 0.25 um process is limited, so it is necessary to model the inductors. Modeling of inductors was done using a computer aided design tool called ASITIC (Analysis and Simulation of Inductors and Transformers for Integrated Circuits) [4]. Due to the importance of inductor performance in the chosen architecture of the LNA, a section is also provided which discusses briefly about the modeling of on-chip inductors for RF applications and their limitations. Simulation results for the designed LNA are also furnished.
2.1 LNA Design

2.1.1 Specifications

Basic requirements of an LNA are to provide good gain, low noise figure, sufficient linearity, stable input impedance and low power consumption. The design of a low noise amplifier presents a considerable challenge because, the above stated requirements of the LNA are all equally important but to achieve them simultaneously is a difficult task. For example, the source impedance, which yields minimum noise figure, may differ considerably from one that maximizes power gain [5]. Hence it is essential to understand the trade offs involved in the LNA design.

The technology used for the design of the low noise amplifier is the TSMC 0.25 um CMOS process that supports five metal layers and one poly layer. The specifications for the design are as follows:

Table 2.1 Specifications

<table>
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<tr>
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<tr>
<td>Operating Frequency</td>
<td>2.4 GHz</td>
</tr>
<tr>
<td>Bias Current</td>
<td>&lt;10 mA</td>
</tr>
<tr>
<td>Source Resistance</td>
<td>50 ohms</td>
</tr>
<tr>
<td>Power Supply</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>&lt;15mWatts</td>
</tr>
</tbody>
</table>
2.1.2 LNA Topology

Each requirement of the LNA is considered when coming up with a design. The design is started with a method to achieve stable input impedance of 50Ω, which is an important criterion. Some of the commonly used topologies to achieve the required input match are presented here [6].

Fig. 2.1 Different topologies for input impedance matching
One method to achieve impedance matching at the input is, by using resistive termination as shown in Fig. 2.1 (a). But, use of resistors is detrimental to the amplifier’s noise figure. Another approach is to use the source of a common gate stage for input termination as shown in Fig. 2.1 (b). In this case, the noise figures will degrade at high frequencies especially because of noise due to gate current. The third topology as shown in Fig. 2.1 (c), is to use resistive shunt and series feedback. This is not chosen due to high power dissipation. It is mostly used for broad band applications [6].

The architecture chosen for the design is that of a cascode amplifier with inductive source degeneration as shown in the Fig 2.1 (d). This architecture provides the best noise performance because, no real resistors are used. The inductor at the source is used for impedance matching at the resonant frequency and an inductor at the gate terminal is used to set the resonant frequency.

The cascode topology aids in achieving high gain and the cascode transistor helps in isolating the Miller capacitance of M1 from the output. A single stage is used in order to reduce power consumption.
2.1.3 Design Procedure

For the cascode amplifier with source degeneration, the input impedance is given by:

\[
Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs1}} + \frac{g_{ml}}{C_{gs1}} L_s + R_g + R_{ls} + R_{lg}
\]  

(2.1)

where \( L_g \) is the gate inductance, \( L_s \) is the source inductance, \( C_{gs1} \) is the gate to source capacitance of transistor M1, \( g_{ml} \) is the transconductance of M1, \( R_g \) is the gate resistance of M1, \( R_{ls} \) is the series resistance of the source inductor and \( R_{lg} \) is the series resistance of the gate inductor.

The value of the distributed gate resistance \( R_g \) is calculated using [7]:

\[
R_g = \frac{R_{sh} W}{3n^2 L}
\]  

(2.2)

where \( R_{sh} \) is the sheet resistance of the polysilicon, \( W \) is the total gate width of the device, \( L \) is the gate length and \( n \) is the total number of gate fingers. The factor 1/3 comes from distributed gate analysis, going by the assumption that each of the gate fingers is contacted only at one end. The factor can be reduced to 1/12 by contacting the gate finger
at both ends [6]. These are some of the layout techniques that can be used to improve the performance.

At resonance, the input impedance is given by the following equation:

\[ Z_{in} = \frac{g_{ml}}{C_{gs1}} L_s + R_g + R_{is} + R_{ig} \]  

(2.3)

From the above equation, it is clear that the values of \( R_g \) and \( R_{ig} \) have to be known in order to get the correct matching. The values of the series resistance of the on-chip inductors can be got from the pi model of these inductors. For this, the value of \( L_s \) is first calculated using:

\[ Z_{in} = \frac{g_{ml}}{C_{gs1}} L_s + R_g \]  

(2.4)

Here, the value of \( Z_{in} \) is set to 50 \( \Omega \). Hence the value of \( L_s \) sets the input impedance at resonance.
The value of the gate inductor can then be calculated using:

\[
L_g + L_s = \frac{1}{\omega_0^2 C_{gs}}
\]  

where \( \omega_0 \) is the resonant frequency.

The gate inductor \( L_g \) is used to set the resonance frequency at the input of the amplifier. Normally, a DC blocking capacitor is used to prevent the gate-to-source bias of the input transistor from changing [5]. If such a capacitor is used, then there will be a shift in the resonant frequency and the value of gate inductor should be recalculated. If a large capacitor is used, then the reactance at the signal frequency can be neglected.

Once the values for \( L_s \) and \( L_g \) were obtained, they were modeled using ASITIC. The modeling of inductors is explained in Section 2.2. The series resistance of the inductors was obtained from the pi model. It was found that the series resistance of the gate inductor \( R_{lg} \) was significant and non-negligible. Hence, with the knowledge of the values of \( R_s \) and \( R_{lg} \), another iteration of the design procedure was done. By doing so, all the parasitic resistances were accounted for.
The channel width of the input transistor is calculated using the following formula [5]:

\[
W = \frac{1}{3\omega L C_{ox} R_s}
\]

(2.6)

where \( C_{ox} \) is the oxide capacitance and \( R_s \) is the source resistance (=50 ohms).

The size of the cascoding transistor M2 is chosen to be the same as that of M1. This is a trade-off in order to suppress the noise magnitude of M2 and the Miller effect of M1 [5]. The cascode transistor M2 reduces Miller effect, improves reverse isolation and also isolates the matching network at the output from the one at the input.

At the output side, the value of \( L_d \) is chosen in order to set the center frequency. For this, the value of the total capacitive loading which includes the gate to drain capacitance \((C_{gd})\) of M2, the drain to bulk capacitance \((C_{db})\) of M2 and the input capacitance \(C_L\) of the following stage (which is usually a mixer) should be known. Also the parasitic capacitance associated with the inductor \( L_d \) \((C_{ld})\) should be calculated. The formula to set the resonance frequency at the output is as follows:

\[
\omega_o = \frac{1}{\sqrt{L_d(C_{gd} + C_{db} + C_{ld} + C_L)}}
\]

(2.7)
The determination of the load inductance value depends on the total capacitance seen at the output node, which is actually not limited to the capacitance of the following stage $C_L$, $C_{gd}$, $C_{db}$ and $C_{ld}$. Apart from the above mentioned capacitances, the interconnect capacitance should also be taken into account. The interconnect capacitance value can be obtained by performing an extraction of the layout.

After calculating the device sizes and the values of the required inductors, the bias network was designed [5]. The bias network consists of transistor M0 and the resistors R0 and R4 as shown in the schematic in Fig. 2.3. M0 forms a current mirror with the input transistor M1. The value of R4 is chosen to be large (around 2 KΩ) such that its equivalent noise current is negligible. Also a DC blocking capacitor is used in order to prevent any change in the gate to source biasing of M1. This DC blocking capacitor value is chosen large enough such that the reactance at the signal frequency is negligible.
After the LNA is designed, the performance metrics like noise figure and power gain are analyzed. The small signal noise model is as shown in Fig. 2.2. [6].

![Small signal noise model](image)

The channel thermal noise is the dominant source of noise and is modeled as a shunt current source on the output side of the device. It is given by \( i_d^2 \) and shown in the figure as I4. Another noise source is that due to distributed gate resistance which is modeled by \( R_g \) (series resistance at gate) and \( v_{rg}^2 \) (white noise generator) which is represented as R3 and V4 respectively in the above figure. Gate noise is another source of noise, which occurs due to the capacitive coupling of current in the gate. The gate noise itself is expressed as two parts, one which is correlated with drain noise (\( i_{g.c}^2 \)) shown as I1 and the second part which is uncorrelated with drain noise (\( i_{g,u}^2 \)) depicted as I2. The inclusion of the gate current noise sets a lower limit on the achievable noise figure.
The expression for Noise factor (NF) is [8]:

\[
NF = 1 + \frac{R_{bg} + R_{ls}}{R_s} + \frac{R_s}{R_s} + \gamma g_{do} R_s \left( \frac{\omega_o}{\omega_l} \right)^2
\]  

(2.8)

where \( g_{do} \) is the zero-bias drain conductance of the device and \( \gamma \) is a bias dependent factor which satisfies \( 2/3 \leq \gamma \leq 1 \) for long channel devices. For short channel devices in saturation, the value of \( \gamma \) is greater than 2/3.

The equation for gain is as shown [9]:

\[
A_v = g_{m1} Q_{in} \frac{Z_{ld}}{2}
\]  

(2.9)

If the width of the transistor M1 is decreased, then, the gate to source capacitance of M1 decreases. Accordingly the value of \( L_g \) and \( L_s \) will increase in turn increasing \( Q_{in} \). But increasing the inductance \( L_g \) will result in an increase in the series resistance of inductor \( L_g \). This parasitic resistance will degrade noise figure and also affect the impedance matching.
The value of inductance $L_s$ and $L_g$ will affect the impedance matching and resonance frequency, but the quality factor of the inductors would influence both noise figure and gain. Hence in the chosen architecture of the LNA, the performance of the inductors is very important and they have to be modeled carefully especially in terms of the quality factor and self-resonant frequency.

Also as a result of technology scaling and small feature sizes of transistors, the value of the tranconductance has increased leading to an increase in the unity gain frequency of the transistors. This in turn has improved the noise performance of CMOS circuits.
The complete schematic of the LNA design is as shown in Fig. 2.3. Each inductor is replaced by its pi model in order to account for the parasitics of the on-chip inductor.
2.2 Inductor Modeling

All the inductors required for the LNA design had to be built on-chip considering the fact that the LNA had to be fully integrated. The range of inductances that were characterized by the TSMC 0.25um process was limited and did not cater to the requirements of the design. The inductors characterized for the process were for a specific geometry and for a limited number of turns. Hence the required inductor values were modeled using a computer aided design tool called ASITIC (Analysis and Simulation of Inductors and Transformers for Integrated Circuits). This section presents a brief description of on-chip inductor modeling and the issues involved.

The lossy silicon substrate poses a challenge to the design of high quality inductors on-chip. The performance of an inductor is generally expressed in terms of the quality factor $Q$ that is given by [10]

$$Q = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}}$$  \hspace{1cm} (2.10)

The geometry of the inductor is specified by the number of turns $n$, the width of the turns $w$, spacing between adjacent turns $s$ and the inner diameter $d_{\text{in}}$ or the outer diameter $d_{\text{out}}$. These parameters are varied in order to get the required inductance and $Q$ factor.
Another important figure of merit for an on-chip inductor is its self-resonant frequency. The silicon substrate is usually close by and also conductive, creating a parallel plate capacitor. This capacitor resonates with the inductor and the resonant frequency, which arises from the LC combination, defines the upper useful frequency limit of the inductor also called self-resonant frequency [5].

The on-chip inductors are usually planar spirals and are built on the top metal layer. The TSMC 0.25 um process supports a thick top metal layer. The top metal layer is preferred for constructing the passives because it is comparatively far from the substrate and hence the substrate losses can be minimized. The following model for an on-chip spiral shows the various parasitics associated with it [11]:

![Fig. 2.4. Spiral Inductor Model](image)
The parasitics associated with an on-chip spiral can be explained using the following equations [11]. \( R_s \) is the series resistance of the spiral and is given by:

\[
R_s = \frac{\rho l}{w \delta (1-e^{-\delta})}
\]  

(2.11)

where \( \rho \) is the metal resistivity at dc, \( l \) is the overall length of spiral, \( w \) is the line width, \( \delta \) is the metal skin depth and \( t \) is the metal thickness.

\( C_p \) is the shunt capacitance and is expressed as follows:

\[
C_p = n w^2 \frac{\varepsilon_{ox}}{t_{ox,M1-M2}}
\]  

(2.12)

where \( t_{ox,M1-M2} \) is the thickness of oxide between the main spiral and the center tap. \( n \) is the number of crossovers between the spiral and center tap.

\( C_{ox} \) is the capacitance between the spiral and the substrate and is written as:

\[
C_{ox} = w l \frac{\varepsilon_{ox}}{t_{ox}}
\]  

(2.13)

where \( t_{ox} \) is the oxide thickness between spiral and substrate.
R1 and C1 model the silicon substrate and they are expressed as shown:

\[
R_1 = \frac{2}{lwG_{sub}} \quad (2.14)
\]

\[
C_1 = \frac{lwC_{sub}}{2} \quad (2.15)
\]

where \( G_{sub} \) is the substrate conductance per unit area and \( C_{sub} \) is the substrate capacitance per unit area.

Different geometries of the spiral inductor, to achieve the required value of inductance accompanied by a reasonable Q and self-resonant frequency, were investigated using ASITIC by varying the inner and outer diameter of the spiral, the metal width and the metal spacing. Square spirals are used in this LNA design. It is found that by increasing the width of the spiral results in a decrease in the series resistance, but the parasitic capacitances increase. Increase in the shunt capacitance would in turn degrade the self-resonant frequency of the spiral. The width of the spiral should be carefully decided.

An increase in the number of turns of the spiral increases the value of inductance. It is observed that the contribution of inner turns to the inductance is very less. But they tend to increase the series resistance and also the parasitic capacitance to the substrate. Hence hollow inductors favor the improvement of self-resonant frequency [9].
In order to theoretically predict the value of the inductance for a particular geometry of the square spiral, expression based on current sheet approximation [12] was used. The expression is as shown:

\[ L = \frac{\mu n^2 d_{avg} c_1}{2} \left[ \ln \left( \frac{c_2}{\rho} \right) + c_3 \rho + c_4 \rho^2 \right] \] (2.16)

\[ \rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \] (2.17)

where \( L \) is the inductance, \( d_{avg} \) is the average diameter, \( n \) is the number of turns, \( \rho \) is the fill ratio, \( c_i \) are coefficients which are layout dependent.

Equation (2.16) was used to determine the dimensions of the spiral that resulted in the required inductance. This was done by varying the number of turns and the fill ratio. Then a pi model for the same at the operating frequency was obtained using ASITIC.

The inductance values required for this design ranged from 0.35 nH to 11 nH and all the necessary inductors were modeled using ASITIC. The geometry of the spiral, which resulted in an optimum value of inductance, Q factor and self-resonant frequency was chosen and used in the low noise amplifier design.
2.3 Simulation Results

In this section, the various simulation results are presented. Table 2.2 provides a summary of the LNA's performance.

<table>
<thead>
<tr>
<th>Process</th>
<th>0.25um</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias Current</td>
<td>5mA</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.4GHz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>3.3dB</td>
</tr>
<tr>
<td>Power Gain</td>
<td>11dB</td>
</tr>
<tr>
<td>S11</td>
<td>-13.3dB</td>
</tr>
<tr>
<td>S12</td>
<td>-36.5dB</td>
</tr>
<tr>
<td>1dB Compression</td>
<td>-5dBm</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>15.7mW</td>
</tr>
</tbody>
</table>
The plots for the power gain and noise figure are as shown in Fig. 2.5 and 2.6 respectively.

![Gain plot](image1)

**Fig. 2.5. Gain plot**

![Noise figure plot](image2)

**Fig. 2.6. Noise figure plot**
The TSMC 0.25 um technology provides constant gate finger widths of 5 um and 10 um. Simulations done using the model for the devices using 5 um gate finger width resulted in a noise figure of 3 dB as against 3.3 dB for a finger width of 10 um. This confirms that by increasing the number of gate fingers and decreasing the width of each finger lowers the noise figure. For RF design, the gate width is kept small because otherwise it tends to gain axial resistance and the signal at the other end of the gate is delayed.

The calculated value of the gate inductance was around 11 nH but the value of the inductor used was around 10.5 nH. This is because, for this value of inductor, the model from ASITIC predicted a Q factor of 4 with a series resistance of 4.8 Ω. When an optimization was done to get an inductance of 11 nH, the simulator provided an inductor model for which the series resistance was close to 10 ohms and the Q factor was around 3. A shift in the inductance value from 11 nH to 10.5 nH resulted only in a slight shift in the resonant frequency. Since the Q factor of the 10.5 nH inductor was higher, the gain and the noise figure improved. This is because, the Q of the input tank affects the gain and noise figure and it depends largely on the input inductor’s quality factors.

When the simulation was done with the 11 nH inductor whose Q factor was around 3, the gain was a little lesser than 11 dB and the noise figure was around 3.7 dB. Hence in order to get a better noise figure, the Q of the inductor should be high and the series resistance of the inductor should be small. It can be concluded that a small shift in
the resonant frequency caused by using an approximate value of inductance can be tolerated when compared to degrading noise figure and gain.

From the simulator it was observed that the maximum noise contributors were the parasitic resistances of the inductor \( L_g \), the drain current noise of M1 and noise due to the distributed gate resistance.

A LNA with a bias current of 8 mA was also designed in order to emphasize some of the trade-offs involved in the design. An increase in bias current from 5 mA to 8 mA resulted in the following:

(a) gain of the amplifier improved to 12.5 dB. An increase in bias current causes the transconductance of M1 to increase. Since gain is directly proportional to \( g_m \) from eq.2.9, the gain increases.

(b) noise figure reduced to 3.15 dB

(c) power dissipation increased to 25.5 mW

If such high power dissipation can be tolerated, then an increase in bias current would be favorable to achieve better gain and noise figure. But most of the portable systems require low power consumption. In order to obtain an improvement of 1.5 dB in gain and 0.15 dB in noise figure, an increase of 10 mW of power dissipation has to be
tolerated. A second stage can be added at the output of the LNA in order to increase the power gain. But addition of an extra gain stage will lead to additional power dissipation.

Another important consideration of the LNA is its stability, which is characterized in terms of the Stern stability factor expressed as follows [2]:

\[
K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{21}||S_{12}|}
\]  

(2.18)

where \( \Delta = S_{11}S_{22} - S_{12}S_{21} \). If \( K > 1 \) and \( \Delta < 1 \), the circuit is said to be unconditionally stable. The circuit does not start oscillating for any combination of load and source impedances. From simulations, the s parameter values for the designed LNA were obtained and substituted in Eq.2.18. It was found that the circuit satisfied the condition for stability.

The performance of RF circuits relies largely on the way in which the layout is done. Hence layout should be carefully done, by taking all the layout issues into consideration.
CHAPTER 3

High Performance LNA using Embedded Inductors

In this chapter, the feasibility of planar embedded inductors that improve the quality factor significantly is demonstrated. RF CMOS technology is extensively used for wireless applications owing to its low cost and possibility of integration with baseband circuits. Most RF applications, like the LNA presented in the previous chapter, require inductors in order to meet circuit specifications. In the first section, the various techniques used in the past to isolate the spiral from the substrate are discussed. The second section presents the novel fabrication technique called Integrated Materials Wafer (IMW) used to build embedded inductors [13].

The embedded inductors were modeled using ASITIC and the simulation results are presented in the third section. The section also discusses the results obtained through simulation. The last section presents the performance of the low noise amplifier, which uses embedded inductors instead of on-chip spirals built on the topmost metal layer.

It has been demonstrated at R.I.T by Dr. William Grande (Professor in Microelectronics Engineering Department) that such high Q embedded inductors can be fabricated using the IMW process.
3.1 Background

As explained in the first chapter, the on-chip spirals limit the performance of the Low Noise Amplifier. This is because the quality of integrated inductors plays a crucial role in the performance of RF ICs. Due to the losses in parasitics associated with vias and substrate coupling, the performance has been limited in spiral inductors that are typically fabricated in the top metal layer in CMOS technology. On-chip integration of inductors is of great interest because it overcomes the parasitic effects associated with going from chip to package if off-chip inductors are employed. However, the conductivity of silicon itself creates a set of parasitic losses that have hampered the progress in achieving integrated inductors with high Q.

The most widely used approach of building integrated inductors is to construct them on the top-most metal of a multilevel metallization process. This is done in order to keep these inductors far from the substrate to reduce losses due to substrate coupling. Other integration strategies demonstrated to date include selective etching of the silicon substrate [14] and electrostatic shielding of inductors using patterned conductive layers under the device [10]. But, all of these approaches have limitations because they either create undesirable topology or they only partially de-couple the inductor from the substrate.
In this chapter, a novel fabrication approach that can provide planar high Q embedded inductors is described and modeled. The design creates no topological artifacts and significantly reduces coupling losses to the substrate.

3.2 Integrated Materials Wafer

In silicon technology, the substrate is close to the spiral and fairly conductive. A straightforward approach to achieving high Q inductors is to use a highly resistive substrate and a dielectric layer for separation [4]. However, it would be preferable to remove the inductor far from the substrate such that high performance could be achieved even on conductive starting wafers. But existing schemes of integration do not permit such isolation of inductors from the substrate. A new approach called the Integrated Materials Wafer (IMW) is presented here which is an effective technique to isolate the inductor from the substrate.

In this new concept, the spiral inductor is separated from the substrate by a considerable distance through the use of a thick insulative layer embedded in the substrate. A good isolation from the substrate reduces the parallel plate capacitance that is formed between the spiral and substrate and will also minimize the energy coupled to the lossy substrate. A typical fabrication sequence is as shown in Fig.3.1.
Initially, a deep trench in the substrate is etched as shown in Fig. 3.1(a). The trench is then refilled with insulative material as depicted in Fig. 3.1(b). The next step is planarization so as to form an embedded insulative plug, as in Fig. 3.1(c). Finally, the inductor is built either on or into the plug, as shown in Fig. 3.1(d). Because the initial trench etch can be carried out to a nearly arbitrary depth the inductor can be widely
separated from the substrate. Various parasitics associated with on-chip spirals as explained in Chapter 1 are eliminated in these embedded inductors.

The expressions for the parasitics associated with spirals made on the top metal layer is repeated here for convenience. $R_s$ represents the series resistance and is given by

$$R_s = \frac{\rho l}{w\delta(1-e^{-\delta})} \tag{3.1}$$

where $\rho$ is the metal resistivity at dc, $l$ is the overall length of spiral, $w$ is the line width, $\delta$ is the metal skin depth and $t$ is the metal thickness.

The advantage of the IMW process is that the thickness of the metal used in the inductors can be increased and hence from Eq. 3.1 the series resistance can be reduced considerably. This in turn results in a considerable improvement in the quality factor of the inductor.

$C_{ox}$ is the capacitance between the spiral and the substrate and is written as:

$$C_{ox} = \frac{w l}{t_{ox}} \frac{C_{ox}}{t_{ox}} \tag{3.2}$$
where \( t_{ox} \) is the oxide thickness between spiral and substrate.

In the IMW process, the thickness of the insulative plug can in principle be extended to the thickness of the substrate and by doing so, the oxide capacitance \( C_{ox} \) from (3.2) is completely eliminated. Also, the parasitic resistance of the substrate accounts for the loss associated with current flowing into the substrate through \( C_{ox} \) and the flow of image currents induced in the substrate by the current in the spiral [5]. Both these currents become negligible in the case of IMW embedded inductors.

The cross section of the microcoil is as shown.

Fig. 3.2 Cross-section for the microcoil simulation
The parameters used for the microcoil simulation are as shown in the following table.

### Table 3.1. Parameters for Microcoil Simulation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bulk Substrate</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{wafer}} = \text{wafer thickness}$</td>
<td>525 $\mu$m</td>
<td>525 $\mu$m</td>
</tr>
<tr>
<td>$\rho_{\text{wafer}} = \text{wafer resistivity}$</td>
<td>0.001 $\Omega$-$\text{cm}$</td>
<td>1000 $\Omega$-$\text{cm}$</td>
</tr>
<tr>
<td>$\varepsilon_{\text{wafer}} = \text{wafer permittivity}$</td>
<td>11.8 $\varepsilon_0$</td>
<td>11.8 $\varepsilon_0$</td>
</tr>
<tr>
<td><strong>Mystery Layer</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{layer}} = \text{layer thickness}$</td>
<td>$h + 1$</td>
<td>525 $\mu$m</td>
</tr>
<tr>
<td>$\rho_{\text{layer}} = \text{layer resistivity}$</td>
<td>0.001 $\Omega$-$\text{cm}$</td>
<td>$\infty$ $\Omega$-$\text{cm}$</td>
</tr>
<tr>
<td>$\varepsilon_{\text{layer}} = \text{layer permittivity}$</td>
<td>3.9 $\varepsilon_0$</td>
<td>11.8 $\varepsilon_0$</td>
</tr>
<tr>
<td><strong>Metal</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$h = \text{metal thickness}$</td>
<td>1 $\mu$m</td>
<td>20 $\mu$m</td>
</tr>
<tr>
<td>$w = \text{metal width}$</td>
<td>1 $\mu$m</td>
<td>50 $\mu$m</td>
</tr>
<tr>
<td>$s = \text{coil separation}$</td>
<td>1 $\mu$m</td>
<td>20 $\mu$m</td>
</tr>
<tr>
<td>$\rho_{\text{metal}} = \text{metal resistivity}$</td>
<td>1.7e-6 $\Omega$-$\text{cm}$</td>
<td>1.7e-6 $\Omega$-$\text{cm}$</td>
</tr>
</tbody>
</table>
Simulations for the embedded inductors fabricated using the Integrated Material Wafer process were done using ASITIC. These simulations were done by varying the various parameters of the IMW process as shown in Table 3.1. The results are as shown in the graphs in Fig. 3.3, 3.4 and 3.5 respectively.
Fig. 3.4

Q Vs Metal Thickness

Frequency = 2 GHz

Fig. 3.5

Q Vs Inductance

Frequency = 2 GHz
Normally it is observed that the quality factor increases with increase in frequency and reduces at very high frequencies close to the self-resonant frequency. This reduction in Q is due to the combined effect of substrate loss and self-resonance [5]. At low frequencies, Q is given by $\omega Ls / Rs$. For typical on-chip inductors, the substrate loss factor causes 10 to 40% reduction from $\omega Ls / Rs$ at 1 to 2 GHz.

Fig.3.3 illustrates that for spiral inductors embedded in the substrate using the concept of IMW, the value of Q is considerably high even up to 8 or 10 GHz. This can be attributed to the good isolation of the spiral from the substrate by the thick insulative material. Generally a highly resistive substrate is preferred to improve the quality factor. But in this process there is no restriction on the substrate resistivity as it does not affect the quality factor.

The variation of Q with the increase in the metal thickness used for the spiral is illustrated in Fig. 3.4. Usually metal layers are strapped in order to increase the effective metal thickness. Since the process permits the use of thick metals of about 15 um, no strapping of metal layers is required to increase the effective thickness. Q factor of 18 can be achieved for a 3 nH inductor using 4 um thickness of metal. Simulation results indicate that increasing the metal thickness beyond 5 um does not yield any significant improvement in Q, though the process allows thickness up to 15 um.
Fig. 3.5 shows the variation of $Q$ with inductance. A $Q$ of 18 was achieved for an 8 nH inductor and a $Q$ of 15 for a 0.5 nH inductor. Hence high quality factors can be achieved for a wide range of inductance values.

The simulation results presented above are for a particular geometry of the spiral, that is, all simulations were done for a metal width of 10 um and spacing of 2 um. The main objective here was to evaluate the quality of embedded inductors, with respect to process parameters such as thickness of metal, substrate resistivity, thickness of insulative material and its resistivity.

Further improvement can be easily accomplished by optimizing the physical design and geometry of the inductors. For example, polygon spirals with more than four sides have higher $Q$ factor when compared to square spirals for the same area [15].

Fig. 3.6 shows an inductor that has been fabricated in the R.I.T. fabrication facility, using a special in-house process. Inductors with varying number of turns and metal thickness have been fabricated and are currently being tested.
It is important to note the substrate doping level does not impact the quality of the inductors. Hence these embedded inductors are not degraded by conductive substrates. Also the ability to use very thick metal for building the inductor enhances its $Q$ significantly.

3.4 LNA Performance with embedded inductors

The low noise amplifier presented in Chapter 2 was simulated using models for on-chip spirals built on the topmost metal layer. Here, the simulation results for the same
LNA using the model for embedded inductors is illustrated and the results are discussed. The performance of the LNA using embedded inductors is as follows.

<table>
<thead>
<tr>
<th>Table 3.2 Simulation results of LNA with Embedded Inductors</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>Noise Figure</td>
</tr>
<tr>
<td>S21 (Power gain)</td>
</tr>
<tr>
<td>S11</td>
</tr>
</tbody>
</table>

It was found that by using embedded inductor models in LNA design, the noise figure improved significantly and the gain also increased by 3 dB. The input impedance matching is also close to the range of interest (i.e. -10 to -14dB). S11 of -10dB implies a reflected power of 10% of incident power, which is sufficient for most applications [16]. Hence the overall performance of the LNA improves which can be attributed to the improved performance of the inductors used.

The geometry of the embedded inductors used in the simulation was similar to that of on-chip spirals. The various parasitics associated with the embedded inductors and the on-chip spirals were obtained as a pi model from ASITIC. The pi model from ASITIC is as shown in Fig.3.7:
The following table provides a comparison of the parasitics obtained from the pi model for embedded inductors and the on-chip spiral built on the topmost metal layer.

Table 3.3 Pi Model for gate and source inductors

<table>
<thead>
<tr>
<th></th>
<th>Gate Inductor</th>
<th>Source Inductor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Embedded Inductor</td>
<td>Inductor on top metal</td>
</tr>
<tr>
<td>Q</td>
<td>23.08</td>
<td>4.15</td>
</tr>
<tr>
<td>L (nH)</td>
<td>10.5</td>
<td>10.5</td>
</tr>
<tr>
<td>R (ohms)</td>
<td>4.98</td>
<td>4.87</td>
</tr>
<tr>
<td>Cs1,Cs2 (fF)</td>
<td>30.1, 20.3</td>
<td>141, 132</td>
</tr>
<tr>
<td>Rs1,Rs2 (ohms)</td>
<td>271, 447</td>
<td>308, 360</td>
</tr>
<tr>
<td>Self Resonant Frequency (GHz)</td>
<td>10.1</td>
<td>4.15</td>
</tr>
</tbody>
</table>
From the pi model it can be found that the parasitic capacitance and the parasitic resistances associated with embedded inductors has reduced considerably when compared to the spiral inductors built on the top metal layer. The pi model was obtained for a spot frequency of 2.4 GHz. The above values were obtained for the following geometry of the spirals.

Table 3.4 Dimensions of the spirals

<table>
<thead>
<tr>
<th></th>
<th>Gate Inductor</th>
<th>Source Inductor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Embedded Inductor</td>
<td>Inductor on top metal</td>
</tr>
<tr>
<td>Inner Diameter (um)</td>
<td>150</td>
<td>120</td>
</tr>
<tr>
<td>Width (um)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Spacing (um)</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Number of turns</td>
<td>6</td>
<td>6.5</td>
</tr>
</tbody>
</table>

For the sake of comparison, square spirals with similar geometries were built on the top metal layer and as embedded inductors. Further improvement in the performance can be accomplished by varying the geometry of the embedded inductors. Also, in the simulation of the embedded inductors, the capacitance due to the metal layer that connects the inner port of the spiral is not considered. This is because, the embedded
inductors were built as stand alone structures. However, the embedded inductors are compatible with the standard CMOS process. So, the metal 1 layer of the standard CMOS process can contact the inner port of the embedded spiral inductor using vias.

Another advantage of embedded inductors is the ability to connect to transistors in the substrate without the loss due to multiple vias. On the contrary, the spiral inductors built on the top metal layer will have to go through all the metal layers using multiple vias if they have to be connected to transistors in the substrate. Also, as a result of the special fabrication process that has been developed, loss due to coupling to the substrate is minimized. It is important to note the substrate doping level does not impact the quality of the inductors. Hence these embedded inductors are not degraded by conductive substrates. Also the ability to use very thick metal for building the inductor enhances its Q significantly.
CHAPTER 4

Effect of ESD Parasitics on the Fully Integrated LNA

The focus of this chapter is to analyze the parasitic effect of standard electrostatic discharge (ESD) structures on the performance of the LNA. The basic requirement of a ESD circuitry is to provide an efficient shunt path between bond pads to safely discharge the transients occurring as a result of an electrostatic discharge. The first section provides a brief introduction to the types of electrostatic discharge encountered by ICs. Some common types of standard ESD protection circuits are presented.

While the ESD protection circuitry is very important in the event of an electrostatic discharge, during the normal operation, the presence of an ESD circuitry at the input and output pad offers a certain amount of capacitance. This capacitance could result in being detrimental to the normal operation of the core circuits. For example, in the LNA, the capacitance due to the ESD circuitry at the input pad will degrade the noise figure, gain and input match. The performance of the LNA, which incorporates some standard protection circuits like MOS ESD protection and diode protection circuitry is then discussed. The importance of co-designing the LNA with the ESD circuitry is highlighted.
4.1 Introduction

Electrostatic discharge (ESD) is becoming an increasingly important issue in the semiconductor industry because of the associated high voltages. This is especially because of the small dimensions of the semiconductor devices. There are three main sources of electrostatic charging and discharging [17]. The first source is due to human handling (Human Body Model or HBM), the second is due to automated test and handling systems (Machine Model or MM) and the third is due to charging of IC due to highly charged surface or during transport (Charged Device Model or CDM).

HBM ESD event arises when a charged person (100 pF) comes in contact with a packaged device through a finger resistance of 1500 ohms which can result in a discharge event with a peak current of 1.3 Amps for 150 ns since the HBM charge level is 2KV. The Machine Model represents a capacitance of 200 pF and a lower series resistance than the HBM that results in higher peak currents of 3 or 4 Amps for 30 ns, at a stress level of 200 V. CDM results in fast transients of higher currents of around 8-10 Amps with a rise time of less than 500 ps [18].

ESD can result in breakdown and thermal damage in the gate oxide or in the junctions. Hence careful design of ESD protection circuit is very important. The design of this protection circuit has become a challenging task with the development of
advanced technologies that incorporate lightly doped drain (LDD) junctions and silicided diffusions, as well as very thin gate oxides [18].

Having seen the importance of the need for ESD protection circuits, another critical aspect to be considered for high speed RF and analog circuits is the parasitics associated with these ESD protection structures. To concurrently achieve high level of ESD protection level (of around 4KV) and considerably lower the parasitic effects offered by the protection circuitry is a very important and challenging task for RF ICs. In this chapter, a detailed analysis of the effects of the parasitics offered by the ESD structures on the performance of the LNA is presented. This is done in order to highlight the need to include the ESD parasitics in the design process of the LNA.

4.2 Types of ESD Protection Circuitry for RF CMOS ICs

4.2.1 Grounded Gate NMOS

In a traditional grounded gate NMOS ESD protection structure, the body, source and gate are shorted to ground. The drain is connected to an I/O pad. The cross section of the grounded gate NMOS is as shown in Fig.4.1. The working of this circuit at the occurrence of an ESD event is as follows [19]:
Since the gate and source are shorted, the device never turns on. At the occurrence of a positive ESD pulse at the I/O pad, the drain to body junction is reverse biased until breakdown. Hole current is generated which is routed to the ground through the body contact. There is a voltage build up at the body to source junction, which eventually turns on the parasitic lateral NPN transistor. Now the ESD transient is safely discharged through this low impedance shunt path. Usually the size of these NMOS transistors is large in order to achieve the desired level of protection.
Another requirement while using multi finger NMOS device is that the current distribution should be uniform. Otherwise only some fingers may take all the ESD current and other fingers will not share the stress, which will lead to early failure [20]. In non-silicided junctions, the ballast resistance can be implemented by spacing drain contacts to a poly edge distance, which would help in uniform current distribution to all fingers. But with silicided technology, the ballast action of N+ regions is eliminated which results in non-uniform current distribution to the device and has limited the performance [20].

4.2.2 Simulation Results and Analysis using GGNMOS ESD Protection

The fully integrated LNA design as explained in the previous chapter, was used to study the effect of ESD parasitics on its performance. The minimum total finger width for ESD PMOS and NMOS as specified by the TSMC 0.25um documents is 360 um. The unit finger width used is 15~30 um as per the specifications. A unit finger width of 30 um was chosen and 12 gate fingers were used.

Since the LNA is fully integrated with all the inductors being on-chip, the position of the ESD protection device is between the input pad and the gate inductor $L_g$. The protection circuitry consists of a grounded gate NMOS between the input pad and the ground.
The simulation results of the noise figure, gain and $s_{11}$ of the LNA using the grounded gate NMOS as ESD protection device at the input pad is summarized in Table 4.1. For the sake of comparison, the results of the LNA performance without ESD are also provided. It is observed that there is significant degradation in the performance of the LNA, which cannot be overlooked.

Table 4.1. Simulation Results with GGNMOS ESD protection

<table>
<thead>
<tr>
<th></th>
<th>Without ESD</th>
<th>With ESD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise Figure</td>
<td>3.3dB</td>
<td>5.19dB</td>
</tr>
<tr>
<td>Gain ($S_{21}$)</td>
<td>11dB</td>
<td>10.18dB</td>
</tr>
<tr>
<td>$s_{11}$</td>
<td>-13.3dB</td>
<td>-6.589dB</td>
</tr>
</tbody>
</table>

The parasitic capacitance due to the GGNMOS structure is around 750 fF. The total parasitic capacitance at the input is not only due to the ESD protection device but also due to the pad and the interconnect capacitance. For example, the minimum width of metal line connecting bond pad and the protection device is 20 um as specified in the TSMC 0.25 um technology file, which would contribute to significant interconnect capacitance.
If the protection level has to be increased, then the size of the grounded gate NMOS should also be increased. Apart from a larger size, certain layout/processing techniques such as wider drain-contact to poly-gate spacing have to be incorporated to sustain an acceptable level of ESD [21,22]. This would mean an increase in the parasitic capacitance, which will immensely degrade the performance and render the LNA useless and also consume a large amount of silicon area. Hence, an alternative protection circuit, which offers only low parasitic effects, has to be used.

4.2.3 Diode ESD Protection Circuit

For RF applications, the maximum loading capacitance for the input pad is only 200 fF for circuit operation at 2 GHz [23]. This capacitance value includes the bond pad and the ESD protection devices. In order to satisfy this condition, diodes are normally used for ESD protection in the input and output circuits [23]. The schematic diagram of a typical ESD protection design for the input/output pad with diodes and power-rail ESD clamp circuit is as shown in Fig. 4.2 [24].
During an ESD event, the dual diode protection circuitry will provide shunt paths around the sensitive internal circuitry [25]. When there is no ESD event (during normal operation), the diodes are all reverse biased. At the occurrence of an ESD event, for example, when there is a positive ESD pulse from VSS to input pad, the diode Dn1 will be forward biased and will form the discharge path.
When there is a positive pulse at the input pad with respect to VSS, then the discharge path would be through the forward biased diode Dp1 to VDD and then to VSS through the Vdd to Vss ESD clamp circuit. This clamp circuit between the power rails VDD and the ground plane VSS contribute to improved ESD protection and also support smaller ESD networks on the input pad [26]. If the o/p pad is grounded, then the ESD current will be conducted into the output pad through the forward biased diode Dn2.

In this type of ESD protection, the diodes operate in the forward biased condition in order to discharge ESD current. By operating diodes in the forward biased condition, much higher ESD levels can be sustained (because these diodes have high current carrying capability) and also relatively small device dimensions will suffice [24]. Smaller device dimensions will in turn contribute comparatively less input parasitic capacitance, which is an important criterion for ESD devices used in RF applications.

4.2.4 Simulation Results and Analysis using Diode ESD Protection

The simulation results for the integrated LNA with diode ESD protection is summarized in table 4.2. For the sake of comparison, the results of the LNA performance without ESD and the results obtained when GGNMOS ESD protection is used are also provided. Since the fully integrated LNA is used for analysis, the position of the diode ESD protection circuit is between the input pad and the gate inductor (as done for the GGNMOS case).
Table 4.2. Simulation Results with Dual Diode ESD protection

<table>
<thead>
<tr>
<th></th>
<th>With Diode ESD</th>
<th>Without ESD</th>
<th>With GGNMOS ESD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise Figure (dB)</td>
<td>3.86</td>
<td>3.3</td>
<td>5.19</td>
</tr>
<tr>
<td>Gain (S21) (dB)</td>
<td>10.54</td>
<td>11</td>
<td>10.18</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>-12.22</td>
<td>-13.3</td>
<td>-6.589</td>
</tr>
</tbody>
</table>

The above simulation result was obtained by keeping the area of each diode to be 100 microns. The total parasitic capacitance offered by the two diodes is around 0.2 pF as opposed to 0.7 pF from the grounded gate device. In order to achieve approximately the same level of protection level as that of a grounded gate NMOS device, much smaller device dimensions are needed when diodes are used which reduces the parasitic capacitance. It is clear from the above table that the performance of the LNA with diode ESD protection is better than that with grounded gate NMOS with respect to all performance metrics.
Also, stacking diodes in series can further reduce the input capacitance. By doing so, the total capacitance will be smaller than that of a single capacitor [24]. The following results were obtained from simulation by stacking two diodes between input pad and VSS (instead of using just Dn1) and two diodes between input pad and VDD (instead of using just Dp1).

Table 4.3. Simulation results for Stacked Diode ESD Protection

<table>
<thead>
<tr>
<th>Noise Figure (dB)</th>
<th>3.588</th>
</tr>
</thead>
<tbody>
<tr>
<td>S21 (dB)</td>
<td>10.77</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>-12.74</td>
</tr>
</tbody>
</table>

It can be seen from the above table that by using diodes in series improves noise figure, gain and S11. But while using the stacked configuration, N+ diodes cannot be used from pad to VSS [24]. This is because the N+ diodes share a common p-type substrate and are not isolated. But the P+ can be realized using separated N wells, which isolate these diodes. Stacking of diodes to reduce the total input capacitance can be achieved using polysilicon diodes [24]. Also another issue with the common substrate is that substrate noise from other circuits can couple into the input node and can cause deleterious effects. Use of polysilicon diodes, which are isolated from the common substrate by a thick field oxide help in avoiding substrate noise coupling.
4.3 ESD Parasitic Simulation Results

During the normal operation (that is when there is no ESD event), the ESD protection devices contribute to a significant amount of parasitic capacitance that can be detrimental to a circuit’s performance. So the ESD device can be modeled as a capacitor at the input. Simulations were done by varying the value of capacitance at the input and the noise figure, gain and input match of the LNA for these capacitance values are plotted in Fig 4.3 (a), 4.3(b) and 4.3(c) respectively. This was done in order to analyze the effect of varying the value of parasitic capacitance on the performance of the LNA. Since the LNA is fully integrated, the capacitor was placed between the input pad and the gate inductor. For the inductor, the on-chip inductor model obtained from ASITIC is used in order to get more realistic results.

Noise Figure Vs ESD Capacitance

![Graph: Noise Figure Vs ESD Capacitance](image)

Fig. 4.3 (a)
S21 Vs Capacitance

Fig. 4.3 (b)

S11 Vs Capacitance

Fig. 4.3 (c)
From the above results, it was confirmed that the capacitance offered by the grounded gate NMOS ESD protection device (described earlier) was around 750 fF. The values of noise figure, S11 and S21 obtained for the GGNMOS device coincided with that obtained for a capacitance value of 750 fF.

From the above graphs, it is evident that the values of S11 and S21 are reasonable till about 500 fF of parasitic capacitance from the ESD device. But the noise figure degrades by about 0.2 dB for every 100 fF increase in the parasitic ESD capacitance.

The desired range of S11 values is between –10 dB to –14 dB in order to get good power match. So an extra degree of freedom can be introduced by realizing a nonperfect input match. This will result in an improved performance of the LNA especially with respect to power gain. This can be explained as follows [16]. The available power of the source (Pav) is given by:

$$P_v = \frac{v_{eq}^2}{4R_{eq}} = \frac{v_s^2}{4R_s}$$  \hspace{1cm} (4.1)

where Rs is 50 Ω.
The output power of LNA ($P_{\text{out}}$) is given by:

$$P_{\text{out}} = i_{\text{out}}^2 R_{\text{load}}$$  \hspace{1cm} (4.2)

where $i_{\text{out}}$ is the current in the load and $R_{\text{load}}$ is the equivalent load resistance. $R_{\text{load}}$ is given by:

$$R_{\text{load}} = \frac{\omega_{\text{r}}^2 L_{\text{d}}^2}{R_s}$$  \hspace{1cm} (4.3)

where $R_s$ is the series resistance of the inductor $L_d$.

The output current is given by:

$$i_{\text{out}}^2 = i_{\text{in}}^2 \left( \frac{\omega_{\text{r}}}{\omega_0} \right)^2$$  \hspace{1cm} (4.4)

where

$$i_{\text{in}}^2 = \frac{4P_{\text{av}} R_{\text{eq}}}{\left( R_{\text{eq}} + R_{\text{in}} \right)^2}$$  \hspace{1cm} (4.5)
From (4.1), (4.2), (4.4) and (4.6) the power gain of the LNA can be written as follows:

\[
G_t = \frac{R_{eq}R_{\text{load}}}{(R_{eq} + R_{\text{in}})^2} \left( \frac{\omega_T}{\omega_o} \right)^2 \tag{4.6}
\]

From the above equation, it can be seen that the maximum power gain for a given value of operating frequency and unity gain frequency is obtained when the input impedance \(R_{\text{in}}\) is as low as possible. This implies that the power is used more efficiently though less power is absorbed at the input of the LNA.

From Fig. 4.3 (c) it can be seen that when the parasitic capacitance value of ESD device increases above 500 fF, the value of \(S_{11}\) is such that the impedance match is significantly affected. In order to obtain \(S_{11}\) value of about \(-10\) dB to \(-14\) dB, the value of the source inductance has to be altered. The procedure to calculate the value of source inductance in order to achieve the necessary power match is presented in the next section.
4.4 ESD Parasitic Analysis

4.4.1 Simulation Results with ESD capacitance

To simplify the analysis, the simulations were done using ideal inductors. The analysis is done for the case in which integrated inductors are used, that is, placement of the parasitic capacitance due to the ESD device is between the input and the gate inductor.

The simulation results for noise figure, power gain and S11 for varying parasitic capacitance on the LNA using ideal inductors is as shown in Fig. 4.4 (a), (b) and (c).

![Noise Figure Vs Capacitance](image)
S21 Vs Capacitance (using ideal inductors)

![Figure 4.4 (b)](image1)

S11 Vs Capacitance (using ideal inductors)

![Figure 4.4 (c)](image2)
As seen in the previous section, it is observed from the above graphs that with the increase in the capacitance value beyond 500 fF, the value of S11 drops below the range of interest. The value of source inductance is the only variable, which can be altered to get the required power match. The theoretical analysis and procedure is presented next.

### 4.4.2 Theoretical Analysis and Procedure to obtain input match

The input impedance of the LNA without considering the ESD device capacitance is given by:

\[
Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gst}} + \frac{g_m}{C_{gst}} L_s
\]  

(4.7)

Since ideal inductors are used, the parasitic series resistances of the inductors are ignored. In the case of a fully integrated LNA, the position of the parasitic ESD capacitance is between the input pad and the input inductor L_g. The placement of the ESD capacitance is illustrated in the schematic in Fig. 4.5.
With the introduction of the parasitic capacitance due to ESD, the equation for input impedance is altered. The term \((1/j\omega C_{\text{esd}})\) will now be in parallel with the expression given in Eq. 4.7 and will be of the form:

\[
Z_{\text{in}} = \left[ s(L_6 + L_s) + \frac{1}{sC_{\text{ps}}^1} + \frac{g_m}{sC_{\text{ps}}^1} L_s \right] \parallel \left[ \frac{1}{sC_{\text{esd}}} \right] \tag{4.8}
\]

The above equation results in a complex expression. In order to simplify the method of calculation, the value of 50 \(\Omega\) in parallel with \((1/j\omega C_{\text{esd}})\) is calculated. Instead of matching the real part of Eq.4.7 to 50 \(\Omega\), it is now matched to \((50/(1/j\omega C_{\text{esd}}))\). This results in the value of \(L_s\) required to achieve the required input match. The equation used is as shown:
Similarly, the imaginary part of Eq. 4.7 is equated to the corresponding imaginary part of \( \frac{50}{(1/j\omega C_{esd})} \). The resulting equation to find \( L_g \) is as follows:

\[
L_g = \frac{1}{\omega^2 C_{gs}} + \frac{C_{esd} * 50}{(1 + \omega^2 C_{esd}^2 * 50^2)} - L_s \tag{4.10}
\]

The value of \( L_s \) calculated from Eq. 4.9 is substituted in the Eq. 4.10 and the value of \( L_g \) to set the resonant frequency at 2.4GHz is calculated.

Also, if a blocking capacitor \( (C_b) \) is used at the input, then the above equations have to be altered in order to accommodate for the blocking capacitor. Usually the value of the blocking capacitor is comparatively high such that the reactance offered will be negligible. The equations for \( L_s \) and \( L_g \) when the blocking capacitor is included in the impedance matching is as shown:
The value of $L_s$ and $L_g$ for a particular value of ESD capacitance can be determined from the following graphs shown in Fig. 4.6, 4.7 and 4.8. The value of the source inductance for varying values of $C_{esd}$ for both with and without considering blocking capacitor is plotted.

$$L_s = \frac{(50*C_{gs} \cdot \omega^2 * C_b^2)}{g_m \left[ (\omega C_{esd} + \omega C_b)^2 + (\omega^2 C_{esd} 50C_b)^2 \right]}$$  \hspace{1cm} (4.11)$$

$$L_g = \frac{1}{\omega^2 C_{gs}} \left[ \frac{C_{esd} 50^2 \omega^2 C_b^2 + C_{esd} + C_b}{(\omega C_{esd} + \omega C_b)^2 + (\omega^2 C_{esd} 50C_b)^2} \right] - L_s \hspace{1cm} (4.12)$$

![Graph showing ESD Capacitance Vs Source Inductance $L_s$](image-url)
In order to achieve input match of 50 Ω, the value of the source inductance has to be decreased for increasing values of the ESD capacitance. The graph indicates the value of inductances required when the DC blocking capacitor is taken into account and the case when \( C_b \) is neglected. The shift in the required value of \( L_s \) is comparatively small when a large dc blocking capacitor is used. But when \( C_b \) value is reduced from 10 pF to 1 pF, the drop in the required \( L_s \) value is significant as illustrated in the graph.

The graph shown in Fig.4.7 can be used to determine a value of blocking capacitor to be used for a particular value of \( L_s \) and \( C_{esd} \). This graph plots the variation of \( L_s \) for a range of values of blocking capacitors.

![Ls v/s Cblock](image)

---

Fig.4.7
For low values of blocking capacitor, the value of $L_s$ becomes very small and hence not realizable. For larger values of blocking capacitor, the value of $L_s$ is realizable and is the preferred region of operation.

Similarly, the value of the gate inductance for varying values of $C_{esd}$ for both with and without considering blocking capacitor is plotted.

When the value of the blocking capacitor is large enough to be neglected, only a very small variation of the gate inductance value is required to achieve the desired resonant frequency. For the case where a 10 pF blocking capacitor is used, the $L_g$ varies only slightly with variation of the ESD capacitance as shown in the above graph.
When a dc blocking capacitor of 10 pF is used and is taken into account for calculation, the value of \( L_g \) required is almost the same when compared to the case where no blocking capacitor is used. By further reducing the blocking capacitor value to 1 pF, the value of \( L_g \) drops from that when \( C_b \) of 10 pF is used. But the required \( L_g \) increases with increase in ESD parasitic capacitance. So, it is advantageous to keep the value of the blocking capacitor comparatively large.

The LNA design has to be further optimized when the ESD circuitry is taken into account.
CHAPTER 5

Chip-Package Co-design and Effect of ESD Parasitics

In this chapter, the effect of ESD capacitance on the input match of the LNA is discussed with respect to the following two cases:

(a) gate inductor is realized completely offchip and
(b) gate inductor is realized as a combination of on-chip and off-chip inductors

First, the ESD parasitic analysis for the gate inductor placed off-chip is presented. A theoretical analysis and procedure to obtain input match is illustrated. In the second section, the ESD parasitic analysis for the case where the gate inductor is a combination of on-chip and off-chip inductors is presented. A theoretical analysis and procedure to obtain input match is presented for this case also.
5.1 ESD Parasitic Analysis in the case when off-chip Inductors are used

The input inductor is normally a large inductor and is achieved using off chip inductors such as bond wire or a combination of on-chip and off-chip inductors. Also, off-chip inductors provide a better quality factor when compared to on-chip spirals. Just as in the case of ESD capacitance analysis when on-chip inductors are used as illustrated in Chapter 4, an analysis is presented here for the influence of ESD capacitance when off-chip inductors are used. The ESD parasitic analysis for the case where a combination of on-chip and off-chip inductors are used is presented in the next section.

5.1.1 Simulation Results with ESD capacitance

Simulations were done by varying the value of capacitance at the input and the performance metrics of the LNA for these capacitance values are plotted in Fig. 5.1 (a), (b) and (c) respectively.
The simulations and analysis are performed using ideal inductors. From the above graphs it is evident that there is considerable degradation in the performance metrics with increase in the ESD capacitance value just as in the case when a fully integrated LNA is used (with on-chip inductors). However, in the case where on-chip inductors were used, the degradation in $S_{11}$ and $S_{21}$ was very gradual with increase in $C_{\text{esd}}$ whereas, in the case of off-chip inductors, the degradation is faster. As far as the noise figure is concerned, the increase is gradual till about 400 fF and then it increases steeply.
5.1.2 Theoretical Analysis and Procedure to obtain input match

The placement of the parasitic capacitance \( C_{\text{esd}} \) is between the gate of the input transistor and the input pad for the case when off chip inductor is used for \( L_g \). This is illustrated in Fig. 5.2.

For the above configuration, the equation for input impedance is as follows:

\[
Z_{in} = sL_g + \left[ \frac{1}{sC_{\text{esd}}} \right] \left[ \left( sL_s + \frac{1}{sC_{g1}} + \frac{g_m}{C_{g1}} L_s \right) \right] \tag{5.1}
\]
In the above equation, the impedance is matched to 50 Ω. In order to simplify the calculations, the matching condition is re-written as shown:

\[ Z_{in}(=50\Omega) + sL_g = \left[ \left( \frac{1}{sC_{esd}} \right) / \left( sL_s + \frac{1}{sC_{gs1}} + \frac{g_m}{C_{gs1}} L_s \right) \right] \]  

(5.2)

The real parts are then equated in order to calculate the value of \( L_s \) to achieve the required input impedance at resonance and for a particular value of ESD capacitance. The simplified equation for the real part of input impedance is as follows:

\[ \text{Re}[Z_{in}] = \frac{\omega^2 g_m C_{gs} L_s}{\left( \omega^2 g_m C_{esd} L_s \right)^2 + \left( \omega C_{gs} + \omega C_{esd} - \omega^2 C_{esd} C_{gs} L_s \right)^2} \]  

(5.3)

The imaginary parts of Eq.5.2 are then equated in order to find the value of \( L_g \) to set the resonant frequency at the input of the LNA for a particular value of ESD capacitance. The equation to find \( L_g \) is as follows:

\[ L_g = \frac{-\left[ \omega^2 C_{gs} L_s \left[ C_{gs} + 2C_{esd} - \omega^2 C_{esd} C_{gs} L_s \right] - C_{esd} \left[ 1 + \omega^2 g_m^2 L_s^2 \right] - C_{gs} \right]} {\left( \omega^2 g_m C_{esd} L_s \right)^2 + \left( \omega C_{gs} + \omega C_{esd} - \omega^2 C_{esd} C_{gs} L_s \right)^2} \]  

(5.4)
The value of $L_s$ got from Eq. 5.3 is used in Eq. 5.4 in order to calculate $L_g$.

The following graphs show the plot of variation of the real part of input impedance with variation in $L_s$ for certain range of ESD capacitances. These graphs are obtained from Eq. 5.3 and can be used to choose the value of $L_s$ for a particular value of ESD capacitance in order to achieve the required value of input impedance.

For the sake of convenience of scale, the graphs for $C_{esd}$ of 100 fF and 200 fF are plotted in Fig. 5.3 and the graph for other ESD values are plotted in Fig. 5.4.
It can be observed from Fig. 5.3 that with an increase in ESD capacitance, the value of $L_s$ has to be increased in order to achieve the input match. This is contrary to the case where the fully integrated LNA was used, wherein the source inductance had to be decreased for increasing values of ESD capacitances. For $C_{\text{esd}}$ of 100 fF and 200 fF, it is observed that the input impedance increases linearly with an increase in the value of $L_s$. But for $C_{\text{esd}}$ of 400 fF and higher, the input impedance increases initially with increase in $L_s$ but before reaching the required input impedance value of 50 $\Omega$, the impedance starts rolling off. It is observed that even though the source inductance is increased, the input impedance cannot be matched to 50 $\Omega$. 
The explanation for such the roll off in input impedance with increasing \( L_s \) is presented with the aid of input impedance equation (Eq. 5.3) repeated here for convenience.

\[
\Re[Z_{in}] = \frac{\omega^2 g_m C_{gs} L_s}{\left(\omega^2 g_m C_{esd} L_s\right)^2 + \left(\omega C_{gs} + \omega C_{esd} - \omega^3 C_{esd} C_{gs} L_s\right)^2}
\]  

\( D_1 \)  \( D_2 \)

From the above equation, it is evident that for a particular value of \( C_{esd} \) and increasing values of \( L_s \), the numerator increases, the term \( D_1 \) increases and the term \( D_2 \) decreases. Initially, the term \( D_2 \) is more significant when compared to \( D_1 \). So, with increasing values of \( L_s \), the denominator decreases effectively and the numerator increases and hence the input impedance increases.

Beyond a certain value of \( L_s \), the term \( D_1 \) that increases with \( L_s \) starts dominating and hence the input impedance starts decreasing. Also, with an increasing value of ESD protection, both \( D_1 \) and \( D_2 \) increase. Hence the maximum achievable input impedance value decreases with increase in \( C_{esd} \). This is illustrated in Fig. 5.4 wherein the curve shifts downward for increasing value of \( C_{esd} \). As a result beyond a certain value of \( C_{esd} \), the input impedance of 50 Ω cannot be obtained even by increasing the value of \( L_s \).
The variation of $L_g$ with the variation of $L_s$ for different values of $C_{esd}$ is plotted in Fig. 5.5 and Fig. 5.6.

**Fig. 5.5**

**Fig. 5.6**
From the graphs, it can be observed that for smaller values of $C_{esd}$, the variation in the value of $L_g$ with $L_s$ is not large. But with increase in $C_{esd}$, $L_g$ also increases with $L_s$. Also, for larger $C_{esd}$, the value of $L_g$ required decreases for a particular value of $L_s$. From the above graphs, the value of $L_g$ required for tuning for a particular combination of $L_s$ and $C_{esd}$ can be determined. It is observed from Fig. 5.6 that the maximum value of $C_{esd}$ for which the input match can be achieved ($S11=-10$ dB or lesser) is around 400 fF.

5.2 ESD Parasitic Analysis for combination of on-chip and off-chip inductors

The gate-inductor is sometimes achieved as a combination of on-chip and off-chip inductors. This is because, the gate inductors in many cases turns out to be fairly large. As the inductance increases, the quality factor of the on-chip spiral will decrease. As a result using an off-chip inductor to achieve a certain portion of the inductance would be a better choice. Then, the position of the parasitic ESD capacitance would be between the two inductors.
5.2.1 Theoretical Analysis and Procedure to obtain input match

The placement of the parasitic capacitance \( C_{esd} \) is between the off-chip inductor and the on-chip inductor as illustrated in Fig. 5.7.

For the above configuration, the equation for input impedance is as follows:

\[
Z_{in} = sL_{g1} + \left[ \frac{1}{sC_{esd}} \right] \left\{ sL_{g2} + sL_s + \frac{1}{sC_{gs1}} + \frac{g_m}{C_{gs1}} L_s \right\}
\]  

(5.6)

In the above equation, the impedance is matched to 50Ω. In order to simplify the calculations, the matching condition is re-written as shown:
\[(Z_{in} + sL_g) // \left( \frac{1}{sC_{esd}} \right) = \left( sL_{g2} + sL_s + \frac{1}{sC_{gs1}} + \frac{g_m}{C_{gs1}} \right) \] \quad (5.7)

The above equation is simplified and the real parts on the left hand side and the right hand side are then equated in order to calculate the value of \(L_s\), to achieve the required input impedance at resonance and for a particular value of ESD capacitance. The simplified equation for \(L_s\) is as follows:

\[L_s = \frac{(50*C_{gs})}{g_m((\omega^2C_{esd}^250^2) + (\omega^2C_{esd}L_{g1} - 1)^2)} \quad (5.8)\]

In the above equation, the value of the off-chip inductor \(L_{g1}\) is set to a constant value and the value of \(L_s\) is then calculated. The imaginary parts on the left hand side of Eq. 5.7 is then equated to the conjugate of that on the right hand side in order to arrive at an expression to calculate the value of \(L_{g2}\). The equation to calculate \(L_{g2}\) is as shown:

\[L_{g2} = \frac{1}{\omega^2C_{gs}}L_s - \frac{(\omega^2C_{esd}L_{g1}^2 - L_{g1} + 50^2C_{esd})}{((\omega^2C_{esd}^250^2) + (\omega^2C_{esd}L_{g1} - 1)^2)} \quad (5.9)\]

The value of \(L_s\) got from Eq. 5.8 and the constant value of \(L_{g1}\) are substituted in Eq. 5.9 in order to obtain the value of the on-chip inductor \(L_{g2}\).
When $L_{g1}$ is zero, the above case will be similar to the on-chip case and the ESD parasitic analysis which was presented in Chapter 4 will hold good. When $L_{g2}$ is zero, the above case will be similar to the off-chip case and the ESD parasitic analysis presented in the previous section will hold. The following graph shows the variation of source inductance with increasing parasitic ESD capacitance.

![Graph showing the variation of source inductance with ESD capacitance](image)

It was observed that as the value of off-chip inductor increased, the value of $L_s$ required for smaller values of ESD capacitances also increases immensely. But beyond a certain value of ESD capacitance, the value of $L_s$ reduces for high values of off-chip inductor. Hence, depending on the achievable values of on-chip and off-chip inductors, the respective combination of $L_{g1}$ and $L_{g2}$ values can be chosen. From the above graph, the value of $L_s$ for a particular value of $C_{esd}$ and $L_{g1}$ can be found.
The value of $L_{g2}$ can be found from the following graph, which shows the variation of $L_{g2}$ with ESD capacitance for particular values of $L_{g1}$.

![Graph showing $L_{g2}$ vs $C_{esd}$](image)

For certain values of ESD capacitance and off-chip inductors, the value of the on-chip inductor is calculated to be a negative value. The region where $L_{g2}$ becomes negative should be avoided. It is found from simulations that for such combinations of $C_{esd}$ and $L_{g1}$, the impedance match can be obtained by using only off-chip inductors or a different value of $L_s$ for which an on-chip inductor can be achieved.

Also it is observed that for higher values of $C_{esd}$ (greater than around 300 fF), when the value of the off-chip inductor increases, the values of on-chip inductor required to achieve impedance match also increases and the source inductance value reduces. So it
is advisable to keep the off-chip value fairly small in order to reduce the value of on-chip inductor. This is especially because if the on-chip inductors were to be achieved using spirals on the topmost metal layer then, their quality factor would decrease significantly for high inductance values.
CHAPTER 6

Conclusion

This thesis basically focussed on optimizing the design of a low noise amplifier with respect to the parasitics associated with the on-chip spiral inductors and also the parasitic capacitance due to ESD protection circuitry. First, the design of a fully integrated CMOS LNA was presented wherein all possible parasitics have been taken into account. It was found that the parasitics associated with the on-chip spiral inductors built on the top most metal layer were non-negligible. Hence a low noise amplifier design which does not account for these parasitics would result in a significant degradation in performance. Also, the performance of this LNA is found to depend to a large extent on the quality of inductors used. So, the inductors were carefully modeled using ASITIC and the geometry that provided the best performance in terms of quality factor and self-resonant frequency was chosen.

In the first iteration of the design process, the values of the inductors were determined and thesis inductors were modeled. From the pi model of the inductors, the associated parasitics were determined and the another iteration of the design procedure was necessary to account for all the parasitics. Hence the design was optimized with respect to the parasitics associated with the on-chip spiral inductors.
Since the performance of the LNA significantly depends on the performance of the inductors used, high quality factor inductor modeling and fabrication method was also presented in this work. Existing schemes of integration do not permit isolation of inductors from the substrate. As a part of this thesis, a new approach called integrated materials wafer (IMW) was presented. Using the IMW technique, inductors could be embedded in the substrate and isolated from the substrate using an insulative material. Simulation results of the LNA using embedded inductor models showed improved performance.

The thesis also has presented a thorough analysis of the effect of the parasitic capacitance from the ESD protection circuitry on the performance of the LNA. The parasitic analysis has been presented for the following three cases:

(i) when the gate inductor is realized completely on-chip
(ii) when the gate inductor is realized completely off-chip
(iii) when the gate inductor is realized as a combination of on-chip and off-chip inductors

A procedure and methodology to obtain input match by varying the source and gate inductors was also discussed for all the above cases.
Future Work

In this work, the inductors were restricted to a square spiral. Using other geometries like octagonal or even circular spirals could further optimize the performance of the inductors for both embedded structures and inductor structures built on the top metal layer. Also, the embedded inductors were modeled without considering the metal layer and vias which will be used to connect to the inner port of the spiral. This was because these inductors were built as stand alone structures. Including the vias and metal layer connecting the inner port can enhance the accuracy of the embedded inductor models. The embedded inductors are currently being tested. Further, these embedded inductors can be integrated into the CMOS process and tested using some test structures. This would enable the comparison of the simulation results with measured data.
References


[16] Paul Leroux, Johan Janssens, and Michiel Steyaert, “A 0.8-dB NF ESD-Protected 9-mW CMOS LNA Operating at 1.23 GHz”, IEEE Journal of Solid State Circuits, Vol. 37, No. 6, June 2002


Appendix A

Process Parameters

// **********************************************
simulator lang=spectre
// *
TSMC RF SPICE MODEL *
// **********************************************
// PROCESS: 0.25um Mixed-Signal SALICIDE(1P5M+, 2.5V/3.3V)
// MODEL: BSIM3 (V3.2)
// DOC. NO.: T-025-MM-SP-005
// VERSION: 1.6
// DATE: Nov. 7, 2001
// SPECTRE VERSION: V4.4.5

//

________________________________________________________________________
****

IN THIS MODEL LIB CONTAINS:

1. LIB RF_MACRO
   (RF MOS, MIM capacitor, spiral inductor, MOS varactor sub-circuit)

2. LIB TT_RFMOS
   (Typical model for 2.5V/3.3V nominal Vt N/P devices)

3. LIB FF_RFMOS
   (Fast-Fast corner model for 2.5V/3.3V nominal Vt N/P devices)

4. LIB SS_RFMOS
   (Slow-Slow corner model for 2.5V/3.3V nominal Vt N/P devices)

________________________________________________________________________
****

1) To use these models directly by programming in this style:

   include "lib_path/lib_name" section=tt_rfmos
   include "lib_path/lib_name" section=rf_macro
//
// EX1: include `/home/user/tsmc/LOGIC/rf025.1` section=rf_macro
//     include `/home/user/tsmc/LOGIC/rf025.1` section=tt_rfmos
//     for all typical Devices
//
// EX2: include `/home/user/tsmc/LOGIC/rf025.1` section=rf_macro
//     include `/home/user/tsmc/LOGIC/rf025.1` section=ff_rfmos
//     for all Fast-Fast corner Devices
//
// EX3: include `/home/user/tsmc/LOGIC/rf025.1` section=rf_macro
//     include `/home/user/tsmc/LOGIC/rf025.1` section=ss_rfmos
//     for all Slow-Slow corner Devices
//
// 2)Please note that AS/AD and PS/PD must be set to zero to result in correct
//    output impedance.
//
library MyLib

section tt_rfmos
parameters nmos_rgfac=1.0
parameters pmos_rgfac=1.0
parameters nmos_rsubfac=1.0
parameters pmos_rsubfac=1.0
parameters nmos_uefffac=1.0
parameters pmos_uefffac=1.0
parameters nmos_vthfac=1.0
parameters pmos_vthfac=1.0
parameters nmos_toxfac=1.0
parameters pmos_toxfac=1.0
parameters nmos_dlfac=1.0
parameters pmos_dlfac=1.0
parameters nmos_dwfac=1.0
parameters pmos_dwfac=1.0
parameters nmos_rdswfac=1.0
parameters pmos_rdswfac=1.0
parameters nmos_k1fac=1.0
parameters pmos_k1fac=1.0
parameters nmos_cgdfac=1.0
parameters pmos_cgdfac=1.0
parameters ndio_cjfac=1.0
parameters pdio_cjfac=1.0
section rf_macro
ahdl_include "rf_ahdl.va"

//
//************************************************************************
//************************
//
//\ 1) MOS MODEL (w=10um):
//
// 1. 2.5V MOS DEVICE MODELS
//
//
// Subckt name | NF  | L (um) | Wf (um)
//
//   nmos_rfw10 | 8   | 0.24  | 10.0  (with twin well)
//
//   pmos_rfw10 | 8   | 0.24  | 10.0  (with twin well)
//
//   nmos_rftrw10 | 8   | 0.24  | 10.0  (with triple well)
//
// **NF: Finger number

subckt nmos_rfw10 ( nd ng ns nb )
parameters lr=0.24u nr=16

mcore ( n1 n2 n3 n4 ) nch_rfw10 w=10u l=lr m=nr ad=0.0 as=0.0 pd=0.0 ps=0.0 rd ( nd n1 ) resistor r=0.886 + 0.084 / ((lr + 30n - 2 * 20n) * 1e6) - 0.003 * (nr + / 2.0) / ((lr + 30n - 2 * 20n) * 1e6)
rg ( ng n2 ) resistor r=-( - 6.55 + 2.39 / ((lr + 30n) * 1e6) + 35.69 / (nr * (lr + + 30n) * 1.0e6)) * nmos_rgfac
rs ( ns n3 ) resistor r= - 0.433 + 0.654 / ((lr + 30n - 2 * 20n) * 1e6) - 0.027 + * (nr / 2.0 + 1.0) / ((lr + 30n - 2 * 20n) * 1e6)
rsubl ( n6 n4 ) resistor r=((238.53 - 1476.81) / nr + 42.39 * ((lr + 30n) * 1.0e6) + / nr) * nmos_rsubfac
rsub2 ( n5 n4 ) resistor r=((238.53 - 1476.81) / nr + 42.39 * ((lr + 30n) * 1.0e6) + / nr) * nmos_rsubfac
rsub3 ( n4 nb ) resistor r=(168.65 + 2898.65 / nr - 933.65 * ((lr + 30n) * 1.0e6) + / nr) * nmos_rsubfac

resistor r=(238.53 - 1476.81 / nr + 42.39 * ((lr + 30n) * 1.0e6) + / nr) * nmos_rsubfac

ends nmos_rfw10

subckt pmos_rfw10 ( nd ng ns nb )
parameters lr=0.24u nr=16

mcore ( n1 n2 n3 n4 ) pch_rfw10 w=10u l=lr m=nr ad=0.0 as=0.0 pd=0.0 ps=0.0
rd ( nd n1 ) resistor r=0.937 + 0.061 / ((lr + 30n - 2 * 52n) * 1e6) - 0.002 * (nr + / 2) / ((lr + 30n - 2 * 52n) * 1e6)
rg ( ng n2 ) resistor r=(0.5 + 116.66 / nr + 24.92 / (nr * (lr + 30n) * 1e6)) + pmos_rgfac
rs ( ns n3 ) resistor r= - 0.187 + 0.414 / ((lr + 30n - 2 * 52n) * 1e6) - 0.017 + * (nr / 2 + 1) / ((lr + 30n - 2 * 52n) * 1e6)
rs ( n6 n4 ) resistor r=85.09 + 372.02 / nr + 836.28 * ((lr + 30n) * 1e6) / + nr) * nmos_rsubfac
rs ( n5 n4 ) resistor r=(85.09 + 372.02 / nr + 836.28 * ((lr + 30n) * 1e6) / + nr) * nmos_rsubfac
rs ( n4 nb ) resistor r=(82.69 + 372.02 / nr + 836.28 * ((lr + 30n) * 1e6) / + nr) * nmos_rsubfac

ends pmos_rfw10

subckt spiral_turn ( p1 p2 )
parameters nr=2.5

ls ( p1 n2 ) inductor l=(0.3169 * nr * nr - 0.3719 * nr + 1.1343) * 1.0e-9
rs ( n2 p2 ) resistor r=1.512 * nr - 0.5766

ends spiral_turn
cs ( p1 p2 ) capacitor c=(4.115 * nr + 6.4045) * 1.0e-15
cox1 ( p1 n1 ) capacitor c=(10.91 * nr + 96.365) * 1.0e-15
cox2 ( p2 n3 ) capacitor c=(10.71 * nr + 106.79) * 1.0e-15
csub1 ( n1 0 ) capacitor c=(12.051 * nr + 7.2865) * 1.0e-15
csub2 ( n3 0 ) capacitor c=(12.051 * nr + 7.2865) * 1.0e-15
rs sub1 ( n1 0 ) resistor r=-18.83 * nr + 489.02
rs sub2 ( n3 0 ) resistor r=-18.83 * nr + 489.02
rdummy1 ( p1 0 ) resistor r=1e+12
rdummy2 ( p2 0 ) resistor r=1e+12
ends spiral_turn

// **************************************************************************
// N MOS DEVICES IN TWIN-WELL MODEL
// **************************************************************************
model nch_rfw10 bsim3v3 type=n minr=le-60 lmin=2.4e-07 lmax=5e-07 wmin=1.2e-06 wmax=1.01e-04
+ tnom=25 xl=3e-08 * nmos_dlfac noimod=1 ef=0.9524 af=0.9124 kf=5.550e-28 xw=0 *
+ nmos_dwfac version=3.2 tox=5.4e-9 * nmos_toxfac xj=1e-07 nch=1.63e+17 lln=1 lwn=1

+ wln=1 wwn=1 lint=2e-08 wint=2e-08 mobmod=1 binunit=2 dwg=0 dwb=0
vth0=0.5486611
+ * nmos_vthfac lvth0=-2.469959e-09 wvth0=7.938721e-08 pvth0=2.301899e-14
k1=0.403429
+ * nmos_k1fac lk1=1.725285e-08 wk1=-3.072359e-08 pk1=-3.872562e-16
k2=0.03135336
+ lk2=1.238293e-08 wk2=1.859888e-09 pk2=2.891545e-15 k3=0 dvt0=0 dvt1=0

dvt2=0
+ dvt0w=0 dvt1w=0 dvt2w=0 nlx=0 w0=0 k3b=0 vsat=103237.4 lvsat=-0.001586308
wvth=0.003755342
+ * nmos_vthfac lvth0=-9.466342e-10 wvth0=9.929151e-17 wua=8.099974e-17
puv=8.460469e-23
+ ub=1.680473e-18 lub=1.748276e-25 pub=-8.461518e-26
uc=4.822789e-11
+ luc=8.460881e-18 wuc=-2.012348e-17 puc=7.039261e-25 rdsw=187 * nmos_rdswfac
prwb=0
+ prwg=0 wr=1 ul0=0.0300978 * nmos_uelfac lu0=-4.590353e-10 wu0=5.920663e-10
pu0=-6.285965e-16
+ a0=0.260679 la0=1.236537e-07 wa0=4.002671e-07 pa0=-2.250091e-13 keta=0.01653278
+ lketa=-1.14756e-14 a1=0 a2=0.552563
la2=2.145243e-08
+ wa2=9.555396e-08 pa2=-2.693616e-14 ags=0.02769231 lags=-8.669232e-09 b0=0 b1=0
+ voff=-0.1309933 lvoff=-7.23485e-09 wvoff=8.131762e-09 pvoff=5.155098e-15
+ nfactor=1
+ cit=0.001 cdsc=0 cdscb=0 cdscd=0 eta0=-0.0009629505 leta0=1.293616e-09 weta0=-2.950198e-10
+ peta0=-2.1329999e-16 etab=0.0007282808 letab=-6.018576e-10 wetab=-6.151851e-08
+ petab=3.347511e-16 dsub=0 pclm=1.549809 lpclm=1.89116e-07 wpclm=3.036521e-07
+ ppclm=4.142599e-14 + pdiblc1=1e-05 pdiblc2=-0.009022731 lpdiblc2=1.357523e-09 wpdiblc2=2.474329e-09
+ ppdiblc2=-5.690957e-16 pddibcb=0.01 drout=0 pscbe1=3.595446e+08
+ pscbe1=6.874803 + wpscbe1=-5.550639 ppscbe1=4.818866e-06 pscbe2=1e-06 pvag=0 delta=0.01
+ alpha=18.2625 beta0=20.54463 kt1=-0.3197329 lkt1=2.470867e-08 wkt1=6.111851e-08
+ pkt1=-2.481497e-14 kt2=-0.03581266 lkt2=5.001353e-10 pkt2=-5.655404e-09
+ pkt2=3.221474e-15 + at=3.5000 ute=-1.794323 lute=1.092588e-07 wute=2.077792e-07 pute=-9.524377e-14
+ ual=9.999999e-11 ub1=0 uc1=-6.039701e-11 luc1=1.151504e-17 wuc1=1.68016e-16
+ puc1=-4.588739e-23 + kt1l=0 prl=0 cj=cjn_rfw10 mj=0.4708251 pb=0.9597901 cjsw=cjswn_rfw10
+ mjsw=0.379613 + pbsw=0.9597901 cjswg=cjgaten_rfw10 mjswg=0.379613 pbswg=0.9597901
+ cta=0.007391288 + ctp=0.0009081566 pta=0.001293296 ptp=0.001178533 js=2e-06 jsw=5e-10
+ cgdo=cgon_rfw10 + cgso=cgon_rfw10 capmod=0 nqsmod=0 xpart=0 cf=0 tle=1 tlevc=1 xti=3 n=1
+ hdir=hdifn_rfw10 + ldif=1.2e-07 rsh=4.5 rs=0 rd=0
+
// //**********************************************
// // PMOS DEVICES IN TWIN-WELL MODEL            *
// //**********************************************
model pch_rfw10 bsim3v3 type=p minr=1e-60 lmin=2.4e-07 lmax=5e-07 wmin=1.2e-06
+ wmax=1.01e-4 + tnom=25 version=3.2 noimod=1 ef=1.2052 af=1.3 kf=2.55e-29 tox=5.4e-9 *
+ pmos_toxfac + xj=1e-07 nch=4.15e+17 lln=1 lwn=1 wln=1 wwn=1 lint=5.2e-08 l=0 lw=0 lwl=0
+ wint=2.5e-08 + w=0 wwl=0 mobmod=1 binunit=2 xl=3e-08 * pmos_dlfac xw=0 * pmos_dwfac
+ dwg=0
+ dwb=0 vth0= - 0.6146093 * pmos_vthfac 1vth0=1.225977e-08 wvth0=1.985369e-08
+ pvt0=-6.06429e-15
+ k1=0.7276184 * pmos_k1fac lk1=-2.716388e-08 wk1=-1.395578e-07 pk1=2.130584e-14
+ k2=0.01029779 lk2=-3.485872e-09 wk2=3.685143e-08 pk2=-5.604526e-15 k3=0
dv0=0
+ dv1=0 dv2=0 dvtw0=0 dvtw=0 nlx=0 w0=0 k3b=0 vsat=173192.3 lvsat=-
0.001359923
+ ua=8.541846e-11 lua=9.733665e-17 wua=1.519905e-16 pua=1.02419e-23
ub=8.476358e-19
+ lub=1.046959e-25 wub=-2.65695e-25 pub=-8.967035e-34 uc=-1.847504e-11
+ wu=5.906381e-18 puc=-1.304751e-23 rdsw=1000 * pmos_rdswfac prwb=0 prwg=0
wr=1
+ u0=0.007833129 * pmos_uefffac lu0=1.842939e-10 wu0=5.259558e-10 pu0=-
5.688812e-17
+ a0=0.5132501 la0=3.381841e-08 wa0=9.134673e-08 pa0=1.130424e-14 keta=-
0.03102319
+ lketa=5.166434e-09 wketa=7.930221e-09 pketa=-1.746611e-15 a1=0 a2=0.8911977
la2=3.749746e-09
+ wa2=1.277979e-08 pa2=-5.44419e-15 ags=0.008331296 wags=7.108682e-10
+ pags=-7.073146e-15 b0=0 b1=0 voiff=-0.1054648 lviff=-2.424728e-09 wvoff=-
1.799239e-08
+ pvoff=6.692681e-15 nfactor=1 cit=-0.0008942893 lcit=-5.69356e-11 wcit=-1.154705e-
09
+ pcit=2.26256e-16 cdsc=0 cdscb=0 cdscd=0 eta0=-0.002334355 leta0=-1.083206e-09
weta0=1.200188e-10
+ peta0=-3.872342e-17 etab=0.001142361 letab=-5.718457e-10 wetab=1.887219e-10
petab=-8.039552e-17
+ dsub=0 pclm=1.04323 lpclm=4.169387e-08 wpclm=2.347217e-07 ppclm=-3.059635e-
14
+ pdib1c1=1e-05 pdiblc2=0.005 pdiblcb=0.01 drout=0 pscbel=4.512553e+08
lpscbe1=2.275782
+ wpscbe1=8.813572 ppscbe1=-5.524364e-06 pscbe2=1e-06 pvag=0 delta=0.01
alpha0=0
+ alphal=0.46878 beta0=19.43759 kt1=-0.2149899 lkt1=-9.097961e-09 wkt1=-
1.270587e-08
+ pkt1=2.643099e-15 kt2=-0.03321986 lkt2=2.863286e-09 wkt2=8.506876e-09 pkt2=-
3.206299e-15
+ at=10000 ute=-0.8437479 lute=-9.539935e-09 wute=2.728344e-08 put=1.441154e-14
+ ual=4.15469e-10 lua1=-1.343898e-16 wua1=-3.627893e-16 pua1=1.545482e-22
ub1=0
+ ucl=2.159457e-11 luct=-1.006969e-17 wuc1=-4.128744e-17 puc1=2.288286e-23
kt11=0
+ prt=0 hdif=hdifp_rfw10 ldif=1.2e-07 rsh=3.5 rs=0 rd=0 cj=cjprfw10 mj=0.4746122
+ pb=0.9522272 cjsw=cjswp_rfw10 mjsw=0.3296904 pbsw=0.9522272
cjswg=cjgatep_rfw10
+ mjswg=0.3296904 pbswg=0.9522272 cta=0.0008154354 ctp=0.0006079875
pta=0.00140666
+ ptp=0.001610754 cgdo=cgop_rfw10 cgso=cgop_rfw10 capmod=0 nqsmod=0 xti=3
n=1 xpart=0
+ cf=0 tlev=1 tlevc=1 js=7e-07 jsw=1.4e-10
//
Appendix B

Technology Files

For Embedded Inductor:

<chip>
chipx=512
chipy=512
fftx=256
ffty=256
TechFile=esimt8.tek
TechPath=. 
freq=0.1

<layer>0
rho=10
T=425
eps=11.8

<layer>1
rho=1000000
T=100
eps=4

<metal>0
layer=1
rsh=2.125
T=8
d=92
name=metal0
color=blue

For Inductor on Top-Metal Layer in TSMC .25um Technology:

<chip>
chipx=512
chipy=512
fftx=256
ffty=256
TechFile=tsmc_mod.tek
TechPath=. 

freq=0.1

<layer>0
rho=9
t=300
eps=11.9

<layer>1
rho=1e10
t=9.12
eps=4

<metal>0
layer=1
rsh=76
t=.57
d=1.145
smin=.32
wmin=.32
name=METAL1
color=blue

<via>0
top=1
bottom=0
r=4
width=.36
space=.36
overplot1=.12
overplot2=.12
name=VIA12
color=white

<metal>1
layer=1
rsh=76
t=.57
d=2.715
smin=.4
wmin=.4
name=METAL2
color=yellow
<via>1
top=2
bottom=1
r=4
width=.36
space=.36
overplot1=.12
overplot2=.12
name=VIA23
color=white

<metal>2
layer=1
rsh=76
t=.57
d=4.28
smin=.4
wmin=.4
name=METAL3
color=yellow

<via>2
top=3
bottom=2
r=4
width=.36
space=.36
overplot1=.12
overplot2=.12
name=VIA34
color=gray

<metal>3
layer=1
rsh=76
t=.57
d=5.855
smin=.4
wmin=.4
name=METAL4
color=yellow

<via>3
top=4
bottom=3
r=4
width=.36
space=.36
overplot1=.12
overplot2=.12
name=VIA45
color=purple

<metal>4
layer=1
rsh=27.33
t=0.99
d=7.4250
smin=.46
wmin=.44
name=METAL5
color=green
Appendix C
LNA Layout

Gate Inductor

Drain Inductor

Source Inductor

Cascode Topology