Design of a 14-bit fully differential discrete time delta-sigma modulator

Sumit Kumar Nathany

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Design of a
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by
Sumit Kumar Nathany
A Thesis submitted in Partial Fulfillment of the
Requirements for the Degree of
MASTERS OF SCIENCE in ELECTRICAL ENGINEERING
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ROCHESTER, NEW YORK
NOVEMBER 2006
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ACKNOWLEDGEMENT

The path to success through the deep sea of knowledge is quite an uphill task. But this success is the epitome of hard work, perseverance, purpose of goal and most of all encouraging guidance. The implementation of my purpose to come out successfully was only due to the strong, powerful enthusiastic forces that were put together to achieve my goal. So with gratitude I acknowledge all the guiding hands that helped me move towards my watch word “Success”. I have worked on this thesis for more than a year. It is impossible to mention all the names here but I would definitely take this opportunity to thank the following people who have guided, encouraged, motivated and helped me through the different phases of my thesis.

I would like to thank my thesis advisor, Dr. Syed S. Islam, for his guidance, encouragement, support and confidence in me through the course of my studies at RIT. Without his motivating discussions and unwavering desire for achieving high research standards, this work would not have been possible. He has taught me a great deal as a human being in addition to being an advisor.

I would also like to express my sincere gratitude towards Dr. James E. Moon for not only going through my thesis and providing his valuable insights and constructive criticism but also for all his time he devoted to me in answering
all my little questions about the thesis report before it took its final form. I would also thank Dr. Sannasi Ramanan for his time to review this manuscript.

I would also like to thank Mr. James Stefano, our system administrator for always providing me with all the technical resources that I needed. My lab-mates and friends were invaluable in their support. I will thank Ashish Digvadekar, Ashish Vora, Mandapi Mishra, Shailesh Rai, Sankha Mukherjee, Viral Shah and the rest for their motivational talks and constructive criticism.

I express my sincere thanks to all of them who have even in the smallest possible way been a part of this project. And above all I would like to thank my parents and God, without their blessing and encouragement this thesis would not have been possible. I know they are always there for me and always help me get out of all intriguing situations I get myself into.
ABSTRACT

Analog to digital converters play an essential role in modern mixed signal circuit design. Conventional Nyquist-rate converters require analog components that are precise and highly immune to noise and interference. In contrast, oversampling converters can be implemented using simple and high-tolerance analog components. Moreover, sampling at high frequency eliminates the need for abrupt cutoffs in the analog anti-aliasing filters. A noise shaping technique is also used in ΔΣ converters in addition to oversampling to achieve a high resolution conversion. A significant advantage of the method is that analog signals are converted using simple and high-tolerance analog circuits, usually a 1-bit comparator, and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter.

In this thesis, a technique to design the discrete time ΔΣ converters for 25 kHz baseband signal bandwidth will be described. The noise shaping is achieved using a switched capacitor low-pass integrator around the 1-bit quantizer loop. A latched-type comparator is used as the quantizer of the ΔΣ converter. A second order ΔΣ modulator is implemented in a TSMC 0.35 μm CMOS technology using a 3.3 V power supply. The peak signal-to-noise ratio (SNR) simulated is 87 dB; the SNDR simulated is 82 dB which corresponds to a resolution of 14 bits. The total static power dissipation is 6.6 mW.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acknowledgement</td>
<td>i</td>
</tr>
<tr>
<td>Abstract</td>
<td>iii</td>
</tr>
<tr>
<td>Table of Contents</td>
<td>iv</td>
</tr>
<tr>
<td>List of Figures</td>
<td>vii</td>
</tr>
<tr>
<td>List of Tables</td>
<td>xi</td>
</tr>
<tr>
<td>Abbreviations &amp; Symbols</td>
<td>xii</td>
</tr>
<tr>
<td><strong>CHAPTER 1: MOTIVATION AND INTRODUCTION</strong></td>
<td></td>
</tr>
<tr>
<td>1.1 Motivation</td>
<td>1</td>
</tr>
<tr>
<td>1.2 Introduction</td>
<td>3</td>
</tr>
<tr>
<td>1.3 Thesis Contribution</td>
<td>6</td>
</tr>
<tr>
<td>1.4 Thesis Organization</td>
<td>7</td>
</tr>
<tr>
<td><strong>CHAPTER 2: DATA CONVERTERS AND THEIR CLASSIFICATIONS</strong></td>
<td></td>
</tr>
<tr>
<td>2.1 Data Converter Fundamentals</td>
<td>8</td>
</tr>
<tr>
<td>2.1.1 Performance Metrics of Data Converters</td>
<td>10</td>
</tr>
<tr>
<td>2.2 Classification of Data Converters</td>
<td>17</td>
</tr>
<tr>
<td>2.2.1 Nyquist-Rate Converters</td>
<td>17</td>
</tr>
<tr>
<td>2.2.2 Oversampled Converters</td>
<td>17</td>
</tr>
<tr>
<td>2.3 Definition of Important Terms</td>
<td>18</td>
</tr>
<tr>
<td><strong>CHAPTER 3: DELTA–SIGMA CONVERTERS</strong></td>
<td></td>
</tr>
<tr>
<td>3.1 Introduction</td>
<td>21</td>
</tr>
<tr>
<td>3.2 The Concept of Noise Shaping</td>
<td>22</td>
</tr>
<tr>
<td>3.3 Discrete Time $\Delta\Sigma$ Modulator</td>
<td>24</td>
</tr>
<tr>
<td>3.3.1 Qualitative Time Domain Analysis</td>
<td>27</td>
</tr>
</tbody>
</table>
3.4 Continuous Time $\Delta\Sigma$ Modulator .................................................. 30
3.5 DT vs. CT $\Delta\Sigma$ Modulator .................................................. 31

CHAPTER 4: DESIGN OF DELTA-SIGMA CONVERTERS

4.1 Introduction .......................................................... 33
4.2 Switched Capacitor Integrator ........................................... 35
  4.2.1 Switches .................................................. 41
  4.2.2 Operational Amplifier .......................................... 43
  4.2.3 Stability Analysis ............................................. 51
4.4 Non-Overlapping Clock Phase Generator ......................... 57
4.5 The feedback 1 Bit DAC ............................................. 58

CHAPTER 5: RESULTS and DISCUSSIONS

5.1 Introduction .......................................................... 59
5.2 Behavioral Modeling of the $\Delta\Sigma$ ADC ....................... 60
5.3 Operational Amplifier ............................................. 63
5.4 Discrete Time Integrator ............................................. 67
5.5 Comparator – 1 bit Quantizer ..................................... 68
5.6 Non Overlapping Clock Phase Generator ....................... 71
5.7 Second Order $\Delta\Sigma$ Modulator ................................. 72
  5.7.1 Second Order $\Delta\Sigma$ Modulator using TG switches ......... 72
  5.7.2 Second Order $\Delta\Sigma$ Modulator using NMOS switches .... 78
  5.7.3 Stability Check ............................................. 82
5.8 Summary .......................................................... 84

CHAPTER 6: CONCLUSION

6.1 Practical Limitations ................................................ 86
  6.1.1 Noise Sources in the $\Delta\Sigma$ Loop ......................... 86
6.1.2 Thermal Noise .................................................................................. 88
6.1.3 Operational Amplifier ....................................................................... 90

6.2 Conclusion .............................................................................................. 91

6.3 Future Work .......................................................................................... 92

REFERENCES ............................................................................................. 95

**APPENDIX A** Matlab Code of Time Domain Simulations of ΔΣ Modulator 98

**APPENDIX B** Presentation Slides .................................................................. 99
**LIST OF FIGURES**

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Block diagram of a DSP system</td>
<td>2</td>
</tr>
<tr>
<td>1-2</td>
<td>Block diagram of the A/D converter</td>
<td>3</td>
</tr>
<tr>
<td>2-1</td>
<td>Block diagram of an ADC</td>
<td>8</td>
</tr>
<tr>
<td>2-2</td>
<td>(a) Output characteristics of an ADC for a ramp input. (b) Showing the quantization error of the ADC</td>
<td>9</td>
</tr>
<tr>
<td>2-3</td>
<td>Ideal Transfer Curve and Quantization Error in a 3 bit ADC</td>
<td>10</td>
</tr>
<tr>
<td>2-4</td>
<td>Transfer curve of an ADC showing DNL</td>
<td>11</td>
</tr>
<tr>
<td>2-5</td>
<td>Transfer curve of the ADC showing INL</td>
<td>12</td>
</tr>
<tr>
<td>2-6</td>
<td>Transfer curve of the ADC showing offset</td>
<td>13</td>
</tr>
<tr>
<td>2-7</td>
<td>Transfer curve of the ADC showing gain error</td>
<td>13</td>
</tr>
<tr>
<td>2-8</td>
<td>An Ideal Plot of Input vs. SNR measuring the dynamic range</td>
<td>15</td>
</tr>
<tr>
<td>2-9</td>
<td>Quantization noise spectrum in Nyquist-rate and oversampled converters</td>
<td>18</td>
</tr>
<tr>
<td>2-10</td>
<td>Showing the error in sampling due to aperture jitter at signal transition points</td>
<td>19</td>
</tr>
<tr>
<td>3-1</td>
<td>Generalized ΔΣ Modulator with loop-filter G (z)</td>
<td>22</td>
</tr>
<tr>
<td>3-2</td>
<td>Spectrum at the output of a noise shaping quantizer loop</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>compared to those obtained from Nyquist and Oversampling converters</td>
<td></td>
</tr>
<tr>
<td>3-3</td>
<td>First order sigma-delta ADC</td>
<td>24</td>
</tr>
<tr>
<td>3-4</td>
<td>Block diagram of second order ΔΣ ADC</td>
<td>26</td>
</tr>
<tr>
<td>3-5</td>
<td>Shows the mapping of zeroes of the NTF to DC on the frequency axis</td>
<td>27</td>
</tr>
</tbody>
</table>
Figure 3-6  First order sigma-delta ADC (time domain approach).......................... 28
Figure 3-7  Continuous-Time first order ΔΣ Modulator................................. 30
Figure 3-8  (a) Switched-Capacitor Integrator  (b) Continuous-Time Integrator
Figure 4-1  Proposed Second Order Modulator........................................ 34
Figure 4-2  Continuous-Time Integrator.................................................. 35
Figure 4-3  Discrete-Time Integrator..................................................... 36
Figure 4-4  Equivalent circuit during sampling, phase $\Phi_1$....................... 37
Figure 4-5  Equivalent circuit during sampling, phase $\Phi_2$....................... 37
Figure 4-6  Integrator with Bottom Sampling Technique.......................... 40
Figure 4-7  (a) NMOS switch; (b) Transmission Gate (TG) Switch.............. 43
Figure 4-8  A Fully Differential Folded Cascode OTA................................. 44
Figure 4-9  Wide Swing Current Mirror............................................... 48
Figure 4-10 Switched Capacitor Common Mode Feedback Circuit............. 50
Figure 4-12 Latched Comparator.......................................................... 54
Figure 4-13 Non-Overlapping Clock Phase Generator Circuit................... 57
Figure 4-14 Expected Output of the Clock Generator................................. 58
Figure 5-1  Behavioral model of ΔΣ ADC............................................... 60
Figure 5-2  Modulated output signal................................................... 61
Figure 5-3  Frequency spectrum of the modulated signal......................... 61
Figure 5-4  Modulated output signal using Time Domain Analysis............. 62
Figure 5-5  Frequency spectrum of the modulated signal......................... 62
Figure 5-6  Transient Response of the Op Amp showing a gain of 58 dB..... 63
Figure 5-7  AC Response of the OTA showing the gain to be 58 dB, UGBW 137.2 MHz and Phase Margin of 72° 64
Figure 5-8  Transient Response showing the swing of 2 V of the OTA......... 64
Figure 5-9  Transient Response showing the slew rate of the OTA............. 65
Figure 5-10 Input Common Mode Range of the OTA................................. 65
Figure 5-11 Integrator output with TG switches showing a phase shift of 90°.. 67
Figure 5-12 Integrator output with NMOS switches showing a phase shift of 90° 67
Figure 5-13 Output of the comparator..................................................... 68
Figure 5-14 Output of the Comparator showing the minimum voltage 69
difference required for the comparator to change state is 670 mV
Figure 5-15 Output of the Comparator showing a Propagation delay of 3.8 ns 70
Figure 5-16 Hysteresis of the Comparator showing a voltage difference of 70
976 μV/V
Figure 5-17 Output of the clock generator in comparison with the ideal clocks 71
Figure 5-18 Output of the Second Order Delta-Sigma Modulator.............. 73
Figure 5-19 Output of the Delta Sigma modulator (1 cycle)..................... 73
Figure 5-20 Frequency spectrum of the differential output signal of the delta 74
sigma modulator using TG showing an SFDR of 83 dB
Figure 5-21 Plot of output SNR vs. Input Range showing a dynamic range of 75
80 dB
Figure 5-22 Frequency spectrum of modulator, corner (TT) V<sub>DD</sub> = 3.6 V, 76
Temperature 120° C
Figure 5-23 Frequency spectrum of modulator corner (TT) V<sub>DD</sub> = 3.6 V, 76
Temperature 0° C
Figure 5-24  Frequency spectrum of modulator corner (TT) $V_{DD} = 3.0$ V, Temperature $120^\circ$ C  77
Figure 5-25  Frequency spectrum of modulator corner (TT) $V_{DD} = 3.0$ V, Temperature $0^\circ$ C  78
Figure 5-26  Output of the Second Order Delta-Sigma Modulator with NMOS switches  79
Figure 5-27  Output of the modulator with NMOS switches (1 cycle)............  79
Figure 5-28  Frequency spectrum of $\Delta\Sigma$ modulator using NMOS switches showing an SFDR of 75 dB  80
Figure 5-29  Plot of output SNR vs. Input Range showing a dynamic range of  81
  70 dB
Figure 5-30  Stability check of the modulator with a short duration current pulse (TG)  83
Figure 5-31  Stability check of the modulator with a short duration current pulse (NMOS)  83
Figure 6-1  Block Diagram of $\Delta\Sigma$ modulator with the noise sources..............  87
Figure 6-2  Noise source in a switch---------------------------------------------  88
Figure 6-3  A switched capacitor circuit-----------------------------------------  89
LIST OF TABLES

Table 1-1  Comparison table of most popular designs with the current work…. 5
Table 4-1  Transistor sizes of the folded cascode op amp………………….. 47
Table 4-2  Bias circuit transistor sizes……………………………………. 49
Table 4-3  Transistor sizes of the designed comparator………………….. 56
Table 5-1  Comparison Table of results for the designed operational amplifier.  66
Table 5-2  Summary of results comparing both the modulators designed with a popular design  84
Table 5-3  Comparison table of corners analysis results of the two modulators.  85
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D</td>
<td>Analog to Digital</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CMFB</td>
<td>Common Mode Feedback</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>CT</td>
<td>Continuous Time</td>
</tr>
<tr>
<td>D/A</td>
<td>Digital to Analog</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential Non Linearity</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic Range</td>
</tr>
<tr>
<td>DR\textsubscript{i}</td>
<td>Input Dynamic Range</td>
</tr>
<tr>
<td>DR\textsubscript{o}</td>
<td>Output Dynamic Range</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective Number Of Bits</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>ICMR</td>
<td>Input Common Mode Range</td>
</tr>
<tr>
<td>INL</td>
<td>Integral Non Linearity</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-Pass Filter</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>NMOS</td>
<td>n-channel MOSFET</td>
</tr>
<tr>
<td>NTF</td>
<td>Noise Transfer Function</td>
</tr>
<tr>
<td>Op Amp</td>
<td>Operational Amplifier</td>
</tr>
</tbody>
</table>
OSR  Oversampling Ratio
OTA  Operational Transconductance Amplifier
PMOS p-channel MOSFET
PSD  Power Spectral Density
SC   Switched Capacitor
SFDR Spurious Free Dynamic Range
SNR  Signal to Noise Ratio
SNDR Signal to Noise and Distortion Ratio
SR   Slew Rate
STF  Signal Transfer Function
TG   Transmission Gate
THD  Total Harmonic Distortion
TSMC Taiwan Semiconductor Manufacturing Company
VLSI Very Large Scale of Integration
UGBW Unity Gain Bandwidth
C_s  Sampling Capacitor
C_f  Feedback Capacitor
V_{IN}  Input Voltage
V_{OUT}  Output Voltage
V_{REF}  Reference Voltage
\Delta \Sigma Delta-Sigma
f_s  Sampling Frequency
f_B  Baseband Frequency
Chapter 1

1 Motivation and Introduction

1.1 Motivation

1.2 Introduction

1.3 Thesis Contribution

1.4 Thesis Organization

1.1 Motivation

Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC) are the links between the analog world of transducers and the digital world of signal processing and data handling. Many of the communication systems today utilize digital signal processing (DSP) to resolve the transmitted information. Therefore, between the received analog signal and DSP system, an analog to digital (A/D) interface is necessary. This interface achieves the digitization of a received waveform subject to a sampling rate requirement of the system. Figure 1-1 shows the block diagram of a DSP system illustrating the importance of an A/D or D/A interface [27].

The trend of increasing integration level for integrated circuits has forced the A/D interface to reside on the same silicon with large DSP or digital circuits. These digital circuits use digital technology that offers fast transistors biased at low voltages; therefore the ADC becomes the most challenging interface block.
Figure 1-1 Block diagram of a DSP system

The tendency is therefore to use ADC architectures which trade accuracy for speed or vice versa as per the applications. Faster analog designs needing less complex and lower-performance component blocks to attain a given conversion accuracy are the design challenges in the A/D interface implementation.

The technology sets the upper limit for the switching speed, and so the trade-off speed-accuracy must be applied both ways to find the best fitting architecture. For a given application, different architectures are used for different analog signal bandwidths and different available technologies. Nyquist-rate ADC’s are used for high bandwidth conversion while oversampling, noise shaping Delta-Sigma (ΔΣ) converters are used for low and intermediate frequency signals, their range of applicability extending with faster switching speeds available.
**1.2 Introduction**

Delta-Sigma (ΔΣ) analog to digital converters have been successful in realizing high resolution consumer audio products, such as MP3 players and cellular phones for some time now. ΔΣ converters are well suited for low bandwidth, high-resolution acquisition, and low cost, making them a good ADC choice for many applications. Sigma-delta converters combine an analog sigma delta modulator with a more complex digital filter. Accuracy depends on the noise and linearity performance of the modulator, which uses high performance amplifiers. Delta-Sigma modulators trade resolution in time for resolution in amplitude such that the use of imprecise analog circuits can be tolerated. The narrow bandwidths in digital audio applications have made oversampled converters particularly appealing.

![Figure 1-2 Block diagram of the A/D converter](image_url)

A block diagram of an analog to digital converter using delta-sigma modulator is shown in Figure 1-2. Delta-Sigma converters come into the category of oversampled converters. Oversampling is simply the act of sampling the input signal at a frequency much greater than the Nyquist frequency. One significant advantage of the method is that analog signals are converted using only a 1-bit
ADC and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. The penalty paid for the high resolution achievable with delta-sigma is that the hardware has to operate at the oversampled rate, much larger than the maximum signal bandwidth, thus demanding great complexity of the digital circuitry. Because of this limitation, these converters have traditionally been relegated to high-resolution, very-low frequency applications.

To further improve the conversion resolution N at the same sampling speed $f_s$, noise shaping can be applied. This is accomplished by high-pass filtering the quantization noise to displace most of its power from low frequencies where the input signal spectrum is placed to higher frequencies close to $f_s/2$ as shown earlier. One method to attain high pass filtering is to implement a delta-sigma loop around the quantizer, with a loop filter setting the noise shaping. In doing this the quantization noise at the output of the quantizer is attenuated at low frequencies and pushed to higher frequencies away from the signal band. The decimation filter that follows the quantizer then removes the quantization noise appearing at the frequencies greater than $f_B$ (desired frequency band) to improve the effective resolution of the converter.

The current state of the art in the design of delta-sigma modulator is limited by the technology and the sampling speeds it is able to achieve. Here is a comparison table of the most popular designs which also compares the published
works with the current work. It can be seen that the current work is faster than most published work and achieves the resolution of 14 bits using one of the most modern TSMC 0.35 µm CMOS process.

Table 1-1 Comparison table of most popular designs with the current work (*)

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<thead>
<tr>
<th></th>
<th></th>
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<tbody>
<tr>
<td></td>
<td>(dB)</td>
<td>(MHz)</td>
<td>(mW)</td>
<td>(µm)</td>
<td>(CMOS)</td>
<td>Bandwidth</td>
<td>Dynamic</td>
<td>Range</td>
<td></td>
</tr>
<tr>
<td>13.9 bit</td>
<td>128</td>
<td>83.4</td>
<td>5.12</td>
<td>4</td>
<td>2 µm</td>
<td>20 kHz</td>
<td>-</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>14 bit</td>
<td>256</td>
<td>81.5</td>
<td>10.24</td>
<td>75</td>
<td>1.75 µm</td>
<td>20 kHz</td>
<td>88.5 dB</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>8 bit</td>
<td>64</td>
<td>49.7</td>
<td>1.024</td>
<td>6.6</td>
<td>0.6 µm</td>
<td>8 kHz</td>
<td>-</td>
<td>1</td>
<td>3</td>
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<tr>
<td>16 bit</td>
<td>64</td>
<td>91</td>
<td>10.24</td>
<td>76</td>
<td>1.5 µm</td>
<td>160 kHz</td>
<td>80 dB</td>
<td>1-1-1</td>
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<tr>
<td>14 bit</td>
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<td>2.2</td>
<td>200</td>
<td>0.35 µm</td>
<td>100 kHz</td>
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<td>5</td>
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<td>13 bit</td>
<td>32</td>
<td>88</td>
<td>10.24</td>
<td>-</td>
<td>3 µm</td>
<td>160 kHz</td>
<td>-</td>
<td>1-1-1</td>
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<tr>
<td>11 bit</td>
<td>10</td>
<td>62.5</td>
<td>300</td>
<td>70</td>
<td>0.13 µm</td>
<td>15 MHz</td>
<td>67.5 dB</td>
<td>4</td>
<td>7</td>
</tr>
<tr>
<td>14.5 bit</td>
<td>256</td>
<td>89</td>
<td>4</td>
<td>12</td>
<td>3 µm</td>
<td>8 kHz</td>
<td>89 dB</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>14 bit</td>
<td>96</td>
<td>85</td>
<td>53</td>
<td>15</td>
<td>0.18 µm</td>
<td>300 kHz</td>
<td>80 dB</td>
<td>2</td>
<td>9</td>
</tr>
<tr>
<td>14 bit*</td>
<td>256</td>
<td>86.8</td>
<td>12.8</td>
<td>6.6</td>
<td>0.35 µm</td>
<td>25 kHz</td>
<td>80 dB</td>
<td>2</td>
<td>-</td>
</tr>
</tbody>
</table>
1.3 Thesis Contribution

This thesis presents the design and the design concerns of a 14 bit Delta-Sigma Modulator for voice based applications - i.e. frequencies up to 25 kHz with the sampling frequency being 12.8 MHz, and oversampling ratio 256 implementable using TSMC 0.35 µm technology. A complete analysis of the circuit is presented here which shows the implementation of the modulator which achieves 14 bits of resolution with individual components having a resolution less than the overall resolution of the converter. Oversampling is achieved using high speed clocks sampling the signal over a CMOS Transmission Gate switch or a NMOS switch. The modulator implemented here is a 2\textsuperscript{nd} order discrete time modulator which uses two low pass filters and latched comparator acting as a 1 bit quantizer to achieve the desired signal to noise ratio. A brief comparison of the performance of the modulator when designed using different switches is also presented. The target specifications of this work are,

- Resolution, 14 bits
- Dynamic range, 70 dB
- Baseband signal bandwidth, 25 kHz
- Oversampling ratio, 256
- Sampling frequency, 12.8 MHz
- Power dissipation, less than 20 mW
- Full scale input range, ±1 V
- Supply Voltage, 3.3 V
- Voice Based Application, frequencies up to 25 kHz
1.4 Thesis Organization

This thesis is divided into six chapters. Chapter 2 briefly discusses the fundamentals of data converters. It also sheds light on different classifications of data converters and their applications. Some important definitions of terms relating to converters are also presented here. Chapter 3 presents a complete analysis and the mathematical model of delta-sigma converters. It also presents a brief description of continuous time delta-sigma modulators and a brief comparison between the two showing the advantages of the discrete time modulators over their continuous time counterparts.

Chapter 4 contains the complete design methodology adopted to the successful implementation of the modulator. It also presents the analysis and the design of the individual components used CMOS transmission gate switches, discrete time integrator and the comparator. It also presents the design of the non-overlapping clock phase generator.

Chapter 5 presents the results and discussions of all the components designed and implemented and also shows the simulation result of the mathematical model using Simulink in Matlab. Finally, in Chapter 6, a brief overview of the practical limitations in designing a modulator is presented. A summary and conclusions of this work is also presented. Some suggestions regarding the future work that can be pursued are also presented.
Chapter 2

2 Data Converters and their Classifications

2.1 Data Converter Fundamentals

2.1.1 Performance Metrics of Data Converters

2.2 Classification of Data Converters

2.2.1 Nyquist-Rate Converters

2.2.2 Oversampled Converters

2.3 Definition of Important Terms

2.1 Data Converter Fundamentals

In this chapter, fundamental aspects of A/D and D/A converters are presented without regard for their internal architecture or circuit design. Figure 2-1 shows the block diagram of an ADC.

Figure 2-1 Block diagram of an ADC

An anti-aliasing filter is used to remove the high frequency components from incoming signals to avoid aliasing of the signals in the frequency domain during sampling. Sampling is achieved by means of a sample and hold circuit. A sample and hold circuit freezes the analog input voltage at the moment the sample is
required. This voltage is held constant while the A/D converter digitizes it. It is the sampling speed that classifies data converters into categories - *Nyquist Rate Converters* and *Oversampled Converters*, as explained later.

The process of converting continuous time samples from continuous values of information to a finite number of discrete values is called quantization. The response of an ideal ADC with finite resolution for a ramp input is shown in Figure 2-2(a). $V_{in}$ is the input ramp signal and $V_1$ is the output of the ADC. It can be seen in each step that the quantizer generates the same digital code for a range of input values. The difference between the generated code and the original analog value is referred to as quantization error or quantization noise.

![Figure 2-2 (a) Output characteristics of an ADC for a ramp input. (b) Showing the quantization error of the ADC](image)

This error is limited by the sampling frequency used and the resolution of the converter. Subtracting the two signals results in the quantization error $V_Q$ shown in Figure 2-2 (b). It can be noted that if the signal doesn’t exceed the full swing, the error is uniformly distributed and limited to $\pm V_{LSB}/2$ where
If the signal exceeds the full swing the ADC is said to be overloaded and the quantization error exceeds $V_{\text{LSB}}/2$. It is also proven that the average of the quantization noise is 0. The quantizer output is then followed by a digital filter to remove any unwanted noise and increase the overall resolution of the converter.

### 2.1.1 Performance Metrics of Data Converters

Some commonly used terms that describe the performance of a data converter are presented here [10, 11, 12, and 13]. The performance metrics explained here are defined with respect to a 3 bit ADC. A similar analogy can be applied to a DAC as well. An ideal transfer curve of a 3 bit ADC and quantization error ($Q_e$) is shown in Figure 2-3.

![Figure 2-3 Ideal Transfer Curve and Quantization Error in a 3 bit ADC](image-url)
**Resolution** of a converter is defined to be the number of distinct analog levels corresponding to the different digital words. Thus, an N-bit resolution implies that the converter can resolve $2^N$ distinct analog levels.

The following performance metrics are referred to as the static characteristics of the ADC:

**Differential Non Linearity (DNL)** is the maximum deviation in the difference between two consecutive code transition points on the input axis from the ideal value of 1 LSB. A conceptual transfer curve with the quantization noise of the 3 bit ADC is shown in Figure 2-4.

![Figure 2-4 Transfer curve of an ADC showing DNL](image-url)
**Integral Non Linearity (INL)** is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured horizontally as shown in Figure 2-5.

![Figure 2-5 Transfer curve of the ADC showing INL](image)

**Offset Error** is the analog value of the digital output word for the input signal which should have ideally produced a zero output. It is the constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at the vertical jump. Figure 2-6 shows an example of offset error.
Gain Error is defined to be the difference at the full scale value between the ideal and the actual curves when the offset error has been reduced to zero. Also measured as the difference between the ideal slope of the transfer curve and the actual slope of the transfer curve, as shown in Figure 2-7.
Monotonicity; A monotonic converter is one which the output always increases as the input increases. In other words, the slope of the converter’s transfer response is of only one sign. If the maximum DNL error is less than 1 LSB, then a converter is guaranteed to be monotonic.

Often specified as a function of the sampling and input frequencies, the following terms are used to characterize the dynamic performance of the converters:

Dynamic Range (DR) of an ADC is defined as the range of amplitudes the ADC can effectively resolve. If the signal is too large it overloads the ADC and if it is too small it gets lost in the quantization noise. It is defined as the ratio of the full scale value to the smallest difference it can resolve - i.e., $V_{\text{LSB}}$.

$$\text{DR}_{\text{dB}} = 6.02N$$  \hspace{1cm} \text{2-1}

The input dynamic range can also be defined as the magnitude of the baseband signal power at SNR = 0 dB. An ideal plot of the Input Signal (in dB) and the SNR is shown in Figure 2-8.
Signal to Noise Ratio (SNR) is the ratio of the signal power to the total noise power at the output. The quantization noise in Nyquist rate converters (explained later) is given by the mean square value of the quantization error shown in Figure 2-2 (b). Using the double sided spectrum, the quantization noise is given by,

\[
P_{Q,Nyquist} = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} q^2 dq = \frac{\Delta^2}{12} \tag{2-2}
\]

where, \( \Delta = \frac{\text{Full Scale}}{2^N - 1} \) and is assumed to fall between \(-f_s/2\) and \(+f_s/2\), where \( f_s \) is the sampling frequency and \( N \) is the resolution of the converter. In Nyquist rate converters, the sampling frequency is usually twice the signal bandwidth. The SNR of a Nyquist rate converter is given as [13],

\[
\text{SNR} = 6.02N + 1.76 \text{ dB} \tag{2-3}
\]
Signal to Noise Distortion Ratio (SNDR) is the ratio of the signal power to the total noise and the harmonic power at the output.

Spurious Free Dynamic Range (SFDR) The ratio of the RMS value of the input sine wave for an ADC to the RMS value of the peak spur observed in the frequency domain. It is typically expressed in decibels. SFDR is important in certain communication applications that require maximizing the dynamic range of the converter.

Total Harmonic Distortion (THD) of a signal is the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency. It is usually expressed as a percentage. The formula is,

\[
THD = \frac{\sum \text{Harmonic Powers}}{\text{Fundamental Frequency Power}} = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \ldots}{V_1^2}}
\]

Effective Number of Bits (ENOB) is defined by the following equation:

\[
ENOB = \frac{\text{SNR}_{\text{Actual}} - 1.76}{6.02}
\]

Accuracy; is defined to be the difference between the expected and the actual transfer responses. The absolute accuracy includes the offset, gain and linearity errors. The term relative accuracy is sometimes used and is defined to be the accuracy after the offset and gain errors have been removed.
2.2 Classification of Data Converters

Data converters can be broadly classified into two categories depending upon the sampling frequency used for the conversion process [14].

2.2.1 Nyquist-Rate Converters

A analog to digital conversion requires analog input to first be sampled (sampling frequency, \(f_s\)) by a sample-and-hold circuit, which transforms it into an analog, discrete-time signal, only having amplitudes at periodic discrete intervals (\(T_s = 1/f_s\)). The name Nyquist-rate architectures comes from the sampling theorem also known as Nyquist Theorem, stating that \(f_s\) should be at least two times larger than the highest frequency component present in the signal to avoid aliasing and for successful reproduction of the signal after filtering. Hence, specifying the Nyquist rate is equal to specifying the bandwidth of the decimation filter. Equation 2-3 gives the SNR of a Nyquist rate converter, the only noise source being the inherent quantization noise.

2.2.2 Oversampled Converters

In oversampling ADC’s, the input signal is sampled at a rate much higher than twice the bandwidth. The oversampling rate, \(M\), is defined as the ratio of the sampling frequency to the Nyquist rate. This can be expressed as,

\[
M = \frac{f_s}{f_N} = \frac{f_s}{2f_B}
\]
An oversampling rate of unity implies a Nyquist-rate ADC. The signal-to-noise ratio of an oversampled converter can be calculated as \[14\],

\[
\text{SNR} = 6.02 \, N + 1.76 + 10 \log_{10}(M) \, \text{dB} \quad 2-7
\]

This result shows that it is possible to use an ADC with fewer bits to achieve the same SNR performance as a higher performance Nyquist rate ADC. Further it is seen that every doubling of the sampling frequency in an oversampling ADC improves the SNR performance by 3 dB. It can also be noticed that the same amount of quantization noise power is present as for the case of a Nyquist-rate converter, but the amount that actually falls into the bandwidth of the oversampled ADC is less, as shown in Figure 2-9.

Figure 2-9 Quantization noise spectrum in Nyquist-rate and oversampled converters

### 2.3 Definition of Important Terms

Some important terms with respect to a data converter and sample and hold circuits are defined here to have a better understanding of this thesis [13].

**Acquisition Time** is the time between releasing the hold state and the output of the sample circuit settling to the new input voltage value.
Aperture Jitter or Sampling Time Uncertainty; this is an error caused due to variations in the sampling time. This is also called the clock jitter, which causes the instance at which the signal is sampled to change because of variations in the non-ideal clocks. This can result in large error if the aperture jitter happens close to large signal transition points - i.e., the rate of change is maximum at zero crossing. This is well explained in Figure 2-10. If $\Delta t$ represents sampling time uncertainty, then it is desired to keep $\Delta V$ less than one $V_{\text{LSB}}$; then,

$$\Delta t < \frac{1}{2^N \pi f_{\text{in}}}$$

Figure 2-10 Showing the error in sampling due to aperture jitter at signal transition points

ADC Conversion Time and Sampling Rate; Conversion Time is the time taken for the converter to complete a single measurement including the acquisition time of the input signal. Sampling Rate is the speed at which the samples can be continuously converted and is typically the inverse of the
conversion time. However, some converters have a large latency between the input and output due to pipelining or multiplexing, and yet have a high sampling rate.

**Sampling Pedestal** is the transition error when the sample and hold circuit switches from the sample mode to the hold mode.

**Signal Feed Through;** happens during the hold mode wherein a small amount of input signal feeds through to the load, due to parasitic capacitances across MOS switches during sampling.

**Clock Feed Through;** As an analog switch turns on and off, a small amount of charge can be capacitively coupled (injected) from the digital control line to the analog signal path.

**Charge Injection;** occurs when the sampling switch turns off to hold mode and the channel charge of a MOS switch is injected to the load. Charge injection can occur as gain and offset errors when sampling across analog MOS switches.

**Droop Rate;** is the slow change in the output voltage of the sampling switch due to leakage of charge from the sampling capacitor, $C_s$. This is more prominent with slow sampling rates wherein there are large hold times and the capacitor tries to discharge. It can be ignored for cases that have fast sampling rates.
Chapter 3

3 Delta-Sigma Converters

3.1 Introduction

3.2 The Concept of Noise Shaping

3.3 Discrete Time ΔΣ Modulator

3.3.1 Qualitative Time Domain Analysis

3.4 Continuous Time ΔΣ Modulator

3.5 DT vs. CT ΔΣ Modulator

3.1 Introduction

A generalized discrete time representation of the ΔΣ modulator structure is shown in Figure 3-1 [14]. It requires two transfer functions to be implemented, a high pass noise transfer function (NTF) and a low pass signal transfer function (STF). The loop filter has two sections, a forward filter G(z) and a feedback filter H(z). The input signal X(z) is applied and compared with the signal fed back by H(z), filtered through G(z) and is quantized to give the digital output. Hence the quantizer digitizes the sum of previous differences. Thus the term ΔΣ comes from the name of such modulator. The “sigma” and “delta” represent the summation and difference operations respectively. The quantization introduces an error E(z) which is modeled as input-signal-independent and directly added to the output, in the quantizer (represented as a summation point).
The STF is to characterize the transfer function from \( X(z) \) to \( Y(z) \) and the NTF for the partial contribution of \( E(z) \) in \( Y(z) \).

\[
Y(z) = \text{STF}(z) X(z) + \text{NTF}(z) E(z) \tag{3-1}
\]

The input signal \( X(z) \) and the quantization error \( E(z) \) are treated separately. The superposition theorem is then applied, and the two equations are combined to describe the output of the modulator in terms of a single equation with \( X(z) \) and \( E(z) \) and \( H(z) \). Therefore,

\[
\text{STF}(z) = \frac{Y(z)}{X(z)} = \frac{G(z)}{1 + G(z) H(z)}
\]

\[
\text{NTF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + G(z) H(z)}
\tag{3-2}
\]

### 3.2 The Concept of Noise Shaping

A further improvement in the SNR can be achieved by pushing most of the in-band noise left after oversampling outside the signal frequency band. This is
attainable if the STF is all-pass whereas, and most important, the NTF is high pass. Therefore, STF can be approximated to 1 at frequencies where \( G(z) \) is large and \( H(z) \) is unity, while, at the same frequencies, NTF can be approximated as 0. From this theory, it follows that if filters are implemented using integrators, the frequency band where \( G(z) \) is large is around DC.

For low frequency applications integrators are therefore, preferred to function as forward filters. The stability of the system can be established by a large forward path gain. Therefore, \( G(z) \) should be high. If \( G(z) \) is an integrator, noise can be shaped out of the band of interest. All the noise components can be pushed to higher frequencies and the required band can be filtered out using a simple low pass filter. Figure 3-2 shows the spectrum at the output of a noise shaping quantizer loop compared to those obtained from Nyquist and Oversampling converters [15]. The noise shaping modulator does not eliminate the quantization noise; rather, it pushes the quantization noise to higher frequencies.

![Figure 3-2 Spectrum at the output of a noise shaping quantizer loop compared to those obtained from Nyquist and Oversampling converters](image-url)
3.3 Discrete Time ΔΣ Modulator

Following the above analysis, the basic block diagram of a first order delta-sigma converter is shown in Figure 3-3. The input signal comes into the modulator via a summing junction. It then passes through the integrator which feeds a comparator that acts as a one-bit quantizer. The comparator output is fed back to the input summing junction via a one-bit digital to analog converter (DAC), and it also passes through the digital filter and emerges at the output of the converter.

![Figure 3-3 First order sigma-delta ADC](image)

Taking \( G(z) \) to be an integrator for noise shaping, its transfer function can be derived as,

\[
G(z) = \frac{z^{-1}}{1 - z^{-4}}
\] 3-3

Therefore from equation 3-1,
\[ Y(z) = z^{-1} X(z) + (1 - z^{-1}) E(z) \]  \hspace{1cm} 3-4

Equation 3-4 implies that,

\[ \text{STF} = z^{-1} \]  \hspace{1cm} 3-5

\[ \text{NTF} = 1 - z^{-1} \]

The equation 3-4 can be written in time domain as,

\[ y[n] = x[n-1] + e[n] - e[n-1] \]  \hspace{1cm} 3-6

The output is just the delayed version of the input plus the first order difference of the quantization noise. This proves that using integrators as a forward filter makes the STF all pass and NTF high pass. The SNR of first order noise shaping can be derived as [11],

\[ \text{SNR} = 6.02N + 1.76 - 5.17 + 30 \log (M) \]  \hspace{1cm} 3-7

where \( M \) is the oversampling ratio. Clearly there is an increase in the resolution given by,

\[ N_{\text{inc}} = \frac{30 \log (M) - 5.17}{6.02} \]  \hspace{1cm} 3-8

The advantage of first order noise shaping is an improvement of the SNR by 9 dB for every doubling of the oversampling ratio as opposed to a 3 dB increase without noise shaping. It can be also be proved that implementing a second order
delta-sigma (ΔΣ) ADC can provide for much better noise shaping and a higher order resolution. Thus, the signal to noise ratio (SNR) is higher for a second order ΔΣ ADC. The transfer function for the second order system can be given by,

\[
Y(z) = (z^{-1})^2 X(z) + (1 - z^{-1})^2 E(z)
\]

As it can be seen from the transfer function, the input signal is to be delayed by two cycles and two integrators can be used in cascade to implement the square term in the transfer function expression. Therefore, implementing a second order system does not cause any serious changes in the design procedure except for using two integrators. Hence, a first order system will be designed and implemented as a second order system to yield the advantages of high resolution and better signal-to-noise ratio. The SNR of the second order noise shaping modulator is [11],

\[
\text{SNR} = 6.02N + 1.76 - 12.9 + 50 \log \left( \frac{M}{M_0} \right)
\]

![Figure 3-4 Block diagram of second order ΔΣ ADC](image)

The block diagram of the second order system is shown in Figure 3-4. It can be noted from equations 3-3 and 3-5 that the poles of the integrator transfer
function become the zeroes for the noise transfer function (NTF). Thus, second order noise shaping can be more clearly observed from Figure 3-5 which shows the mapping of zeroes of the NTF in z-domain to the frequency axis. The figure shows that the NTF zeroes are mapped to DC, and hence noise shaping can be obtained [29].

Figure 3-5 Shows the mapping of zeroes of the NTF to DC on the frequency axis

3.3.1 Qualitative Time Domain Analysis

Following the frequency domain behavior discussed in the previous section, it is important to analyze the delta-sigma modulator in the time domain as well. Redrawing Figure 3-3 and labeling the discrete time domain signals as shown the following sets of equation can be obtained. The input to the modulator is \( x[n] \) and the final output of the modulator is \( y[n] \). Various intermittent signals as labeled as shown. From the Figure 3-6 it can be shown that,

\[
\begin{align*}
\text{u}[n] &= \text{x}[n] - \text{y}_a[n] \\
\text{v}[n] &= \text{u}[n-1] + \text{v}[n-1]
\end{align*}
\]
\[ y[n] = v[n] + e[n] \]

Figure 3-6 First order sigma-delta ADC (time domain approach)

Assuming the comparator’s digital output is 1 or -1, then \( y[n] \) and \( y_a[n] \) can be used interchangeably. Therefore,

\[
y[n] = \begin{cases} 
1 & v[n] \geq 0 \\
-1 & v[n] < 0
\end{cases}
\]

It is to be noted that the signal that is quantized is not the input \( x[n] \) but a filtered version of the difference between the input and an analog representation, \( y_a[n] \), of the quantized output, \( y[n] \). The filter, often called the feed forward loop filter, is a discrete time integrator. The “error” between the modulator output and input is \( u[n] \). Note that this is not the quantization error, which is given by 3-15,

\[
e[n] = y[n] - v[n]
\]
Since \( y[n] \) can take on values of 1 or -1 only, it can never equal the input unless the input happens to be one of these two values exactly. Consequently, except for the mentioned cases, there will always be an error,

\[
\text{u}[n] \neq 0
\]  \( 3\text{-}16 \)

Consider a DC input for \( x[n] \). When \( y[n] = 1 \), \( y[n] \) is greater than the input \( x[n] \) and the error \( u[n] \) is negative, and so negative values are accumulated by the integrator to produce \( v[n] \). After a number of clock cycles, enough negative values will have accumulated to cause the quantizer to produce \( y[n] = -1 \), thereby changing the sign of the error \( u[n] \) to be positive. The error between the output and input has been reduced, in some sense, because the positive errors will now cancel the prior negative errors when averaged over a period of time. Now with \( y[a] = -1 \), the errors will be positive, and positive values of the error will be accumulated again until the quantizer output changes, this time back to \( y[n] = 1 \). Over a period of time, the proportion (or density) of 1’s and -1’s will be related to the DC input value: the larger the input, the more 1’s will be present in the output, and vice versa, for smaller inputs. For this reason, the output of a sigma-delta modulator using a 1 bit quantizer is often said to follow the average of the input. A similar analysis can be extended to a second order modulator as well.
3.4 Continuous Time $\Delta \Sigma$ Modulator

In a discrete-time $\Sigma\Delta$ modulator, the input is a sampled signal. It is possible to realize a continuous-time modulator as shown in Figure 3-7. In this case the input signal and the loop-filter are continuous and the sampling operation only occurs before the quantizer. A similar analysis is used as previously used to show that STF and NTF for continuous-time modulator are given by [11],

$$STF(s) = \frac{1}{s+1} \quad 3-17$$

$$NTF(s) = \frac{s}{s+1} \quad 3-18$$

where, STF has a first-order low-pass characteristics and NTF has a first-order high-pass filter characteristics so that quantization noise is shifted to higher frequencies.

![Figure 3-7 Continuous-Time first order $\Delta \Sigma$ Modulator](image-url)
3.5 DT vs. CT ΔΣ Modulator

Modulators can be implemented either as a sampled-data system or in the continuous-time domain [16, 17]. The primary difference is that sampled-data systems employ switched-capacitor integrators while continuous-time systems use active-RC integrators in the modulators. There are a number of advantages and disadvantages associated with each option, as will be discussed below. Switched-capacitor integrators take advantage of fine-line VLSI capabilities by eliminating the need for physical resistors. On-chip resistors with very high linearity are difficult to achieve in a standard CMOS process. In addition, resistors in continuous-time integrators need to be kept small to minimize thermal noise. For the same time-constant, reducing the resistors implies that the feedback capacitors need to be increased. This may make the area prohibitively large and the capacitors impractical to realize on-chip.

The frequency response of switched-capacitor integrators can be more accurately predicted because the time-constant is a function of capacitor ratios ($C_s/C_f$) and of the sampling frequency. The time-constant of continuous-time integrators, on the other hand, is a product of the resistor and the capacitor, and suffers severely from process variations. The absolute value of on-chip poly resistors typically vary by 30% from the nominal/desired value, whereas capacitor ratios are usually better controlled (typical variation is only 1%).
Another advantage of switched-capacitor systems is that they are less sensitive to clock jitter and to the manner in which the opamp settles [18]. As long as the Operational Amplifier (opamp) settles to the required accuracy, it does not matter whether the opamp slews or linearly settles. Continuous-time integrators, however, must be linear at all times.

Continuous-time systems have their share of advantages over sampled-data systems. Because the opamp in an active-RC integrator does not have to settle to full accuracy every half clock period, a very high oversampling ratio is achievable [28]. The oversampling ratio in switched-capacitor integrators is limited by the achievable bandwidths of the opamps. This makes continuous-time modulators very appealing for high-speed applications.

Finally, continuous-time systems eliminate the need for an anti-alias filter prior to the sigma-delta ADC. The anti-alias filter is needed in sampled-data systems to attenuate energies at multiples of the sampling frequency which may potentially fold down to baseband. The elimination of this filter results in significant power savings for the receiver.
Chapter 4

4 Design of Delta-Sigma Converters

4.1 Introduction

4.2 Switched Capacitor Integrator
   4.2.1 Switches
   4.2.2 Operational Amplifier
   4.2.3 Stability Analysis

4.4 Non-Overlapping Clock Phase Generator

4.5 The feedback 1 Bit DAC

4.1 Introduction

Due to the numerous advantages of the Discrete Time Modulator over its Continuous Time counterparts as discussed earlier, this work discusses and implements a Discrete Time Modulator. This section presents an overview of the design methodology adopted in implementing a fully differential second order modulator and also addresses the issues involving the design of the modulator. The proposed architecture of the modulator is shown in Figure 4-1 which follows straight from the basic block diagram of the modulator shown in Figure 3-4. The reference voltages are chosen to be ±1 V around the common mode voltage (1.65 V in this design). Therefore, $V_{REF+}$ is 2.65 V and $V_{REF-}$ is 0.65 V.

The integrator implemented here is a switched-capacitor parasitic-insensitive integrator; the advantages of this will be discussed shortly. Since the integrator itself is discrete in time, a sample and hold circuit which is to precede the
integrator can be eliminated. Discrete Time Integrators are implemented using switched capacitor circuits and Op Amps, the design of which will also be presented. Switched Capacitor circuits are to be driven by non-overlapping clocks. The design of the non-overlapping clock phase generator is also presented.

![Proposed Second Order Modulator](image)

**Figure 4-1 Proposed Second Order Modulator**

A latched comparator is also to be designed to work as a 1 bit quantizer. An advantage of the latched comparator is that, it is driven by a clock which keeps it in synchronization with the other fast switching components of the circuit. Other benefits include the feature that it refreshes its internal nodes every other clock cycle, resulting in a very small hysteresis.
4.2 Switched Capacitor Integrator

A single-ended integrator can be implemented in continuous time very simply with an operational amplifier, a resistor and a feedback capacitor. It is difficult to imagine a differential continuous-time integrator (Figure 4-2) because the resistors occupy huge space in a layout and they are also the sources of noise. In switched capacitor circuits, a capacitor can be used to emulate the behavior of resistor by switching it in and out of the circuit.

![Figure 4-2 Continuous-Time Integrator](image)

A differential switched capacitor integrator is shown in Figure 4-3. The three main differences that can be noticed when this integrator is compared with continuous-time are 1) The resistor is replaced by a capacitor $C_s$; 2) Four switches have been included in the circuit that are controlled by two different phases;
3) The op-amp in the continuous-time integrator is replaced by an Operational Transconductance Amplifier (OTA) in the discrete-time case.

![Figure 4-3 Discrete-Time Integrator](image)

The operation of the **Switched Capacitor (SC) integrator** circuit can be demonstrated by examining the transfer function of charge on the capacitors during each clock phase. The SC integrator has been redrawn for each phase in Figure 4-4 and Figure 4-5. It is assumed that the OTA has a very high gain and that the initial voltage stored on \(C_f\) is zero. During \(\Phi_1\) all the switches that are clocked by the other phase are open and the input of the OTA is disconnected from the circuit. Since the bottom plate of sampling capacitor \(C_s\) is connected to the input and the top plate is connected to the ground the capacitor is charged up to an initial charge of \(Q_{\text{initial}} = C_s V_{\text{in}}\). It should be noted that the output from the integrator is zero due to the fact that the initial voltage across \(C_f\) is zero.
During phase $\Phi_2$ all of the switches that were previously closed are all opened. Thus the input is disconnected from the circuit and the output is no longer available from the integrator. The bottom plate of $C_s$ is connected to ground and top plate of $C_s$ is connected to the input terminal of the OTA. The connection of the OTA output to its input forces the differential input voltage of the OTA to
zero. Meanwhile since the bottom-plate of \( C_s \) is connected to ground and top-plate of \( C_s \) is forced to zero due to the OTA, the charge on the sampling capacitor \( C_s \) can only be transferred to the feedback capacitor \( C_f \). Note that the polarity is the same polarity as the input voltage as the capacitor terminals were reversed from one phase to other. The charge transferred is equal to \( Q_{\text{final}} = C_f V_{\text{out}} \). However this charge must be equal to the original charge sampled onto \( C_s \). Equating \( Q_{\text{final}} \) with \( Q_{\text{initial}} \) and rearranging for the output voltage yields

\[
V_{\text{out}} = \frac{C_s}{C_f} V_{\text{in}} \tag{4-1}
\]

When phase \( \Phi_1 \) is active again, the input voltage is sampled again onto \( C_s \) while the integrator output voltage is equal to the previous sample multiplied by a gain factor of \( C_s/C_f \). Then again during \( \Phi_2 \) the charge from the new sampled input is transferred to the feedback capacitor where it adds to the previous charge stored from the first sampling operation. The charge stored on the feedback capacitor is always maintained by the OTA and is never discharged. Thus the feedback capacitor accumulates the charge taken from each sampling operation of the input signal. Since the output of the SC integrator at a particular moment in time is equal to the previous output voltage in addition to the input voltage sampled in the previous operation multiplied by a gain factor \( C_s/C_f \), the output of the integrator may be written mathematically as,
\[
V_{\text{out}}(nT_s) = V_{\text{out}}(T_s[n - 1]) + \frac{C_s}{C_f} V_{\text{in}}(T_s[n - 1])
\]  
4-2

Taking the Z transform of equation 4-2 yields

\[
V_{\text{out}}(z) = z^{-1} V_{\text{out}}(z) + \frac{C_s}{C_f} z^{-1} V_{\text{in}}(z)
\]  
4-3

And rearranging this equation for \(V_{\text{out}}(z)\) gives

\[
V_{\text{out}}(z) = \frac{C_s}{C_f} \frac{z^{-1}}{1 - z^{-1}} V_{\text{in}}(z)
\]  
4-4

Now the integrator is made to employ the bottom-plate sampling technique to minimize signal dependent charge-injection. This is achieved through delayed clocks \(\Phi_{1d}\) and \(\Phi_{2d}\). When switches labeled \(\Phi_1\) are first tuned off, the charge injection from those switches remains, to a first order, independent of the input signal. Because one of the plates is now floating, turning off switches labeled \(\Phi_{1d}\) shortly after does not introduce charge injection errors. The circuit diagram that employs bottom-plate sampling is shown in Figure 4-6 [20].

The sampling capacitors are chosen to be 2 pF, the feedback capacitor being 0.45 pF. The circuit is simulated and the results are verified using the transfer function of the integrator (Results will be presented in Chapter 5).
Figure 4-6 Integrator with Bottom Sampling Technique

The transfer function of the integrator is given as [30]

$$H\left(e^{j\omega T_s}\right) = H_i\left(e^{j\omega T_s}\right)\left[1 + m(\omega)\right]e^{j\theta(\omega)}$$ \hspace{1cm} 4-5

The magnitude of the transfer function is given as

$$|H\left(e^{j\omega T_s}\right)| = |H_i\left(e^{j\omega T_s}\right)|\left[1 + m(\omega)\right]$$ \hspace{1cm} 4-6

where $m(\omega)$ is the relative gain error and $\theta(\omega)$ is the relative phase error due to the op amp’s finite gain. Here,

$$|H_i\left(e^{j\omega T_s}\right)| = \left|\frac{-C_1}{2j\sin\left(\omega T_s/2\right)}\right|$$ \hspace{1cm} 4-7

$$m(\omega) = -\frac{1}{A_0}\left(1 + \frac{C_1}{2C_2}\right)$$ \hspace{1cm} 4-8
\[
\theta(\omega) = \frac{C_1/C_2}{2A_0 \tan(\omega T_s)}
\]

4.9

The relative phase shift is given by,

\[
\theta = \tan^{-1}\left[\frac{\sin(\omega T_s)}{\cos(\omega T_s) - 1}\right]
\]

4.10

### 4.2.1 Switches

One of the most fundamental aspects of designing an ADC is the design of sampling switches. Switches are ideally designed to have zero ON resistances and infinite OFF resistances. MOS transistors used in the triode region, can function as switches with ON resistances varying from a few ohms to a few kilo ohms and very high OFF resistances. In addition to the finite ON resistances, there are also parasitic capacitances associated with the switch [21, 22], which when taken into account can result in charge-injection and clock feed through causing gain error or offset error in the performance of the converter. Therefore, the designing of the switches become an integral part in the design of a data converter.

One of the most commonly used switches is a NMOS switch (Figure 4-7a). One major concern of the NMOS switch is high ON resistance for input values very close to the power supply (V_{DD}). Designing switches that allow rail-to-rail swings is a challenge in low-voltage applications. The reason for this is that as technology scales, the supply voltage scales down at a much faster rate than the
threshold voltage of a transistor. Since the threshold voltage of a transistor limits the swing of a switch using such a transistor, the swing capability decreases with each migration of technology.

The technique that can be used to accommodate greater swings is to use complementary switches or transmission gates that consist of a PMOS in parallel with NMOS transistor, as shown in Figure 4-7(b). Although such a switch has the disadvantage of requiring complementary clocks, this is a small price to pay for the improvement in the signal swing across the switch. The major design challenges include the designing and optimization of switching techniques to be used in the modulator. The switches designed here have minimum sizes supported by the process and the modulator performance is tested using both NMOS and TG switches.

The size of the NMOS switch was chosen to be minimum sizes transistors with the W/L being 0.7 µm/0.35 µm. The PMOS switches of the TG were chosen to be 3 times that of NMOS switches to account for varying switching times. W/L_{pmos} is 2.1 µm/0.35 µm
Figure 4-7 (a) NMOS switch; (b) Transmission Gate (TG) Switch

4.2.2 Operational Amplifier

Operational Transconductance Amplifiers (OTA) are key components of integrators in the ΔΣ ADC. The OTA to be used is a folded cascade, fully differential amplifier. The OTA to be designed is to meet the following specifications.

- Voltage Gain, \( A_v \geq 60 \text{ dB} \)
- Positive going slew rate = 200 V/\( \mu \text{s} \)
- Gain-bandwidth (GB) \( \approx 120 \text{ MHz} \)
- Output Voltage Swing, \( 0.4 \text{ V} \leq V_{out} \leq 2.9 \text{ V} \)
- Phase Margin \( \geq 60^0 \)
- Power Supplies \( V_{DD} = 3.3 \text{ V}, V_{SS} = 0 \text{ V} \)
- Load Capacitance \( C_L = 2 \text{ pF} \)

Folded cascode architecture has been used as an operational amplifier as it offers good self compensation, good input common mode range and can maintain the gain of a two stage Op Amp. It has a better noise rejection from the substrate
and the power lines, too, than conventional two stage OTAs. The idea of folding the cascode is to have a Common Source stage driving a Common Gate stage having complimentary transistors. The advantage of this approach is that the input and output voltages are at the same level. Even though a folded-cascode amplifier is considered as a single stage, the gain can be relatively large, on the order of 700-3000, due to the high output impedance of the cascode technique [23, 24]. The basic architecture used here is shown in Figure 4-8.

![Figure 4-8 A Fully Differential Folded Cascode OTA](image)
When compared with other topologies like a conventional two-stage amplifier, the two-stage amplifier has a lower dominant pole than the folded cascode circuit; hence it cannot be used in high frequency applications. Folded cascode circuit doesn’t need frequency compensation as needed for a two-stage amplifier. The two-stage amplifier has poorer power supply rejection ratio (PSRR) than the folded-cascode circuit at high frequencies. Hence, keeping all these aspects in mind, the folded-cascode amplifier is chosen for the design of this sigma-delta modulator.

The current in the circuit is determined using the slew-rate, given as

$$SR = \frac{I}{C_L}$$  \hspace{1cm} 4-11

$$I = 400 \, \mu A$$  \hspace{1cm} 4-12

The bias-generator circuit is to be designed generating this current and appropriate gate–source voltages of the transistors of the cascode pair to which this bias generator is connected. The maximum swing between the rail voltages (0 V – 3.3 V) is specified as 0.4 V– 2.9 V. Then the drop across the transistors M₉, ₇ and M₈, ₁₀ for the maximum swing should be 0.4V (drain-source voltages). If the W/L ratios of the transistors M₇, ₁₀ are made same then it can be said that the drain-source voltage \( V_{DS} \) of the transistor M₉, ₁₀ at the maximum swing is 0.2V. Therefore, for M₁₀, ₁₃ to be in saturation,
\[ V_{ON} = 0.2 \text{ V} \quad 4-13 \]

\[
\therefore \left( \frac{W}{L} \right)_{7,8} = \left( \frac{W}{L} \right)_{9,10} = 564.51 = \frac{400 \mu \text{m}}{0.7 \mu \text{m}} \quad 4-14
\]

Considering the output swing going low to 0.4 V, the transistors (M\(_{14-17}\)) accommodating this drop should still be in saturation. Now since the current flowing through M\(_{3,4}\) is twice (i.e., 400 µA due to the topology) the current flowing through M\(_{5,6}\), it can be said that the drain source voltage of M\(_{5,6}\) and M\(_{3,4}\) each is 0.2 V if the size of M\(_{3,4}\) is made twice the size of M\(_{5,6}\). Therefore, for \( V_{ON} = 0.2 \text{ V} \),

\[
\left( \frac{W}{L} \right)_{3,4} = 2 \times \left( \frac{W}{L} \right)_{5,6} \quad 4-15
\]

\[
\left( \frac{W}{L} \right)_{5,6} = \frac{125 \mu \text{m}}{0.7 \mu \text{m}} \quad 4-16
\]

\[
\left( \frac{W}{L} \right)_{3,4} = \frac{250 \mu \text{m}}{0.7 \mu \text{m}} \quad 4-17
\]

The transistor M\(_{11,12}\) is made same as the size of M\(_{7,10}\) so as to have the same 400 µA of current through the differential amplifier. The size of M\(_{1,2}\) is calculated from the gain bandwidth specification given (\( \omega_i = 120 \text{ MHz} \)). The equations used are,
The sizes of the input transistors $M_{1,2}$ are increased to 1000µm/0.7µm to boost the open loop gain of the op amp. The transistor sizes used to implement the design of the folded cascode are summarized in Table 4-1.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Multiplier</th>
<th>Size $(W/L)_{\mu m}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{1,2}$</td>
<td>10</td>
<td>100/0.7</td>
</tr>
<tr>
<td>$M_{3,4}$</td>
<td>10</td>
<td>25/0.7</td>
</tr>
<tr>
<td>$M_{5,6}$</td>
<td>10</td>
<td>12.5/0.7</td>
</tr>
<tr>
<td>$M_{7-10}$</td>
<td>10</td>
<td>40/0.7</td>
</tr>
<tr>
<td>$M_{11,12}$</td>
<td>10</td>
<td>40/0.7</td>
</tr>
</tbody>
</table>

Table 4-1 Transistor sizes of the folded cascode op amp
As it can be seen that the cascode pair needs to be biased, a standard wide swing cascode current mirror is used to provide for the biasing of the transistors in the cascode pair. The “wide swing cascode current mirror” is one circuit that does not limit the signal swing as much as the other conventional current mirrors and also provides higher output resistance and a better matching for the currents. A basic wide swing current mirror is shown in Figure 4-9.

![Figure 4-9 Wide Swing Current Mirror](image)

Now a bias generator circuit is to be designed generating fixed DC voltages and fixing the current in the circuit. The topology of the bias generator circuit used is the standard wide swing current mirror circuit. The current in the bias circuit is chosen to be 40 μA. This current will be mirrored into the folded
cascode to 400 µA as per the design specified earlier. The transistors in the bias circuit are made 10 times smaller than the transistors in the cascode of the op amp. The current in the final leads of the bias circuit are multiplied to 400 µA by making their sizes the same as the ones used in cascode. This ensures proper matching of the currents in the cascode of the op amp. The transistors M₃ and M₉ are made approximately four times smaller than M₂ and M₈ respectively to ensure proper biasing of the DC voltages [11]. The gate lengths of the transistors of the bias circuit are chosen to be 4X (1.4 µm) times the minimum allowable length for matching purposes during layout. The transistor sizes of the bias circuit used are summarized in Table 4-2.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Multiplier</th>
<th>Size (W/L)µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>M₁, M₂</td>
<td>1</td>
<td>25/1.4</td>
</tr>
<tr>
<td>M₃</td>
<td>1</td>
<td>2.8/1.4</td>
</tr>
<tr>
<td>M₄-7</td>
<td>10</td>
<td>25/1.4</td>
</tr>
<tr>
<td>M₈, 9</td>
<td>10</td>
<td>80/1.4</td>
</tr>
<tr>
<td>M₉</td>
<td>10</td>
<td>14/1.4</td>
</tr>
<tr>
<td>M₁₁-13</td>
<td>1</td>
<td>8/1.4</td>
</tr>
</tbody>
</table>

Table 4-2 Bias circuit transistor sizes
Since the output is fully differential a Common Mode Feedback Circuit must be added to establish the output common mode voltage. The purpose of the CMFB circuit is to keep the common-mode (average) output voltage at a constant level (usually halfway between the power-supply voltages). The CMFB circuit must first sense the differential output voltages and average them to produce the output common-mode level. Then this level must be compared to the desired common-mode level (which in this design is 1.65 V) and the difference between the actual CM level and the desired CM level is used to change the CM bias current in the OTA to bring the actual CM level back to the desired CM level. The speed of the CMFB circuit should be comparable to the unity-gain frequency of the differential path. Otherwise noise on the power supplies may be amplified. A simple switched capacitor circuit is used to establish the common mode voltage $V_{cm}$. The common mode feedback circuit is implemented using a switched capacitor circuit (shown in Figure 4-10) driving these switches. The capacitor $C_C$ is chosen to be 1 pF and $C_S$ being $1/5^{th}$ of $C_C$ equal to 0.2 pF [11].

![Figure 4-10 Switched Capacitor Common Mode Feedback Circuit](image)
4.2.3 Stability Analysis

To understand the stability of the delta-sigma loop the block diagram in Figure 3-6 is redrawn incorporating the gains of the integrator as $G_I$ and comparator $G_C$ as shown in Figure 4-11. A first order delta-sigma modulator is considered and the concept can be extended to the second order modulator.

Figure 4-11 Block diagram of 1st order ΔΣ modulator

The gain of the integrator is given by, shown earlier in 4-4,

$$G_I = \frac{C_S}{C_F}$$  \hspace{1cm} 4-22

Also the forward gain $G_F$ is defined as the product of the integrator gain and the comparator gain.

$$G_F = G_I \times G_C$$  \hspace{1cm} 4-23

Equation 3-4 can be re-written as [13],

51
\[ Y(z) = \frac{z^{-1} G_F}{1 + z^{-1} (G_F - 1)} X(z) + \frac{1 - z^{-1}}{1 + z^{-1} (G_F - 1)} E(z) \]

4-24

If \( G_F \) approaches zero, the output,

\[ Y(z) = E(z) \]

4-25

The output is just the quantization noise not spectrally shaped and recovery of the original signal with a low pass filter becomes difficult. If \( G_F \) is greater than 2, then the poles of the modulator lie outside the unit circle in the \( z \)-domain. The modulator becomes unstable. Therefore to ensure stability,

\[ 0 \leq G_F \leq 2 \]

4-26
4.3 Quantizer Design

An important component of any ADC is a quantizer. Typically, a quantizer design includes a very precise sample-and hold circuit and a high-accuracy comparator working at Nyquist sampling frequency. The accuracy requirement of the comparator depends on the accuracy requirement of the converter, e.g. an 8-bit ADC requires a comparator with at least 8-bit accuracy. In contrast, in ΔΣ modulators, the comparator is required to work at a high oversampling frequency but its resolution can be as small as 1 bit. Therefore, the comparator design in ΔΣ modulators focuses more on high-speed operation instead of accuracy.

To combine the sample and hold function and the comparator function and also to match speeds, a latched comparator is the best choice [25, 26]. A comparator is used here to act as 1-bit quantizer converting from the analog signal to digital signal. Comparators are circuits which change the output state depending on the difference of the two input signals. A clocked comparator is used here to synchronize its operation with the other circuits in the ADC as they are run by high speed clocks. The architecture of the comparator is shown in Figure 4-12. The principle design parameters of this comparator are speed (which must be adequate enough to achieve the desired sampling rate), input offset, input referred noise, and hysteresis. It has been pointed out already that offset and noise at the comparator input are suppressed by the feedback loop of the modulator.
Also, the sensitivity of ΔΣ modulators to comparator hysteresis is several orders of magnitude smaller than that of Nyquist rate converters. Therefore, this relaxes the performance requirements of the comparator.

![Figure 4-12 Latched Comparator](image)

M1 and M4 are the input transistors which are connected to a feedback network formed by M2 and M3. M5 and M6 are control transistors. M8 and M9 form another feedback network for M7 and M10, which are precharge transistors used for refreshing the internal nodes when not in operation to reduce hysteresis. M11-M14 forms two inverters which act as buffers to isolate the latch from the output load and to amplify the comparator output. During the pre-charge phase,
i.e. when CLK goes low, transistors M5 and M6 are cut off and the comparator does not respond to any input signal. The voltages $V_{oc^+}$ and $V_{oc^-}$ will be pulled to the positive rail, $V_{DD}$, and the output of the inverters will be pulled to ground. At the same time, M1 and M4 discharge the voltages $V_{F^+}$ and $V_{F^-}$ to ground. During the evaluation phase, i.e. when CLK goes high, both the voltages $V_{oc^+}$ and $V_{oc^-}$ drop from the positive rail and both the voltages $V_{F^+}$ and $V_{F^-}$ rise from ground.

If the voltage at $V_{in^+}$ is higher than that at $V_{in^-}$, M1 draws more current than M4. Thus, $V_{oc^+}$ drops faster than $V_{oc^-}$ and $V_{F^-}$ rises faster than $V_{F^+}$. As $V_{oc^+}$ drops a threshold voltage below $V_{DD}$, M9 turns on and charges $V_{oc^-}$ to high level while $V_{oc^+}$ keeps going to ground. Also, as $V_{F^-}$ raises a threshold voltage above ground, M2 turns on and discharges $V_{F^+}$ to ground while $V_{F^-}$ keeps rising to $V_{DD}$. The regenerative action of M8 and M9 together with that of M2 and M3 pulls $V_{oc^+}$ to ground and pulls $V_{oc^-}$ to positive rail. Hence, following the inverters M11- M14, $V_{o^+}$ is pulled to positive rail and $V_{o^-}$ is pulled to ground. The operation for the case when the voltage at $V_{in^-}$ is higher than that at $V_{in^+}$ is similar.

In designing the W/L ratios of the transistors for the comparator, considerations have to be made for high-speed operation. The delay of the whole comparator determines the fastest operation frequency of the comparator. For high-speed operation, the sizes of transistors M5 and M6 should be large enough so that their resistance values are minimal but should be small enough at the same
time to reduce the capacitance in order to have minimal comparator delay. The sizes of transistors M1 and M4 should be large enough to ensure quick response to the input signal, but small enough for minimal gate capacitances for high-speed operation. The sizes of transistors M2, M3, M8 and M9 should be small enough for high-speed operation, but large enough for quick regenerative action. Finally, the inverter transistors M11-M14 should be large enough for driving the output load to reduce the inverter delay, but small enough for minimal gate-capacitances to reduce the comparator delay. The transistor sizes chosen for this design are summarized in Table 4-3.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Size (W/L)(_{\mu m})</th>
</tr>
</thead>
<tbody>
<tr>
<td>M(_{1,4})</td>
<td>2/1</td>
</tr>
<tr>
<td>M(_{2,3})</td>
<td>10/1</td>
</tr>
<tr>
<td>M(_{5,6})</td>
<td>2/1</td>
</tr>
<tr>
<td>M(_{8,9})</td>
<td>30/1</td>
</tr>
<tr>
<td>M(_{7,10})</td>
<td>20/1</td>
</tr>
<tr>
<td>M(_{11,13})</td>
<td>2.1/0.35</td>
</tr>
<tr>
<td>M(_{12,14})</td>
<td>0.7/0.35</td>
</tr>
</tbody>
</table>

Table 4-3 Transistor sizes of the designed comparator
4.4 Non-Overlapping Clock Phase Generator

The clock generator for producing non-overlapping clock signals can be realized with a simple circuit constructed of logic gates. Such a circuit is shown in Figure 4-13 [29, 31]. It consists of two transistor level NOR-gates and several inverters. Complementary signals for TG switches can be generated adding inverters subsequently (not shown). Further delayed clock can be produced by using several inverters again to one of the output clocks to produce its delayed clock. Note that the complementary phase signals are taken one inverter after each phase and that no compensation delay gate was needed to equalize the delay from the inverter. The expected timing diagram of clocks $\Phi_1$ and $\Phi_{1D}$ ($\Phi_1$ delayed), $\Phi_2$ and $\Phi_{2D}$ is shown in Figure 4-14.

![Figure 4-13 Non-Overlapping Clock Phase Generator Circuit](image)

The main advantage of this circuit is its simplicity. At least a part of the buffering of output signals can be included in the delay elements, making the circuit quite robust. On the other hand, the non-overlap time often becomes larger than necessary because of the buffering included and the margin added to
accommodate the process and temperature variations. The resulting speed penalty is emphasized in high clock rate circuits. Furthermore, the duty cycle of the generated clock signals is inherited from the input clock, requiring it to be close to 50%.

![Figure 4-14 Expected Output of the Clock Generator](image)

**4.5 The feedback 1 Bit DAC**

The quantizer used in this design is of 1 bit resolution hence the feedback DAC is also 1 bit in resolution. The 1 bit DAC can be implemented using a simple wire connected with the reference voltages. The advantage of a 1-bit DAC is that it is inherently linear. This linearity results in the output of the DAC being only two values (V_{REF+} and V_{REF-}) and no calibration or trimming is required.
Chapter 5

5 Results and Discussions

5.1 Introduction

5.2 Behavioral Modeling of the ΔΣ ADC
5.3 Operational Amplifier
5.4 Discrete Time Integrator
5.5 Comparator – 1 bit Quantizer
5.6 Non Overlapping Clock Phase Generator
5.7 Second Order ΔΣ Modulator
   5.7.1 Second Order ΔΣ Modulator using TG switches
   5.7.2 Second Order ΔΣ Modulator using NMOS switches
   5.7.3 Stability Check
5.8 Summary

5.1 Introduction

This section shows all the results obtained from the designed values of various components discussed in the previous section. It shows plots of all performance metrics of the Operational Amplifier, the Comparator and the Fully Differential Integrator. Also a comparison table is presented after each section comparing with the specifications designed for. Performance of the Op Amp and the Discrete Time Integrator can be compared when different sampling switches are used - i.e., NMOS switch and TG switch. All the results shown here are using TG switches unless otherwise specified. The results using NMOS switches are summarized at the end of each section.
Finally, the results of the Second Order Fully Differential Discrete Time Delta-Sigma Modulator are presented. A results table showing various performance metrics of the modulator can be found in this section. The circuit is also simulated against four typical corners. Results are finally compared with one popular design.

5.2 Behavioral Modeling of the ΔΣ ADC

The functional diagram of the second order modulator simulated using Simulink in MATLAB is shown in Figure 5-1. The single bit DAC is replaced by a simple wire. The input is a sinusoidal signal with 1 V amplitude and frequency 12.5 kHz. This signal is fed through two integrators in cascade and is connected to the comparator at the output. Intermediate gain stages are used to provide stability to the system to ensure that all the poles of this system are well within the unit circle in the z domain.

![Figure 5-1 Behavioral model of ΔΣ ADC](image)

The modulated output as seen through the scope is shown in Figure 5-2 with the input signal overlaid on it. A discrete Fourier Transform (DFT) of the sampled output signal (2048 samples) is performed to calculate the SNR of the system.
The logarithm of the amplitude of the signal is plotted versus the signal frequency and the SNR is found to be close to 58 dB (shown in Figure 5-3). It can be seen that second order noise shaping is taking place wherein most of the noise is pushed to the higher frequency bands. The original signal can be retrieved using a digital low pass filter.

![Figure 5-2 Modulated output signal](image1)

![Figure 5-3 Frequency spectrum of the modulated signal](image2)

Matlab can also be directly used to model the behavior of the modulator as shown in Appendix A. Here the time domain mathematical models (shown in the
previous section) are run for a sinusoidal source of input amplitude 1 V. The results are shown in Figure 5-4 and Figure 5-5 showing the SNR to be close to 61 dB. Simulink can be used model other non idealities of the delta-sigma modulator as well [19].

Figure 5-4 Modulated output signal using Time Domain Analysis

Figure 5-5 Frequency spectrum of the modulated signal
5.3 Operational Amplifier

The fully differential folded cascode is simulated as per the designed values and the results obtained are as follows. The transient response of the Op Amp for a 2 mV_{pp} differential signal is shown in Figure 5-6. Initial transients can be seen in the output which is due to the time taken by the CMFB circuit to take effect and the bring the output common mode DC to the desired voltage, in this case half way between the supply rails - i.e., 1.65 V. The open loop gain of the op amp was found to be 58 dB and the unity gain-bandwidth for this configuration was 137.2 MHz as shown in Figure 5-7. The phase margin measured is 72°.

![Figure 5-6 Transient Response of the Op Amp showing a gain of 58 dB](image)
Figure 5-7 AC Response of the OTA showing the gain to be 58 dB, UGBW 137.2 MHz and Phase Margin of 72°

Figure 5-8 Transient Response showing the swing of 2 V of the OTA
The output swing measured peak to peak shown in Figure 5-8 is found to be 0.65 V to 2.65 V. The slew rate of the op amp was found to be 130 V/µS, shown in Figure 5-9. The input common mode range of the OTA is shown in Figure 5-10 to be between -0.6 V to 2.2 V; same for the case using NMOS switches in the CMFB circuit (also shown).

Figure 5-9 Transient Response showing the slew rate of the OTA

Figure 5-10 Input Common Mode Range of the OTA
A summary of results is shown in Table 5-1 which compares the results of the op amp using the two switches and compares them with the targeted specifications.

**Table 5-1 Comparison Table of results for the designed operational amplifier**

<table>
<thead>
<tr>
<th></th>
<th>Target Specifications</th>
<th>Results of the Op Amp using TG switches in the CMFB circuit</th>
<th>Results of the Op Amp using NMOS switches in the CMFB circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Open Loop Gain</strong></td>
<td>60 dB</td>
<td>58 dB</td>
<td>58 dB</td>
</tr>
<tr>
<td><strong>UGBW</strong></td>
<td>120 MHz</td>
<td>137.2 MHz</td>
<td>140 MHz</td>
</tr>
<tr>
<td><strong>Phase Margin</strong></td>
<td>60°</td>
<td>72°</td>
<td>72.5°</td>
</tr>
<tr>
<td><strong>Swing</strong></td>
<td>2.5 V</td>
<td>2 V</td>
<td>2 V</td>
</tr>
<tr>
<td><strong>ICMR</strong></td>
<td>-</td>
<td>-0.6 V - 2.2 V</td>
<td>-0.6 V - 2.2 V</td>
</tr>
<tr>
<td><strong>Slew Rate</strong></td>
<td>200 V/µs</td>
<td>130 V/µs</td>
<td>126 V/µs</td>
</tr>
</tbody>
</table>
5.4 Discrete Time Integrator

A switched capacitor fully differential integrator was simulated (circuit shown in Figure 4-6) using both NMOS and TG as sampling switches. $C_s$ and $C_f$ were chosen to be 0.45 pF and 2 pF respectively. The outputs are shown in Figure 5-11 and Figure 5-12.

Figure 5-11 Integrator output with TG switches showing a phase shift of 90°

Figure 5-12 Integrator output with NMOS switches showing a phase shift of 90°
5.5 Comparator – 1 bit Quantizer

A latched comparator which switches to the rail supply depending on the input signal is used here to act as a 1-bit quantizer. It is designed as per the methodology discussed earlier. The results are as follows. Figure 5-13 shows the output of the comparator for a DC input at one input terminal and a sine source with a DC offset at the other input terminal. Since it is a clocked comparator it evaluates the result of comparison at every clock cycle.

![Figure 5-13 Output of the comparator](image)

A minimum voltage difference is required at the input of the comparator to change its state. This minimum voltage should be sufficiently high so that any noise occurring at the inputs does not cause the comparator to switch states, whereas at the same time it should be low enough not to reduce the dynamic
range at the input [11]. The minimum voltage measured for this design is 670 mV. This was obtained by grounding one of the inputs of the comparator and a ramp input to the other terminal and was seen that the output of the comparator does not switch until the input voltage difference has reached 670 mV (shown in Figure 5-14).

![Figure 5-14](image)

Figure 5-14 Output of the Comparator showing the minimum voltage difference required for the comparator to change state is 670 mV

The propagation delay of the comparator is the time taken to reach 50% of its final value when switching states. A DC input compared to a ramp input enables a measure of the propagation delay. Figure 5-15 shows a propagation delay of 3.8 ns. Due to the regenerative latch the hysteresis of the comparator is measured to be as small as 976 µV/V; shown in Figure 5-16.
Figure 5-15 Output of the Comparator showing a Propagation delay of 3.8 ns

Figure 5-16 Hysteresis of the Comparator showing a voltage difference of 976 µV/V
5.6 Non Overlapping Clock Phase Generator

The non-overlapping clock phase generator was designed as shown in Figure 4-13. A series of cascaded inverters with their W/L ratios being less than 1 cause a significant delay in the output of the inverter. Figure 5-17 shows the output of the clock generator and also compares it with the ideal clocks (also) shown. Phi1 clock corresponds to clk1 in the figure and Phi2 to clk2 and so on. Phi1, Phi1d, Phi2 and Phi2d are the ideal clocks and the outputs of the clock generator (clk1, clk1d, clk2, clk2d) are plotted against it for comparison. The outputs of the clock generator are in accordance with ones shown in Figure 4-14.

Figure 5-17 Output of the clock generator in comparison with the ideal clocks
5.7 Second Order ΔΣ Modulator

The Delta-Sigma Modulator is implemented as shown in Figure 4-1. The next section shows all the results of the delta-sigma modulator using TG switches and the following section discusses the results obtained when using NMOS switches.

5.7.1 Second Order ΔΣ Modulator using TG switches

The output of the modulator using TG switches is shown in Figure 5-18. As seen, \( v_{in} \) is a 500 mV\text{PP} sine wave which is the input to the negative terminal of the switched capacitor filter and \( v_{in+} \) is the same sine wave with opposite phase. \( X \) and \( Y \) are the outputs of the modulator. It can be seen that the output is as expected, therefore it can be concluded that the modulator successfully modulates the input signal source.

The original signal can be retrieved using a digital decimation filter which digitally down-samples the oversampled signal followed by a simple half-band filter. The close-in capture of the output shown in Figure 5-18 can be seen in Figure 5-19 (1 cycle) which is the expected response as shown in Figure 5-2 and Figure 5-4. To further analyze the modulator output, an FFT is performed on the differential output signal to obtain the frequency spectrum of the signal. It is shown in Figure 5-20.
Figure 5-18 Output of the Second Order Delta-Sigma Modulator

Figure 5-19 Output of the Delta Sigma modulator (1 cycle)
It can be concluded from the frequency spectrum of the output that second order noise shaping is taking place with the measured SNR being 87 dB. The SNDR was found to be 82 dB, SFDR (shown Figure 5-20) measured is approximately 83 dB and the total harmonic distortion was calculated to be $7.05 \times 10^{-7}$ %. The effective resolution of the modulator was calculated to be 14 bits.

The input dynamic range of the modulator using TG switches is found to be 80 dB as shown in Figure 5-21. SNR and SNDR were computed for various input levels and thus the graph was constructed.
The dotted curve is the SNR and continuous curve is the SNDR. It is seen that both curves follow each other very closely until input values very close to 1 dB. At this point the modulator is overloaded and an increase in the harmonic distortion can be noted. Input dynamic range is input signal value in dB for which the SNR is zero. As seen from the plot, SNR at -80 dB input signal is ~ 2 dB.

Corner analysis was performed on the modulator against variations in temperature and power supply. Power supply was varied ± 10% of its nominal value-i.e., 3.6 V and 3.0 V. Temperature was changed to 0° C and 120° C. Results for all corners shown are as follows. Figure 5-22 shows the frequency spectrum of the modulated output for a 1 V_{pp} differential signal sine source for V_{DD} of 3.6 V and simulation temperature set to 120° C (TT corner). The SNR measured was 92 dB, SNDR was 76 dB, SFDR measured (shown) is 75 dB and the total harmonic distortion was 2.5 x 10^{-6} %.
Figure 5-22 Frequency spectrum of modulator, corner (TT) $V_{DD} = 3.6$ V, Temperature 120° C

Figure 5-23 Frequency spectrum of modulator corner (TT) $V_{DD} = 3.0$ V, Temperature 120° C
Figure 5-23 shows the results for the corner (TT) $V_{DD}$ 3.0 V and simulation temperature being 120$^\circ$. SNR was 108 dB, SNDR was 46 dB, and SFDR measured is 46 dB with the total harmonic distortion calculated as 0.0027%. Figure 5-24 shows the results for the corner $V_{DD}$ being 3.6 V with the simulation temperature set to 0$^\circ$ C. SNR and SNDR were measured to be 87 dB and 84.6 dB respectively. SFDR was measured to be 80.7 dB with the total harmonic distortion being $3.5 \times 10^{-7}$%.

Figure 5-24 Frequency spectrum of modulator corner (TT) $V_{DD} = 3.6$ V, Temperature 0$^\circ$ C

Figure 5-25 shows the results for the corner $V_{DD}$ being 3.0 V with the simulation temperature set to 0$^\circ$ C. SNR and SNDR were measured to be 83 dB and 73 dB respectively. SFDR was measured to be 73 dB with the total harmonic distortion being $5.7 \times 10^{-6}$%. All the results are summarized after the next section.
Shown below are the output and the performance metrics of the Delta-Sigma modulator using NMOS switches. The output of the modulator is shown in Figure 5-26. As seen, \( vin \) is a 300 mV\(_{pp} \) sine wave which is the input to the negative terminal of the switched capacitor filter and \( vin^+ \) is the same sine wave with opposite phase. \( X \) and \( Y \) are the outputs of the modulator. Therefore it can be concluded that the modulator successfully modulates the input source. The close-in capture of the same Figure 5-26 can be seen in Figure 5-27.
Figure 5-26 Output of the Second Order Delta-Sigma Modulator with NMOS switches

Figure 5-27 Output of the modulator with NMOS switches (1 cycle)
Figure 5-28 Frequency spectrum of ΔΣ modulator using NMOS switches showing an SFDR of 75 dB

Figure 5-28 shows that SNR is close to 85 dB, the SNDR was 74 dB, SFDR measured is 75 dB and the total harmonic distortion was calculated to be $3.85 \times 10^{-6}\%$. The effective resolution of the modulator was calculated to be 14 bits. Corner Analysis was performed on the modulator with NMOS switches, results of which are summarized in Table 5-3. The input dynamic range of the modulator is shown in Figure 5-29.
Figure 5-29 Plot of output SNR vs. Input Range showing a dynamic range of 70 dB
### 5.7.3 Stability Check

It was shown in Figure 5-14 that the $V_{\text{min}}$ for the comparator was found to be 670 mV. Therefore the gain $G_C$ of the comparator can be calculated as,

$$
G_C = \frac{V_{\text{DD}} - V_{\text{SS}}}{V_{\text{min}}} = \frac{3.3 \text{ V}}{0.67 \text{ V}} = 4.93
$$

The gain of the integrator is calculated as

$$
G_I = \frac{C_s}{C_f} = \frac{0.45 \text{ pf}}{2 \text{ pf}} = 0.225
$$

Therefore for second order modulator,

$$
G_F = G_I^2 \times G_C = 0.25
$$

The condition in equation 4-26 is satisfied. To further check the stability of the circuit in simulation, a short duration current pulse is applied at one input and a common mode DC voltage at the other input. Voltages at various nodes are plotted to check for transients. No oscillations were found. Figure 5-30 and Figure 5-31 show the response of the modulator for the current pulse using TG and NMOS switches, respectively. $X$ and $Y$ are the outputs of the modulator. $vo1$ and $vo2$ are the outputs of the first integrator, $vo3$ and $vo4$ are the outputs of the second integrator and $feedback+$ and $feedback-$ are the outputs of the feedback 1-bit DAC.
Figure 5-30 Stability check of the modulator with a short duration current pulse (TG)

Figure 5-31 Stability check of the modulator with a short duration current pulse (NMOS)
5.8 Summary

The summary of results for the second order delta-sigma modulator is shown in Table 5-2.

Table 5-2 Summary of results comparing both the modulators designed with a popular design

<table>
<thead>
<tr>
<th></th>
<th>Target Specifications</th>
<th>ΔΣ Modulator with TG switches</th>
<th>ΔΣ Modulator with NMOS switches</th>
<th>ΔΣ Modulator by Boser et al. measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Order</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Resolution</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14.5</td>
</tr>
<tr>
<td>SNR</td>
<td>86 dB</td>
<td>87 dB</td>
<td>85 dB</td>
<td>89 dB</td>
</tr>
<tr>
<td>SNDR</td>
<td>86 dB</td>
<td>82 dB</td>
<td>74 dB</td>
<td>-</td>
</tr>
<tr>
<td>SFDR</td>
<td>-</td>
<td>83 dB</td>
<td>75 dB</td>
<td>-</td>
</tr>
<tr>
<td>THD</td>
<td>-</td>
<td>7.05 x 10^{-7} %</td>
<td>3.85 x 10^{-6} %</td>
<td>-</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>70 dB</td>
<td>80 dB</td>
<td>70 dB</td>
<td>89 dB</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>25 kHz</td>
<td>25 kHz</td>
<td>25 kHz</td>
<td>8 kHz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>&lt; 20 mV</td>
<td>6.6 mW</td>
<td>6.6 mW</td>
<td>12 mW</td>
</tr>
<tr>
<td>Speed</td>
<td>12.8 MHz</td>
<td>12.8 MHz</td>
<td>12.8 MHz</td>
<td>4 MHz</td>
</tr>
<tr>
<td>Power Supply</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>5 V</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>3 µm</td>
</tr>
</tbody>
</table>
Summary of the corner analysis with variation in $V_{DD}$ and temperature for a typical process (corner TT and FF) of both the modulators is shown in Table 5-3.

**Table 5-3 Comparison table of corners analysis results of the two modulators**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Delta-Sigma Modulator with TG switches</th>
<th>Delta-Sigma Modulator with NMOS switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corner 1 (TT)</td>
<td>SNR 92 dB</td>
<td>83 dB</td>
</tr>
<tr>
<td>$V_{DD} = 3.6$ V</td>
<td>SNDR 76 dB</td>
<td>67 dB</td>
</tr>
<tr>
<td>Temperature 120° C</td>
<td>SFDR 75 dB</td>
<td>72 dB</td>
</tr>
<tr>
<td></td>
<td>THD $2.46 \times 10^{-6}$%</td>
<td>$1.91 \times 10^{-5}$%</td>
</tr>
<tr>
<td>Corner 2 (TT)</td>
<td>SNR 108 dB</td>
<td>58 dB</td>
</tr>
<tr>
<td>$V_{DD} = 3.0$ V</td>
<td>SNDR 46 dB</td>
<td>52 dB</td>
</tr>
<tr>
<td>Temperature 120° C</td>
<td>SFDR 46 dB</td>
<td>53 dB</td>
</tr>
<tr>
<td></td>
<td>THD $0.0027$%</td>
<td>$0.0006$%</td>
</tr>
<tr>
<td>Corner 3 (TT)</td>
<td>SNR 87 dB</td>
<td>80 dB</td>
</tr>
<tr>
<td>$V_{DD} = 3.6$ V</td>
<td>SNDR 85 dB</td>
<td>73 dB</td>
</tr>
<tr>
<td>Temperature 0° C</td>
<td>SFDR 81 dB</td>
<td>75 dB</td>
</tr>
<tr>
<td></td>
<td>THD $3.47 \times 10^{-7}$%</td>
<td>$5 \times 10^{-6}$%</td>
</tr>
<tr>
<td>Corner (FF)</td>
<td>SNR 82 dB</td>
<td>94 dB</td>
</tr>
<tr>
<td>$V_{DD} = 3.6$ V</td>
<td>SNDR 64 dB</td>
<td>78 dB</td>
</tr>
<tr>
<td>Temperature 0° C</td>
<td>SFDR 64 dB</td>
<td>78 dB</td>
</tr>
<tr>
<td></td>
<td>THD $4.2 \times 10^{-5}$%</td>
<td>$1.7 \times 10^{-6}$%</td>
</tr>
</tbody>
</table>
Chapter 6

6 Conclusion

6.1 Practical Limitations

6.1.1 Noise Sources in the ΔΣ Loop
6.1.2 Thermal Noise
6.1.3 Operational Amplifier

6.2 Conclusion
6.3 Future Work

6.1 Practical Limitations

The implementation of delta-sigma modulator was discussed in the previous section. However, the modulator is subjected to practical limitations and this applies to both SC and CT modulators. These limitations are caused by non-ideal operation of various components like the integrators, quantizer and DAC. There also may be non-linear operations due to jitter of clock pulse edges, mismatches, etc. The non-ideal behavior of the integrator could be attributable to finite gain, bandwidth and slew rate of the op amp. An understanding of these non-idealities is thus important for successful implementation of a delta-sigma modulator.

6.1.1 Noise Sources in the ΔΣ Loop

There can be various noise sources in the delta-sigma loop shown in Figure 6-1. There can be external noise accompanying the input signal labeled as $e_1 (n)$. The thermal/flicker noise at the input stage of the integrator is shown as
$e_2(n)$. Noise due to clock jitter and feed through are modeled in $e_1(n)$ and $e_2(n)$ themselves. Noise due non-linear operation of the integrators - i.e., due to slew rate or clipping appears at the output of the integrators and is shown as $e_3(n)$, which also includes noise due to any non-linear operation of the quantizer. Non-linear operation of the local DAC is shown equivalent to $e_{DAC}(n)$. $e_q(n)$ is the quantization noise of the quantizer. All these noise sources may affect the output of the modulator.

![Block Diagram of ΔΣ modulator with the noise sources](image)

Figure 6-1 Block Diagram of ΔΣ modulator with the noise sources

Evaluating the transfer function of the block diagram shown in Figure 6-1 results in [15],

$$Y(z) = X(z) + E_1(z) - z^{-1}E_{DAC}(z) + \left[ E_2(z) - z^{-1}E_{DAC}(z) \right] \left[ 1 - z^{-1} \right] + \left[ E_q(z) + E_3(z) \right] \left[ 1 - z^{-1} \right]^2$$  \[6-1\]

Clearly, from the transfer function it can be seen that the critical noise sources are the $e_{DAC}(n)$ and $e_1(n)$ as they appear directly at the output. $e_2(n)$ is subjected to first order noise shaping whereas $e_3(n)$ is added to $e_q(n)$ and noise shaped by the order of two. $e_{DAC}(n)$ becomes less critical for this design, as a
1-bit DAC has been chosen, which is inherently linear. $e_{DAC}(n)$ becomes more prominent in the case of multi-bit DAC’s.

### 6.1.2 Thermal Noise

A MOSFET switch can be modeled as an ideal switch with some on resistance labeled as $R_{on}$ which has a noise component $n_i(t)$ because of thermal noise, as shown in Figure 6-2.

![Figure 6-2 Noise source in a switch](image)

It is known that thermal noise source $n_i(t)$ has a power spectral density $P(f)$ [32],

$$P(f) = 4kT R_{on}$$  \hspace{1cm} 6-2

Therefore in switched capacitor circuits wherein resistors are replaced by capacitors, the thermal noise is generated by finite on-resistances of the switches. A parasitic-insensitive switched-capacitor circuit equivalent to a resistor is shown in Figure 6-3. Therefore the total thermal noise (also called KTC noise) generated is given by,
\[ P_{\text{Thermal}} = \frac{2kT}{C_S} \]

\[ \text{Figure 6-3 A switched capacitor circuit} \]

As seen, the spectrum of this noise is white, but due to oversampling, the overall in-band thermal noise is given by [15],

\[ P_{\text{Th, in}} = \frac{2kT}{C_S} \frac{1}{\text{OSR}} \]

Therefore, it is noted that increasing the over-sampling ratio reduces the in-band thermal noise. Also, using larger sampling capacitors reduces the effects of thermal noise.
**6.1.3 Operational Amplifier**

Due to the finite op amp gain the transfer function of the SC integrator is proven to be \([15]\),

\[
\frac{Y(z)}{X(z)} = \frac{gz^{-1}}{1-pz^{-1}} \quad (6-5)
\]

where, ‘g’ is the gain and ‘p’ is the pole which is not at unity in the z-domain. As the poles of the integrator are the zeroes of the noise transfer function and the poles have moved inside the unit circle, zeroes have moved away from the DC point in the s plane. As a direct consequence of that, there is a reduction in the attenuation of the quantization noise. There is no proper noise shaping taking place. This is called pole error and is shown to be proportional to \(1/A\) (\(A\) is DC gain of the op amp). Therefore, for maximum attenuation of in-band quantization noise the DC gain of the op amp should be as high as possible.

In SC integrators another important parameter is the settling time of the integrator, which depends on the bandwidth of the op amp. In usual filters the unity gain bandwidth of the op amp has to be at least 10 times larger than sampling frequency [33]. If the settling time is larger than the sampling time the modulator may become unstable. As far as slew-rate of the op amp is concerned in SC circuits, the effect can be ignored if proper settling can be achieved.
6.2 Conclusion

In this work a delta-sigma modulator design has been presented that met the performance requirements. The modulator was designed in 0.35μm technology at an operating voltage of 3.3 V. A fully-differential switched-capacitor implementation was used. The final design is a 14-bit, second-order, fully differential, delta-sigma modulator with an oversampling ratio of 256. Simulations in Cadence indicate that a signal-to-noise ratio of approximately 86 dB is achievable.

Second-order sigma-delta modulators constitute an efficient architecture for implementing high-resolution analog-to digital converters in scaled high-performance integrated circuit technologies. Both simulations and analytical results have been used to establish design criteria for the analog circuit blocks comprising such a modulator. Specifically, it has been found that integrator linearity has a crucial influence on the performance of these converters, whereas delta-sigma modulators impose only modest demands on integrator bandwidth and are relatively insensitive to offset and hysteresis in the comparator. The analysis presented here has also been used to identify mechanisms other than quantization noise that may limit the performance of delta-sigma modulators regardless of the oversampling ratio.
It has been proven that TG switches are more immune to imperfections like charge-injection and clock feed through due to the complementary pair connected in parallel which cancels out the effect of each other. Therefore, they deliver much better performance when compared to NMOS switches in delta-sigma modulators, the only disadvantage being the need for complementary clocks. Fully differential architectures, too, have been an added advantage of immunity against noise when compared to their single-ended counterparts.

**6.3 Future Work**

Future work to extend the current design could be design optimization. For example, the cascode op amp designed can be gain boosted for enhanced noise shaping. Use of multi-bit ADC and DAC also can help increasing the resolution of the modulator. Dithering can also help increase the SNR. Dithering is a technique of intentional addition of white noise in the circuit which has proven to yield better in-band noise attenuation. The second order modulator can be cascaded to a first order modulator to increase the resolution.

Once the design of the modulator is successfully done, the next step could be to integrate the modulator with the other blocks in the receive path to demonstrate an overall system. One of the blocks required to complete the system is decimation filter. Design of decimation filter is a challenge in itself. An ADC consists of a decimation filter which differs from the digital processing block found in Nyquist-rate ADCs. This decimation filter performs two important
functions. First, it low-pass filters the output signal from the quantizer so that all frequency components above $f_B$ are removed. Hence, this filtering action removes all of the quantization noise that doesn’t appear within the bandwidth. The second function that it performs is to down-sample the data from the oversampling frequency of $f_S$ to the Nyquist rate of the input signal, i.e. $2f_B$. Note that the filtering action that precedes the down-sampling operation ensures that aliasing doesn’t occur. Hence due to these functions the decimation filter is one of the important blocks.

The other area of interest is to design a Bandgap Reference Circuit. It is one of the essential building blocks of most of the analog circuits including ADC, DAC, DRAM and flash memory. The principle of bandgap circuits relies on two groups of diode-connected BJT transistors running at different emitter current densities. By canceling the negative temperature dependence from one group of transistors with the positive temperature dependence from a proportional-to-absolute-temperature (PTAT) circuit which includes another set of transistors, temperature dependence is removed. It is a very essential component in an ADC design which helps keep the reference voltage constant with respect to temperature. These essential aspects just mentioned complete the design of an ADC.
REFERENCES


APPENDIX A

The MATLAB code used for time domain simulation of equations of the behavior of the delta-sigma modulator is shown.

clear all
close all
t=1;
n=(2^10)*2*t;
integ(1)=0;
y(1)=0;
x2(1)=1;
d=1:n;

for i=1:n;
    x(i)=sin(2*t*pi*(i)/n);
end

%2nd order sdadc modulator
for i=1:(n-1);
    sum1(i+1)=x(i+1)-y(i);
    x2(i+1)=sum1(i+1)+x2(i);
    sum2(i+1)=x2(i+1)-y(i);
    integ(i+1)=integ(i)+sum2(i+1);

    if integ(i+1)>=0
        y(i+1)=1;
    else
        y(i+1)=-1;
    end
end

subplot(2,1,1), plot(d,y,'r')
subplot(2,1,2), plot(d,x);hold on

% FFT computation
N = length(y) ;
i = 0: N-2 ;
figure(2)
B = abs(fft(y, N));
B = B(1:N-1)/(N-1) ;
f = i(1:length(i))*fin;
plot(f,20*log10(B)) ;
grid on;
xlabel ('Frequency (Hz)'); ylabel ('Amplitude (dB)');
APPENDIX B

Design of a 14-bit, Fully Differential Discrete Time Delta-Sigma Modulator

Dissertation of Master’s Thesis

By
Sumit Kumar Nathany,
Advisor: Dr. Syed S. Islam

Block Diagram of a DSP System

- Digital Systems are used for Data Handling, Processing and Storing
- ADC’s and DAC’s link Analog World and Digital World
- Integrated circuit technology trends have caused these analog interfaces to reside alongside the digital systems on the same chip
- Therefore, these interfaces pose a design challenge
### ADC Architectures

<table>
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<tr>
<th>Architecture</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
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<tr>
<td>Flash</td>
<td>Fast</td>
<td>High Power Consumption Low Resolution</td>
</tr>
<tr>
<td>Pipeline</td>
<td>High Accuracy Low Power Consumption</td>
<td>Requires a minimum clock frequency</td>
</tr>
<tr>
<td>SAR</td>
<td>High Resolution and Accuracy Low Power</td>
<td>Limited Sample Rate Low Bandwidth</td>
</tr>
<tr>
<td>Delta-Sigma</td>
<td>High Resolution Fewer Design Constraints</td>
<td>Low Speed Limited Bandwidth</td>
</tr>
</tbody>
</table>

### Block Diagram of the A/D Converter

- **Analog Signal in** → **Delta Sigma Modulator** → **Digital Decimation Filter** → **Digital Signal out**

**Functions of the Modulator are:**

- **Sampling** - A sample and hold circuit freezes the analog input voltage at the moment the sample is required. This voltage is held constant while the A/D converter digitizes it.
- **Quantization** - is process of converting continuous time samples from continuous values of information to a finite number of discrete values.
Performance Metrics of a Data Converter

Resolution

Static Characteristics
- Differential Non-Linearity (DNL)
- Integral Non-Linearity (INL)
- Offset Error
- Gain Error

Dynamic Characteristics
- Dynamic Range (DR)
- Signal to Noise Ratio (SNR)
- Signal to Noise & Distortion Ratio (SNDR)
- Spurious Free Dynamic Range (SFDR)
- Total Harmonic Distortion (THD)

\[ \text{THD} = \frac{\sum \text{Harmonic Powers}}{\text{Fundamental Frequency Power}} = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \ldots}{V_1^2}} \]
Classification of Data Converters

Based on Sampling Speed, data converters can be classified into two categories:

- **Nyquist-Rate Converters** – have sampling rates equal to the Nyquist-rate of the baseband signal. Typically 2~3 times the baseband signal bandwidth. The quantization noise is white within the signal bandwidth. The SNR of these converters, taking into account the quantization noise only is given by,

\[ \text{SNR} = 6.02 N + 1.76 \, \text{dB} \]

- **Oversampled Converters** – have sampling rates much higher than baseband signal bandwidth. Typically 8~256 times the baseband signal bandwidth. The quantization noise is spread across the whole spectrum. The SNR of oversampled converters is given by,

\[ \text{SNR} = 6.02 N + 1.76 + 10 \log_{10}(M) \, \text{dB} \]

Quantization noise spectrum in Nyquist-rate and oversampled converters

**Advantage of Oversampling**
- Less quantization noise within the baseband signal bandwidth hence high resolution achievable.

**Disadvantage of Oversampling**
- Circuit components have to operate at oversampled speeds and hence limited by the technology.
Generalized ΔΣ Modulator

Applying superposition theorem to calculate the transfer function of the system shown in the block diagram. The Signal Transfer Function (STF) and the Noise Transfer Function (NTF) can be defined as,

\[ STF(z) = \frac{Y(z)}{X(z)} = \frac{G(z)}{1 + G(z)H(z)} \]

\[ NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + G(z)H(z)} \]

Therefore, \( Y(z) \) can be written as,

\[ Y(z) = STF(z)X(z) + NTF(z)E(z) \]

Concept of Noise Shaping

From the block diagram it follows that

\[ STF(z) = \frac{Y(z)}{X(z)} = \frac{G(z)}{1 + G(z)H(z)} \]

\[ NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + G(z)H(z)} \]

If \( G(z) \) is large and \( H(z) \) is 1 then

\( STF(z) \sim 1 \)

\( NTF(z) \sim 0 \)

If \( G(z) \) is implemented as an Integrator

\[ G(z) = \frac{z^{-1}}{1 - z^{-1}} \]

Then

\[ Y(z) = z^{-1}X(z) + [1 - z^{-1}]E(z) \]

Therefore,

\[ STF = z^{-1} \]

\[ NTF = 1 - z^{-1} \]
**Concept of Noise Shaping contd…**

\[ G(z) = \frac{z^{-1}}{1 - z^{-1}} \]

\[ \text{STF} = z^{-1} \]

\[ \text{NTF} = 1 - z^{-1} \]

Spectrum at the output of a noise shaping quantizer loop compared to those obtained from Nyquist and Oversampling converters*


---

**The ΔΣ Modulator**

Block Diagram of a First order Noise Shaping Delta-Sigma ADC

\[ \text{SNR} = 6.02N + 1.76 - 5.17 + 30 \log (M) \]

Block Diagram of a Second Order Noise Shaping Delta-Sigma ADC

\[ \text{SNR} = 6.02N + 1.76 - 12.9 + 50 \log (M) \]
Comparison Curve due to Oversampling

\[ M = \frac{f_s}{f_N} = \frac{f_s}{2f_R} \]

\[ N_{\text{inc}} \] - Increase in Resolution

SNR vs. OSR (M)

SNR vs. OSR (M)

Qualitative Time Domain Analysis

Input is \( x[n] \) and the final output of the modulator is \( y[n] \). Therefore from the diagram,

\[ u[n] = x[n] - y_s[n] \]

(Error Signal is Quantized)

\[ v[n] = u[n-1] + v[n-1] \]

\[ y[n] = v[n] + e[n] \]

\[ e[n] = y[n] - v[n] \]

\[ y[n] = \begin{cases} 1 & v[n] \geq 0 \\ -1 & v[n] < 0 \end{cases} \]
Behavioral Modeling of ΔΣ Modulator

Simulink Discrete Frequency Domain Model

Output of the Second Order Modulator

Behavioral Modeling of ΔΣ Modulator

Frequency Spectrum of the Output
Target Specifications of the $\Delta\Sigma$ Modulator

- Resolution, 14 bits
- Dynamic range, 70 dB
- Baseband signal bandwidth, 25 kHz
- Oversampling ratio, 256
- Sampling frequency, 12.8 MHz
- Power dissipation, less than 20 mW
- Full scale input range, ±1 V
- Power Supply, 3.3 V
- TSMC 0.35 µm process
- Voice Based Applications

Circuit Implementation

Second Order Modulator
**Discrete Time - SC Integrator**

Parasitic Insensitive Switched Capacitor Discrete-Time Integrator using Bottom Plate Sampling to minimize charge injection

<table>
<thead>
<tr>
<th>$C_s$</th>
<th>0.45pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_i$</td>
<td>2pF</td>
</tr>
</tbody>
</table>

Clocking Sequence

**Switches**

- NMOS Switch - High On-Resistance ($R_{on}$) at $V_{in}$ values close to $V_{DD}$
- TG Switch - Low On-Resistance ($R_{on}$) but need complementary clocks to function
- On-Resistance ($R_{on}$) of a switch can be modeled as Thermal Noise source in Noise Analysis.
- This project implements the modulator using both the switches to validate this theory

Transmission Gate (TG) Switch
**Op Amp Specifications**

\[
A_{CL} = \frac{A}{1 + \beta A}
\]

\[
\omega_{3dB_{CL}} = \frac{1}{\beta \omega_i}
\]

One Phase of the SC circuit

\[
V_{out} = V_F \left[ 1 - e^{-\frac{T_s}{\tau}} \right]
\]

\[
\frac{V_F - V_{out(T_s/2)}}{V_F} = e^{-\frac{T_s}{\tau}}
\]

Error < \frac{1}{2} \cdot \frac{V_{REF}}{2^N}

For \( V_{REF} = 2 \) V, \( N = 14 \) and \( f_s = 12.8 \) MHz

\[ \tau < 4 \text{ ns} \]

\[ \frac{1}{\beta \omega_i} < 4 \text{ ns} \]

If \( \beta = \frac{C_f}{C_s + C_f} = 0.82 \)

\( \omega_i > 48 \) MHz

In practice, \( \omega_i \approx 8 \times f_s \)

In this design \( \omega_i > 120 \) MHz

Step Response of the SC circuit when Linear Settling

Step Response of the SC circuit when in Slew Rate Limiting Mode

\[ SR = \frac{0.5 V_F}{T_s/10} \]

\[ SR = 211 \text{ V/µs} \]

In this design \( SR = 200 \) V/µs
Fully Differential Folded Cascode OTA

Wide Swing Bias Circuit

Design Summary
- Current 400 µA
- Swing 2.5 V
- Gain 60 dB
**Common Mode Feedback Circuit**

- $C_c$ accumulates the output DC potential
- When Clk2 is high, $C_c$ accumulates the common mode voltage
- When Clk1, charge redistribution takes place to pin the output of the cascode to common mode voltage

**Latched Comparator**

- If Clk is high and M1-M4 then $V_{cc-}$ begins to lower and turns on M9
- $V_{cc-}$ charges to $V_{DD}$ and turning on M2
- Therefore, setting $V_{cc-}$ high and $V_{c}$ low
- If Clk is low, M7 and M10 are on, latch is disconnected, $V_{cc}$ and $V_{c}$ are grounded
**Non Overlapping Clock Phase Generator**

Cascaded Inverters cause Delay

Clocking Sequence

**Op Amp Results**

<table>
<thead>
<tr>
<th></th>
<th>Target Specifications</th>
<th>Op Amp using TG switches in the CMFB circuit</th>
<th>Op Amp using NMOS switches in the CMFB circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open Loop Gain</td>
<td>60dB</td>
<td>58 dB</td>
<td>58 dB</td>
</tr>
<tr>
<td>UGBW</td>
<td>120 MHz</td>
<td>137.2 MHz</td>
<td>140 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>60°</td>
<td>72°</td>
<td>72.5°</td>
</tr>
<tr>
<td>Swing</td>
<td>2.5 V</td>
<td>2 V</td>
<td>2 V</td>
</tr>
<tr>
<td>ICMR</td>
<td>-</td>
<td>-0.6 V - 2.2 V</td>
<td>-0.6 V - 2.2 V</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>200 V/μs</td>
<td>130 V/μs</td>
<td>126 V/μs</td>
</tr>
</tbody>
</table>
Comparator Results

Clock Generator Results
\( \Delta \Sigma \) Modulator using TG switches

Output of the Second Order Modulator

\( \Delta \Sigma \) Modulator using TG switches

Frequency spectrum of the differential output signal of the \( \Delta \Sigma \) modulator

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>87 dB</td>
</tr>
<tr>
<td>SNDR</td>
<td>82 dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>85 dB</td>
</tr>
<tr>
<td>THD</td>
<td>7.05 x 10^{-7} %</td>
</tr>
</tbody>
</table>
\( \Delta \Sigma \) Modulator using TG switches

Plot of output SNR vs. Input Range showing a dynamic range of 80dB

\( \Delta \Sigma \) Modulator using NMOS switches

Output of the Second Order Modulator
\[\Delta \Sigma \text{ Modulator using NMOS switches}\]

Frequency spectrum of the differential output signal of the \(\Delta \Sigma\) modulator

\[
\begin{array}{c|c|c|c|c}
\text{SNR} & 85 \text{ dB} \\
\text{SNDR} & 74 \text{ dB} \\
\text{SFDR} & 75 \text{ dB} \\
\text{THD} & 3.85 \times 10^{-6}\% \\
\end{array}
\]

\[\Delta \Sigma \text{ Modulator using NMOS switches}\]

Plot of output SNR vs. Input Range showing a dynamic range of 70dB
Comparison Summary

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Target Specifications</th>
<th>∆Σ Modulator with TG switches</th>
<th>∆Σ Modulator with NMOS switches</th>
<th>∆Σ Modulator by Boser et al* measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Order</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Resolution</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14.5</td>
</tr>
<tr>
<td>SNR</td>
<td>86 dB</td>
<td>87 dB</td>
<td>85 dB</td>
<td>89 dB</td>
</tr>
<tr>
<td>SNDR</td>
<td>86 dB</td>
<td>82 dB</td>
<td>74 dB</td>
<td>-</td>
</tr>
<tr>
<td>SFDR</td>
<td>-</td>
<td>83 dB</td>
<td>75 dB</td>
<td>-</td>
</tr>
<tr>
<td>THD</td>
<td>-</td>
<td>7.05 x 10^-7 %</td>
<td>3.85 x 10^-6 %</td>
<td>-</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>70 dB</td>
<td>80 dB</td>
<td>70 dB</td>
<td>89 dB</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>25 kHz</td>
<td>25 kHz</td>
<td>25 kHz</td>
<td>8 kHz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>&lt; 20 mV</td>
<td>6.6 mW</td>
<td>6.6 mW</td>
<td>12 mW</td>
</tr>
<tr>
<td>Speed</td>
<td>12.8 MHz</td>
<td>12.8 MHz</td>
<td>12.8 MHz</td>
<td>4 MHz</td>
</tr>
<tr>
<td>Power Supply</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>5 V</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>3 µm</td>
</tr>
</tbody>
</table>


Comparison Summary of Corner Analysis

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Corner 1 (TT) VDD = 3.6 V Temperature 120ºC</th>
<th>Corner 2 (TT) VDD = 3.6 V Temperature 120ºC</th>
<th>Corner 3 (TT) VDD = 3.6 V Temperature 0ºC</th>
<th>Corner 4 (FF) VDD = 3.6 V Temperature 0ºC</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>92 dB</td>
<td>76 dB</td>
<td>87 dB</td>
<td>82 dB</td>
</tr>
<tr>
<td>SNDR</td>
<td>76 dB</td>
<td>75 dB</td>
<td>85 dB</td>
<td>64 dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>75 dB</td>
<td>72 dB</td>
<td>81 dB</td>
<td>74 dB</td>
</tr>
<tr>
<td>THD</td>
<td>2.46 x 10^-7 %</td>
<td>1.91 x 10^-7 %</td>
<td>3.47 x 10^-7 %</td>
<td>4.2 x 10^-4 %</td>
</tr>
<tr>
<td>SNR</td>
<td>108 dB</td>
<td>46 dB</td>
<td>85 dB</td>
<td>82 dB</td>
</tr>
<tr>
<td>SNDR</td>
<td>46 dB</td>
<td>52 dB</td>
<td>85 dB</td>
<td>64 dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>46 dB</td>
<td>53 dB</td>
<td>81 dB</td>
<td>78 dB</td>
</tr>
<tr>
<td>THD</td>
<td>0.0027 %</td>
<td>0.0006 %</td>
<td>5 x 10^-4 %</td>
<td>1.7 x 10^-4 %</td>
</tr>
</tbody>
</table>
Conclusion

- 14-bit modulator realized from a 1-bit quantizer
- Fully Differential architectures have a better noise immunity
- Techniques like Oversampling, Noise Shaping result in increased resolution
- TG switches work better than NMOS
- Slow process corner and lower $V_{dd}$ result in higher harmonic distortion

Future Work

- Design Optimization for better resolution
  - Gain Boost the Op Amp
  - Multi-bit quantizer and feedback DAC
  - Use of Dithering Technique
- Complete the ADC, by designing a Decimation Filter
- Band gap Reference Circuit for the $V_{REF}$