Optical and Mechanical Investigation of InAs /GaAs Quantum Dots Solar Cells and InAs Nanowires for the Application of Photovoltaic Device

Yushuai Dai

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Optical and Mechanical Investigation of InAs/GaAs Quantum Dots Solar Cells and InAs Nanowires for the Application of Photovoltaic Device

by

Yushuai Dai

A Thesis Submitted
In Partial Fulfillment
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In
Material Science and Engineering

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Optical and Mechanical Investigation of InAs/GaAs Quantum Dots solar cells and InAs Nanowires for the Application of Photovoltaic Device

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Yushuai Dai
Dedication

To my family
Acknowledgements

I have hesitated in writing these acknowledgements, for the difficulty in adequately expressing what should be said and inevitability of forgetting someone or some contribution. I must apologize in advance then, for anyone I have left out. You are not forgotten, merely out of mind for a short moment.

First I would like to thank my advisor Dr. Seth Hubbard for his tireless dedication, insight and eternal optimism. He offered me a chance to work in Nano Power Research Laboratory with exciting environment to conduct research, providing supportive atmosphere among the students and various collaborators. And it is an honor for me to be continuing under his advisement as I work towards a PhD.

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Abstract

In this thesis, in order to enhance understanding of the short circuit current improvement in InAs/GaAs quantum dots solar cells (QDSC), the mechanisms of carrier escape by thermal activation and tunneling from InAs quantum dots (QDs) confined in InAs/GaAs QDSCs are investigated. The significance of thermal escape and direct tunneling effects with regard to QDSC carrier escape were first theoretically analyzed. Experiment data from spectroscopy measurements were also examined to show established trends under different temperatures and bias voltages. The fitted activation energy of electrons from temperature dependent photoluminescence (TDPL) is 114 meV, which is close to the energy difference (120 meV) between the ground state and first excited state inside QDs instead of conduction band off-set (210 meV) from theory. With this fitted activation energy, the calculated thermal escape time and the tunneling time of electrons from the ground state of the QDs are $10^{-12}$ seconds and $10^{-6}$ seconds at 300K, respectively. These results indicate that at room temperature thermal escape is the dominant for electrons escape from ground state. At low temperature (8K), tunneling mainly affect the electrons escape from ground state, since thermal energy cannot support electrons to overcome the fitted activation energy (barrier, 114 meV). Temperature dependent EQE shows that carrier escape from the ground state of QDs relies on thermal activation. Bias dependent EQE measurements shows the strength of electric field had a dramatic effect on the carrier escape from deeper confinement in QDs and strongly suggested that most carriers from wetting layer can be collected at zero bias through tunneling.
In addition, in order to describe the new physics and successfully NW devices for photovoltaic applications, the first step is to obtain high-quality semiconductor nanowires on the selected substrates. Morphological characterizations were performed on both InAs NW sample grown with and without Au seeds on GaAs substrate via SEM. From SEM results, NW growth direction mainly depends on the substrate. NWs can grow with Au seed on (111)B GaAs substrate with a large base and narrow tip in the growth direction that normal to the substrate. Surface preparation greatly affects NWs density InAs NW uniformity is initially related to the Au seed coverage. A deionized water rinse after spin coating a gold solution will help the gold form a less congregated and result in better uniformity, and finally leads to a higher density of NWs. Increasing the V/III ratio from 6.5 to 38.8 causes better indium diffusion in growth direction and lowers aspect ratio (length/bottom width) from 38.93 to 12.00. However, higher V/III ratio also changes the direction of lowest free energy change, and then kinks were observed at V/III ratio at 38.8. Increasing temperature slightly decreases in aspect ratio, but accelerates the growth rate in both axial and radial directions. On the other hand, NWs grown using a pattern mask but no Au seeds, show no tapering along the growth direction but a smaller average diameter in 26 nm. The structure properties were analyzed using TEM. From TEM measurements, it was observed that all defects stop in the buffer layer when InAs NWs grown with Au seeds. On the other hand, InAs NWs grown via DBC nano-patterning showed no tapering but a mixture of ZB and WZ crystal phases along the growth directions. Finally, in order to achieve PL response between 1000~1300 nm, modeling indicates that the diameter of InAs NW should be further reduced to 3~6 nm.
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Chapter 1

Introduction

The concept of converting light to electricity was first introduced with the discovery of the photovoltaic (PV) effect by Edmond Becquerel in 1839 [1]. Since the sun is the most plentiful source for renewable energy, solar photovoltaic energy conversion is used today for both space and terrestrial power. The importance of solar cells in space applications is well known because PV is the only feasible method of generating power in space at sub-Jupiter solar distance [2]. On earth, solar cells have a myriad of applications varying from supplementing the power grid to powering road lights. To best harness the power of the sun, efficient and cost-effective solar PV energy conversion is required.

1.1 Current technologies for harnessing the power of the sun

As can be seen in Figure 1.1, current state-of-the-art solar cell technologies can be generally divided into four categories. They include III-V-type semiconductor solar cells, crystalline Si solar cell, and thin-film technologies and emerging PV technologies. Emerging PV technologies, such as organic cell and dye-sensitized solar cell, have aroused considerable interest as a promising low-cost photovoltaic. However, they have suffered from several shortcomings
including low electron mobility, environmental degradation [3]. These disadvantages lead to low efficiencies (less than 12%). The most prevalent material for solar cell applications is still Si, because it is inexpensive and abundant. Unfortunately, Si has an indirect band gap, which translates to low absorption up to the band edge. Thin film technology can reduce the cost of solar power by using inexpensive substrates. However, the resulting short optical path length and minority carrier diffusion length necessitates either a high absorption coefficient or excellent light trapping [4].

High quality single crystalline III-V semiconductor materials made by epitaxial deposition enable the development of high performance III-V photovoltaics. For example, GaAs, one of the earliest III-V materials with direct band gap to be developed was preferable over Si. Not only can GaAs devices be significantly thinner, they also exhibited increased radiation tolerance [2]. As shown in Figure1.1, single crystal GaAs cells have an advantage over Si cells in efficiency (29.1% achieved by FhG-ISE under 117-sun condition in 2011). Additionally, it had long been realized that the high-efficiency structure of III-V multi-junction solar cells (MJSC) makes them highly attractive for cost-effective terrestrial concentrator systems, if designed for the terrestrial solar spectrum and the high current densities under concentration [5]. In fact, seen in Figure1.1, III–V multi-junction concentrator solar cells are also the technology for which the efficiency is growing most rapidly. A current world record efficiency of 43.5% was achieved with III-V MJSC under concentration. Such high efficiencies (>40%) reduce the cost of power generation. Improving the efficiency of III-V solar cells is a goal for both space and terrestrial research communities.
Since semiconductors are the basis for the solar cells, there has been much focus on pn-junction devices. As shown in Figure 1.2, for a single junction solar cell (SJSC), the excess energy of photons absorbed with energies greater than semiconductor bandgap is lost as heat (also known as thermalization); photons with energy less than semiconductor band gap are not absorbed, so energy is lost to transmission. A theoretical SJSC maximum efficiency of 31% under unconcentrated sunlight was calculated by Shockley and Queisser in 1961 using detailed balance [6].
Figure 1.2 Visualization of heat loss and transmission in solar cell

Compared to SJSC, MJSC can allow the efficiency of cell beyond the Shockley and Queisser theoretical limit for a single junction device, by combining the absorption and conversion from sub-cells with different bandgaps. As a result, a broader section of the solar spectrum can be used in MJSC than in SJSC, reducing energy lost to both transmission and thermalization. Making a crystalline III–V MJSC begins with discrete layers of crystalline semiconductor epitaxially deposited onto the substrate. Cells with wider bandgaps are grown epitaxially on top of one another with connecting tunnel junction in between. It is the electrical equivalent of many individual cells connected in series. To provide efficient operation and low defect densities, each of the subsequent layers of the device are grown lattice matched to the previous layer. Figure 1.3 shows the available band gaps and lattice constants for some selected III-V elements and their alloys.
Figure 1.3 The crystal grower’s chart show available band-gaps Vs. lattice constant for III-V material with a dashed arrow indicating a lattice matched triple junction solar cell on Ge [7].

The top p–n junction has the highest band gap energy and collects light from the shortest wavelengths in the solar spectrum. Photons with energy lower than the band gap are transmitted to the next junction, and photons with energy lower than this threshold traverse to the lowest junction in the stack. Since the SJSC is fundamentally a diode, MJSCs are multiple diodes in series and therefore the total current output depends on the current limiting junction. In a typical, triple junction solar cell (TJSC), the middle junction usually limits current output due to its limited absorption. Recent progress in nanostructured solar cells has provided an opportunity to current-match the middle cell in a standard upright TJSC [8][9][10]. The focus of this thesis is on optical and mechanical investigations of quantum dots and nanowires for application in III-V solar cells.

In order to improve the conversion efficiency of both SJSC and MJSC, several approaches have been proposed and are under active investigation. These approaches include extracting hot
carriers from the photo-converter before they cool (hot carrier solar cells) [11][12], producing multiple electron–hole pairs (EHP) per photon excitation (multiple-exciton-generation cells) [13][14], and capturing and using photons with energies less than the band gap energy (intermediated band solar cells) [14] and so on. These approaches can be realized by embedding nanostructures such as quantum well [15], quantum dots [16] and nanowire [17] in SJSCs. The breakthroughs in a nano-materials approach to semiconductor device are based on the fact that electrical and optical properties of these materials can be controlled by changing their size. The use of nanostructures in PV devices offers the potential for high efficiency by either using new physical mechanisms or by allowing solar cells which have efficiencies close to their theoretical maximum.

1.2 Quantum Confinement

As mentioned above, nanostructures can be used to tune the band gap through quantum confinement. Semiconductor quantum confinement was experimentally demonstrated almost 50 years ago in layer-like nano-crystals of MoS$_2$ [18] and shortly thereafter in similarly shaped GaAs quantum wells [19]. Quantum confinement (quantum size effects) refers to the fact that carriers (electrons and holes) are confined by potential barriers in small region of space where the dimensions of the confinement are less than the de Broglie wavelength of these charge carriers. The length scale below which strong quantization effects begin to occur ranges from 5nm to 25nm for typical semiconductors (Groups IV, III-V, II-VI) [20].

In general, it is the physical confinement of charge carriers that lead to the creation of discrete energy levels. In the simplest case, these discrete energy levels can be calculated by solving the Schrodinger equation with infinite barrier at one-dimensional confinement. Certain other shape
of higher dimensional confinement can also be treated theatrically. In regions of zero potential, the Schrodinger equation is

\[-\frac{\hbar^2}{2m} \nabla^2 \psi = E\psi\]  \hspace{1cm} (1)

Where \(\psi\) are solutions to the wavefunctions of the electron, \(\hbar\) is Planck constant, \(m^*\) is effective mass of electron, and \(E\) is energy level given by

\[E = \frac{\hbar^2}{2m} k^2\]  \hspace{1cm} (2)

The magnitude, \(k\), of the wavevector is related to the wavelength, \(\lambda\), by \(k=2\pi/\lambda\). Reduced dimensionality leads to the a change in density of energy states (DOS), which refers to the number of quantum states per unit energy [21]. Integrating the DOS of the quantum states over a range of energy will produce a number of states in that energy range, so DOS affects the electrical transport properties and optical properties of nanostructures [22][23].

Figure 1.4 depicts the DOS in the conduction band for materials with various dimensionalities of quantum confinement. In bulk materials charge carriers are continuously distributed to higher energy states, while size quantization leads to an increase of the DOS near the sub-band edge in QWs. With further reducing dimensionalities, for NWs, injected charge carriers concentrate in an increasingly narrow energy range near the sub-band edge. In QDs carriers (electrons and holes) are confined in three-dimensions, allowing zero dimensions (0D) in their degrees of freedom, and creating atom-like levels with discrete (Dirac delta) densities of states. Furthermore, with the same dimensionality, both energy levels and related DOS are also affected by the shape of nanostructure. For example, the energy levels of ideal cubic shape QD can be simply calculated


from the famous quantum mechanical model of the particle-in-a-box problem, while in a pyramidal InAs QD, due to the overlap of electron and hole wave-functions, the energy level calculation is based the multiband $k \cdot p$ Hamiltonian [24].

![Figure 1.4 Schematic showing structure and density of states (D (E)) in the conduction band (CB) and valance band for (a) bulk, (b) quantum well, (c) quantum Wire, and (d) quantum dot heterostructures.](image)

1.3 **Quantum dot solar cells**

For photovoltaic applications, there are generally two broad classes of QDSCs: (1) inorganic colloidal quantum dots (usually CdSe quantum dots) through chemical synthesized in an organic host matrix and (2) epitaxial or vapor phase grown crystalline QDs (group III-V materials) [20]. The focus of this work is on the performance of the second type of QDSC because improving efficiency of III-V solar cells is a goal for both space and terrestrial research communities.
There have been numerous reported methods to grow epitaxial III-V quantum dots. Two such methods are electron-beam lithography [25] and self-assembled [7]. In this study, the self-assembled QDs are epitaxially grown by Metal Organic Vapor Phase Epitaxy (MOVPE), also called Metal organic chemical vapor deposition (MOCVD), using the strain-induced Stranski-Krastanov (SK) process, which happens naturally in the initial stages of growth for lattice-mismatched materials. In this study, the compressive strain of InAs on a GaAs substrate (7.8%) is used to drive a volumetric strain relaxation. The growth starts layer by layer, forming a 2-dimensional (2D) wetting layer (WL), and after a certain critical thickness is reached, the structure spontaneously forms nanometer-sized islands, giving strained, but coherent, quantum dot structures. Due to the nature of the elastic strain relaxation process in SK growth, the QD nucleation, growth, and uniformity are quite sensitive to the growth parameters (e.g. growth temperature, growth rate and V/III ratio) as well as the preparation of the substrate (e.g. surface orientation and vicinal off-cut) [16][26]. An example of optimized growth conditions for lens-shaped InAs quantum dots on GaAs can be seen in Figure 1.5, which shows size uniformity, 2.5 nm in average height and 14 nm in diameter, and large surface densities (6.7×10^{10} cm^-2) of quantum dots. Further QD growth details have been discussed elsewhere [16] and will be covered in the next chapter.
As mentioned above, QDs are manmade nano-scale structure in which electrons can be confined in all three dimensions, which is achieved by having a very small volume of a low band gap material embedded in larger band gap material, thus creating the potential barrier for quantum confinement of the carriers. Because of quantum confinement, multiple energy subbands are formed inside QDs region.

QD superlattices have been proposed as a means to realize band engineering of TJSC. Semiconductor material with embedded QDs can harness the photons with energy lower than the host band gap that are normally lost to transmission due to sub-band absorption in the QDs and its wetting layer, so more electron-hole-pairs (EHP) can be generated with photon energy below the bandgap of the bulk material. An overall 47% efficiency is predicted using detailed balance under one sun AM0 illumination [8]. This high efficiency is achieved by bandgap engineering to increase the overall current in a TJSC. Bandgap engineering refers to one of the QD applications proposed by Raffaelle et al. [7]. By changing the QD width, spacing of the QDs layers (i.e. the
thickness of the barriers between the QD layers), and the composition of the QD and/or barrier material, one can effectively tune the band gap without changing the junction material and thus introducing fewer defects caused by strain.

InAs/GaAs quantum dots are also a research material that could be used for the intermediate band solar cells (IBSC) proposed by Luque and Marti [27], which has a maximum efficiency over 60% at 1000 suns concentration under AM1.5 illumination [28]. It is required to closely space a quantum dot superlattice to force individual wave functions to begin to overlap and then form a continuum “miniband.” Nonradiative recombination into the intermediate band is suppressed due to the continuous nature of the impurity band and a detail balance analysis can be applied. Figure 1.6 presents the standard single-junction solar cell absorption ($E_{cv}$). The intermediate band formed as above provides two additional absorption pathways, $E_{iv}$ and $E_{ic}$. The electronic states in the intermediate band should only be accessible via direct transitions. Absorption of photon energy, $E_{iv}$ will pump an electron from the valence band to the intermediate band. A subsequent photon of energy, $E_{ic}$ then pumps an electron from the intermediate band to the conduction band. The increased performance of this design is by reducing transmission loss and spectrum splitting (reduced thermal loss). Current is extracted from the intermediate band only by optical pumping.
Figure 1.6 Simplified band diagram of an IBSC

Figure 1.7 shows an example of devices with embedded QDs. A graph of in external quantum efficiency (EQE), which measures the number of electrons or holes collected as photocurrent per incident photon at a particular wavelength vs. wavelength. As can be seen, the EQE for a baseline cell without QDs is enhanced with embedded 10-40 layers of QDs at room temperature. Both QD cells show an increased response at wavelength greater than the GaAs band edge (~880 nm at 300K), which indicates that a portion of short-circuit current of these cells is generated by QD-related absorption process.
Figure 1.7 10 and 40 layer QD-enhanced solar cells show a net increase in external quantum efficiency (EQE) at IR wavelengths as compared to the baseline GaAs.

Once electrons and holes are excited into QD states by photon energy lower than the bandgap of bulk material, they have to overcome the confining potential barrier prior to collection. There are three basic physical mechanisms that contribute to carrier escape: thermal activation, tunneling, and light assisted activation. In order for the light assisted activation to be efficient, the QDs must be either half filled with electrons [29] or operated under sufficient concentration to optically pump the IB [30], which is a challenge for current growth technique, so the two photons process may limited [31][32] by the $E_{ib} - E_{cb}$ transition. Currently, thermal activation and tunneling are considered the two main mechanisms of carrier escape for most devices [33][34]. However, the detailed model of tunneling process in quantum dots is still unclear. Understanding the mechanism of carrier escape from the QD confinement is important not only on fundamental grounds but also for the realization of reducing recombination, and thus enhance photocurrent.
One of the most important factors determining the carrier escape process is the quantum confinement depth of the carriers with respect to the GaAs band edge. In chapter 2 of this thesis, the depth of electron escape from ground state was used as the activation energy extracted from temperature dependent photoluminescence. With the fitted activation energy, the escape times of electrons from ground state were calculated via a thermal activation and tunneling model. The mechanisms for carrier escape are also discussed. Temperature and bias dependent external quantum efficiency measurements were used to experimentally investigate the mechanisms of carrier escape.

1.4 Nanowires Solar cell

Nanowires are under intense research for the next generation of electronics, photonics, sensors and energy applications. As one-dimensional nanostructures, nanowires offer opportunities to control the density of states of semiconductors, and in turn, their electronic and optical properties. Furthermore, strain is a fundamental issue in semiconductor heterostructures. It limits the design of conventional bulk and quantum well system. In planar epitaxial growth, a thin film with lattice constant $a_f$, grown on a thick, single crystalline and large area substrate with lattice constant $a_s$, deforms tetragonally in response to interfacial strain from lattice mismatch.

$$f = \frac{a_s - a_f}{a_s} = \frac{\Delta a}{a_s}$$

As the film is much thinner than the substrate, the majority of this strain is elastically accommodated by the film. With increasing film thickness, volume strain energy accumulates until surface roughening, island formation, or dislocations begin to reduce this energy to relax the strain. The equilibrium critical thickness for dislocation formation is defined as the thickness
when the volume strain energy equals the energy of an interfacial edge dislocation, or misfit dislocation. A large lattice mismatch results in poor-quality interfaces with high misfit dislocation density; these dislocations influence the electrical behavior in several ways. For instance, they are preferred sites for impurity atoms, high-diffusivity paths for dopants and nonradiative recombination centers.

Compared to quantum dots and quantum well, the beauty of NWs is they allow the growth of axial heterostructures without the constraints of lattice mismatch. This provides flexibility to create heterostructures of a broad range of materials and allows integration of compound semiconductor based optoelectronic devices with silicon-based microelectronics. In heterostructural NWs, based on different junctions formed by NWs, there are generally three types of NW as shown in Figure 1.8. These are radial-junction NW, axial-junction NW and substrate-junction NW. Either axial or radial dimensions are finite, but size is effectively infinite along the wire growth direction. The small diameter/height aspect ratio is expected to favor volume elastic strain relaxation by their elastic boundary conditions, making them virtually free of dislocations. This is consistent with their excellent optical properties [35][36]. When diameters of nanowires are below a critical value (20 nm) [37], the volume strain energy is too small for dislocations [17].
Figure 1.8 Structure of three different junction of NWs. (a) Radial junction, (b) Axial junction, (c) substrate junction.

For energy applications in the field of PV, the NW geometry provides potential advantages over planar wafer based or thin film solar cells in every step of photo-conversion process. In general, the NWs provides potential advantages including increased defect tolerance, reduced reflection, better light trapping, and improved band gap tuning. Firstly, light absorption is critical for efficient energy conversion in PV devices. It was demonstrated by Garnett et al. [17] that ordered arrays of silicon NWs increase the path length of incident solar radiation by up to a factor of 73, which is above the randomized scattering (Lambertian) limit ($2n^2\sim25$ without a back reflector) [4].

Secondly, because p/n junctions in NW solar cells can be formed in radial or axial directions, these unique geometric properties of NW structures enhance charge generation and facilitate the transportation of carriers. For example, in core-shell structures, the geometry of the vertical NW array separates the pathways of incident photon absorption (along the axial direction) and charge separation by the built-in electric field (along the radial direction) [38]. Additionally, in heterostructures, effective masses of electrons and holes vary between materials, which give rise
to a quasi-electric field for electrons or holes. The charge separation scheme in these staggered
band core-shell NW solar cell suppress the intrinsic recombination at the junction without need
for additional doping processes [39].

Thirdly, charge collection is plagued by recombination, which can occur at the surface, interface,
and at bulk defects. Though surface recombination remains a major challenge in the case of NW
solar cell, because of the inherently large surface-to-volume ratio, proper device design and
fabrication can solve this issue. On the other hand, the dye sensitized solar cells (DSSCs) are
considered for inexpensive, large scale solar energy conversion. In DSSCs, the NW morphology
provides direct conduction paths for the electrons from the point of injection to the collection
electrode while maintaining high surface area for the dye adsorption [40][41]. Additionally, the
quantum confinement in the NW will decrease the average band gap of the semiconductor
material. As a result, photons with energy below the band gap can be absorbed to generate
electron and hole pairs.

1.4.1 Growth of III-V Nanowire

To describe the new physics and successfully grown nanowire device for the photovoltaic
applications, the first step toward the goal is to obtain high-quality semiconductor nanowires on
the selected substrate. Various techniques were developed to achieve this. Generally, there are
two techniques commonly used in the growth of NW solar cells: patterned chemical etching and
chemical vapor deposition. Patterned chemical etching is a top-down or hybrid top-down/
bottom-up approach that involves a lithographic step after an etch step. On the other hand,
chemical vapor deposition (CVD) in III-V NW bottom-up growth. The CVD technique relies on
volatile metal-organic compounds, such as trimethylgallium (TMGa) or trimethylindium (TMIn),
which act as precursors for the semiconductor material. The materials grown contain some combination of gallium, indium, aluminum, nitrogen, phosphorus or arsenic.

As is known, MOCVD technology is most commonly used to grow materials for high brightness light-emitting diodes (LEDs) and high-efficiency solar cells. This is due to MOVPE having an advantage in high capacity reactors, fast growth rate, and low down time during maintenance. In addition, a number of growth parameters can be tailored to achieve optimum NW quality including the ratio of group V to III precursor flow rates (V/III ratio), and growth temperature. Figure 1.9 shows the schematic of the process inside the chamber. The substrate is placed in the deposition zone of the furnace, where it is heated for chemical thin-film deposition. Nanowires are synthesized by flowing chemical precursor vapors into the hot zone of a furnace. Then the precursor vapors react on a substrate, often with the assistance of a metal catalyst nano-particle (Au, Ag, etc.). The vapor source can be a gas, liquid or heated solid. The precursor vapors are transported to the substrate with an inert carrier gas often combined with other reactant gases along the way.

![Figure 1.9](image)

Figure 1.9 (a) Schematic of the process inside the chamber (b) Veeco D125LDM system located at NASA Glenn Research Center in Cleveland, OH.
In this study, because of its very large electron mobility and small band gap, InAs nanowires were grown via a vapor-liquid-solid (VLS) mechanism. As is known, the direction of a phase transition is related to reducing the energy of the system. If two phases, V and L, are not in equilibrium, difference between the chemical potentials (µ) of the two phases is the driving energy towards equilibrium.

\[ \Delta \mu = \mu_V - \mu_L \]  

(4)

The difference \( \Delta \mu \) is called super-saturation [42] and at equilibrium \( \Delta \mu = 0 \). The chemical potential of a phase \( V, \mu_V \), is determined by the Gibbs free energy, \( G \), if adding a small amount of material, \( n \), to phase \( V \) at constant pressure \( P \) and temperature \( T \):

\[ \mu_V \equiv \left( \frac{dG}{dn} \right)_{P,T} \]  

(5)

During NW growth process, the most commonly cited method is the vapor-liquid-solid (VLS) mechanism, which uses a metal catalyst that forms a liquid eutectic with the desired NW material. This mechanism was first demonstrated by Wagner and Ellis when creating such 1D structure via CVD growth in 1964 [43]. As shown in Figure 1.10, metal (Au) is deposited onto the surface of a single crystalline semiconductor by evaporation by sputtering or in colloid form.

In the VLS growth mechanism of semiconductor NWs, the reactants are supplied in the vapor phase, and the diameters of the wires are dictated by the size of the metallic seed particles. The VLS mechanism implies that the solid wire is formed by precipitation from a droplet of metal alloyed by the constituents of the growing material, with a melting-point depression due to the formation of a eutectic melt. The driving force for crystallization is super-saturation within the droplet, which is established by catalytic absorption of the gaseous reactants from the surroundings. The additional flux of dissolved species leads to further precipitation and NW
growth. With the proper substrate precursor, temperature, catalyst, and concentration, vertical NW growth is possible.

Figure 1.10 Gold (Au)-assisted growth of III–V compound-semiconductor NWs. (a) Au NPs are deposited onto the substrate. (b) They are ideal sinks for the group III species supplied from vapor and form an Au-group III alloy. (c) III–V material is deposited preferentially at the nanoparticle-substrate interface. (d) Adsorption and diffusion of reaction species contributing to further NW growth.

According to the literature, InAs NWs are usually grown in a temperature range from 350°C to 600°C [44][45][46]. In fact, solid solubility of As in Au is very low, less than 1% [47][44], but melting of an Au-In alloy may increase the As solubility because As is highly soluble in both liquid Au and liquid In [44]. As seen in Figure 1.11, the Au-In phase diagram shows that eutectic temperature for some phases is at a low-temperature (below 500°C). This allows growth from liquid Au–In in a wide concentration region as long as the growth process can be performed with a small Arsenide content in the liquid droplet. For example, solid phases ε/ε' with 24.5-25.0%
Indium, and \( \gamma/\gamma' \) with 28.8-31.5% Indium, both melt at approximately 490°C. Upon cooling and re-solidifying, the particle may then form the phase \( \psi \) with 35.4-39.5% Indium, which melts around 460°C. Furthermore, the small scale of the alloyed Au NPs makes them subject to size-dependent melting effects, according to the Gibbs–Thomson relation [48]. Therefore, the melting point of the alloy NPs may be depressed relative to the bulk melting point, so eutectic melting may occur at a lower temperature than the bulk phase diagrams predict.

![Calculated Au-In binary phase diagram](image)

Figure 1.11 Calculated Au-In binary phase diagram[49].

Although the size of these NWs can be controlled to some extent by metal nanoparticles (NP), there are still important issues to control for reproducibility of NW position, size and shape, because they determine their electrical and optical properties and capability of high density
integration. As mentioned, NW size and shape are crucial in the nano-scale regime. Even small variations in size can have a large effect on overall device performance. For instance, NW dimensions determine the degree of confinement, and consequently affect the behavior of charge carriers in quantum electronic devices. It is important to control the NW diameter, because most device applications require a well-defined uniform diameter. As a result, some efforts have been reported to control the position of the metal catalysts as well as their size by using lithographic technique [50][51].

A novel technique to grow InAs NW without gold seed using a patterned polystyrene/polymethylMethacrylate (PS/PMMA) diblock copolymer (DBC) pattern was also investigated in this work. As can be seen in Figure 1.12, a self-assembled PS/PMMA DBC mask [52] is spin-coated on top of a GaAs wafer, which consists of GaAs and a dielectric mask (typically SiN$_x$). Reactive Ion Etching (RIE) is then performed to transfer the pattern into the dielectric. After removing the DBC mask using wet etching, the wafer is put into the MOCVD reactor chamber for NW growth. Finally the dielectric mask can be removed via RIE or simply wet etching [53].
Figure 1.12 Schematic of the InAs NW growth process with diblock copolymer without gold seed in cross section view.

The morphological characterizations of the InAs NWs were studied by scanning electron microscopy (SEM) and the structural properties were investigated with transmission electron microscopy (TEM). The growth direction, size, shape and position control of InAs nanowire via both VLS mechanism and selective area growth with self-assembled diblock copolymer are reported in this thesis.

1.5 Organization of This Work

The following chapters discuss how carrier escape mechanisms affect the performance of III-V quantum dots solar cell performance and how basic growth parameter affect the InAs NW material quality. Chapter 2 focuses on thermal escape and tunneling in QDSC via simulation, temperature dependent photoluminescence (TDPL), temperature dependent spectral response (TDSR), and voltage bias spectral response. Chapter 3 presents data on characterization on InAs
NW with and without Au seed, and an analysis on the relationships between both the InAs NW growth direction and the aspect ratio (base diameter verses length) and the basic growth parameters: substrate orientation, substrate preparation, growth temperature and V/III ratio. Chapter 4 presents conclusions for both quantum dots solar cell and InAs NW studies, and finally a discussion on future work.
Chapter 2

Optical Study of Carrier Escape in InAs/GaAs Quantum Dots Solar Cell

2.1 Introduction

Self-assembled quantum dots (QDs) are under extensive study currently due to their promising applications in optoelectronic devices, such as laser [54][55] and solar cells[14]. Because QDs provide quantum confined states that lower the average band gap of the matrix material, in solar cell applications, lower photon energies than the band gap of the bulk material can be absorbed and generate carrier. Recent progress in InAs/GaAs QDs have provided opportunities to current-match the middle cell in standard upright triple junction solar cells (TJSC) [56] and realizations of intermediate band solar cells (IBSC) [57]. Compared with efficiency 31% under unconcentrated sunlight calculated by Shockley-Queisser in 1961[6], for TJSC, an overall 47% efficiency is predicted using detailed balance under one sun AM0 illumination [8]; for IBSC, a maximum efficiency of 60% is calculated under 1000 suns concentration under AM1.5 illumination[28]. TJSC can be achieved by band gap engineering with QDs to increase overall current with strain balance, while IBSC requires a closely space InAs/GaAs QD superlattice to form an optically isolated intermediate band (IB) within the band-gap of a single junction solar cell. Furthermore, this IB should be half filled with electrons. Not only for fundamental grounds
but also for the realization of enhancing photocurrent output with different applications, it is important to understand the mechanism of carrier escape from the QD confinement.

In general, once electrons and holes are excited into QD states by photon energies lower than the band-gap, then they have to overcome the confining potential barrier prior to collection. There are three potential physical mechanisms that contribute to carrier escape as shown in Figure 2.1: light assisted activation, thermal activation and tunneling effect. Photon-assisted carrier escape involves a two-photon process. The first transition is from valence band to quantum confinement and the second transition from quantum confinement level to conduction band. Both arise from photons with energies less than the bulk material band gap. However, the two photon process is negligible in this thesis based on the design of experiment. Firstly, at room temperature one sun condition, due to the shallow confinement of InAs/GaAs QDs, the thermal escape rate is at least $10^4$ times faster than the rate of optical emission according the work from Hwang et al.[58]. Secondly, the two-photon process requires QDs to be physically highly ordered and brought close enough that individual wave functions begin to overlap, thus forming a continuum “miniband” in the application of an ideal QD-IBSC. It is a challenge to grow homogeneous QDs across wafer to satisfy the request to form a “miniband”. Furthermore, due to thermal escape and tunneling, it also difficult to achieve the “miniband” with half-filled carrier concentration, so the two photons process must be limited [31][32].
A deeper insight into this dynamical processes in InAs/ GaAs quantum dot arrays has been provided using the plane-wave method [59] with periodic boundary conditions in expansion of the $k \cdot p$ Hamiltonian for the calculation of the electronic and optical properties of InAs/GaAs QD, such as density of states, absorption and etc. The assumed Hamitonian took into account the band mixing between the lower conduction band s-antibonding and top three valence-band p-bonding states, all spin degenerate, and included the strain and piezoelectric field [60][61]. However, the actual device carrier escape extraction process not only relies on QD size, shape, and distribution but also on the device structure [62] and material quality[63].

Currently, thermal activation and tunneling are considered the two main mechanisms of carrier escape from the QDs in InAs/GaAs quantum dots solar cells [33][34]. One of the most
important parameters that determines the carrier escape process is the depth of quantum confinement (barrier height), which is from electrons or holes energy levels with respect to the GaAs band edge. This thesis investigates the thermal escape and tunneling of carriers in the two champion cells in performance, which were published by Mackos et al.[64] and Bailey et al.[65], respectively. The strength of the built-in field is varied between the two cells, due to the different length of the intrinsic region (10-layer and 40-layer QDs embedded). The barrier height of the electrons in the ground state was extracted from temperature dependent photoluminescence (TDPL). With this barrier height, the electrons thermal escape time and the tunneling time were estimated using the equations derived from the quantum well structure. In order to further investigate the mechanisms of carrier escape, the photo-current of 10-layer or 40-layer QDSC under different bias voltage and temperature were experimentally compared. It is found that, at room temperature, thermal activation is dominant in electrons escape from the ground state in QDs. At low temperature (8K), tunneling becomes more important than thermal activation for electrons escape from QDs.

2.2 Theoretical Approach

As mentioned in the introduction, once an electron and hole pair are excited into a QD confined state by a photon, carriers can either recombine or escape from the QD. As shown in Figure 2.2, recombination can be either radiative recombination or non-radiative recombination, while the escape mechanisms are mainly related to thermal assisted escape from QDs or tunneling through the triangular barrier formed by a built-in electric field. Because the semiconductor-based solar cell is fundamentally a diode, the built-in field determined by the length of depletion region and
the built-in potential that based on the doping in the base and emitter of QDSC in the thermal equilibrium. This built-in potential, \( V_{bi} \), yields the equation (6) as showed below[66].

\[
V_{bi} = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}
\]  

(6)

Where \( k \) is Boltzmann constant, \( T \) is temperature, \( q \) is charge of electron, \( N_a \) is acceptor concentration, \( N_d \) is donor concentration and \( n_i \) is intrinsic carrier density. Because \( n_i^2 \) increases faster than \( N_a N_d \) with temperature[66], Equation (6) actually shows that the built-in potential decreases with temperature.

In addition, carrier exchange between the ground state and the excited state was observed by Zhou et al.[67]. It was found that carriers in ground state can be thermal excited to an excited state. On the other hand, due to Auger process [66], if one electron is initially in an excited state and hole is in its ground state, the energy transfer occurs when electron relaxes to its ground state to transfer excess energy to the hole in order to excite it into excited energy state.

![Figure 2.2 Schematic of the process taken into account in the electron dynamic model.](image)
A simple rate equation was adopted for the investigation of the process of carrier escape. The carrier loss rate in an \(n\)th quantum confined level from ground state with carrier generation rate \(G\) and carrier population \(C\) is given by:

\[
G = \left( \frac{C}{\tau_{esc}} + \frac{C}{\tau_{rec}} + \frac{C}{\tau_{exc}} \right) = C \left( \frac{1}{\tau_{tun}} + \frac{1}{\tau_{th}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{non-rad}} + \frac{1}{\tau_{exc}} \right) \tag{7}
\]

Where \(\tau_{esc}\) is escape time, \(\tau_{rec}\) is recombination time for the carrier and \(\tau_{exc}\) is carrier exchange time. The recombination time can be further divide into radiative recombination time and non-radiative recombination time, \(\tau_{rad}\) and \(\tau_{non-rad}\), respectively. According to literature, in InAs/GaAs QD, \(\tau_{rad}\) and \(\tau_{non-rad}\) are of the order of 1 ns [61] and 100 ps [68], respectively. \(\tau_{exc}\) is from 1 ps to 10 ns, varied from QD size and distribution [61], which is related to both thermal activation and the Auger process. In an Auger process, the energy from the recombination of an electron and hole is conserved by transferring energy to another electron or hole. The Auger rate can be derived under the standard time-dependent perturbation theory and using Fermi's golden rule [69]. As outlined in the introduction, the two-photon process related optical escape is negligible [58], due to its low probability of occurring in this study.

For the carrier escape process, since the quantum confinement of InAs/GaAs QDs is mainly on the growth direction (Z direction as shown in Figure 2.2), the calculations of escape rate from QDs can be simplified by modeling a quantum well structure. The thermal escape time \(\tau_{th}\) is determined primarily by the barrier height and the ambient temperature [66]. Furthermore, due to Fermi-Dirac statistics, the density of carriers decreases exponentially as a function of barrier height. Additionally because the escape of carriers from the quantum well from left to right
(along Z direction) as shown in Figure 2.2, the width of quantum well has to be considered. As a result, for QW, \( \tau_{th} \) is given by [70][71]:

\[
\frac{1}{\tau_{th}} = \frac{1}{L_z} \sqrt{\frac{kT}{2\pi m_Q}} \exp \left( -\frac{\Delta E_h}{kT} \right)
\]  \(\text{(8)}\)

Where \( m_Q \) is the carrier’s effective mass in the quantum confinement; \( L_z \) is the width of the confining structure, and \( \Delta E_h \) is the barrier height in the presence of an electric field \( F \) for the \( n_{th} \) energy sub-band.

The tunneling time \( \tau_{tun} \), the inverse of tunneling probability per unit time, is evaluated using a transfer matrix method in the effective mass approximation[72]. As is known, tunneling rates are dependent on both the height and the thickness of a barrier. For the different energy level in a QD, \( \tau_{tun} \) is given by [73][74]

\[
\frac{1}{\tau_{tun}} = \frac{1}{L_z} \frac{n\pi \hbar}{2m_b} \exp \left( -\frac{2}{\hbar} \int_0^b \sqrt{2m_b(qV(z) - E_n - qFz)} \, dz \right)
\]  \(\text{(9)}\)

Where \( m_b \) is the carrier effective mass in the barrier, \( E_n \) is the energy of the \( n \)-th energy subband measured from the center of the well, and \( q \) is electron charge. As shown in Figure 2.2, \( V(z) \) is an arbitrary potential between 0~\( \Delta E_h \) and due to the triangle shape of the barrier caused by electric field. Equation (9) shows that tunneling rate increases with the strength of the electric filed. At zero bias, the electric field is determined by the built-in voltage as outlined before. Because the built-in voltage decreases with increasing temperature, the tunneling rate also slightly decreases with increasing temperature. At low temperatures (<20K), thermal energies are too small to allow carrier escape from ground states in QDs, so tunneling is dominant in carriers escape.
Assuming all carriers that escaped from the quantum confinement can be collected, external quantum efficiency (EQE) reflects the ratio between carrier collection and photon input at each wavelength under certain conditions based on device structure, doping level, operation temperature, etc. [75]. Thus, EQE relates to the ratio of carrier escape rate and total generation rate:

\[
EQE \sim \left( \frac{1/\tau_{esc}}{1/\tau_{esc} + 1/\tau_{rec} + 1/\tau_{exc}} \right) = \left( \frac{1/\tau_{esc}}{1/\tau_{esc} + 1/\tau_{non-rad} + 1/\tau_{rad} + 1/\tau_{exc}} \right)
\]

Similarly, photoluminescence (PL) intensity is related to the carriers’ radiative recombination rate versus the other processes: non radiative recombination rate, thermal escape rate, direct tunneling rate and carrier flow into the \(n_{th}\) energy level from other energy level.

\[
I_{PL} = C \left( \frac{1/\tau_{rad}}{1/\tau_{esc} + 1/\tau_{non-rad} + 1/\tau_{rad} + 1/\tau_{exc}} \right)
\]

Thus, both EQE intensity and PL intensity change with temperature. The thermal activation energy \(E_a\) is related to the barrier height. Furthermore, from temperature dependent photoluminescence (TDPL) measurements, \(E_a\) can be fitted using an Arrhenius relationship [76].

\[
I(T) = \frac{I_0}{1 + A \exp(-\frac{E_a}{kT})}
\]

Where \(I_0\) is the PL integrated intensity at 0K, and A is non-radiative to radiative ratio[76]. At high temperature, the equation can be further simplified as below [77].

\[
I(T) = \frac{I_0}{A} \exp\left(\frac{E_a}{kT}\right)
\]
2.3 Experimental method

2.3.1 Sample Set

In this study, QW test structures (a structure without electrode) for TDPL, as well as QD embedded p-i-n solar cell structures for TDPL and EQE measurements, have been grown using a low-pressure rotating disk metal organic vapor phase epitaxy (MOVPE) reactor (Veeco D125LDM) located at NASA Glenn Research center. Standard precursors of trimethylgallium (TMGa), trimethylindium (TMIn), trimethylaluminum (TMAI) and arsine (AsH3) were used for alkyl and hydride sources, respectively. Growth temperature was monitored in-situ using emissivity corrected optical pyrometer.

The QDs were grown at 500ºC under SK growth mode with InAs coverage 1.8 mono layers (ML) on 350 µm thick Si doped GaAs (100) substrates misoriented toward the (110) direction. The misorientation angle was 2º. After growth of a low temperature GaAs capping layer, temperature was ramped to 585 ºC for growth of the GaAs spacer layers and a 4 ML GaP strain compensation layer. Correct strain-balancing is essential to growing the significant numbers of QD layers necessary for these devices, due to the strain driven nature of the SK growth mechanism of epitaxial QDs [78]. Especially for InₓGa₁₋ₓAs/GaAs QD superlattice with a large number of periods, without proper strain balancing the lattice mismatch with the substrate can result in the generation of a high density of misfit dislocations that degrades cell performance such as open circuit voltage [79]. Total repeat unit thickness is nominally 12-13 nm and the repeat periods are sandwiched between two 33-nm-thick intrinsic GaAs. The average hemisphere-shaped QDs size is 3-4 nm in height and 20-25 nm in diameter [65].
Figure 2.3a shows the structural layer layout of the investigated QDSCs. The QDSCs consisted of a base of the solar cell consisted of 350 µm of Si-doped GaAs with doping density of $10^{18}$ cm$^{-3}$, followed by a 250 nm thick n-type GaAs buffer layer. A 10-period and 40-period superlattice in the intrinsic region of the solar cells was used to form barrier to QD. The emitter consisted of 0.5 mm of Zn-doped GaAs with a doping density of $2.2 \times 10^{18}$ cm$^{-3}$. Thin (50 nm) InGaP front and back surface layers are employed to reduce surface and interface recombination. Finally, a doped GaAs layer is used to facilitate Ohmic contact formation. Solar cells were fabricated using standard III–V processing and microlithography techniques. Ohmic contacts to a thickness of 1 µm were made to the p- and n-type regions using thermally evaporated Au/Zn/Au and Au/Ge/Ni/Au metallization, respectively. As can be seen in Figure 2.3b, each wafer contained an array of 1×1 cm$^2$ solar cells with grid finger shadowing of 4%. Individual cells were isolated using wet chemical etching techniques. Anti-reflective coatings were not used in order to focus on the QD incorporation [80]. The performance of the baseline and QD cells have been discussed in detail elsewhere [65]. Measurements were performed on 1×1 cm$^2$ QE pads without grid finger on both devices.

![Figure 2.3(a)Structural layer layout for QD embedded GaAs p-i-n solar device, (b) Crystalline III-V solar cell.](image)
As mentioned in the introduction, both cells investigated are champion cells in performance. Figure 2.4 shows the J-V curves under 1-sun AM0 illuminated condition for the 10-layer p-i-n QDSC, the 40 layer p-i-n QDSCs and a baseline p-i-n GaAs solar cell without QDs. The short circuit density $J_{sc}$ of the baseline GaAs solar cell is 22.5 mA/cm$^2$. With the absorption and energy conversion from the QDs embedded region, the short-circuit density $J_{sc}$ is as high as 23.7 mA/cm$^2$ in 10-layer QDSC and 23.8 mA/cm$^2$ in 40-layer QDSC, which are correlated with the external quantum efficiencies showed in the inset. The open circuit voltages for 10-layer and 40-layer QDSC are 0.975 V and 0.990V, respectively, while the fill factors that determine the maximum power of 10-layer and 40-layer QDSCs are 81.4% and 82.3%, respectively.

Figure 2.4 Illuminated 1-sun J-V curves for 10-layer and 40-layer p-i-n QDSC. The inset is the external quantum efficiency.
The quantum well sample was used to verify the method to derive activation energy from TDPL experiment via equation (13). As can be seen in Figure 2.5a, a 7 nm In$_{0.26}$GaAs layer was buried between two 200 nm GaAs Barrier layer, due to it is difficult to grow without exceeding the Matthews and Blakeslee limit for the defect free QW. Unlike QDSC, Figure 2.4b shows that the surface of QW test structure were not coated with any metal to form electrode.

![Structural layer layout for QW embedded GaAs test structure](image)

Figure 2.5(a) Structural layer layout for QW embedded GaAs test structure (b) quantum well test structure

### 2.3.2 Photoluminescence (PL)

In order to experimentally get the barrier height for the energy state in the QD, temperature dependent PL (TDPL) experiments was performed because its intensity is less affected by tunneling. Here is a brief introduction to PL. Many materials are capable of emitting visible luminescence when subjected to some form of excitation light (i.e. photoluminescence). There are two pre-requisites for luminescence: firstly the luminescent material must have a
semiconductor structure with a nonzero band gap $E_g$; secondly energy must be imparted to this material before luminescence can take place.

The mechanism of PL in semiconductors is schematically illustrated in Figure 2.6. Photons with energy higher than the band gap energy can be absorbed and thereby excite an electron from the valence band above the band gap. This process is called photo excitation. If radiative relaxation occurs, the process light emission is called PL. The energy of emitted photon is determined by the band gap energy $E_g$, because electrons usually experience thermal relaxation to conduction band edge prior to radiative recombination. The intensity of the emitted light is related to number of carriers involved in the radiative process. Thus the emission peak energy and intensity from photoluminescence measurements are important to investigate material properties.

![Schematic band diagram for the photoluminescence processes.](image)

Figure 2.6 Schematic band diagram for the photoluminescence processes.

In addition, photoluminescence spectroscopy is considered as a contactless, nondestructive method of probing the electronic structure of material. In summary, PL measurements provide
spectral information and are useful to determine semiconductor band gap and quantum confinement, while it is also useful to probe recombination processes.

Figure 2.7 shows the set up for TDPL measurements in this study, a 514.5 nm Spectra-Physics Argon-ion laser with a power flux 37W/cm² was used as the excitation source for optical probing of the samples. The laser signal was physically modulated by a mechanical chopper at a frequency of 167 Hz then reflected by a mirror and through a focusing lens before striking the sample. A 780 nm cut-on filter was placed in front of the JY iHR 320 Monochromator to filter out diffused laser signal. The emitted PL signal was focused into a 2 mm slit of the iHR 320 monochromator (with 3 gratings at 330 nm, 750 nm, and 1500 nm blazes, respectively), which greatly reduced any background distortion, and fed the low-noise signal through a 2 mm exit slit to a thermoelectrically cooled InGaAs photodiode. The signal from the detector alternating current is measured by a Stanford Research S830 digital lock-in amplifier, which phase-locks to the chopped signal. The sample was fixed via silver paint on an Oxford probe station with input liquid nitrogen.
2.3.2 External quantum Efficiency (EQE)

In order to investigate carrier escape mechanisms, the effect of thermal activation on carrier escape was evaluated by temperature dependent EQE measurements, while the tunneling of carriers was evaluated by bias dependent EQE measurements at room temperature. As mentioned in the theoretical approach, EQE provides a spectroscopic means to study how QDs affect the device current output characteristics, which measures the number of carriers collected as photocurrent per incident photon at a particular wavelength. The intensity of EQE usually decreases at photon energies less than the semiconductor band-gap due to the transmission. Furthermore, not every generated electron-hole pair results in collection. EQE of solar cell depends on both device design and material quality, because bulk and surface recombination events and reflection loss result in lost potential current [81]. For example, Figure 1.7 in Chapter
1 shows the intensity EQE above the GaAs band-edge increases with design of increasing embedded QD layers. Willis et al. also showed defects related non-radiative recombination in QD material degrade EQE performance in QDSC [63].

However, EQE cannot be measured directly, but can be derived from spectral response (SR). Spectral response is a ratio between the current generated by the solar cell to the power incident on the solar cell, which is conceptually similar to EQE. The EQE can be determined from the SR by replacing the power of the light at a particular wavelength with the photon flux for that wavelength. This gives

\[
EQE(\lambda) = \frac{hc}{q\lambda} SR(\lambda)
\]  

(14)

where \(\lambda\) is wavelength of incident light, \(h\) is Planck constant, \(q\) is electron charge, and \(c\) is light speed.

Temperature dependent Spectral Response (TDSR) measurements were carried out on QDSC samples by an OL Series 750 Spectroradiometric Measurement System with a high intensity source attachment. Figure 2.8 shows the setup of TDSR. A tungsten bulb provides the narrow spectral bandwidth via a diffraction grating, and then presents one wavelength or band pass at a time from its exit slit. The light in a certain wavelength was going through chopper and lens, and reflected by a mirror, then finally illuminated the test cell that placed in Janis ST-500-1-(3TX) Cyrogenic-probe station. The current generated under short circuit conditions at this wavelength was measured and normalized to a calibration file to get SR. To get nearly noise-free signal, an OL 750-610DSM adapter combined with optical chopper were placed in the system.
2.4 Results and discussion

2.4.1 Temperature dependent PL on QW test structure

As mentioned in the section on the sample set, the QW test structure was used to verify the method of extraction of thermal activation energy from TDPL measurements. Figure 2.9a shows the TDPL spectra of the QW sample. Varying temperature from 280 to 77 K, only one peak at lower energy than the bulk GaAs band-edge transition can be observed. This peak is from the transition between bound states in quantum well. The intensity of the peak decreased with increasing temperature, due to reduced radiative recombination as more thermally activated carriers escape from the QW confinement. Furthermore, at 280K the position of the peak is at 1040 nm, then it blue shifts with decreasing temperature, while at 77K the position of the peak is at 1012 nm. This phenomenon is related to temperature dependent semiconductor band gap [82].

Figure 2.8 Block diagram of a Spectral Responsivity setup
Additionally, the spectral FWHM of QW increases from 61 meV at 77K to 99 meV at 280K with temperature due to phonons related homogeneous broadening [83]. The thermal activation energy was calculated from equation (13) was 113 meV. Figure 2.9b shows that Arrhenius plot of integrated PL peak intensity and inverse temperature. As can be seen, the fitted temperature region is from 280K to 200K, which is due to ground state transitions are sensitive to temperature. The change in slope below 200K may be due to the thermal escape of the hole.

![Image](image.png)

Figure 2.9 (a) Temperature dependent photoluminescence results of InGaAs quantum well test structure. The excitation intensity is 37 W/cm2; (b) the peak intensity fitting using equation (12).

In order to verify the activation energy from the TDPL, a simulation on the relationship between carrier energy (the position of bound state) and the width of InGaAs quantum well was performed using Matlab software. The simulation was generated by solving one-dimensional Schrödinger equation [84] under finite square barrier condition, as showed in equation (15),

\[-\frac{\hbar}{2m} \nabla^2 \psi + U \psi = E \psi\]  \hspace{1cm} (15)
Where $U$ is mainly affected the barrier height, which refers to the band offset [85] between the InGaAs and GaAs; $m$ is the effective mass of an electron or heavy hole or light hole in the QW. Due to the difference of lattice constant between In$_{0.26}$GaAs (5.95Å at 300K) and GaAs (5.65Å at 300K), the strain induced band offset was also considered [86]. Figure 2.10 shows the results of the simulation by assuming that in a InGaAs QW, a heavy hole effective mass of $m_{hh}=0.44m_0$, a light hole mass of $m_{lh}=0.041m_0$ and an electron mass of $m_e=0.033m_0$ [87], while in GaAs bulk, $m_{hh}^*=0.51m_0$, $m_{lh}^*=0.08m_0$ and $m_e^*=0.067m_0$ [66]. Blue and red colors represent the odd and even solution of the Schrödinger equation, respectively. The number of bound states of electron, heavy hole and light hole are all increasing with the width of well as expected. Furthermore, because of heaviest mass of heavy holes compared to electrons and light holes, Figure 2.10b shows four bound states of heavy hole, while Figure 2.10a and Figure 2.10c show two bound states of electron and light hole each, at the well-width of 7 nm. As mentioned in sample set, the thickness of InGaAs layer inserted in the QW test structure used in TDPL measurements is also 7 nm. Furthermore, as can be seen in Figure 2.10a, the barrier height (the energy difference between bound state and conduction band edge) of electron ground state is 110 meV. This value is very close to the fitted results 113 meV from TDPL measurements as showed previously, so it is reliable to use equation (12) to get activation energy from quantum confinement in nanostructure.
Figure 2.10 Calculation of In$_{0.26}$GaAs/GaAs quantum well energy bands with (a) electron, (b) heavy hole and (c) light hole.

2.4.2 TDPL on QDSC

In order to investigate the optical transitions and experimentally get the activation energy of the carrier escape from QDs, TDPL was performed. Figure 2.11a shows the TDPL emission spectra of the 10-period QDSC with temperature ranging from 86K to 320K. At 320K, seen in Figure 2.11a, a GaAs substrate band to band transition is observed near 880 nm, a wetting layer transition at 946 nm, and a ground state QD transition located at 1064 nm. Similar to the observation in the TDPL of the QW test structure, all three peaks in QDSC shows blue shift with decreasing temperature. Furthermore, each ground state of a QD can be occupied by only two electrons. The density of states is therefore described by a $\delta$ function. The broad Gaussian-shaped PL peak of QD region is due to inhomogeneous broadening [88] and the quantum confined Stark shift. As temperature increases, carriers can be thermally excited to higher energy states. This causes the shape of the PL emission spectra to deviate from the standard Gaussian...
profile. The width of PL emission also changes with temperature, 73 meV at 86K and 126 meV at 320K, which is due to thermal induced changes in carriers’ distribution with temperature.

Figure 2.11a also shows that the PL emission is primarily from the ground QD states at low temperature (86K). This result is due to less thermal energy injection at 80K, more carriers (electron and holes) are radiatively recombining in QD ground states. As temperature increases to 320K, the main peak is located at 930 nm, which is due to radiative recombination from the wetting layer. This firstly indicates carriers in deep QD confined states thermally escape to the wetting layer. Secondly, the number of carriers captured from wetting layer per unit time is proportional to the product of the area occupied by the wetting layer and the probability of carrier capture per unit area [89].

![Figure 2.11(a)](image1)

Figure 2.11(a) the inset shows the temperature dependent photoluminescence results. (b) Arrhenius plot of integrated photoluminescence of 10-layer QD solar cell.

Figure 2.11b shows the Arrhenius plot of integrated intensity of the QD ground state peak from TDPL measurements on 10-layer QDSC. As mentioned in the theoretical approach, the intensity
of the PL is related to the ratio between the number of carrier radiative recombination and carrier
generation. At high temperature (320K), radiative carrier recombination in QD is reduced due to
fast thermal escape. Carriers have a higher probability of escape from ground states of the QDs
to the wetting layer or the conduction band edge. Furthermore, non-radiative paths also increase
as temperature increases, in particular phonon-scattering, which also contribute to decreased PL
intensity. While at low temperature (86K), the thermal escape of the carriers in the ground states
is limited by reduced thermal energy available. Thus, it increases the probability of the carrier’s
radiative recombination. As a result the intensity of the integrated PL increases with decreasing
temperature.

The high-temperature region (200K-320K) was fitted using a variant of equation (12) to obtain
the activation energy of the ground state in QDs, because deep confinement is more sensitive to
temperature than shallow confinement (wetting layer confinement). Thermal activation energy
$E_a$ of the ten-layer QDSC is 114 meV from the fitting. Compared with the theoretical simulations
on electronic structure by Tomic et al. via an eight band $k \cdot p$ model [24], the measured carriers in
TDPL should be electrons, because there are too many bound states of holes due to their heavier
masses than electrons. Furthermore, the fitted activation energy (114meV) from the ground state
is smaller than the theoretical energy difference (barrier height, 210 meV) [24] between the
ground state of electrons and conduction band edge. However, the fitted activation energy is
close to the difference of energy (120 meV) between ground state of electrons and first excited
state of electrons in QDs. This result can be explained by two possible reasons as shown in
Figure 2.12. First, electrons may mainly escape from the ground state to the excited state instead
of from ground state to conduction band edge. Furthermore, the carriers first thermally moves
into an excited state then tunnel through the thin barrier and finally escapes from QDs
confinement at room temperature [75][90]. Secondly, the existing built-in field inside QDSC may lower the average effective height of the barrier.

![Diagram of electron escape from ground state in QDs]

Figure 2.12 Schematic two possible reasons for electron escape from ground state in QDs

In addition, there may be two other reasons for deviation between the activation energy and barrier height. First, the activation energy from TDPL is an average value among the activation energies from ground states of inhomogeneous QDs. Second, due to the built-in electric field in the QDSC, the barrier height may be varied between different layers of QDs along the growth direction.

Using the fitted activation energy (114 meV), the thermal escape time was estimated using equations (8) by assuming that the InAs QDs with an average height of 2 nm and an electron mass of $m_e=0.06m_0$ [91]. The red line in Figure 2.13 shows the relationship between temperature and thermal escape time of electrons from the ground state in QD.
electrons exponentially increase with decreasing temperature, which is correlated with equation (8). Furthermore, at room temperature the thermal escape time of an electron from the ground state of a QD is only a few picoseconds or less, while at low temperature (60K), the thermal escape time of electrons increases above $10^{-4}$ seconds. At 8K, the temperature for EQE measurements that will be discussed in next section, the thermal escape time of electrons from the ground state of QDs (114 meV) is very slow ($>>1$ second).

![Figure 2.13 The thermal escape time and tunneling time of electron from the ground state of QDs vs. temperature](image)

The fitted activation energy (114 meV) was also used for the calculation of tunneling time of electron from ground state in QDs. However, based on Equation (9), the tunneling process is more complicated than thermal emission, because it involves strength of the electric field, width of the barrier, and height of the barrier [74][70]. In the p-i-n QDSC investigated, at short circuit, the built in voltage is 1.35V at 300K from Equation (6), so the relative strength of electric field is
E=54kV/cm. Assuming that the thickness of the barrier between any two different layers of QDs is 13 nm, which is larger than the effective barrier thickness due to the built-in field, the green line in Figure 2.13 shows that the tunneling time of electron from ground state is roughly $10^{-1}$ seconds via Equation (9). Additionally, assuming that the barrier height of the electrons in the wetting layer is 32 meV, the tunneling time is $10^{-6}$ seconds. Compared with the thermal escape time of the electron from the ground state in the QDs outlined before, at room temperature (300K), thermal escape is dominant, while at low temperature (8K), the calculated thermal escape time of electron from ground state is at least $10^6$ times larger than the tunneling time, so tunneling rate is faster than thermal escape rate.

However, compared to the radiative life time ($10^{-9}$ seconds), most of the electrons should recombine instead of escape from QDs or wetting layer at temperatures less than 50K. In order to detect the carrier collection above the GaAs band edge at extremely low temperature, a temperature dependent study of EQE measurements were performed. The experimental results that showed in the following section also help to further investigate the effects of thermal activation on carriers escape from QD and wetting layer, because the amount of thermal energy $kT$ increases with temperature. Table 2-1 shows a summary of thermal escape time and tunneling time of electron from ground state at different temperatures.
Table 2-1 Time of Electron Escape from Ground State

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>Thermal Escape Time (s)</th>
<th>Tunneling Time (s)</th>
<th>The ratio between thermal escape time and tunneling time</th>
</tr>
</thead>
<tbody>
<tr>
<td>300K</td>
<td>$10^{-12}$</td>
<td>$10^{-1}$</td>
<td>$10^{-11}$</td>
</tr>
<tr>
<td>60K</td>
<td>$10^{-4}$</td>
<td>$10^{-1}$</td>
<td>$10^{-3}$</td>
</tr>
<tr>
<td>8K</td>
<td>$&gt;&gt;1$</td>
<td>$10^{-1}$</td>
<td>$&gt;10^6$</td>
</tr>
</tbody>
</table>

2.4.3 Temperature and Bias dependent EQE measurements

Figure 2.14a and 2.14b show the results of the temperature dependent EQE measurements on the 10-layer QDSC with temperature in the range of 8K to 295K, and the 40-layer QDSC with temperature in the range of 80K to 295K, respectively. There are generally two peaks including the carrier collection from bulk GaAs (intensity of EQE around 0.7) and from wetting layer (intensity of EQE around 0.07) of 10-layer QDSC in Figure 2.14a, while there are three peaks from bulk GaAs (intensity of EQE around 0.7), wetting layer (intensity of EQE around 0.2) and ground state of QDs (intensity of EQE around $10^{-4}$) of 40-layer QDSC in Figure 2.14b. As can be observed, firstly, similar to TDPL, the curves of EQE from wetting layer in both samples shift to higher energy as temperature decreases. This phenomenon again indicates that the QD ensembles experience the same trend of temperature dependent energy gap variations as the bulk GaAs [62].
Figure 2.14 Temperature dependent external quantum efficiency of devices with $10 \times$ QDs (a) and $40 \times$ QDs (b).

Secondly, the wetting layer related EQE peaks (at wavelengths slightly greater than the temperature dependent GaAs absorption edge) observed in Figure 2.14b indicate that the thermal energy may still be large enough to support electrons escape from shallow quantum confinement. However, the intensity of EQE from wetting layer first increases slightly from 295K to 240K, and then remains constant down to 8K as shown in Figure 2.14a. A similar experimental result with constant temperature-independent EQE from InGaAs QD absorption in QDSCs with an inter-dot spacing of 3.5 nm were also found by Sugaya et al. [92]. If the carrier being collected is mainly from electron escape, the thermal escape is fast at room temperature ($10^{13}$ seconds at 300K), these facts may indicate that the predominant mechanism of electron escape from wetting layer or other shallow confinement is Fowler-Nordheim like tunneling through the confinement potential, because built-in voltage increase with decreasing temperature. On the other hand, at low temperature (8K) the thermal energy is too small to assist carrier escape [93].
Thirdly, Figure 2.14b also shows that the intensity of EQE from QD ground state absorption decrease with decreasing temperature. This results shows that the carrier escape from the ground state of the QD rely on thermal activation as expected. Additionally, there is still some spectral response from QD ground state absorption at 80K and using the fitted activation energy (114 meV), the escape time of electrons from ground state is $10^{-7}$ seconds. Though the recombination life time of electron is $10^{-9}$ seconds \[61\], there are still possibilities for carrier thermal escape. It also cannot totally exclude the possibility that carriers tunneling from the ground state in the QDs of one layer through the barrier to the excited states in the QDs of another layer. Furthermore, if the carriers being collected are mainly from hole escape, due to the many bound states described in Tomic et al. paper \[24\], these holes can easily escape though thermal activation or tunneling.

Finally, note that the thermal escape time of electron from ground state in the QDs is $10^{-12}$ seconds at room temperature, but the EQE response is weak (around $10^{-4}$). This may be due to weak absorption by QD because of low QD coverage on the surface. From the AFM image shown in the introduction chapter, the distance between dots is larger than 10 nm, and most areas are covered with a wetting layer. Furthermore, this weak response from QD may be also be caused by carrier re-trapping in quantum confinement, recombination during transit across intrinsic region inside QDSC, or non-radiative recombination after generation.

In order to experimentally detect the tunneling effect on carrier collection, bias dependent EQE measurements were carried out on the 10-layer QDSC at room temperature. A higher reverse bias will increase the width of the depletion region, and reduce the diffusion introduced dark current flowing across the pn junction, so more photo-excited minority carriers can be collected and vice versa. On the other hand, for quantum dot embedded regions, as shown in the
theoretical approach, tunneling rate increase with the strength of electric field by assuming that absorption is a constant with bias, so more carriers can be swept out from QD region. Figure 2.15a shows the intensity of EQE under bias varied from -3 V to 0.7 V. Both wetting layer peak (918 nm) and quantum dots peaks (953 nm and 973 nm) under 0V bias shown in the Figure 2.15a are slightly decreased under a forward bias voltage. Similar experimental results were also shown by Chang et al.[75]. The curve of EQE that at lower energy than the GaAs band edge show a slight red shift with increasing reverse bias voltage. This phenomenon is partly due to inhomogeneous distribution of QDs. Under zero reverse bias, carrier tunneling may happen from the shallow bound states in small QDs or from the wetting layer. With increasing reverse bias, more tunneling may happen to carriers from deep bound state in larger dots. Thus more carriers can be collected from a region further away the GaAs band edge. The quantum confined Stark effect also contributes to the red shift.

Figure 2.15b shows the normalized EQE at different wavelength versus bias voltage, which demonstrated the percentage change in EQE or charge collection efficiency (CCE) under different bias. By assuming that all carriers can be collected under maximum reverse bias at room temperature, CCE was proposed by Fujji et al. in their QW solar cell study, which was originally defined as the ratio of the carriers extracted as photocurrent to the total number of the carriers that were photo-excited within the p-n junction area [10]. As can be seen in Figure 2.15b, the wetting layer peak (918 nm) only decrease 5% with decreasing reverse bias from -3V to 0V, because most carriers are tunneling to the conduction band at zero bias. However, the EQE peak (973 nm) from QDs decreases 42% from -3 V to 0 V, a change of over 10% per volt. Voltage bias had a dramatic effect on carrier escape from deeper confinement in QDs, because the effective height and thickness of barrier may increase with decreasing the strength of the electric
field across the intrinsic region from 216 kV/cm at -3V to 54 kV/cm at zero bias, then both tunneling and thermal escape are reduced. The forward bias counteracts the built-in field, which further decreases the rates of both tunneling and thermal escape, so the escape and collection of carrier are further suppressed.

Figure 2.15 (a) External Quantum Efficiency under voltage bias condition at room temperature of 10-layer QD solar cell, (b) normalized EQE at different wavelength versus applied voltage

2.5 Conclusion

In summary, in order to investigate the effect of thermal activation and tunneling on the escape of carriers from bound states in QDSC, temperature and bias dependent spectroscopy were performed. The fitted activation energy of electrons from TDPL is 114 meV, which is close to the energy difference (120 meV) between the ground state and the first excited state inside QDs instead of conduction band off-set (210 meV) in theory. The results may be explained by two possible reasons. First, thermal escape path of electrons of the ground state in QDs is from the ground state to the first excited state. Second, the existing built-in field inside QDSC lowers the
average effective height of the barrier. Using this fitted activation energy, calculated thermal escape time and tunneling time of electrons from the ground state of the QDs are $10^{-12}$ seconds and $10^{6}$ seconds at 300K, respectively. These results indicate that at room temperature thermal escape is dominant for electrons escape from ground state. At low temperature (8K), tunneling mainly affect the electrons escape from ground state, since thermal energy cannot support electrons to overcome the fitted activation energy (barrier, 114 meV). The calculated thermal escape time of electron from ground state is at least $10^6$ times larger than the tunneling time at 8K. Temperature dependent EQE shows that the EQE peaks QD ground state in 40-layer QDSC decrease with decreasing temperature. This fact shows that carrier escape from the ground state of QDs depends on thermal activation. Bias dependent EQE measurements shows the strength of electric field had a dramatic effect on the carrier escape from deeper confinement in QDs. The EQE peak (973 nm) from QDs decreases 42% from -3 V to 0 V in a change rate over 10% per volt. This phenomenon may be due to the effective barrier height may decrease with increasing the strength of electric filed. Additionally, the EQE peaks from wetting layer in both 10-layer and 40-layer QDSCs with different strength of built-in field are independent with temperature, while at room temperature increase 5% under reverse bias varied from 0V to -3V. These facts show that most carriers from wetting layer can be collected at zero bias through tunneling.
Chapter 3

Morphological and Crystal Structure Characterizations of InAs Nanowires

3.1 Introduction

Semiconductor NW heterostructures have attracted considerable attention in recent years because of their great potential in microelectronic and optoelectronic nano-devices [94]. They are interface strain free, provide broad material selection, and have quantum confinement when the diameter is on order of the De Broglie wavelength. In this work, the choice of Indium arsenide (InAs) as a base material for NW devices is motivated by its physical properties. First of all, it is a narrow-band gap semiconductor (0.354eV) and problems with ohmically contacting of wires should be minimal. Secondly it has high electron mobility, up to 20,000cm²V⁻¹s⁻¹, which is 20 times higher than that of Si at room temperature. This is due to its small electron effective mass, m*=0.023m₀, which is three times lower than that of GaAs. Low effective mass also provides strong quantum confinement effects and a large energy level separation in the wires. Another distinctive feature of InAs is that this material is less effective against surface depletion that usually results from surface states, because the surface Fermi level is within the conduction band. This means that conductive InAs NWs can be obtained easily without any surface passivation. The growth of InAs NW has enabled the demonstration of nanowire devices, such as field effect transistors [95][96], tubular conductors [97], solar cells and photo-detectors [98].
To describe the new physics and achieve final success in nanowire device, the first step toward the goal is to obtain high-quality semiconductor nanowires on the selected substrate. The most common method to fabricate III–V NW is to apply a nanoparticle (NP) catalyst to the substrate surface prior to epitaxy. These NPs are typically colloidal Au particles in suspension with diameters on the order of 50 nm. The Au particle acts as a nucleation site and the nanowires grow via the vapor–liquid–solid (VLS) mechanism. Although the size of these NWs can be controlled to some extent by metal NP, there are still important issues to control and reproduce NW in position, size and shape, so some effort has been reported to control the position of the metal catalysts as well as their size by using lithographic techniques [50][51].

Recently, there have been many experimental demonstrations of InAs NWs grown on InAs [99][94] or Si substrate. In comparison, InAs grown on GaAs substrates have been less reported. In this study, InAs nanowires have been grown via MOCVD technique on GaAs using VLS growth mechanism with Au as the catalyst. In order to achieve optimum NW quality, a number of growth parameters are tailored, including the ratio of group V to III precursor flow rates (V/III ratio), and the growth temperature. As a comparison, a catalyst free approach to grow InAs NW using PS/PMMA DBC nano-patterning is also demonstrated. The morphological characterization was studied by scanning electron microscopy (SEM) and the structural properties were investigated using transmission electron microscopy (TEM).
3.2 InAs NW preparation

InAs NW using Au seeds were all grown in a Veeco D125 LDM rotating disk MOVPE reactor using a Au-assisted VLS method. Before the growth process, the native oxide on the GaAs substrate was etched in an HCl/H₂O (2:1) solution for one minute, poly-l-lysine (PLL) from Ted Pella was used as adhesion promoter for the 50 nm Au colloidal NP. Furthermore, the negatively charged Au NP stick to the positively charged PLL, so the affinity of the Au NP for PLL prevents the NPs from aggregating while the suspension dries on the substrate[100][101].

After deposition of Au NP, GaAs substrates were placed into an MOVPE chamber in a flow of hydrogen carrier gas. With relatively low reactor pressure (60 Torr), a constant flow of the group-V precursor gas arsine (AsH₃) was maintained during heating to prevent substrate decomposition. Following a high temperature (~575°C) deoxidation step under an AsH₃ atmosphere, the wafer was cooled to the nucleation temperature. Trimethylindium (TMIn) was injected into the chamber with Arsine to generate the metallic droplets on the surface at temperature ranging from ~350°C. The growth temperature was varied between 350 °C and 420°C measured in-situ using a thermocouple, and thus does not refer to the substrate itself. It is assumed here that thermal conduction is sufficient, so any temperature difference between the thermo couple and the sample surface does not affect the conclusion of the study. V/III ratios ranging from 12 to 39 by adjusting the flow rate of Arsine were also investigated. After growth was complete, the precursors and heaters are shut off and the wafers allowed cooling to 30°C before removal from the reactor. Table 3-1 shows typical growth conditions used for this process.
Table 3-1: Typical InAs NW growth parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reactor pressure</td>
<td>60 Torr</td>
</tr>
<tr>
<td>Catalyst</td>
<td>50 nm Au Particle</td>
</tr>
<tr>
<td>Rotation</td>
<td>1000rpm</td>
</tr>
<tr>
<td>Adhesion Promoter</td>
<td>Poly-l-lysine</td>
</tr>
<tr>
<td>Carrier gas</td>
<td>Hydrogen</td>
</tr>
<tr>
<td>Organometallic precursors</td>
<td>Trimethylindium and Arsine</td>
</tr>
<tr>
<td>Partial pressure of Trimethyldium</td>
<td>2.0×10^{-3} torr</td>
</tr>
<tr>
<td>Partial pressure of Arsine</td>
<td>0.02 torr ~0.12 torr</td>
</tr>
</tbody>
</table>

NWs were also formed by selective-area MOCVD InAs growth from nano-scale openings defined by the process of Apolystyrene/polymethylmethacrylate (PS-b-PMMA) diblock copolymer (DBC) nano-patterning [102], which was performed through collaboration with Luke Mawst at the University of Wisconsin. Plasma enhanced chemical vapor deposition (PECVD) was used to deposit 10nm SiNₓ layer on a (111)B GaAs substrate. Then an annealing process is used to improve adhesion of the template mask [103] as well as to avoid cracking caused by thermal expansion introduced stress during the MOCVD growth [52]. The sample was annealed for hardening of the SiNₓ mask, following a toluene-diluted neutral brush of PS-ᵣ-PMMA spin coated on the top. After baking the spin-coated sample in a vacuum, a near 5-nm brush layer provided non-preferential affinity to the both blocks of cylinder-forming PS-b-PMMA, which enabled the formation of the cylinder morphology with the cylinder axis oriented perpendicular to substrate surface [103]. Then 1% (W/W) toluene solution that formed by the PS-b-PMMA
DBC was spin-coated on the SiN$_x$ layer. Then the sample was annealed under vacuum in order to complete micro-phase separation. After self-assembly, the PMMA cylinders were removed through exposure to Ultraviolet (UV) light, which only degraded the PMMA block by breaking the polymer chain and cross-linking the PS at the same time. UV-exposed PMMA were finally removed by acetic acid to produce a hole-pattern in the PS. A plasma-based reactive ion (RIE) etching technique was employed to transfer the pattern of holes into the SiN$_x$ layer[101]. The process were discussed in detail elsewhere [104][105].

After RIE, a vertical chamber MOVPE (3 × 2) reactor with a close-coupled showerhead (CCS) gas delivery system was used for InAs nanowire growth, also performed through collaboration with Luke Mawst at the University of Wisconsin. Total pressure of the reactor was set to 100 Torr, while the partial pressures for TMIn and AsH$_3$ were 3.7x10$^{-7}$ Torr and 9.9x10$^{-2}$ Torr, respectively. The growth temperature was initially ramped up to 600°C under a flow of AsH$_3$ which removed residual oxide from the exposed GaAs within the nano-patterned openings in the SiN$_x$. Then the growth of InAs NW was initiated when the substrate was cooled down to 550°C.

As mentioned in the introduction, in order to improve the cross wafer uniformity and quality, the results of InAs NW growth under different conditions were characterized and evaluated. As is known, NW growth is affected by engineering factors including substrate orientation and surface preparation, as well as, physical factors including V/III ratio and growth temperature. Table 3-2 shows the sample set as well as the growth detail used for the investigation of InAs NWs growth.
Firstly, sample A and B were used to study the effects of substrate orientation on the growth of InAs nanowire, because NWs generally grow along the crystal direction that minimizes the total free energy that usually dominated by the surface free energy of the interface between the semiconductor and the metal catalyst [106]. For compound zinc-blende semiconductors and their alloys (i.e. GaAs, GaP, InAs and InP), \(<111>\) directions can be further distinguished into \(<111>\)A and \(<111>\)B depending upon the atomic layering sequence and thus surface termination. The (111)B (group-V terminated) is the lower energy plane [107]. In this study, (100) GaAs substrate (sample A) was compared with (111)B GaAs (sample B though sample J) substrate at growth temperature around 420°C with V/III ratio of 12.8.

Secondly, sample C and D was used to investigate the effect of substrate preparation on NW growth, because the distribution of nanowire relates to the position of Au catalyst. Before growth,
the PLL and the Au NP were deposited using a spin coater for the substrate preparation of sample C. PLL was puddled on the wafer, spun at 500 rpm for 10 seconds to wet the surface then followed by a 3000 rpm, 1 minute step to dry the surface. After that, Au NP with diameter of 50 nm were also puddled on the surface, and spun at 140 rpm for 45 seconds to wet the surface while maintaining coverage on the surface, followed by a step at 3500 rpm for 15 seconds to remove any excess. Additionally, demonized (DI) water rinse was applied to sample D (as well as E though J), while the sample C did not receive the rinse step after the Au NP coating. The temperature and V/III ratio of the growth are 420ºC and 12.8, respectively.

Thirdly, sample E, F and G were used to investigate the effect of growth temperature, because growth rate [50], directions [106] and morphology [108] of InAs nanowire would be influenced by the growth temperature. The growth temperatures for sample E, F, G were set at 353ºC, 364 ºC and 375 ºC, respectively, while the V/III ratio was set at 12.9.

Fourthly, sample G, H and I were used to study the effect of V/III ratio, because it suggested that the growth direction [106], crystal structure [42] and growth rate of InAs nanowire related to V/III ratio. The growth temperatures of all three samples were fixed at 375 ºC and the V/III ratios was for sample G, H, I were 12.9, 6.5 and 38.8 respectively.

Finally, Sample J was used selective area growth with a DBC nano-pattern in MOVPE technique. Note that the growth of sample J was without Au NP, so the diameter of the InAs nanowire related to the diameter of the hole in the mask.
3.3 Experimental section

The morphological characterization of the InAs NWs were studied by scanning electron microscopy (SEM) using LEO EVO50 LaB₆ system and LEO ZEISS 1550 field emission scanning electron microscope (FESEM). Images of three different views were taken: a top-down view, 45° tilt, and cross-section view. Scanning electron microscopy in this study is to help assess overall length, shape, density and the orientation of InAs nanowire. Notice that due to the fact SEM utilizes electrons to form an image, special preparations must be treated to the sample. All water must be removed from the samples, because the water would vaporize in the vacuum. Some samples need to be made conductive by covering the sample with a thin layer of conductive material (Au, etc). Clean cleaved InAs NW samples in this study were directly attached to the sample stage via a round carbon tape.

As shown below in Figure 3.1, accelerated electrons in an SEM carry significant amounts of kinetic energy, and this energy is dissipated as variety of signals produced by interactions between electron and sample, when the incident electrons are decelerated in the solid sample. These signals include secondary electrons (that produce SEM images), back scattered electrons (BSE), diffracted back scattered electrons (EBSD that used to determine crystal structures and orientations of materials), photons (characteristic X-rays that are used for elemental analysis and continuum X-rays), visible light (cathodoluminescence –CL), and heat. Secondary electrons and back scattered electrons are commonly used for imaging samples: secondary electrons are most valuable for showing morphology and topography on samples and back scattered electrons are most valuable for illustrating contrast in composition in multiphase samples. A scintillation detector acts as a television camera and the image of the sample is displayed on a television
screen. By changing how the electrons are bent and how the beam of electrons strikes the sample, the magnification and focus can be adjusted.

Figure 3.1(left) possible electron and specimen interaction: When the electron beam strikes the sample, both photon and electron signals are emitted. By detection of the secondary electrons, a topographic representation of the sample can be visualized; (right) LEO EVO 50 LaB$_6$ system at Rochester Institute of Technology.

The structural properties were further investigated using a JEOL 100CX II TEM operated under 100kV, and a JEOL 3011 high resolution electron microscope (HREM) under 300kV. Generally, the term high resolution imaging is used to refer to imaging of lattice of the crystal. As can be seen below, the basic parts of a TEM is similar to SEM, but most of the imaging is done by detecting electrons that have been transmitted through a sample in TEM. The electron are only able to pass through the material consists of lighter atoms or where the specimen is thinner or less concentrated [109]. Therefore the sample in the TEM is required to be very thin (thickness <100 nm).
Figure 3.2 Schematic of working principles in TEM and SEM.

For TEM samples preparation, the samples of as-grown InAs NWs were first mechanically removed from the substrate via a blade into isopropyl alcohol. The NWs were dispersed with an ultrasonic bath for 1 min, and a 1mL droplet was placed onto a 300 mesh carbon film-coated copper grids. However, this complex procedure was soon replaced by using the carbon grid directly to touch the grown InAs NWs wafer, which greatly improved the efficiency of TEM sample preparation. Cross-section samples for TEM were prepared using two face-to-face bonded cleaved wafer pieces. A coarse cross-section lamella was cut from the center of the NW bundle and transferred to a Tripod Grinder before ion-milling. Then lamella was sliced into thin sections using a Gatan 691 Precision Ion Polishing System (PIPS) Ar-ion-milling technique.
3.4 Morphological characterizations

3.4.1 Substrate Orientation effects

Figure 3.3 shows the cross-section view of InAs NW grown on GaAs (100) and GaAs (111)B substrates during the same run. As can be seen, a marked difference between the two orientations exists. The InAs NWs on (111)B GaAs substrate align in <111> direction, which is normal to the substrate. The NWs also show a strong tapering effect, with a larger base and narrow tip. In the case of the (100) sample, NWs still predominantly grow along the [111] plane, but the angle between (100) substrate and <111>B is 35.3°, which was also shown by Fortuna et al.[106].

From table 3-3, both the base diameter (0.55 μm) and length (3.74 μm) of NWs grown on (111)B substrate are larger than the base diameter (0.22 μm) and length (2.87 μm) of NWs grown on (100) substrate. This indicates that (111)B substrate is more favorable for the Indium deposition and diffusion and increases both radial and axial growth rates. The ratios between base diameter and tip diameter of both sample A (the ratio of 11) and B (the ratio of 4) show that nanowire grown on (111)B GaAs substrate have more tapering than nanowire grown on (100) GaAs substrate. The NW density is greater on the (111)B GaAs substrate which is likely due to the preferred NW orientation normal to the surface. All subsequently grown NW used (111)B GaAs substrates. Notice that all measurements in this chapter was done by Image J, which is an image processing program developed at the National Institutes of Health [110].
Figure 3.3 Cross-sectional SEM image of InAs nanowire arrays grown on (111)B GaAs substrate and (100) GaAs substrate.

Table 3-3: Measurement of substrates orientation effect on NWs growth via Image J processing software.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Base diameter(µm)</th>
<th>Tip diameter</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(111)B GaAs</td>
<td>0.55</td>
<td>0.05</td>
<td>3.74</td>
</tr>
<tr>
<td>(100) GaAs</td>
<td>0.22</td>
<td>0.06</td>
<td>2.87</td>
</tr>
</tbody>
</table>

As mentioned above, the NWs grow along the direction that minimizes total free energy. The Au NP-GaAs interface is more energetically favorable than an Au NP–InAs interface[111]. For this reason, the Au NP retains the interface with the GaAs substrate, and minimizes its contact with the growing InAs. Consequently, the Au NP migrates along the GaAs substrate surface, whilst assisting InAs growth as it moves. Thus, an InAs “trace” follows the movement of the Au NP.
Furthermore, for InAs NW grown on GaAs substrates, the (111) B (group V terminated) is the lower energy plane and therefore NWs have been observed to grow in the <111>B direction [106]. The large lattice mismatch (7.2%) between GaAs and InAs and interfacial energy could significantly influence NW nucleation and growth.

3.4.2 Substrate Preparation with Au Seeds

The substrate surface preparation also plays an important role in the initial nucleation of the metal catalyst and subsequent growth of a NW. As a first step to NW growth, a wet etch is frequently used to remove the native oxide on the substrate surface. An in situ anneal step is also commonly employed in the reactor before the growth of NWs to desorb any residual native oxide from the growth surface. In addition, this step will alloy the metal catalyst and substrate, and then will form the initial interface that will eventually become the NW growth front. Without proper removal of the native oxide, NWs will grow without epitaxial relationship with the substrate and thus in a random direction relative to the surface.

From the cross-section SEM image, there are more conglomerations shown in the wafer without DI water rinse. The measurements in table 3-4 show the wafer with DI rinse has a line density of 3.5 NWs per µm as compared to 1.3 NWs per µm for the sample without DI rinse. In addition, without DI rinse, the sample has a larger average base diameter (0.21 µm), a smaller average length (2.16 µm) and more tapering than the sample with DI rinse. The aspect ratios between length and base diameter (14.5 of sample C and 10.3 of sample D) show that the growth rate of length in nanowire with DI rinse is faster than in nanowire without DI rinse. These observations may be due to the Au NP not fully dispersing on the substrate and forming large conglomerations. This in turn leads to large NW base diameters but lower NW density.
Figure 3.4: SEM image in cross-section view of NWs grown with and without DI rinse.

Table 3-4: Measurement of substrates preparation on NWs growth via Image J processing software.

<table>
<thead>
<tr>
<th>Substrate preparation</th>
<th>DI Rinse</th>
<th>No DI Rinse</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Base Diameter (μm)</td>
<td>0.16</td>
<td>0.21</td>
</tr>
<tr>
<td>Average length (μm)</td>
<td>2.32</td>
<td>2.16</td>
</tr>
<tr>
<td>Aspect ratio</td>
<td>14.5</td>
<td>10.3</td>
</tr>
<tr>
<td>Line Density (#/μm)</td>
<td>3.5</td>
<td>1.3</td>
</tr>
</tbody>
</table>

3.4.3 V/III Ratio Effects on InAs Naowires

For III-V materials, as outlined before, that the ratio between the molar flow rates of the group-V and group-III precursors (V/III ratio) can significantly influence the growth rate and morphology of III-V NWs. Furthermore, the effective V/III ratio depends on both input precursor molar fraction and the related growth temperature. Figure 3.5 demonstrates the effect of V/III ratio on the InAs nanowire growth with (111)B GaAs substrate. The growth temperature was 364°C, and the growth time is 10minutes. The highest nanowire density occurs with the lowest V/III ratio of
NWs density decreased when increasing V/III ratio to 12.9. With further increasing V/III ratio, a few kinkscan be observed. Joyce et al. suggested the possibility of stable Arsenic trimmers forming on the (111) surface with a high V/III ratio that may modify the surface energetic and allow for other growth directions, and the proportion of these kinked irregular nanowires increases with V/III ratio. The high V/III ratio may also hinder In diffusion to the Au particle which could modify the In-Au eutectic and change the growth direction[48].

Figure 3.5SEM images of InAs NWs grown at growth temperature at 364°C of and the indicated V/III ratios (a) 6.5, (b) 12.9, (c) 38.8 Samples are tilted at 45°.

Table 3-5 shows that shortest NWs with an average length around 1.8 µm when the V/III ratio is 6.5, while increasing V/III ratio to 38.8, the average NWs length increase to 5.8 µm. The aspect ratio (length/diameter of base) was increased from 12.00 to 38.93, which shows that, with increasing V/III ratio at 364°C, the growth rate along the length is faster than the growth rate along the axial direction.

Table 3-5: Measurement of V/III ratio effect on NWs growth via Image J processing software.
Growth Temperature Effects on InAs NWs.

Growth temperature has a marked effect on NW properties because it determines the thermal-dynamic growth process and affects the effective V/III ratio. The V/III ratio was set at 12.9. The 45° titled SEM images in Figure 3.6 a, b and c illustrate the morphological changes that take place with different growth temperatures of 353°C, 364°C and 375°C, respectively. As can be seen, there is slight decrease in nanowires density. Increasing base diameter of InAs nanowire and roughness of the surface can also be observed with increasing temperature. From the table 3-6, with increasing growth temperature from 353°C to 375°C, the average length of the InAs nanowire increases from 1.37 µm to 2.30 µm and the average base diameter of the NWs increase from 0.13 µm to 0.15µm. The aspect ratio of length to base diameter also increases from 10.54 to 15.33 with temperature. This phenomenon is due to the fact that both degree of precursor decomposition and adatom diffusion length increase with temperature. More Indium adatoms are available. Increasing surface Indium adatom mobility lowered energy barriers, so further enhanced the growth for both axial and radial directions of InAs nanowire.
Figure 3.6 SEM images of InAs nanowires grown at temperature 353°C (a), 364°C (b), 375°C (c) with V/III ratio 13. Samples are tilted at 45°.

Table 3-6: Measurement of V/III ratio effect on NWs growth via Image J processing software.

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>353</th>
<th>364</th>
<th>375</th>
</tr>
</thead>
<tbody>
<tr>
<td>Avg. Length (µm)</td>
<td>1.37</td>
<td>1.66</td>
<td>2.30</td>
</tr>
<tr>
<td>Avg. Base Diameter (µm)</td>
<td>0.13</td>
<td>0.13</td>
<td>0.15</td>
</tr>
<tr>
<td>Aspect ratio (length/ bottom diameter)</td>
<td>10.54</td>
<td>12.77</td>
<td>15.33</td>
</tr>
</tbody>
</table>

### 3.4.5 Selective area InAs NW growth via DBC nano-patterning

As mentioned in sample preparations, sample J is selective area growth via MOVPE without applying Au NP as catalyst. These samples were prepared and grown by the University of Wisconsin and characterized at RIT. An atomic force microscopy (AFM) was firstly used to measure the depth and number density of the holes in the diblock copolymer (DBC) that formed the original pattern for nanowire growth. Veeco Dimension 3100 atomic force microscope was set in the tapping mode, and a high-resolution SHR150 1 nm diameter silicon tip was applied to image the surface of the sample. Imaging processing was done by Scanning Probe Image Processor (SPIP) software. Figure 3.7 shows the AFM image of the honeycomb pattern of the DBC in uniformity with 1µm ×1 µm scan area. The darker of the color the deeper in measured
depth. The density of holes measured is \((7.7\pm 0.2)\times 10^{10}\) holes/cm\(^2\) while the average diameter of the hole is 28.6±0.1 nm.

![AFM image of the diblock copolymer mask](image)

Figure 3.7 AFM image of the diblock copolymer mask

In order to examine the results after growth via MOVPE, the FESEM was used in order to achieve a higher magnification. Figure 3.8 shows a top-down view of InAs nanowire. Comparing to the InAs NWs grown with Au seeds that showed previously, a larger density of \(5\times 10^{10}\) cm\(^{-2}\) InAs NWs grown in the patterned holes from copolymer mask can be observed, although there are a few conglomerations. The measured average diameter of InAs wire is 25.9±0.2 nm correlates with the diameters of the hole from the DBC mask, and this diameter is also much smaller than the diameter of the Au catalyzed NWs (\(>100\) nm).
3.5 The structure property analysis

3.5.1 NW grown with Au seeds

Sample D was used for the TEM imaging due to its relatively high density and low degree of tapering. It was prepared by scratching the wafer surface into a solution of isopropyl alcohol. Afterward, one drop of the solution was applied to the carbon film coated copper grid and allowed to dry. This was repeated several times to ensure many NWs are deposited on the carbon grid.

As shown in the low resolution TEM image in Figure 3.9a, the grey transparent membrane is carbon, which has smaller atomic weight than the Indium and Arsenide atoms, so more electrons are transmitted, leading to the light color observed in the image. The darker feature with the tapering shape is an InAs NW. NW base are grown first, so they are exposed to the reactants for longer than the subsequently grown Au nanoparticle capped tip as shown in Figure 3.9b. Owing
to their proximity to the substrate, the NW bases also receive a greater fraction of precursor materials collected on and diffusing from the substrate [112]. As can be seen in Figure 3.9, the diameter near the bottom of the NW is 111.3 nm, and diameter near the tip is 58.7 nm. The single NW shows a tapering effect with a narrow tip, which is correlated to the SEM image shown before. The dark cap is Au-alloy particle that was used as the catalyst for NWs epitaxial growth with the original diameter of 50 nm.

Figure 3.9 (a) Low resolution TEM image of single NW via gold catalyst. (B) Tapering of nanowire.

Dark and bright bands also can be observed from the picture. The bands could be different crystal structure or planar crystallographic defects. Most III-V materials typically exhibit random intermixing of Zinc blende (ZB) and Wurtzite (WZ) structure when grown as NWs. WZ is a hexagonal crystal structure with alternating atoms (unlike simple hexagonal closely packed (HCP), which has uni-atomic layers) that follows ABAB alternating layer structure as shown in
Figure 3.10, while the ZB structure resembles a normal cubic lattice but with a diatomic basis resulting in a structure that resembles two FCC crystals interleaved with each other with an ABCABC layer structure. Since both WZ and ZB crystal structures of III-V materials have a diatomic basis, resulting in alternating layers of material, they are prone to crystal defects. One of the main defects is stacking faults. For example, in original WZ with an ABAB layer structure, a stacking fault would be ABAACA, where the C layer sits on top of each other instead alternating between A and B. A special type of stacking defaults that can occur in ZB crystals (but not in WZ due to its mere 2 layers) is a twin defect, in which the crystal layers reverse order after a stacking fault. For example, a twin defect would be ABCABCBCABCA, where the original order was ABC but shift to CBA. Polytypism is another type of growth phenomenon where the crystal structure changes, such as shifting from ZB to WZ [113].

Figure 3.10 Schematic illustration of crystal defects including (a) twin plane (b) stacking fault and different crystal phase including (c) zinc blende (d) Wurtzite.
Specifically, the band structure of materials with WZ crystal structure is predicted to be different than that of ZB structure of the same material[114][115], giving rise to abrupt band offsets at the interface between structurally different materials. The interface between these materials may also act as scattering centers for electrons and phonons, potentially affecting both electronic and thermal transport [116].

HRTEM was operated at 300kV with the beam aligned along [110] zone axes in order to obtain high-resolution images to further investigate the structure properties of InAs NW grown with an Au seed. As shown, the cross section view in Figure 3.11a, a 55 nm thick buffer layer is grown between InAs NW and GaAs substrate. Single InAs NW grown normal to the (111)B GaAs surface with base diameter in 131 nm correlates with previous measurements. When further zoom in, seen in Figure 3.11 b, misfit interface can be observed due to the strain from large lattice mismatch. The black dots represent the misalignment between the atomic layers. Line defects in the buffer layer shown in the Figure 3.11 c is due to strain causing plastic deformation.

![Figure 3.11 HETEM cross-section view of the interface between Nanowire and GaAs substrate.](image)

However, as seen in Figure 3.11 and Figure 3.12, the lattice mismatch did not generate dislocations that propagate to the NWs, and all the defects terminated in the InAs buffer layer.
due to NWs volume elastic strain relaxation (high aspect ratio). In the NW itself, as labeled in Figure 3.12, there is a mix of ZB and WZ crystal phases along the growth direction. This is due to the stacking faults adding or subtracting a layer of atoms, which changes the stacking order, creating a small segment of WZ between two ZB domains. The twin planes are also observed in Figure 3.12.

![InAs NW TEM image](image_url)

Figure 3.12: HETEM image of InAs nanowire with gold seed.

### 3.5.2 Selective area growth via diblock copolymer

TEM was also used to measure the size of the smaller NWs grown with the DBC mask. Unlike the InAs sample grown with Au seeds, all DBC grown NWs show a good uniformity along the length of tubes seen in the image area. The smallest NW diameter in Figure 3.13 is 20 nm and the largest is 33 nm. The average diameter of nanowire is 26 nm with a standard deviation
4nm. The striped bands may come from planar defects as mentioned before, including twin planes and stacking faults, or alternating WZ and ZB crystal phases.

![TEM image of InAs NW without gold seed.](image)

Figure 3.13 TEM image of InAs NW without gold seed.

Figure 3.14 shows selective area electron diffraction (SEAD) from TEM imaging. As can be seen, Debye-Scherrer ring patterns are formed due to random NWs orientation. Also, because the lattice constant of WZ is 4.274 Å and the lattice constant of ZB is 6.032 Å, the indexing ring pattern maybe complicated by the fact that both ZB and WZ structure exist for the grown NWs. Note that the crystallographic phase directly affects the band structure and electronic properties of the NWs.
3.6 PL measurements

As mentioned above, the size quantization and optical wave-guiding effects make InAs NWs a promising material for nano-scale optoelectronic effects. PL measurements were performed to measure the band gap change with embedded NWs. With a cooled InAs detector and laser flux of 37W/cm², and a 1 second integration time, all NW samples (from A to J) at room-temperature gave PL results, which are pure noise as shown in Figure 3.15. The data from PL measurement indicates that the measured NW show no confinement between 1400 nm to 2920 nm. This result may be due to defects causing increased nonradiative recombination. Robyn Woo et al. also considered the twin boundaries as efficient non-radiative recombination centers, which decrease radiative recombination [117].
Figure 3.15 PL measurements at room temperature of NW samples. Only noise has been recorded via InAs detector.

The NW was modeled as an ideal cylinder with infinite barriers using the effective-mass approximation in the time independent Schrödinger equation. Then variables were separated in the differential equation. The radial equation is a Bessel function and the energy gap between the quantized ground states of the conduction band and the valence band is given by

\[
E = E_g + \frac{\hbar^2 \chi_{ns}^2}{2D^2} \left( \frac{1}{m_e} + \frac{1}{m_h} \right) \tag{15}
\]

Where \(D\) is the diameter of a single NW, \(E_g\) is the bulk band gap of InAs (0.354 eV); \(\chi_{ns}\) is the \(s_{th}\) root of the Bessel function, \(J_0(\chi)\) and the first root (2.405) was chosen in this simulation. Effective masses of electrons \(m_e\) and holes \(m_h\) of InAs is 0.0265\(m_0\) and 0.41\(m_0\), respectively [118][119].

Figure 3.16 shows the modeling results of band gap of InAs nanowire with different values of diameter of InAs nanowire via Matlab software. Under infinite barrier assumption, the diameter of InAs nanowire should be reduced to 3~6 nanometers to get a tuned band gap from 1.3 eV to
0.9 eV. Here the band gap refers to the gap between the top of valence band and the bottom of conduction band. The NW diameters in this study are between 50 nm to a few hundred nm, so no strong peak was observed in the near infrared region.

Figure 3.16 Calculations of InAs NW band gap Vs. its diameter using cylinder shape assumption under infinite barrier condition.

Figure 3.17 shows the results from temperature dependent PL measurements via a cooled InGaAs photo-diode on sample F. The peak around 840 nm at 15K is from GaAs absorption, while the significant peak is between 900-1400 nm. Both peaks show a blue shift with decreasing temperature as the semiconductor band gap decreases with temperature [82]. This board peak may indicate that an InGaAs buffer layer (with graded incomposition) is formed during the NWs VLS growth process, because from Figure 3.18, the diameter of nanowires grown on sample F
are larger than 10 nm and the relative emission should be over 1500 nm. The InAs buffer layer observed in Figure 3.11 also supports this conclusion.

Figure 3.17 NWs low temperature PL measurements. At 15K, the peak close to 800 nm is from GaAs substrate and the peak around 1000 nm is from InGaAs buffer layer.

3.7 Conclusion

Morphological characterizations were performed on both InAs NW sample grown with and without Au seeds on GaAs substrate. From SEM results, NW can grow with Au seed on (111)B GaAs substrate with a large base and narrow tip in the growth direction. Surface preparation greatly affects NWs density. NW growth direction mainly depends on the substrate. InAs NW uniformity is initially related to the Au seed coverage. A DI rinse after spin coating gold solution will help the gold see less congregated and better uniformity, and finally leads to a higher density
of NWs. Increasing V/III ratio from 6.5 to 38.8 will have better indium diffusion in growth direction so a lower bottom diameter over length aspect ratio was as observed. III/V ratio affects the NW aspect ratio (length/bottom width), change from 12.00 to 38.93. However, higher V/III ratio will also cause lowest free energy directly change, then kinks was observed at V/III ratio at 38.8. Increasing temperature also shows a slight decrease in aspect ratio, but accelerates the growth rate in both axial and radial directions. On the other hand, NWs grown without Au seed using a pattern mask show no tapering along the growth direction with a smaller average diameter in 26 nm.

The structure properties were analyzed using TEM. It was observed that all defects stop in the buffer layer when InAs NWs grown are with Au seeds. Because NW heterojunctions can be highly lattice-mismatched as the induced strain can be coherently accommodated through lateral relaxation, NWs can be grown relatively defect-free on highly dissimilar substrate materials. There is a mix of ZB and WZ crystal phases. This is due to the stacking faults adding or removing a layer of atoms. The twin plane was also observed. On the other hand, InAs NWs grown via DBC nano-patterning showed no tapering but a mixture of different crystal phases along the growth direction. Finally, according the modeling, in order to achieve PL response between 1000~1300 nm, InAs NW diameter should be further reduced to 3~6 nm and density of twin boundary may need to be reduced.
Chapter 4

Summary, Conclusion and Future Work

4.1 Quantum dots solar cells

4.1.1 Summary and Conclusion

Recent progress in the research of QDSCs has provided an opportunity to current-match the middle cell in standard upright triple junction solar cells (TJSC) [56] and the single cell for intermediate band solar cells (IBSC) [57]. The collection of carriers from sub-band QD absorption is correlated with the escape of carrier from bound states, which depends on a two-photon process, thermal activation, and tunneling. In order to finally increase carrier collection from QD absorption in InAs/GaAs QDSC, it is essential to understand the process of carrier escape.

In this thesis, the two photon process is limited at room temperature by assumption, based on the fact that a half-filled IB can hardly be achieved because of the inhomogeneous distribution of QDs, as well as, the strength of thermal activation and tunneling. In order to investigate the effect of thermal activation and tunneling on the escape of carriers from bound states in QDSCs, temperature and bias dependent spectroscopy were performed. The fitted activation energy of electrons from TDPL is 114 meV, which is close to the energy difference (120 meV) between the ground state and first excited state inside QDs instead of conduction band off-set (210 meV) in theory. The results may be explained by two possible reasons. First, the thermal escape path of electrons in QDs is from the ground state to the first excited state. Second, the existing built-in field inside QDSC lowers the average effective height of the barrier. Using this fitted activation
energy, the calculated thermal escape time and tunneling time of electrons from the ground state of the QDs are $10^{12}$ seconds and $10^6$ seconds at 300K, respectively. These results indicate that, at room temperature, thermal escape is dominant for electron escape from ground state. At low temperature (8K), tunneling mainly affect the electrons escape from ground state, since thermal energy cannot support electrons to overcome the fitted activation energy (barrier, 114 meV). The calculated thermal escape time of electron from ground state is at least $10^6$ times larger than the tunneling time.

Temperature dependent EQE shows that the EQE peaks QD ground state in 40-layer QDSC decrease with decreasing temperature. This fact shows that carrier escape from the ground state of QDs relies on thermal activation. Bias dependent EQE measurements shows the strength of electric field had a dramatic effect on the carrier escape from deeper confinement in QDs. The EQE peak (973 nm) from QDs decreases 42% from -3 V to 0 V in a change rate over 10% per volt. This phenomenon may be due to the effective barrier height may decrease with increasing the strength of electric filed. Additionally, the EQE peaks from wetting layer in both 10-layer and 40-layer QDSC are independent with temperature, while at room temperature increase 5% under reverse bias varied from 0V to -3V. These facts show that most carriers from wetting layer can be collected at zero bias through tunneling.

### 4.1.2 Future Work

For short term considerations, first, it is important to do band structure simulations on QDSC under different strength of electric field. The electronic structure in the thesis was from Tomic et al., which was without a built-in field at 300K. However the effective height and thickness of the barrier may vary with electric field, so the tunneling and thermal escape of carriers from different bound states will be affected. Second, since the activation energy of electron escape from ground
state was fitted from TDPL measurements on the 10-layer QDSC with a built-in field, TDPL measurements can be performed on a structure without electric field to calculate activation energy as a comparison. Thirdly, since carrier collection efficiency is important to investigate carrier escape with a bias, more bias dependent EQE measurements need to be performed on a baseline cell without embedded QD and QDSCs with different layers of QDs. Furthermore, because the size of dots is affected by orientation of the wafer and growth recipe, QDSCs with different orientations and growth recipes can also be compared with temperature and bias dependent spectroscopy. Fourthly, carriers escape from ground state in QDSCs is mainly dependent thermal activation at room temperature. On the other hand, from temperature dependent EQE, carrier from ground state can be collected at 86K. It will be interesting to see whether the spectral response from QDs absorption can be eliminate at extremely low temperature with bias dependent experiments.

For long term goals, first, the model of tunneling and thermal activation need to be further modified, because it is less accurate to use model of a QW instead of QD to estimate escape rate in QDSC. Secondly, for the application of TJSC, all three mechanisms of carrier escape from QD, can be accept to increase current output. Tunneling and thermal escape can be enhanced by reducing the height and thickness of the barrier. InGaAs quantum well can grow on top of quantum well, or quantum dots contained with different indium concentration can be embedded. Thirdly, as is well known, QDs are a promising material for the IBSC. To enhance carriers escape from second photon extraction, thermal escape and tunneling should be eliminated, which can be achieved by increase the height and thickness of the barrier. This can be achieved by replace GaAs by the material with a lager band gap (GaP), increase the size of dots, or changing the QD materials, etc. Better control of quantum dot growth for higher uniformity in size and
distribution is still a target for IBSCs. Fourthly, reduce defects related recombination in QDSCs will also increase the escape and collection of carrier.

4.2 InAs NWs Growth for Photovoltaic Application.

4.2.1 Summary and Conclusion
Morphological characterizations were performed on both InAs NW samples grown with and without Au seeds on GaAs substrates. From SEM results, NW can grow with Au seeds on a (111)B GaAs substrate with a large base and narrow tip in the growth direction. Surface preparation greatly affects NWs density. NW growth direction mainly depends on the substrate. InAs NW uniformity is initially related to the Au seed coverage. A DI rinse after spin coating gold solution will help the gold see less congregated and better uniformity, and finally leads to a higher density of NWs. Increasing the V/III ratio from 6.5 to 38.8 results in better indium diffusion in the growth direction so a lower bottom diameter over length aspect ratio was as observed. III/V ratio affects the NW aspect ratio (length/bottom width), change from 12.00 to 38.93. However, higher V/III ratio will also cause lowest free energy directly change, then kinks was observed at V/III ratio at 38.8. Increasing temperature also shows a slight decrease in aspect ratio, but accelerates the growth rate in both axial and radial directions. On the other hand, NWs grown without Au seed using a pattern mask show no tapering along the growth direction with a smaller average diameter in 26 nm.

The structure properties were analyzed using TEM. It was observed that all defects stop in the buffer layer when InAs grown is with an Au seed. Because NW heterojunctions can be highly lattice-mismatched as the induced strain can be coherently accommodated through lateral relaxation, NWs can be grown relatively defect-free on highly dissimilar substrate materials.
There is a mix of ZB and WZ crystal phases. This is due to the stacking faults adding or removing a layer of atoms. The twin plane was also observed. On the other hand, InAs NWs grown via DBC nano-patterning showed no tapering but a mixture of different crystal phases along the growth direction. Finally, according the modeling, in order to achieve PL response between 1000–1300 nm, InAs NW diameter should be further reduced to 3–6 nm.

### 4.2.2 Future Work

First, VLS growth with Au seeds is interesting due to its simple growth process without more lithography steps. Like a sword with two edges, the rapidly growth in nanowire using MOVPE provides opportunity for future application in industry, but it is a challenge to experimentally control of growth process. Substrate preparation (including orientation, seeds distribution) and parameters (including temperature and during the growth) are critical the nanowire growth in terms of length diameter, density an defects, as can be seen in Chapter 3. Since Au distribution relates to nanowire density and the size of nucleation, patterned Au seeds with varied diameter may improve the distribution of nanowire as well as decrease the diameter of nanowire. As recorded in literature, ZB structure is grow in low V/III ratio and low temperature while pure WZ can be achieved using high temperature and high V/III. In order to further improve the quality of nanowire, more growth under different growth parameters is worth to try. A number of techniques including EDS and HRTEM can be used to further investigate the impact of these growth parameters on nanowire like temperature, total gas pressure, V/III ratio and etc.

Secondly, SA MOCVD with diblock copolymer template generally improves the uniformity in density and diameter of InAs naowire. There are other methods to achieve a template for nanowire growth. Highly ordered pores in Anodized aluminum oxide [120] were used for the growth of CdS nanowire[121], so it also worth to use AAO as a template to trans pattern to
silicon oxide during InAs growth. Electron beam lithography is a directly method for drilling patterns into silicon based dielectric material for InAs nanowire growth [51].

Finally, investigations into the growth of nanowire are for photovoltaic applications. Solar cell with embedded nanowire should be made in future. Additionally, the growth of pure InAs nanowire were investigate in this paper. Nanowires with core-shell structure using different material can also be grown through VLS technology.
Reference


Abbreviation

DOS  density of states
DSSC  dye sensitized solar cell
EQE  external quantum efficiency
IBSC  intermediate band solar cell
NW  nanowire
NWSC  nanowire solar cell
MJSC  multi-junction solar cell
PV  photovoltaic
QD  quantum dot
QDSC  quantum dots solar
RIE  Reactive Ion Etching
SJSC  single junction solar cell
TJSC  Triple junction solar cell
VLS  vapor-liquid-solid