Large Area Monolayer Doping Development

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Contents

Objective

Scale existing monolayer doping (MLD) process performed on Si pieces to full 6” wafers

- Design and implantation of an entire system

Investigate the doping characteristics

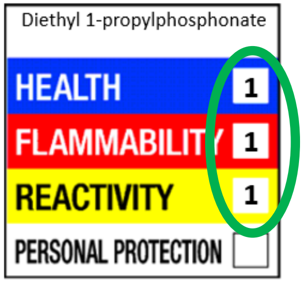
Fabricate diodes to electrically characterize the doping process

Motivation

Existing doping techniques such as ion implantation and spin on dopant have limitations

MLD offers a new method to solve these problems

MLD



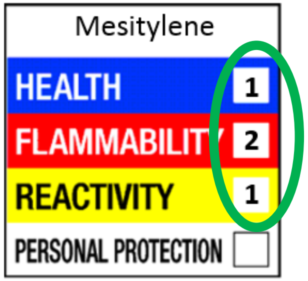
Diethyl 1-propylphosphonate

HEALTH 1

FLAMMABILITY 1

REACTIVITY 1

PERSONAL PROTECTION ☐



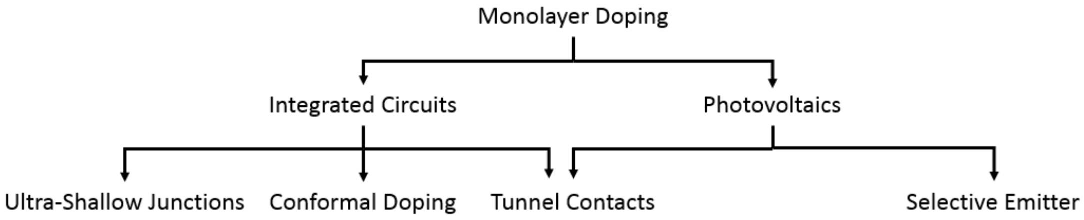
Mesitylene

HEALTH 1

FLAMMABILITY 2

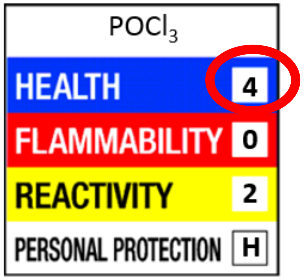
REACTIVITY 1

PERSONAL PROTECTION ☐



Doping	Strengths	Weakness
Ion Implantation	Widely Used Precise Dose Control Complex Doping Profiles	Damages Substrate Shallow Profiles are Difficult Hazardous Materials
Spin-on	No Damage Created Batch Fabrication	Hazardous Materials Forms Glassy Skin
MLD	No Damage Created Conformal Safer Chemistry	Low Dose

Industry



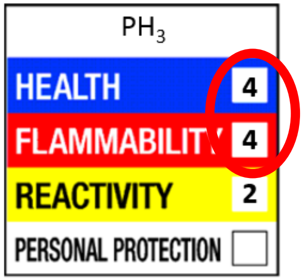
$POCl_3$

HEALTH 4

FLAMMABILITY 0

REACTIVITY 2

PERSONAL PROTECTION H



PH_3

HEALTH 4

FLAMMABILITY 4

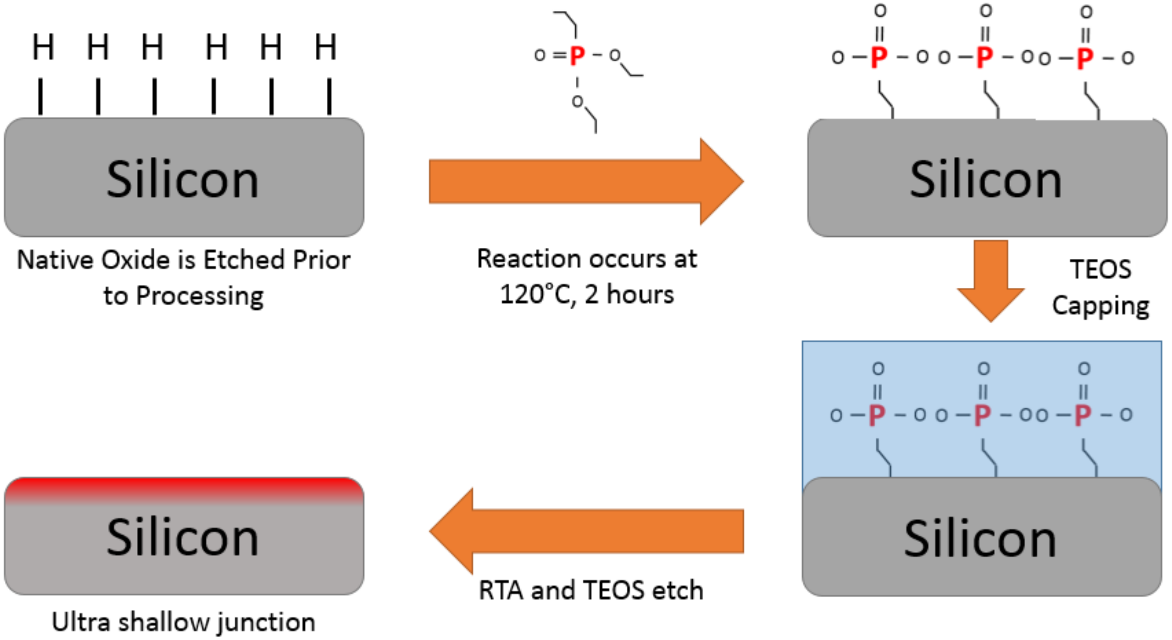
REACTIVITY 2

PERSONAL PROTECTION ☐

Theory

Process by which self-assembled monolayers of a dopant containing molecule are formed on crystalline silicon and driven in with a rapid thermal process

Diethyl 1-propylphosphonate is phosphorus dopant containing chemistry -> mixed with Mesitylene solvent in 1:25 vol/vol ratio



Native Oxide is Etched Prior to Processing

Reaction occurs at 120°C, 2 hours

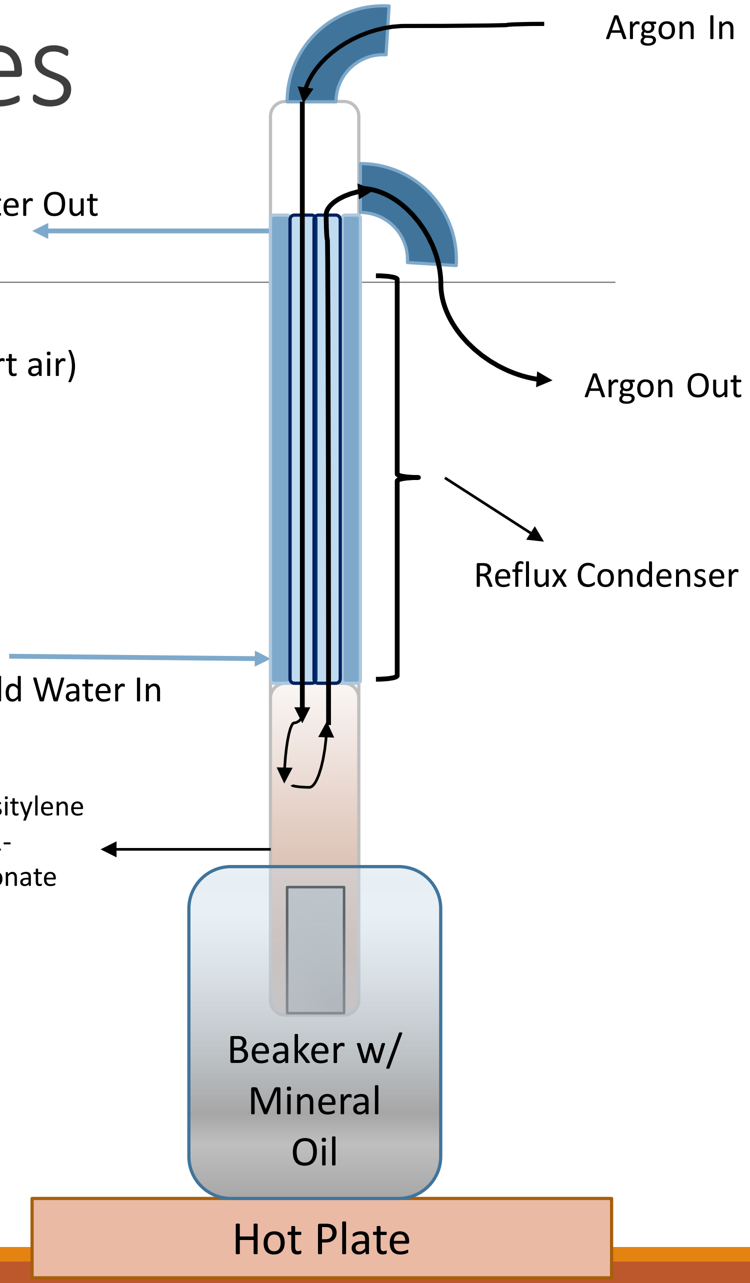
TEOS Capping

RTA and TEOS etch

Ultra shallow junction

Apparatus for Pieces

1) Chemicals are measured out in glove bag
2) Solution in test tube is sparged (aerated with inert air) for 20 minutes
3) Wafer piece is added and connected to reflux condenser
4) Apparatus is lowered into 120°C Mineral Oil for 2 hours for reaction to occur



Argon In

Water Out

Argon Out

Reflux Condenser

Cold Water In

Wafer Piece in Mesitylene and Diethyl 1-propanephosphonate solution

Beaker w/ Mineral Oil

Hot Plate

System Considerations

Withstand 120°C temperature and solvent

Needs to condense any vapors

Needs inlet/outlet for argon

Minimize chemical volume used

Low cost

Scaled Up Apparatus Design
Full 6” Wafers

Purchased container with tight fitting lid

3D Printed sleeve using Nylon

- Connects existing glassware to metal container

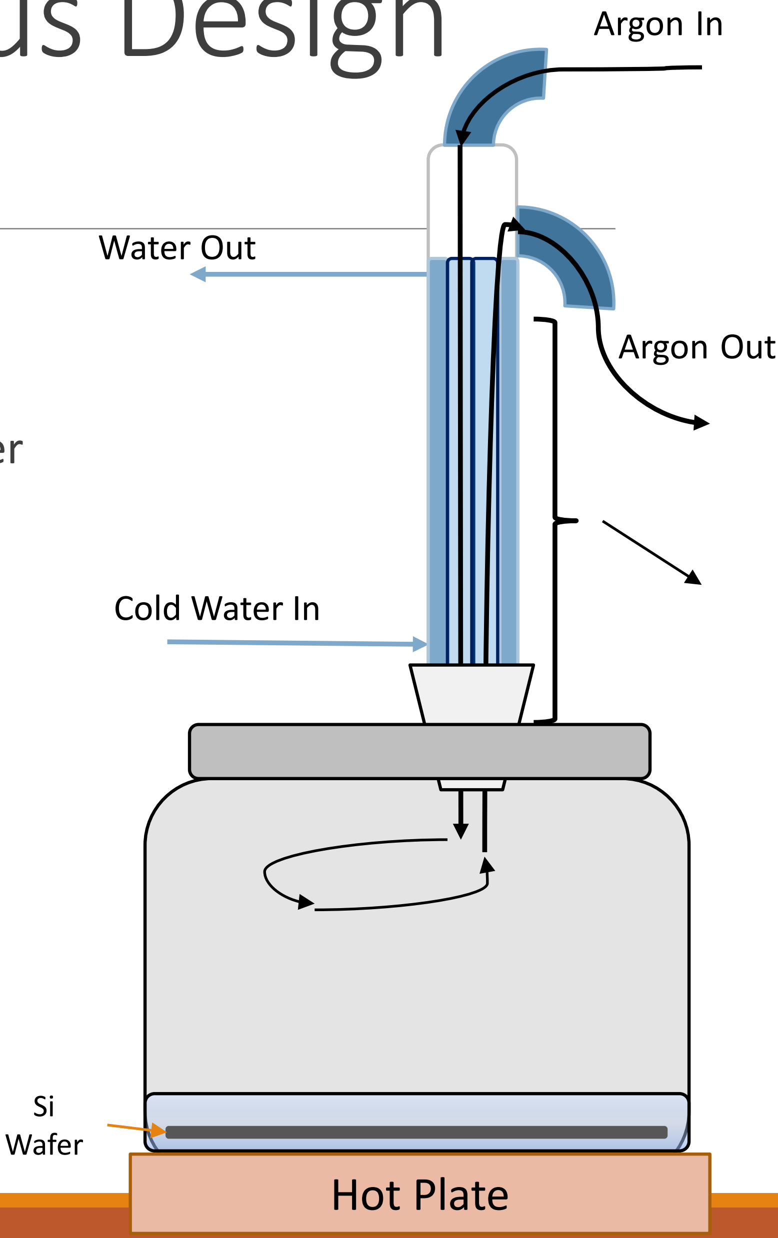
3D Printed Prototype

PLA

Final 3D Print

Nylon

Implementation

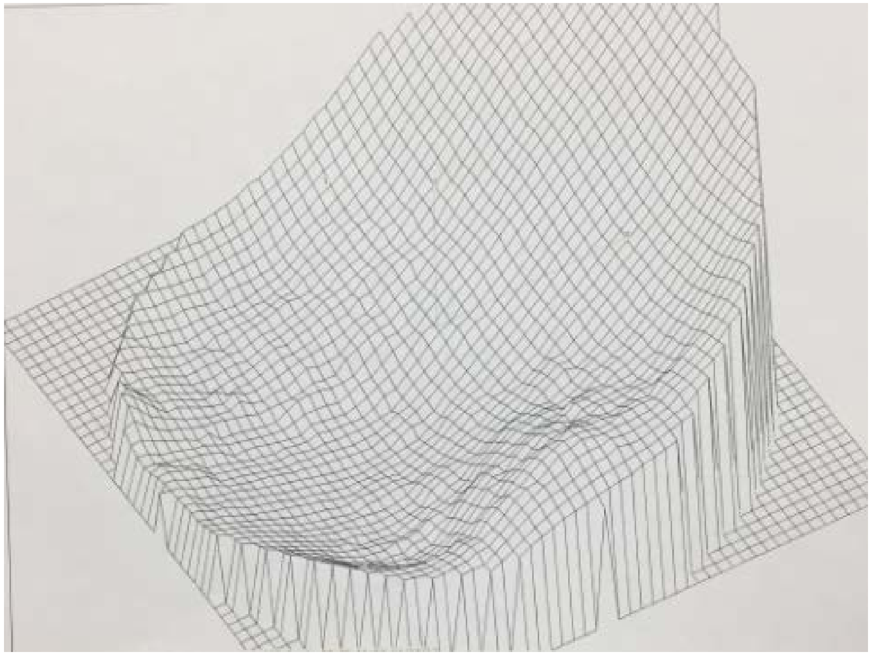


System Results

First run seal on lid did not hold – replaced with RTV seal -> Corrected

- However, results show similar sheet resistance measurements compared to pieces
- Speaks to robustness of the process

Sheet Resistance Measurements		
	Pre-MLD	Post-MLD
6" Wafer:	213 Ω/□	1126 Ω/□
Piece:	191 Ω/□	1031 Ω/□



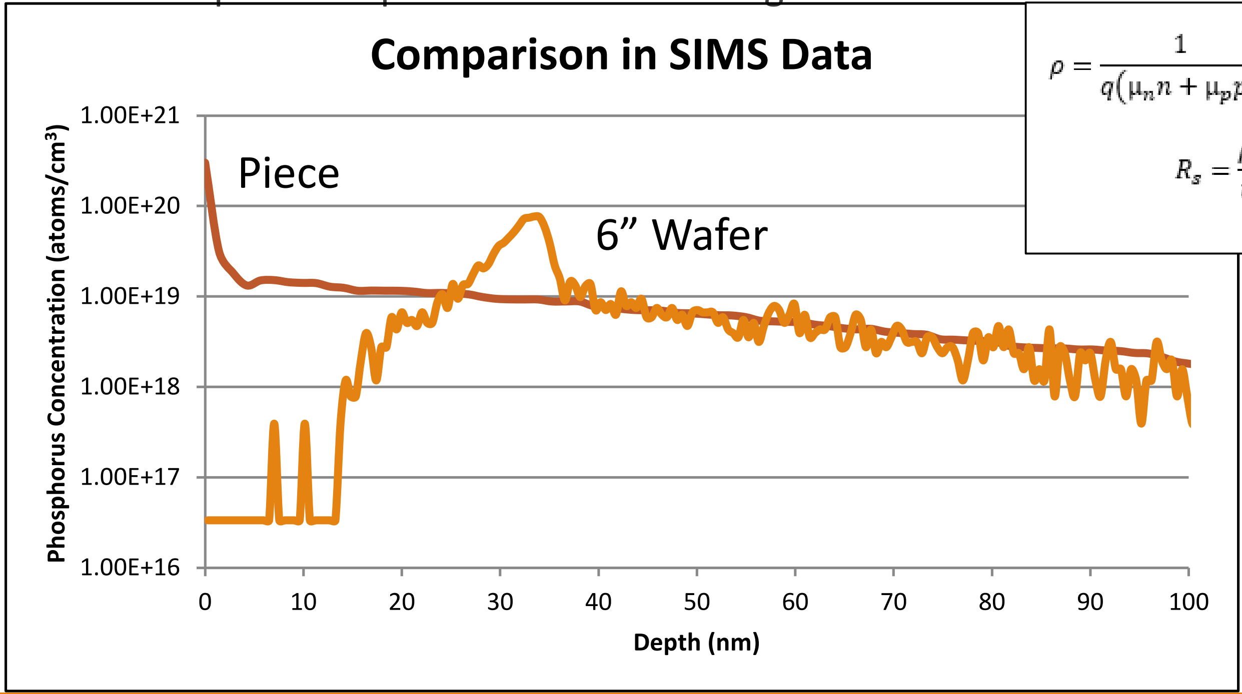
CDE Resmap 3D plot of monolayer doped wafer

Doping Characterization
SIMS

Secondary Ion Mass Spectroscopy measured phosphorus concentration on wafer piece and on doped 6” wafer

Proves phosphorus was doped, matches historical data

- the shape of the profile is under investigation



$$\rho = \frac{1}{q(\mu_n n + \mu_p p)} \approx \frac{1}{q(1.3x10^2 * 5e18)} \approx 0.0096\,\Omega - cm$$

$$R_s = \frac{\rho}{t} \approx \frac{0.0096\Omega - cm}{100nm} \approx 960\ \Omega/\square$$

SIMS Courtesy of:

NREL

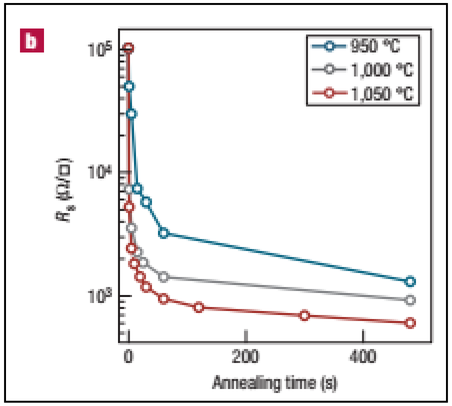
NATIONAL RENEWABLE ENERGY LABORATORY

Doping Characterization Sheet Resistance

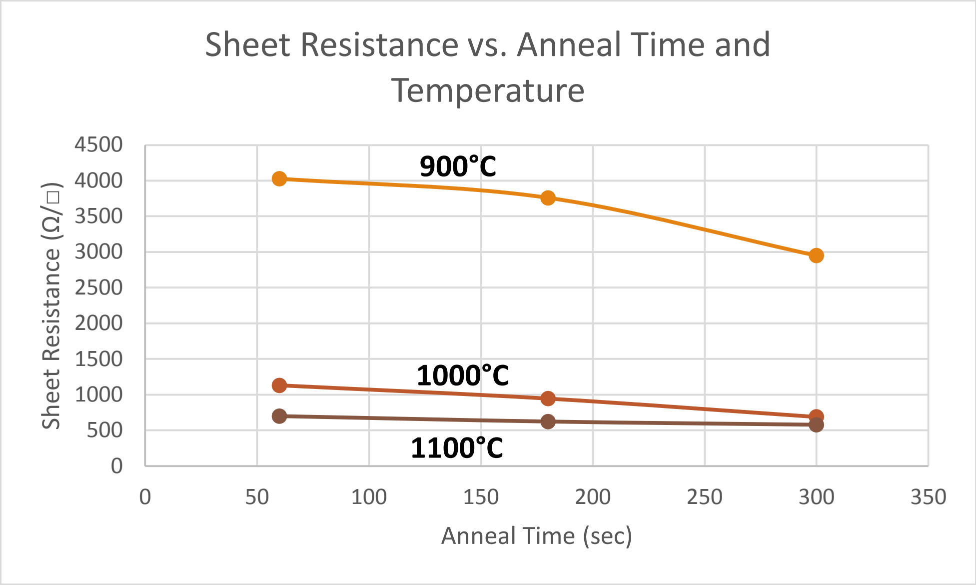
Varied anneal time and temperature and measured sheet resistance

At 900°C, phosphorus is not fully activated

At 1000° and 1100°C phosphorus activates and junction depths increase as anneal time is increased



Similar Trend Reported by Ho et. Al [1]



Electrical Characterization Diode

Fabricated and measured 118x120µm diodes

- Analyzed diode I-V characteristics taken on HP4145 in test lab
- First time diode with monolayer doped junction has been reported

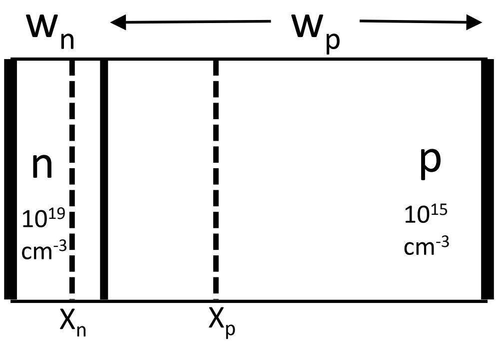
$$J = J_{SCR} + J_{QNR} = \frac{qn_i x_p}{2\tau_n}\left(1-\frac{V}{V_{bi}}\right)^{1/2}\left(\exp\left(\frac{qV}{2kT}\right)-1\right)+\frac{qn_i^2 D_n}{N_A L_n}\left(\exp\left(\frac{qV}{kT}\right)-1\right)$$

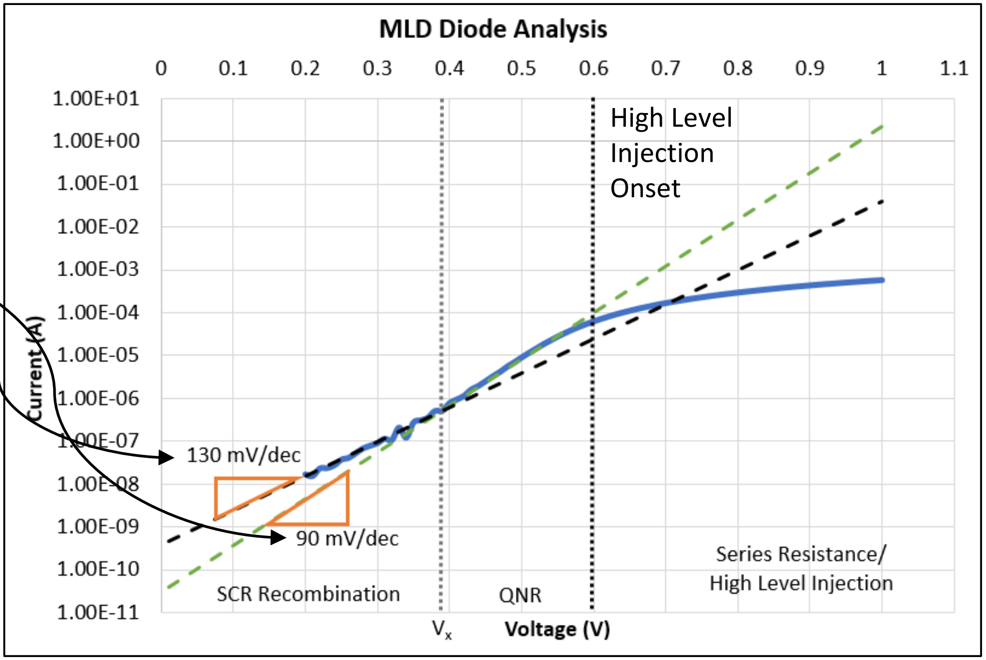
At V_X $J_{SCR} = J_{QNR}$ gives τ_n

Carrier lifetime extracted: τ ~0.23µs

Ideality Factor (QNR): 1.57

Ideality Factor (SCR): 2.16

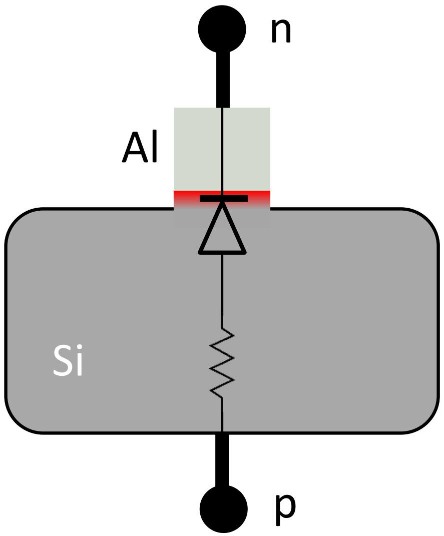




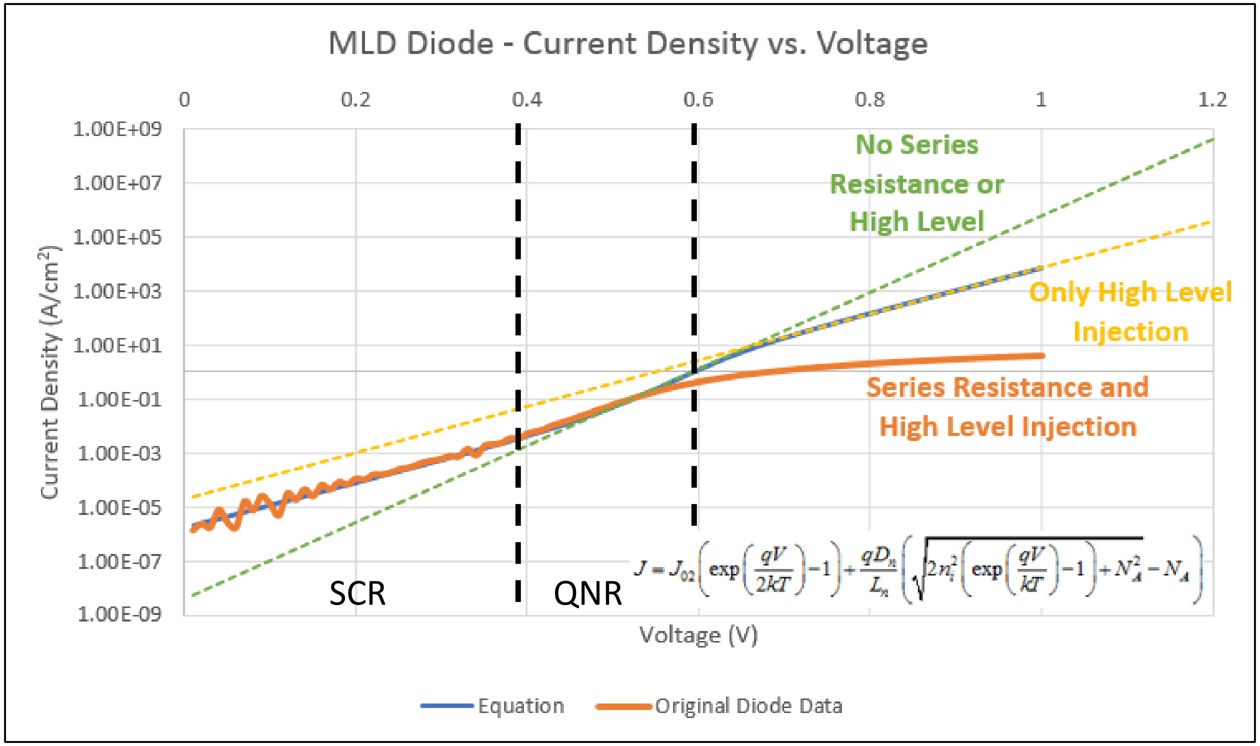
*Sid Grover TLM Senior Design Process Flow

Electrical Characterization Diode

Plugging in extracted values into diode equation to compare to I-V curve with no series resistance and only high level injection shows non-idealities are due to both series resistance and high level injection



Equation courtesy of: Cristea, Miron. "Unified Model for P-n Junction Current-voltage Characteristics."



$$J = J_{02}\left(\exp\left(\frac{qV}{2kT}\right)-1\right)+\frac{qD_n}{L_n}\left(\sqrt{2n_i^2\left(\exp\left(\frac{qV}{kT}\right)-1\right)+N_A^2}-N_A\right)$$

Conclusion

New system design dopes full 6” wafers with phosphorus– opens many research paths as process is now compatible with the RIT SMFL

Sheet resistance measurements are consistent with SIMS data

Diodes were fabricated with MLD junction and characterized, first time reported

Opens up a new doping capability for the SMFL

Future Work

Further characterization research

Modeling of doping profile

Monolayer doping process with Boron

Transistor Source/Drain Doping

- Polysilicon Gate Doping

Conformal Doping Around FinFETs

Selective Emitter for Solar Cells

Through-Silicon Via Doping

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NREL
NATIONAL RENEWABLE ENERGY LABORATORY

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References

[1] Ho, Johnny C., Roie Yerushalmi, Zachery A. Jacobson, Zhiyong Fan, Robert L. Alley, and Ali Javey. "Controlled Nanoscale Doping of Semiconductors via Molecular Monolayers." *Nature Materials* 7.1 (2007): 62-67. Web.

[2] Ho, Johnny C., Roie Yerushalmi, Gregory Smith, Prashant Majhi, Joseph Bennett, Jeffri Halim, Vladimir N. Faifer, and Ali Javey. "Wafer-Scale, Sub-5 Nm Junction Formation by Monolayer Doping and Conventional Spike Annealing." *Nano Letters* 9.2 (2009): 725-30. Web.

[3] Cristea, Miron. "Unified Model for P-n Junction Current-voltage Characteristics." *Open Engineering* 1.1 (2011): n. pag. Web.