Large Area Monolayer Doping Development

R·I·T KATE GLEASON College of ENGINEERING

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MicroE Microelectronic Engineering

I. Project Objectives

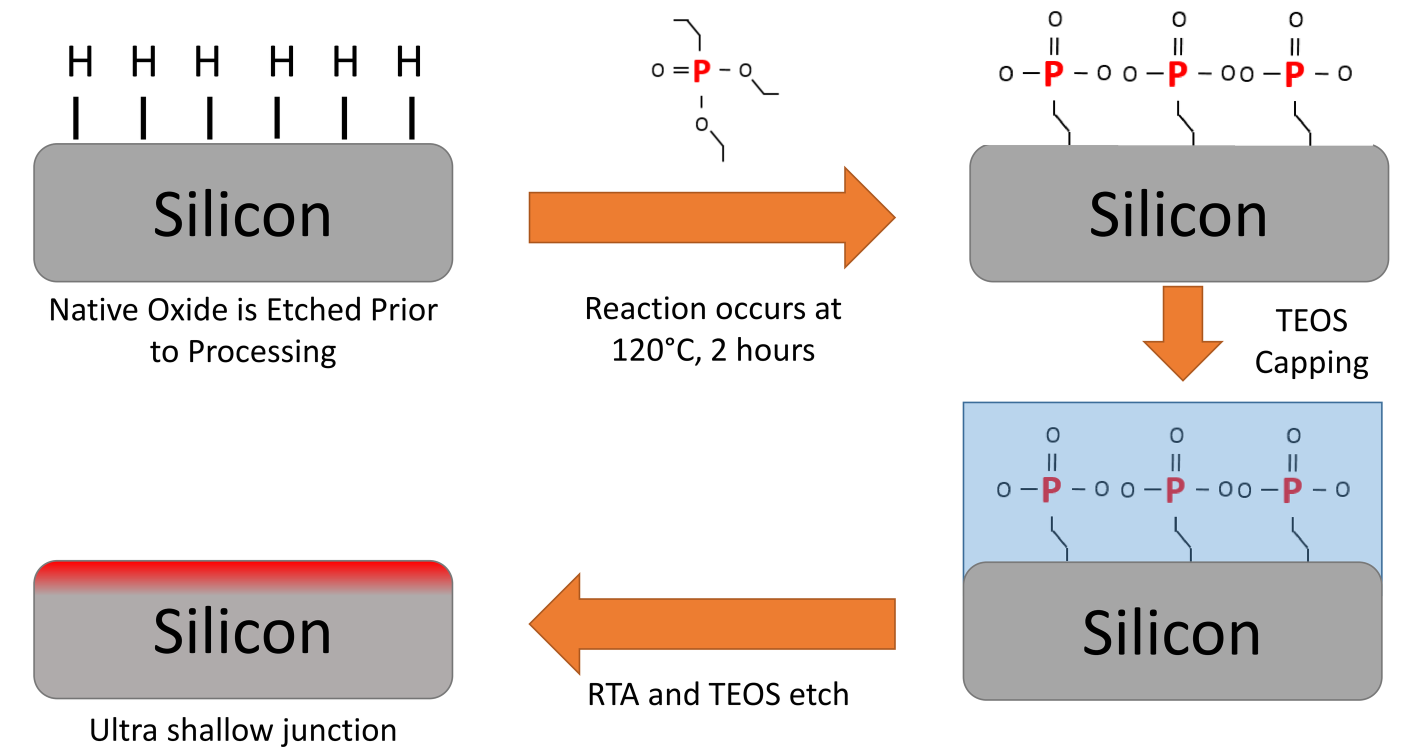
Goal: To develop a method of performing MonoLayer Doping on full 6" wafers using the current knowledge of the process performed on wafer pieces

Secondary: To characterize the doping process with the use of metrology measurements

Tertiary: To perform electrical characterization of fabricated diodes

II. Theory

- MLD involves the formation of self-assembled monolayers of dopant containing molecules on the surface of crystalline silicon which are driven in with a rapid thermal process
- Silicon is reacted with diethyl 1-propylphosphonate and mesitylene in a 1:25 vol/vol ratio for 2 hours at 120°C

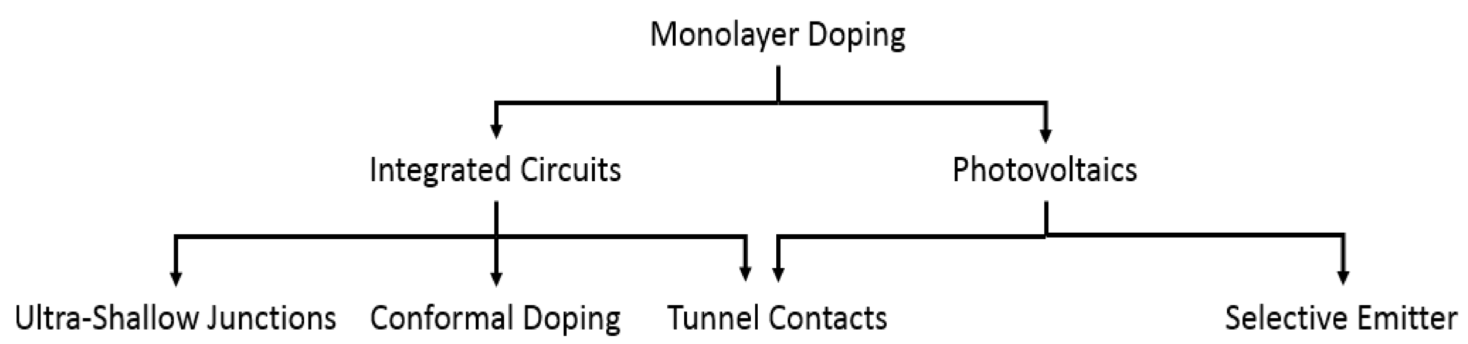


III. Motivation

- Wish to implement MLD process on compatible 6" wafer processes, such as CMOS, at RIT

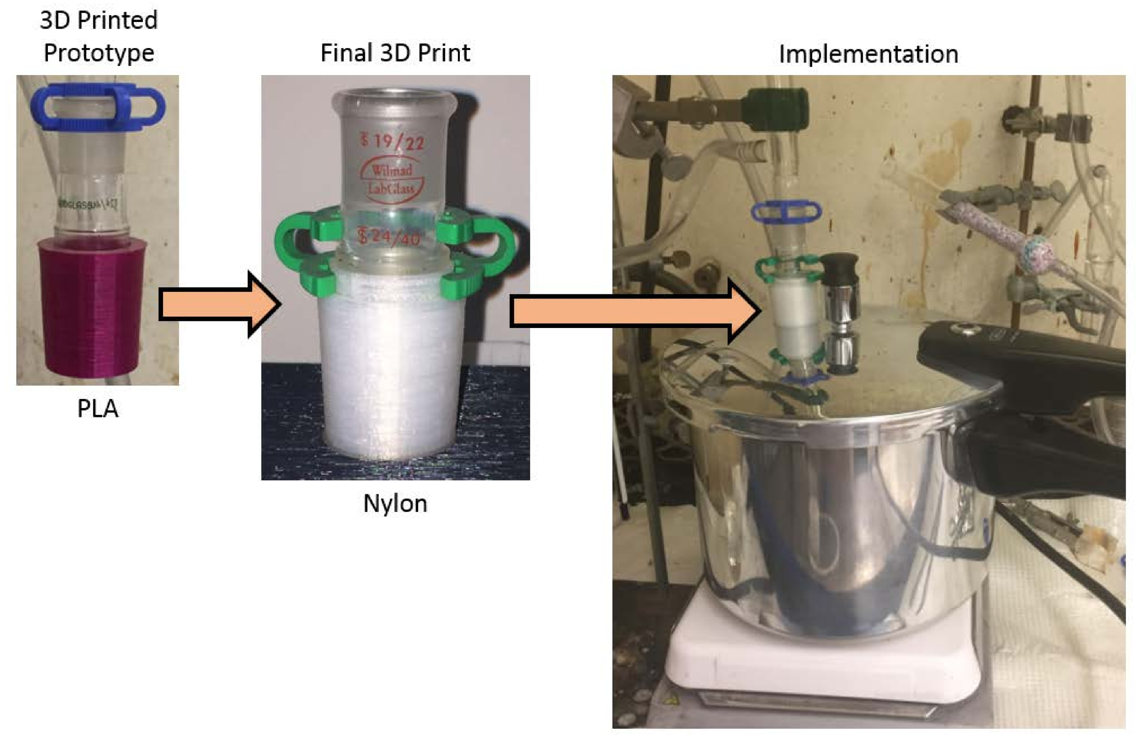
Doping	Strengths	Weakness
MLD	No Damage Created Conformal Safer Chemistry	Low Dose
Ion Implantation	Widely Used Precise Dose Control Complex Doping Profiles	Damages Substrate Shallow Profiles are Difficult Hazardous Materials
Spin-on	No Damage Created Batch Fabrication	Hazardous Materials Forms Glassy Skin

- Applications of MLD include:



IV. System Design

- Container had to be:
  - Sealed with inlet/outlet for argon
  - Able to condense vapors
  - Withstand over 120°C
  - Be resistant to toluene-based chemical
- Best Design
  - Container chosen locks and seals
  - Hole drilled in top to connect to existing condenser setup
  - Had to design method to connect glass (condenser) to metal container
  - Chose 3D printed nylon sleeve for its high chemical and temperature resistance

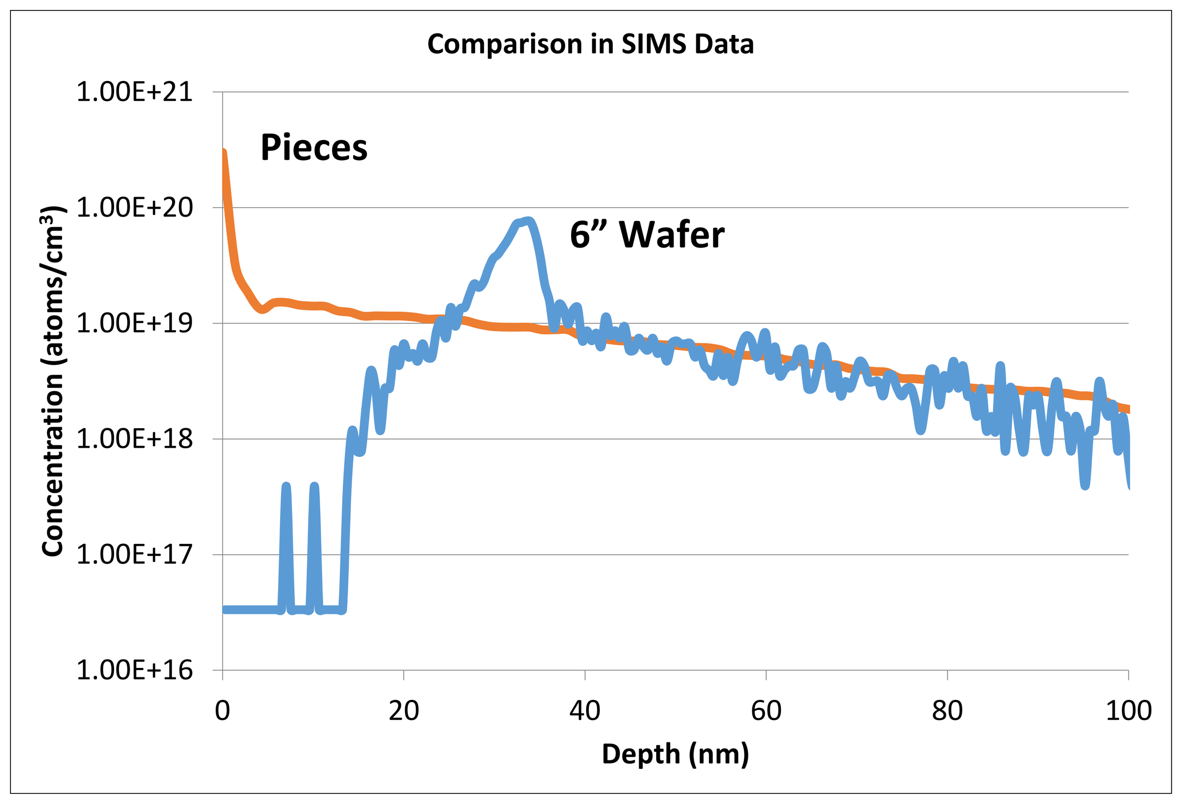


V. Doping Characterization

- To verify the container properly dopes phosphorus, sheet resistance measurements were taken and match collected data on pieces

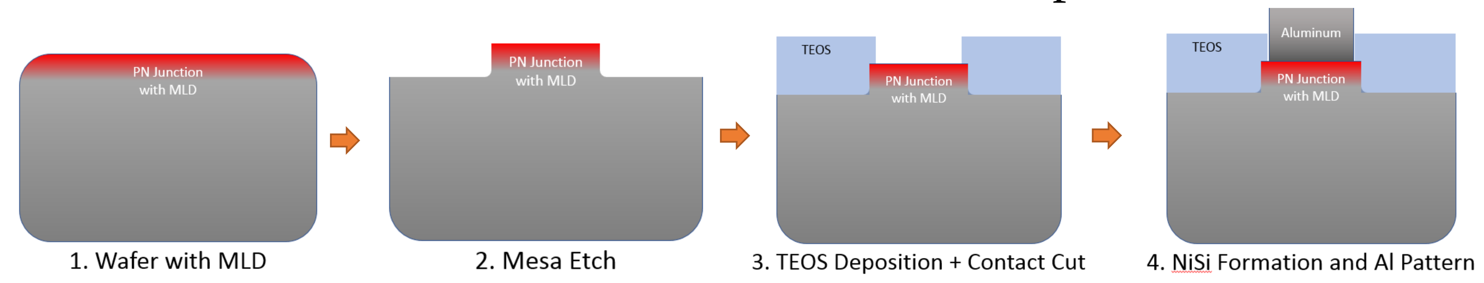
Sheet Resistance Measurements		
	Pre- MLD	Post-MLD
6" Wafer	213 Ω/□	1126 Ω/□
Piece:	191 Ω/□	1031 Ω/□

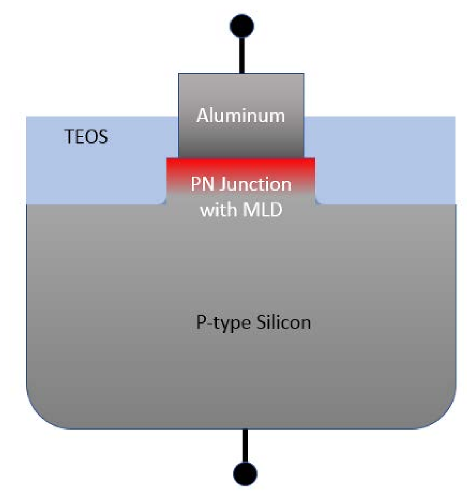
- Secondary Ion Mass Spectrometry shows phosphorus doping that matches doping concentration of wafer pieces. Profile investigation in underway with NREL

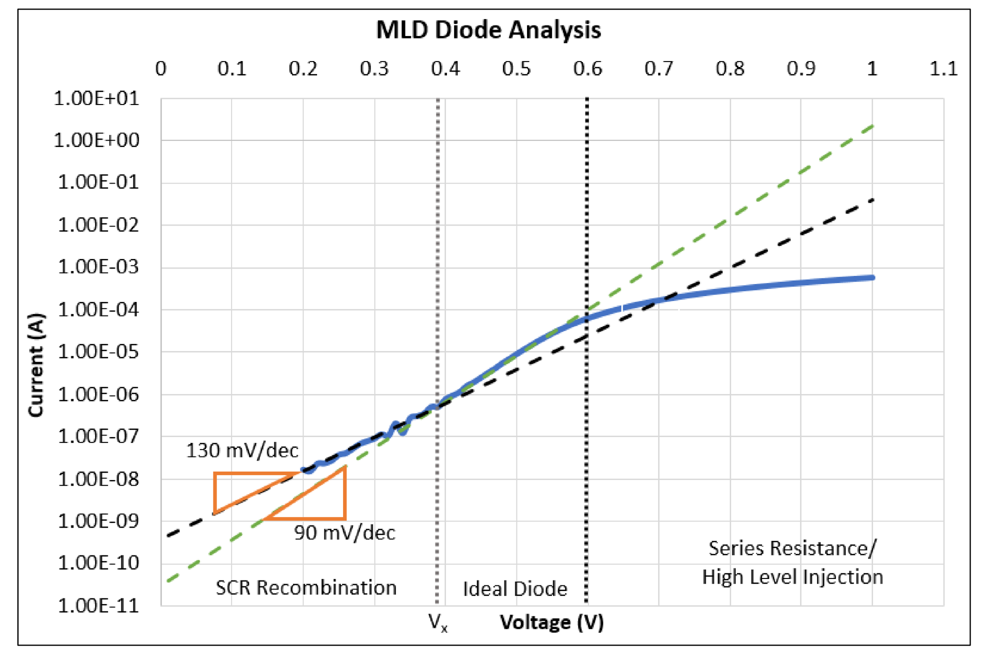


VI. Electrical Characterization

- A 120µm x 180µm square diode was fabricated, tested and characterized
- Carrier lifetime in base extracted as 0.23µs, ideality factors of 1.57 (90 mV/decade) and 2.16 (130 mV/decade) and high series resistance
- First time MLD fabricated diode has been reported







VII. Conclusions

- The design dopes full 6" wafers with similar results to historical data performed at RIT
- Diode fabrication characterized MLD junction for first time

Future Work

- MLD for p-type dopant
- MLD for source/drain and polysilicon of FETs
- MLD for selective emitters for solar cells
- MLD for through-silicon via doping
- MLD for conformal doping of FinFETs

References

- [1] J. C. Ho, et al., Nano Letters, vol. 9, pp. 725-730, Feb 2009.

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