I. Project Objectives

Goal: Develop a Litho-Freeze-Litho-Etch (LFLE) process that can be utilized to create TE mode photonic devices.

- Develop a LFLE process that can achieve a minimum feature separation of ~100 nm
- Create a two level engineering design mask with aligned positive tone and negative tone images
- Develop a UV cure process to produce a compound resist profile on SOI wafer
- Demonstrate a working TE mode ring resonator device to prove validity of the developed process

II. Motivation

Current SMFL equipment and processes limit photonic device fabrication to TM mode devices.

- TE mode photonic devices require minimum feature separation of ~100 nm
- Using a single patterned i-line lithography process can only yield minimum feature separation of ~300 nm
- A double patterned LFLE process can potentially improve efficiency over a more standard LELE process
- Can potentially achieve minimum feature separation of ~100 nm
- Development of a LFLE process will allow creation of TE, TM and mixed mode devices on the same chip

III. Process Development

Proposed LFLE process:
1. Coat, pattern, and develop OR-620 positive photoresist image
2. Crosslink positive image with a UV Cure process
3. Coat, pattern, and develop NLOF-2020 negative photoresist image
4. Etch a-Si layer to create photonic devices

IV. Experimental Results

Initial Lithography Results:

- Waveguide Grating Coupler
- Ring Resonator

References:

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