NMOS Transistor Design and Fabrication for S-Parameter Extraction

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Abstract—A successful test layout for S-parameter analysis was demonstrated. Process characterization accomplished as part of this project demonstrated a pseudo-shallow trench isolation. Active device measurements would have been possible with a DC blocking fixture. 0.37µm-1.0µm transistors were fabricated with a non-ideal characteristic which was due to the source drain implant being blocked by oxide residue from the spacer formation etch.

Index Terms—submicron NMOS, S-parameter measurements.

I. INTRODUCTION

In order to characterize transistor performance for analog circuit design, the frequency response of the devices must be taken into account. S-parameters are used to characterize transistor performance, as a function of frequency [1]. This technique treats a transistor as a two-port network, and measures the power transfer throughout the system being tested. This test has the advantage of being able to extract the parasitic capacitance, which impair transistor operation. S-parameter testing has restriction on the way that the devices may be laid out. The signals must be taken to the device in a ground/signal/ground configuration; this reduces the loss of signal due to incorporation of external noise. In the case of this design a dual polysilicon gate was used so that the source contacts, which are grounded for device testing, would isolate the gate signal as well as the signal being received from the drain. The setup must also be calibrated for the noise already in the system. Special calibration structures are required for this, shorts, opens and through circuits. The shortened devices have the source, drain and gate contacts attached together. This allows for the resistance of the pads to be subtracted from subsequent active measurements. The open circuits eliminate the pad capacitance, and the through circuits eliminate the transmission line inductance. An NMOS transistor process was created keeping parasitic elimination the central design element.

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a power setting of 185 watts. The results from this etch are shown in Fig. 1.

It can be seen from the SEM images that the edge of the etched profile is rough. This roughness was fixed by a thermal oxidation, but first the photoresist was removed from the wafer via an ashing oxygen plasma. The trench depth was varied from 0.75-2 μm. After ashing an RCA chemical clean was performed, this clean consists of three chemical stages, the first chemical stage is a mixture of HCl and Hydrogen Peroxide. This chemical bath removes any metallic components, which are present on the wafer surface. The wafers are rinsed in deionized water, which dilutes and rinses away the HCl mixture. The hydrogen peroxide acts to mediate the HCl so that it does not pit the wafer surface. The next chemical step is a 1-minute etch in 100:1 Hydrofluoric (HF) acid. This removes any native oxide that is on the wafer surface. The wafer is then rinsed, followed by an organic removal step, which is a chemical bath of ammonium hydroxide, and hydrogen peroxide. Following the RCA clean, 1000 Å of oxide was grown in dry oxygen ambient at 1000°C. The wafers were then etched in HF to remove the thermal oxide, and smooth out the etched sidewalls. The wafers were then reoxidized using the same process as before. The purpose of this thermal oxide was to act as a liner for following Tetraethylorthosilicate (TEOS) depositions. The thermal oxide, which is grown rather than deposited, has much less charge, and traps at the silicon/oxide interface. The charge levels with TEOS can be as high as 1x10^{12} electrons/cm². The charge at this interface can cause the formation of a channel which can connect two devices to which a connection is not desired. The original process design included a 2 μm deep trench, which was to be overfilled with TEOS to planarize the surface, so that chemical mechanical planarization would not be required. The wafers were then implanted with 7x10^{13} ions/cm² boron at 80KV. The implantation set the threshold voltage and acted as a channel stop implant. After the implant TEOS was deposited, in the original isolation scheme the TEOS would be etched back so that the desired field oxide thickness could be attained. The problem with this process is that the 2 μm wide trenches as they were filled would cause a void to form in the TEOS, as in Fig. 2.

![Fig. 1. Trench Isolation etch.](image1)

![Fig. 2. Void formed during Trench fill.](image2)

![Fig. 3. Aluminum covering trench fill.](image3)
After the 1 μm trench was filled with 1 μm of TEOS, the TEOS lithographically patterned to form the active region of the device. The wafers were then lithographically patterned with the active level mask, which defined the field oxide. The field oxide was etched to silicon using HF. The resist was stripped from the wafer, and then another RCA clean was performed. The wafers were then oxidized using nitrous oxide for 1 hour at 900°C, approximately 100 angstroms of oxide were grown. Immediately, after the oxidation 2500 angstroms of polysilicon was deposited on the wafer using low pressure chemical vapor deposition. The polysilicon resistivity was measured to be beyond the range of measurement with a 4-point probe. The polysilicon was patterned lithographically using the optimized stepper settings. The polysilicon was etched using the Drytek Quad. The recipe for the etch was 16 sccms of CHF₃, 8 sccms of SF₆, at 70mtorr and 185 watts for 3 minutes, on a quartz carrier. The wafer was implanted with Phosphorous at a dose of 5x10¹² ions/cm² at 20KeV. This implant was for the formation of the low-doped source and drain region. 0.3μm of TEOS was then deposited for spacer formation. The TEOS was etched using a recipe of 70 sccms of CHF₃, 70mtorr pressure, and 185 watts. The approximate time was 9 minutes and 30 seconds. This gave the spacers seen in Fig. 4.

Fig. 4. Spacers formed after anisotropic oxide etch.

After spacer formation the wafers were implanted again with Phosphorous at 20KeV with a dose of 1x10¹⁵ ions/cm². The implant was for source/drain formation. The dopants were activated using the rapid thermal processor, which ramped the temperature from room temperature to 950°C at 60°C/second. Then held the maximum temperature for 1 minute, and then ramped down to room temperature. The wafers were then dipped in HF, and then inserted into the CVC 601 sputter tool. Aluminum was then sputtered using a target power of 1000watts, Ar flow of 5 sccms for 35minutes. This deposited 6500 angstroms of Al with 5% Si. The aluminum was patterned using standard lithography. The aluminum was wet etched for 1 minute in aluminum etch. The wafers were sintered at 450°C for 1 hour. The final device after fabrication is shown in Fig. 5.

Fig. 5. Final device after fabrication.

III. ELECTRICAL TESTS

The devices were test for electrical performance. The results were as follows. Fig. 6 shows the drain current as a function of drain and gate bias for a 0.37-micron transistor. 0.37μm Physically Defined Gate Length

These results can be compared with that of a 0.46μm device shown in Fig. 7.
the oxide spacer was not cleared. The electrical results are shown in Fig. 9.

0.46\textmu m Physically Defined Gate Length

Fig. 9. Device from near wafer edge.

The devices were then tested to find out their frequency response, using a network analyzer. Active device measurements were not possible due to the unavailability of a test fixture, which provides DC blocking to the network analyzer. However, the frequency response of the pads and transmission lines were determined. The pads add an extra 5 ohms of resistance and 45\textmu H of inductance. The frequency response of the pads is shown in Fig. 10.

Phase Plot of the Pad Inductance

Fig. 10. Phase shift due to inductance as a function of frequency.

IV. CONCLUSION

A successful test layout for S-parameter analysis was demonstrated, active device measurements would have been possible with a DC blocking fixture. 0.37\textmu m-1.0\textmu m transistors
were fabricated with a non-ideal characteristic which was due to the source drain implant being blocked by oxide residue from the spacer formation etch.

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REFERENCES


Adam James, from Rochester, NY is graduating from the Rochester Institute of Technology in 2005 with his B.S in Microelectronic Engineering. Adam has work experience co-oping at RIT, and Silicon Laboratories, Austin TX. He will be pursuing graduate studies at the University of Illinois at Urbana-Champaign.