**TANOS (TaN, Al_{2}O_{3}, Si_{3}N_{4}, SiO_{2}, Si) Charge-trap Flash Devices**

Spencer Pringle, Advisors: Dr. Santosh Kurinec, Dr. Michael Jackson

Rochester Institute of Technology, Department of Electrical and Microelectronic Engineering, Rochester NY 14623

---

**Project Objectives**

**Goal:** To demonstrate charge-trapping in a TANOS Stack at RIT

- Gate stack film depositions determined by experimentation, testing
- C-V structures fabricated and tested by patterning gate stack with GCA C-V Mask.
- NMOS charge-trap flash devices currently being fabricated with modified version of AdvCMOS150 Process w/ TANO gate stack.

---

**Charge-trap flash operation**

- Charge-trap flash operates in a similar fashion to EEPROM, only the storage layer is Si3N4 instead of polysilicon. This is advantageous because charge is more likely to remain in the non-conductive charge traps of Nitride than in conductive polysilicon.

---

**C-V Wafer and Structures**

---

**Film Optimization**

**Control Gate: TaN**

Reactively sputtered in partial pressure Ar/N2 ambient in CVC601 plasma sputter. Deposition rates, ~802Å/min, are lower than standard Ta. Refractive index and resistivity (505µΩ-cm) match stoichiometric TaN numbers almost perfectly.

---

**Barrier Oxide:** 100Å, 130Å Al_{2}O_{3}

Deposited in the CHA E-beam evaporator, refractive index describes an Al2O3 film which may have some impurities but should perform well as a dielectric.

---

**Floating Gate (Storage Layer): 100Å Si_{3}N_{4}**

Deposited in ASM LPCVD Tube 2, using a shortened version of the Low Pressure Nitride recipe.

---

**Tunnel Oxide:** 30Å, 50Å, 70Å SiO_{2}

Grown using a shortened version of the Adv CMOS 150 gate oxide recipe which incorporates N_{2}O and O_{2} soaks of equal length, measured on VASE and shown to be in the linear growth region (modeled below). Refractive indexes describe a quality oxide, though trapped charges may be present due to lack of Trans-LC clean.

---

**Measured Device Characteristics**

**Program/Erase C-V**

**Threshold Voltage Characteristics:**

C-V Devices showing charge-trapping flash memory characteristics were successfully fabricated using CMOS processes available in the RIT SMFL. Full Device wafers will be continued and should show enhanced P/E characteristics due to the enhanced ability to program and erase the device by Hot Carrier Injection, rather than by modified Fowler Nordheim tunneling (as in C-V Devices).

**Acknowledgements**

Special thanks to Dr. Kurinec for her insight, Karine Florent for help with XRR, Dr. Lynn Fuller for the use of his Adv_CMOS process, Dr. Jackson, Matt Filmer and Nicholas Edwards for training and help with processing, and most importantly: THANK YOU SMFL STAFF!! We couldn’t do any of this without you!