5-1999

Conference of Microelectronic Research 1999

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**Recommended Citation**  
Wandell, Jerome; Novak, Justin; Fonseca, Carlos; Bolton, Christopher; Wescott, Nate; Winters, Dustin; Gurcan, Burcay; Vachrakankiet, Petya; Schulte, Thomas; Myszka, Michael; Evans, Teresa; Reyes, Alberto; Puchades, Ivan; Wheaton, Tina; Roehner, Keith; and Ritchie, Peter, "Conference of Microelectronic Research 1999" (1999). *Annual Microelectronic Engineering Conference (AMEC) Archive*. Book 9.  
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Editorial

These proceedings contain research papers presented at the 17th Annual Microelectronic Engineering Conference held at the Rochester Institute of Technology (RIT) on May 10 through 12, 1999 by senior undergraduate students of Microelectronic Engineering of RIT. The students graduating with BS degree in Microelectronic Engineering are required to take a four credit hour course, EMCR 660 entitled Seminar/Research in their fifth year. The course consists of submission of a research proposal, related to the field of semiconductor devices and processing, by each student and carrying out the project through the ten week spring quarter. The students are required to present their work at the Microelectronic Engineering Conference held at RIT annually in the month of May and publish in the proceedings.

The class of 1999 presented impressive and technically challenging research projects on various topics ranging from advanced microithography, thin gate dielectrics, novel device structures and processes, circuits, back-end processes, and imaging and luminescent devices.

I congratulate the students for their valuable contributions to the conference and towards the Microelectronic Engineering at RIT. On behalf of the faculty and staff of the Department of Microelectronic Engineering, I wish the students successes in their career ahead.

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Instructor EMCR 660
Professor
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17th Annual Microelectronic Engineering Conference

Rochester Institute of Technology
Rochester, NY 14623

May 10-12, 1999

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I-line Exposure Capability for 6 inch Wafers

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Abstract- The RIT Factory is currently in the development phase for a 6 inch sub-micron CMOS process. The addition of the Canon FPA-2000i1 stepper completes the necessary equipment required to perform a 6 inch photo process at RIT. The major focus of this project is to further the 6 inch photo process development, specifically to setup the exposure process for the first two levels (p-well and active) of the RIT test chip.

TV pre-align mark number 2 and auto-align mark 20P-4F were added to all eleven levels of the RIT test chip layout around the originally designed pattern area. The revised well and active designs were fabricated on a single mask, along with the Canon FRA marks. Six files were written and linked to the job files F983TC_WELL and F983TC_ACT, which can be run to perform the well and active exposures respectively. Well exposure is complete and tested; however, the active exposure will not align to the well pattern. This is most likely due to an error in the active level job and related data files.

1. BACKGROUND

The RIT factory currently fabricates P-well CMOS devices on 4" wafers. This process includes 11 photo levels, p-well through metal 2, and generates devices with a minimum gate size of 6 microns. The next generation of integrated circuits at RIT will be sub-micron CMOS devices, which will be fabricated on 6" wafers. This process is currently in the development phase.

Ground work for the 6" photo process has been underway for some time. The 6" coat and develop tracks are online. RIT recently acquired a Canon i-line wafer stepper, which completes the necessary photo equipment required for the future sub-micron CMOS process. Layouts exist for existing 4" CMOS devices and the design tools necessary for their modification are available. In addition, RIT has a fully functional mask fab, which can create reticles for use with the Canon stepper.

The Canon FPA-2000i1 is a 5X reduction stepper for 6" wafers, which exposes at a wavelength of 365 nm. It is capable of printing 0.5 micron features in conventional i-line photo resists and overlaying patterns to within 0.1 micron error. This exposure tool meets all of the requirements for RIT’s future sub-micron CMOS process.

2. DESIGN

There are two major methods of alignment for the Canon. These are the TV pre-alignment (TVPA) and the wafer auto-alignment (AA). The TV pre-align is the initial alignment sequence. Two TVPA marks are measured with an optical camera and the wafer stage is adjusted according to the measured locations of these marks. The TVPA mark design implemented is the “TVPA Mark #2 – Canon Standard,” which was chosen because it consumes less area than the alternate mark design. Below is a picture of the TVPA mark (Fig. #1) printed with active level photo. The numeral “3” is not part of the actual mark design. It is used to define the level the TVPA mark was printed for. In this situation the active level exposure prints the TVPA mark for level 3 (channel stop).

Fig. #1: TVPA Mark #2

The wafer auto-align is the second and final wafer alignment sequence. Four locations are measured on the wafer and two AA marks are measured per location, which account for x and y stage adjustments. AA marks are measured with two HeNe lasers. Shown below in figure #2 is AA mark 20P-4F. This particular mark design is more effectively measured in a degraded or “washed out” pattern. Unfortunately the HeNe laser is currently down; however, the Canon is capable of alignment using only the TV prealignment.
Figures #3 and #4 display the layouts for the p-well and active areas, which are levels one and two respectively. Each level in this 11 level CMOS process will contain its own set of alignment marks, which are located outside the pattern area. Ideally one would want to always align to the level one pattern to minimize overlay error; however, if this pattern should become degraded to a point where the alignment marks cannot be measured, marks will be needed on the more recently process levels.

The p-well and active patterns for the RIT p-well CMOS test chip can be fabricated on the same reticle. There is space for four separate levels on a single mask. The p-well pattern is dark field and the active pattern is clear field. Fine Reticule Alignment (FRA) marks were inserted outside the pattern area. Refer to figure #5 below for reticle layout.

The job files and the associated data files these jobs are linked to are listed below in figure #6. The process files contain the alignment sequence data. The shot files hold aperture blade settings, shot ordering, and default focus and exposure information. The layout file contains the
shot matrix and the reticle table lists the reticles used and reticle alignment data. The layout and reticle files are common for the entire test chip process.

<table>
<thead>
<tr>
<th>F983TC_WELL (job file)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF983TC_WELL (process file)</td>
</tr>
<tr>
<td>SF983TC_WELL (shot file)</td>
</tr>
<tr>
<td>LF983TC (layout file)</td>
</tr>
<tr>
<td>RF983TC (reticle table)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>F983TC_ACT (job file)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF983TC_ACT (process file)</td>
</tr>
<tr>
<td>SF983TC_ACT (shot file)</td>
</tr>
</tbody>
</table>

Fig. #6: Level 1 & 2 Exposure Jobs

3. RESULTS

The eleven level layout of the RIT test chip has been modified for use with the Canon. The remaining levels can be fabricated on as few as two reticles if metal 2 is not required.

Level one (p-well) exposure with the Canon is setup. Active level lithography remains incomplete. Useable pattern overlay could not be achieved. This problem is most likely due to an overlooked parameter in one of the job files created for the active level exposure.

The continuation of the 6" photo process at RIT will need to include active level job testing. The remaining test chip levels can be fabricated on 2 reticles and their respective job files need to be written. These files will be very similar to the active level job.

There are some optional repairs for the Canon, which are not required for processing; however, these modifications will improve equipment performance. The FRA lamp is out and if this is replaced the operator will be relieved of having to manually align masks. In addition, the repair of the HeNe laser would reduce overlay error, which is not a large issue for the test chip layout; however, the future sub-micron process will require tighter control of pattern overlay.
Critical Dimension Analysis on the RIT Canon i-line Stepper

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Abstract - This project involved the simulation and analysis of critical dimensions (CD) using the RIT Canon 2000i1 i-line stepper. This was accomplished by optimizing the stepper parameters for specific resist feature widths. There are many tools and methods that lithography engineers have at their disposal for use in optimizing current and future lithography processes. The focus-exposure (F-E) matrix and resulting plot are integral parts of standard IC processing. It is one of the most important plots used in lithography since it demonstrates how exposure and focus work together to affect critical dimension, sidewall angle, and resist thickness loss data. This data is then analyzed to determine the process capability or useable limits for both focal depth and exposure latitude values for a given lithography process.

1. INTRODUCTION

The experiment performed focused in on three common substrates that are used in IC processing. These substrates included oxide, polysilicon on oxide, and aluminum on oxide at typical thicknesses for the RIT 6" CMOS process. To begin this analysis, E0 (dose-to-clear) for each material was determined by using a full field exposure of the resist. With that data, a focus-exposure matrix was setup and run for each of the corresponding substrates to determine the optimal settings to generate 0.5μm, 0.7μm, and 1.0μm features that were then measure by a KLA-Tencor 8100XP CD SEM. The CD data was then plotted against the corresponding focus and exposure settings to create the Bossung plot, as shown in Figure 1. This plot was then used to graphically represent the data for ease of analysis in determining the potential exposure latitude and focal depth needed to maintain image fidelity. With the analysis of multiple feature sizes, the optimum parameters were determined by overlapping the process windows and examining the common area, as shown in Figure 2. The effects of a bottom anti-reflective coating (BARC) was also investigated to determine the amount of process improvement that was gained when revolving the same features.
2. SIMULATIONS

Before beginning the lab portion of this experiment, the boundary conditions for focal depth and exposure latitude had to be theoretically calculated. Since no previous baseline has been performed on this process, simulations and initial lab testing was performed to determine a suitable starting point. This was accomplished with the help from the ProLITH 6.0 software package. To theoretically determine the useable focal depth, the Canon 2000i1 stepper parameters were obtained and entered into the modeling software to determine their effect on the aerial image of various feature sizes. The Figure 3 below represents the optimum aerial image for this given system and feature size.

\[ UDOF = k_2 \frac{\lambda}{NA^2} \]

\[ k_2 = \frac{UDOF \times NA^2}{\lambda} \]

Table 1 Simulated TDOF and k1 values

<table>
<thead>
<tr>
<th>Feature Width</th>
<th>TDOF</th>
<th>k2</th>
</tr>
</thead>
<tbody>
<tr>
<td>500nm</td>
<td>1.5\mu m</td>
<td>1.111</td>
</tr>
<tr>
<td>700nm</td>
<td>1.8\mu m</td>
<td>1.333</td>
</tr>
<tr>
<td>1000nm</td>
<td>3.0\mu m</td>
<td>2.222</td>
</tr>
</tbody>
</table>

These k1 factors were then later compared to that of the k1 factors calculated from the experimental UDOF values.

3. EXPERIMENT

Once the theoretical focal depth for each feature size was calculated, the next step of determining a minimum exposure dose or dose-to-clear (Eo) was completed. Again, due to the fact that this was a completely new and previously untested process there was no baseline to use as a reference point for the exposure dose. To begin this analysis, Eo (dose-to-clear) for each material was determined by using a full field exposure of the resist for each substrate material as seen in Figure 4. Once calculated, these values were used as initial exposure doses for each of the subsequent focus-exposure matrices.

To run each of the F-E matrices, the substrate material was first grown or deposited depending upon the type needed. For this project, three substrates and one bottom anti-reflective coating were chosen for this project for their use in current RIT CMOS processing. The substrates and corresponding thickness are shown in table 2.

Table 2 Substrate Type and Thickness

<table>
<thead>
<tr>
<th>Substrate Type</th>
<th>Target Thickness</th>
<th>Actual Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum*</td>
<td>5000Å</td>
<td>5123Å</td>
</tr>
<tr>
<td>Oxide</td>
<td>1000Å</td>
<td>1015Å</td>
</tr>
<tr>
<td>Polysilicon*</td>
<td>3000Å</td>
<td>2943Å</td>
</tr>
<tr>
<td>BARC**</td>
<td>1800Å</td>
<td>1819Å</td>
</tr>
</tbody>
</table>

* The aluminum and polysilicon substrates were deposited onto 1000Å-oxide film.
** The BARC thickness was chosen for the maximum i-line absorptive characteristics between 1700Å - 2000Å.

With the Eo and TDOF range data along with substrates, each F-E matrix was then setup on the Canon stepper using the standard Canon F-E job with modified parameters for each of the substrates. The initial and increment values for both exposure and focus were setup as seen in table 3. The wafers were exposed in an 8x8 array with focus increasing by column and exposure.
increasing by row. The reticle used was the standard resolution reticle that is send along with each tool. This mask has a series of resolution bars ranging from 2μm down to 0.2μm.

Table 3 F-E Parameter Settings

<table>
<thead>
<tr>
<th>Substrate Type</th>
<th>Initial Exposure</th>
<th>Exposure Increment</th>
<th>Initial Focus</th>
<th>Focus Increment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>100mJ/cm²</td>
<td>10mJ/cm²</td>
<td>-0.8μm</td>
<td>0.2μm</td>
</tr>
<tr>
<td>Oxide</td>
<td>250</td>
<td>10</td>
<td>-0.8</td>
<td>0.2</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>120</td>
<td>10</td>
<td>-0.8</td>
<td>0.2</td>
</tr>
<tr>
<td>BARC</td>
<td>240</td>
<td>10</td>
<td>-0.8</td>
<td>0.2</td>
</tr>
</tbody>
</table>

Once the wafers were exposed, each was reviewed optically for image fidelity. The wafers were then sent to KLA-Tencor, in San Jose, California for measurement on the 8100XP CD SEM using recipes setup up for this mask design previously. Returned was the raw data and images for each substrate for analysis.

The raw data was first organized into the proper input file format needed by the ProDATA software for analysis.

4. ANALYSIS

Each substrate was analyzed for the three feature sizes 500nm, 700nm, and 1000nm dense resist lines. As demonstrated earlier each set of raw data was entered into the ProDATA software for analysis. Output by this software was a contrast curve and Bossung plot for each corresponding substrate and feature as seen in Figure 5.

Figure 5 Bossung Plot for 500nm Polysilicon

![Bossung Plot for 500nm Polysilicon](image)

There was 10% exposure latitude and a 10% critical dimension tolerance set as boundary conditions for analyzing the CD data. For each Bossung plot the software analyzed the data and extracted the potential process window for exposure and focus target values as well as the useable focal depth. Depending on the strictness of a given exposure latitude will determine the useable focal depth for that same system, as seen in Figure 6. A corresponding process window was calculated for each substrate. The windows within each substrate were then overlapped to extract a common process window area. This window determined the target focus and exposure settings and useable focal depth common for all three-feature sizes, as seen in Figure 2. A second exposure latitude graph was also generated for all three features, which was analyzed similar to the Figure 6.

5. RESULTS

Each of the four substrates was analyzed using this same method above. The simulation data was analyzed first to determine an aerial image and theoretical focal depth that should be experienced by an ideal system. These values were calculated by hand on each of the simulated aerial image plots. The resulting Bossung plots that were produced from the experimental data did not seem to demonstrate the standard format for a Bossung plot as in the simulations. Each plot seemed to be only a section of the whole plot, which lead to an error that was made. Unfortunately, this error was made and the focal ranges were underestimated when calculated. Even with this issue, the plots still demonstrated a range of CD values above and below the CD tolerance, which was desired for analysis.

The polysilicon was the first set of CD data that was entered into ProDATA. Each of the three Bossung plots demonstrated a similar trend with the CD data, which seemed to show early on that the chosen focal range was not large enough. This same point was reiterated in the exposure latitude graph as seen in Figure 7.
Therefore, the focal depth for many of the Bossung plots showed the same pattern.

The next CD data set analyzed was the oxide substrate. The focal range for this material showed an improved spread in CD data, though not the complete range. The limiting feature showed to be the 0.5μm feature. There was a large decrease in the process window when compared to the 1.0μm and 0.7μm window as seen in Figure 8.

Figure 8 Oxide Process Window

... 

Again, the resulting usable focal depth for this substrate was much lower than the expected when compared to the simulation focal depth.

The sputtered aluminum substrate was difficult to analyze due to the absence of the 0.5μm and 0.7μm resist features at all focus settings. As seen in Figure 9, even with the 1.0μm feature there was an unusually low UDOF at 0.15μm, which varied from the usual 2.5-3.0μm that is normally witnessed. Both of these issues were explained by the overexposure of the resist and the high reflectivity.

The final substrate that was analyzed for this experiment was the Brewer Science Inc. i-line BARC material. This material was coated to a thickness of 1800Å to utilize the optimum absorbing properties of the BARC. With such a high absorbing material, the exposure dose was increased to have complete resist exposure. The CD data, unfortunately, did not demonstrate the resolution enhancing properties that were expected in this experiment. The focal depth of oxide, also a high absorbing material, was greater than that of the BARC as seen in Figure 10. Therefore, the CD data had the effects of an unknown factor that skewed the data.

Figure 10 BARC Focal Depth

...
Table 4 Resulting Target Focus/Exposure, and Focal Depth Setting

<table>
<thead>
<tr>
<th>Substrate Type</th>
<th>Target Exposure</th>
<th>Target Focus</th>
<th>UDOF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>237</td>
<td>-0.54</td>
<td>0.15</td>
</tr>
<tr>
<td>Oxide</td>
<td>257</td>
<td>-0.54</td>
<td>0.60</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>152</td>
<td>0.1</td>
<td>0.85</td>
</tr>
<tr>
<td>BARC</td>
<td>295</td>
<td>-0.59</td>
<td>0.42</td>
</tr>
</tbody>
</table>

When comparing process window for different substrates, the optimum parameter settings varied greatly for exposure and focus as seen in Table 4. This characteristic was related to the difference in the reflectivity of each substrate. Oxide and BARC, both highly absorptive, required a higher exposure dose when compared to the highly reflective substrates of polysilicon and aluminum. Except for polysilicon the optimum focus setting for each centered on -0.6 μm for this experiment.

Table 5 Comparison of k2 values

<table>
<thead>
<tr>
<th>Substrate Type</th>
<th>Sim. k2</th>
<th>Exp. k2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>1.111</td>
<td>0.111</td>
</tr>
<tr>
<td>Oxide</td>
<td>1.111</td>
<td>0.444</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>1.111</td>
<td>0.630</td>
</tr>
<tr>
<td>BARC</td>
<td>1.111</td>
<td>0.311</td>
</tr>
</tbody>
</table>

From k2 comparisons extrapolated from Table 5, the k2 were well under the simulated values that were gathered. A small amount of error should be seen when comparing these values due to non-ideal processing. But due to the focal range error that occurred during the simulation, only a small section of the greater process window was captured during the experiment for many of the Bossung curves and the resulting k2 values were lower than expected. This is not to say that the data was not usable, just that the full UDOF was not able to determined during this baseline test. Unlike photolithography engineers, the project only allowed for a single iteration for the F-E matrices. In industry if the optimum Bossung plot is not obtained the lithographer will just redo the experiment and re-measure the features. Therefore, continued testing with a larger focal range will add to the data already obtained and home in, with more confidence, the optimized process window for each substrate.

6. CONCLUSIONS

This project involved the simulation and analysis of critical dimensions (CD) using the RIT Canon 2000i i-line stepper. This was accomplished by optimizing the stepper parameters for specific resist feature widths. This was completed, but unfortunately due to a calculation error that was made the optimized parameter settings that were obtained were only a section of the complete process window that was desired. Overall, the experiment and procedures were a success even with the error that occurred. Further testing, with a larger focal range, these parameter settings can be realized. Besides CD values, sidewall angle and resist loss are two other parameters that may be explored when testing the effects focus and exposure settings.

7. ACKNOWLEDGMENTS

The author acknowledges Dr. Bruce Smith and Joe Perez for guidance in this work and KLA-Tencor and FINLE Technologies for equipment and software support.

Justin W. Novak, originally from Syracuse, N.Y, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 1999. He obtained co-op work experience at Motorola, Twinstar Semiconductor, and KLA-Tencor. He is joining Photronics, Inc. as an equipment development engineer starting in August 1999.

1 ProDATA v1.0, FINLE Technologies, 1999
2 Ibid.
3 ProLITH v 6.03, FINLE Technologies, 1999
Amorphous Silicon for 157nm Lithography

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Abstract - Amorphous silicon (α-Si) was investigated as a potential masking material at 157nm wavelength. Characterization of α-Si included film deposition on CaF₂ (calcium fluoride) substrates through reactive sputtering, spectroscopic ellipsometry in the UV range, reflection and transmission at 157nm wavelength, and extraction of optical constants (n&k) with a commercial software package. Experimental results suggest that α-Si films deposited at RIT have similar optical constants as published values in the UV range. Simulation work suggests that a 50Å silicon nitride film can be used as an anti-reflective layer to minimize reflections at the a-Si / air boundary. Consequently, silicon nitride films were also investigated in this work. Since these films (stack) must be patterned for mask applications, proper dry etch selectivity among these materials must be achieved.

I. INTRODUCTION

As optical lithography below 193 nm is explored, materials issues become more challenging. The challenge lies in obtaining materials whose optical properties allow them to be applied as masking layers, optical layers, antireflective layers (AR), and phase-shift masking at 157nm, or at other potential VUV wavelengths. Historically, chromium has been used as a masking material at g-line, i-line, and 193nm lithography. Its optical properties (high absorption and adequate optical density) at UV wavelengths have been the main reason why chromium is the preferred choice as a masking material. The problem with using chromium at shorter wavelengths is that its extinction coefficient (k) is relatively lower than other materials at 157nm, thus resulting in a lower absorption coefficient (α). Figure 1 shows the absorption of several materials as a function of wavelength. Furthermore, chromium may not meet optical density (OD) requirements at a film thickness < 1000Å as a masking material at 157nm to give adequate modulation (aerial image contrast). A film thickness <1000Å is desired in order to meet industry standards and to provide satisfactory etched profiles at projected aspect ratios.

Masking material alternatives do exist at 157nm. One such alternative is amorphous silicon (α-Si). As shown in Figure 1, amorphous silicon has a higher absorption coefficient than Chromium at 157nm. Consequently, α-Si exhibits an optical density of 5.0 at 157nm at a film thickness less than 1000Å. However, other considerations such as mask reflectivity at 157nm must be taken into account. The reflectivity of α-Si is relatively high at 157nm. The use of an anti-reflective layer may be required with α-Si as a masking layer. This work investigated thin film deposition, etch considerations, and optical characterization (simulation and experimental data) of amorphous silicon with an AR layer.

II. BACKGROUND

To set a starting point for this project, theoretical calculations for film thickness were employed with the use of fundamental physical equations and industry standards. Equations 1-3 can be used to determine the theoretical film thickness that meets OD requirements. Industry has set OD values of about 3 to 5 as adequate measures for opaqueness of the masking material.

\[ OD = -\log(T) \]  
\[ T = (1-R_1)(1-R_2)e^{-\alpha t} \]  
\[ R = \frac{(n_1 - n_2)^2 + k_1^2}{(n_1 + n_2)^2 + k_1^2} \]

Using published optical constant values for the materials of interest at 157nm wavelength, the required film
thickness can be calculated. Table 1 shows the published optical constants for α-Si, CaF₂, and quartz (SiO₂).

<table>
<thead>
<tr>
<th>Material</th>
<th>n @ 157nm</th>
<th>k @ 157nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>α-Si</td>
<td>0.6749</td>
<td>1.6277</td>
</tr>
<tr>
<td>CaF₂</td>
<td>1.5678</td>
<td>0</td>
</tr>
<tr>
<td>SiO₂</td>
<td>1.6895</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 1: Published optical constants for several materials.

Figure 2 presents a theoretical plot of transmission vs. film thickness for α-Si at 157nm wavelength. This graph suggests that a 60nm film thickness can provide an OD value of about 4. An OD of 4 was arbitrarily chosen since it is in the middle of the range for standard OD values. These theoretical values were verified on RIT's lithography research web-site (http://www.rit.edu/~635dept5).

![Figure 2: Transmission of α-Si film thickness at 157nm.](image)

Since about 50% reflection is expected (Eq -3) at the α-Si/air boundary, simulation and modeling for an A.R. layer were also carried out. Previous knowledge and suitability of certain materials allows for choosing adequate materials as A.R. layers. Silicon nitride (Si₃N₄) was chosen for investigation as depicted in Figure 3.

![Figure 3: α-Si masking scheme with A.R. layer.](image)

Simulation was performed using PROLITH software program and published optical constants (Palik) for Si₃N₄ at 157nm wavelength (n = 2.6750, k = 0.9236). The simulation results indicate that a 50Å nitride film can minimize reflection down to about 4% and a large process latitude can be achieved in terms of the extinction coefficient (k) as shown in Figures 4 and 5, respectively.

![Figure 4: Swing curve for Si₃N₄/α-Si stack.](image)

The goal of this project was to identify or extract the optical constants of deposited films. More specifically, in order to justify the use simulation results, the optical constants must be verified by comparison of extracted values and published values. The procedure for extraction of optical constants is described in the following section.

### III. EXPERIMENTAL

Film deposition was executed by reactive sputtering in a Perkin Elmer 2400 sputter system. Thin films were deposited on CaF₂ substrates and thickness measurements were done with profilometry technique (Tencor stylus). The deposition parameters for α-Si and Si₃N₄ are given below. Chamber conditions and preparation can greatly impact the quality of the films. One way to ensure high...
quality films is to achieve a low chamber base pressure (~10^-7 Torr). This was typically achieved in the Perkin Elmer system by a minimum of a 6-hour pump down.

\[ \text{α-Si Process conditions:} \]
- 1000 Watts
- 30 sccm Ar
-Rotation mode
-Deposition rate = 12.5 Å/minute

\[ \text{Si}_3\text{N}_4 \text{ Process conditions:} \]
- 1000 Watts
- 30 sccm Ar / 10 sccm N\textsubscript{2}
- Rotation mode
-Deposition rate = 5 Å/minute

**Plasma etch studies**

Since ultimately the stack must be patterned with an anisotropic dry etch process, this work also investigated etch selectivity among the different materials under investigation. For these studies, α-Si and Si\textsubscript{3}N\textsubscript{4} films were deposited on thermal oxide substrates. The etch recipes are given below

\[ \text{α-Si Etch conditions:} \]
- 40 Watts
- 42 sccm SF\textsubscript{6}
- 400 mTorr

\[ \text{Si}_3\text{N}_4 \text{ Etch conditions:} \]
- 50 Watts
- 30 sccm SF\textsubscript{6} / 7.5 sccm O\textsubscript{2}
- 300 mTorr

**Extraction of optical constants**

The extraction of optical constants consisted of obtaining a) ellipsometric data (Δ and Ψ) in the UV wavelength range and b) transmission and reflection at 157 nm wavelength. Ellipsometric data was obtained with a variable angle spectroscopic ellipsometer operating from 190 nm to 800 nm. Using a software program called WVASE™ (Woollam Variable Angle Spectroscopic Ellipsometry), the ellipsometric data was fitted to a model in which the expected optical constants (as a function of wavelength) were those of the published values. In addition, the transmission and reflection data at 157 nm was to be used to extract n & k down to 157 nm. The 'goodness' of fit was then reported as a mean square error (MSE).

It is expected that some differences may be observed between the optical constants of deposited films at RIT and the published values. However, the closer the films exhibit n & k values as expected, a higher confidence exists in the stack masking performance as expected from the simulation work.

**IV. RESULTS AND DISCUSSION**

Figure 6 and 7 show the extracted and expected optical constants for α-Si and Si\textsubscript{3}N\textsubscript{4}, respectively. Relative good fits were observed in both plots. The α-Si film exhibited a better fit (MSE = 0.7) than the silicon nitride film (MSE = 5.4). More importantly, a better fit was observed in the UV region for the α-Si film than in the longer wavelength region. This is critical to the studies since the focus of this work concentrates on the optical constants in the VUV region. Note that no optical constants were extracted down to 157 nm. Due to time constraints, transmission and reflection data could not be obtained in a timely manner prior to the authoring of this report. Therefore, realize that until this data has been received from outside laboratories, more fitting will be performed and extraction of optical constants down to the VUV region is expected. However, it is worthwhile to emphasize that because of such great fit in the UV region, a similar fit is expected once the transmission and reflection data is used. Verification of expected results will be published in a future progress report.

The poor fit in the longer region for the α-Si film may be attributed to a crystalline silicon behavior. Another reason could be that some impurities (i.e., Argon, residual oxygen, etc.) might have been incorporated during film deposition. Thus, adequate deposition conditions are desired in order to obtain highest quality films as possible. Similarly, the nitride film exhibited large differences in the optical constants. For this material, it is believed that difficulty in obtaining stoichiometric Si\textsubscript{3}N\textsubscript{4} films is responsible for the differences in optical constants. In general, a MSE of 5.4 is regarded as a good fit for this type of film.

Figure 6: Amorphous silicon optical constants. (MSE = 0.7)
V. CONCLUSIONS

Optical characterization, by means of extraction of optical constants, for amorphous silicon and silicon nitride films has been successfully assessed in the wavelength region of 200nm to 800nm. Although extraction of optical constants down to 157nm could not be assessed at this time, due to time constraints, very good fits in the UV region were observed for both amorphous silicon and silicon nitride films deposited at RIT. Thus, similar results are expected once data at 157nm is incorporated to the model. Plasma etch results indicate that a 1:1 etch selectivity between the amorphous silicon and silicon nitride may be feasible to achieve with a SF₆ and O₂ chemistry. Additionally, an etch-stop layer may be required to minimize substrate etching.

ACKNOWLEDGEMENTS

The author would like to thank the following people for their input in this work:

Dr. Bruce Smith, Lena Zavyalova, Anatoly Bourov, Michael Cangemi, and Tropel Corporation.

Special thanks to Scott Blondell and Richard Battaglia for maintaining the laboratory equipment.

REFERENCES

Resist Characterization for 157nm Lithography

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Abstract — A resist characterization experiment was performed utilizing 157nm Vacuum Ultra-violet (VUV) Lithography. A number of older technology resists such as MXP8, APEX-E, and UVIII were placed in the beam path of a Lumonics Series 700 fluorine excimer laser and subjected to timed exposures on the tool. The features were then developed in a low normality CD26 developer and characterization curves for each of the resists were plotted. Through the experimentation it was found that each of the three resists investigated was able to clearly demonstrate imaging qualities at 157nm. The contrast curves of the MXP8 and APEX-E resist indicate that they may have the characteristics to be used as early negative resists at 157nm, while the Shipley UVIII 248nm resist demonstrated both positive and negative characteristics due to competing mechanisms within the resist.

I. INTRODUCTION

As the demand for semiconductor devices continues to exponentially rise in this technology driven society, the geometry sizes of the devices must follow the downward shrinking spiral to compensate for the increased transistor densities on the chip. This continual reduction in feature geometry has been made possible primarily by phenomenal advances in the field of lithography. Conventional lithography has been able to push through many of the assumed optical limits with the integration of highly unconventional ideas that have proven to be very useful. Projection lithography at 157nm, up until this point, has always been one of these assumed unconventional ideas that would never make it into production. Numerous problems with the construction of a viable laser source and the transmissive quality of most production mask and substrate materials at 157nm have prevented its inauguration into high volume manufacturing. However, recent developments in mask making, especially the introduction of calcium fluoride instead of fused silica, as well as the commercial availability of high volume sources have made 157nm a very attractive transition for lithography. Lithography at 157nm holds the key to the expansion of optical lithography to sub-100nm devices and probably even into the 50nm realm (see figure 1), but its infancy lends itself to requiring more substantial characterization.

II. BACKGROUND

In 1998, RIT’s 193nm ArF Lumonics Series 700 excimer laser was converted into a 157nm F\textsubscript{2} excimer laser (see figure 2). This provided a viable and adequate source to be used in a resist characterization study at 157nm lithography. Lithography at 157nm offers several advantages over conventional lithography at 248nm and
193nm. The shorter wavelength introduces an inherent resolution enhancement, while the technology itself is a natural extension to current lithographic processes, in that it uses excimer lasers, refractive optics, and transmissive masks. The primary enhancement of going to the much shorter wavelength of 157nm also provides for a number of disadvantages that may slightly inhibit the desired transition to the new technology. At extremely short wavelengths such as 157nm, the resist thickness begins to approach the total focal plane depth of the optics. This factor combined with desired high numerical aperture values lead to an overall reduction in the depth of focus at 157nm, therefore very thin imaging layers are needed for single layer processing.

The extreme wavelength of the source introduces certain absorption problems with conventional resists as well. Many hydrocarbon polymers (see figure 3) appear to absorb too much of the radiation even when the film thickness is kept to less than 100nm. Thusly, new techniques must be developed to deal with surface imaging. The resists that were investigated throughout this research were MXP8, UVIII, and APEX-E. The resists were either thinned down beyond conventional means (500-1500Å) in order to create ultrathin thicknesses or they were tested at their standard coat thickness at 4000rpm. This shallow thickness allows for the exposure energy of the F$_2$ laser to penetrate the resist without the energy being wasted by absorption in only the top region.

![Absorption of various thin films at 157nm](image)

**Figure 3: Absorption of various thin films at 157nm**

At this point in time, no commercial resists have been created in industry that can successfully utilize the 157nm wavelength for production. In order to demonstrate imaging capability at this wavelength, a new and innovative resist process must first be researched and developed. However, instead of relying upon manufacturers to develop a brand new resist design, a number of resists employed in older technologies were investigated in this experiment through the use of ultrathin resist coatings and top surface imaging (TSI).

One other disadvantage of the transition to 157nm is that traditional fused silica masks are too absorptive at 157nm, and cannot be used for this experiment. Calcium fluoride is being used as a substitute in industry, but due to complications in fabrication, it was not be used as a mask in this experiment. Therefore a hybrid reticle consisting of a completely reflective, aluminum hardmask was used to effectively block the radiation in the unexposed regions.

### III. EXPERIMENT

Before any type of characterization of the laser began, the optimal settings of the laser were investigated using the initial research of the laser conversion as a starting point. The optimal gas fill settings found for the laser were set at 85mbar of buffered F$_2$ with the Helium introduced at 3500mbar and then evacuating the system to around 3200mbar, and ran at 37.6kV and 50pps. This gas mixture provided a substantial amount of lasing with a minimal amount of arcing in the system. Voltage arcing tends to damage the electrodes in the laser. The laser spectrum was then verified through the use of a phosphor detector, Yttrium oxide doped with Europium that had been previously suspended in isopropanol and coated on the inside of a blank glass mask. This is necessary due to the fact that there is no available detector at RIT that would not become damaged at the fluorine excimer's high-energy wavelength.

In order to prepare the resists for exposure in the beam path, each of the resists was thinned out to different dilutions and then coated onto wafers in order to determine which thicknesses were possible and which could be used in the experiment. Prior to coating on the hand-spinner, the wafers were dehydration baked at 120°C for two minutes to remove any excess moisture and then surface primed with HMDS at 3500rpm for one minute. The resists were then coated using a coat recipe at 4000rpm and soft baked at 120°C for three minutes. The excessively high softbake step was utilized to help eliminate as much solvent as possible leaving only the resist polymers to crosslink in the exposure system. Table 1 gives the resist coat thickness for each dilution as well as the modified refractive index (calculated using the Cauchy coefficients) that was necessary for accurate measurement on the Nanospec.

Once the thicknesses were measured on the Nanospec and recorded, the wafers were then scribed into small pieces. Breaking the wafers up is a necessary step due to the fact that there is no optic setup on the excimer laser.
Table 1: Resist Thickness and Refractive Index data

<table>
<thead>
<tr>
<th>Resist</th>
<th>Dilution</th>
<th>Coat Thickness (4000rpm)</th>
<th>Refractive Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>MXP8</td>
<td>None</td>
<td>1939Å 1.589</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1:1</td>
<td>1900Å</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1:2</td>
<td>1209Å</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1:2.5</td>
<td>920Å</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1:3.5</td>
<td>485Å</td>
<td></td>
</tr>
<tr>
<td>APEX-E</td>
<td>None</td>
<td>6358Å 1.5692</td>
<td></td>
</tr>
<tr>
<td>UVIII</td>
<td>None</td>
<td>6570Å 1.549</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1:1</td>
<td>2193Å</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1:2</td>
<td>1614Å</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1:3</td>
<td>942Å</td>
<td></td>
</tr>
</tbody>
</table>

and there is no wafer stage, but the wafers must be somehow placed into the exposure beam path. This was accomplished by designing and fabricating a modified wafer chuck (see figure 4), constructed of PVC piping and a glass mask blank. The addition of the N₂ inlet and outlet are necessary so that a nitrogen purge may be introduced into the exposure path to remove any hydrocarbons and oxygen that may absorb the 157nm radiation.

The pieces of the wafers were then covered in an aluminum hardmask and placed directly onto the glass plate using adhesive on the backs of the wafers. Each of the resists was then subjected to timed exposures on the laser and then developed in a low normality CD26 developer to bring out the features.

Prior to developing the Shipley 248nm UVIII resist, however, an additional two-minute post-exposure bake at 120°C was employed in order to activate the chemically amplified resist reaction.

IV. RESULTS AND CONCLUSIONS

Once all of the thickness measurements for each resist were finally performed and the data collated, it was placed into Microsoft Excel for graphical analysis. It could be seen through the use of the characteristic curve plots that the most frequent exposure mechanism for the resists was of a negative nature. This would be due to the high-energy 157nm wavelength crosslinking the polymeric compound in each of the resist systems. All three of the resists exhibited this negative nature with a dose to gel or a timed exposure to gel, while the very thick (~6500Å) UVIII resist exhibited positive resist characteristics.

The characteristic curves (see graphs 1-4 on next page) were each plotted similarly to conventional lithographic means, however, without a true dose detector, the real exposure dose could not be found. This leaves the graphs with a normalized thickness of the resist as a function of the log of the timed exposure in seconds. This does not present any real issues in terms of characterizing the resists, but it does, however, leave the contrast or gamma values calculated from the graphs as only comparative values between the three resists. These gamma results cannot be treated as conventional contrast values until they are re-calculated when the exposure dose of the excimer laser can be found.

Both the MXP8 and APEX-E demonstrated very successful negative resist qualities with distinctive exposures to gel and steep on and off contrast curves. The APEX-E had the highest gamma of 301 with about a 200Å increase in thickness after exposure due to crosslinking. All of the values from the characteristic curves are summarized in table 2 below.

Table 2: Summary of Characteristic Curve data

<table>
<thead>
<tr>
<th>Resist</th>
<th>Gamma</th>
<th>Thickness Loss/Gain</th>
<th>Action</th>
<th>Exposure to Gel/Clear (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MXP8</td>
<td>55</td>
<td>+86Å</td>
<td>Neg.</td>
<td>9</td>
</tr>
<tr>
<td>APEX-E</td>
<td>301</td>
<td>+210Å</td>
<td>Neg.</td>
<td>18.8</td>
</tr>
<tr>
<td>UVIII</td>
<td>154</td>
<td>+130Å</td>
<td>Neg.</td>
<td>9</td>
</tr>
<tr>
<td>UVIII</td>
<td>-12</td>
<td>-527Å</td>
<td>Pos.</td>
<td>300</td>
</tr>
</tbody>
</table>
Graph 1: Normalized MXP8 Resist Contrast Curve

Graph 2: Normalized APEX-E Resist Contrast Curve

Graph 3: Normalized UV3 Resist Contrast Curve (Thin)

Graph 4: Normalized UV3 Resist Contrast Curve ( Thick)

It is interesting to note the results obtained for the UVIII resist. At very thick resist coatings of around 6500Å, the chemically amplified resist attempted to act as a positive resist, but fell short with a great deal of scumming and a poor overall nature to the characteristic curve. However, at a very thin coating of around 945Å, the resist attempted to take on negative characteristics with a very short dose to gel of about nine seconds. This can be understood to be competing mechanisms within the resist. On one hand, the chemical amplification is a positive acting mechanism trying to use the exposure energy to rapidly dissolve the exposed regions, while at the same time some crosslinking of the polymer is happening in the same regions. This creates the lackluster appearance for both characteristics curves.

In conclusion, lithography at 157nm will definitely be the next feasible technology node for exposure systems. However, new resists or processes may need to be developed in order to compensate for the current lack of usable resists in manufacturing. Single layer resist processing, utilizing ultrathin resists, may become possible, but certain constraints may be introduced such as a higher susceptibility for defects and problems with current metrology tools. A more feasible approach for production may be the use of a bilayer or silylation schemes that involves thin imaging layers on top of a thicker planarizing layer and a dry etch stop such as in the DESIRE process. Either way, 157nm lithography will help guide microlithography into the sub-100nm realm.

V. REFERENCES

VI. ACKNOWLEDGEMENTS

The author would like to acknowledge Dr. Bruce Smith for all of his support and guidance throughout the course of this experiment, as well as Dr. Santosh Kurinec and Professor Karl Hirschman for their additional advice, and lastly to Richard Battaglia for all of his technical support.

Christopher Bolton, originally from Monroeville, PA, received a B.S. in Microelectronic Engineering from Rochester Institute of Technology in 1999. He attained co-op experience at Intel Corporation in Chandler, Arizona, in the DUV Lithography group as well as in the Process Integration group.
Oxidation Kinetics of Nitrogen Implanted Silicon

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Abstract- Incorporation of nitrogen into the silicon lattice has been shown to severely retard the oxidation rate. The objective of this experiment was to determine a) whether it was a damage related issue and b) the kinetics. Equal doses of silicon were implanted along with the diatomic nitrogen (AMU ~ 28) to determine whether it was a damage related issue. The added silicon did not hinder or benefit oxide growth. From this experiment, the oxidation rate of nitrogen implanted silicon can be best fit by the use of a linear model. Surface charge analysis indicated that flatband charge, interface trap density, and lifetime increased after nitrogen implant.

1. INTRODUCTION

The use of nitrogen in oxidation is becoming more and more necessary as the gate oxide reaches sub 50 Angstroms. Boron doped poly gates allow boron to punch through the thin oxide layer and cause unwanted device failures. Hot carriers pose a similar threat at said thicknesses. Nitrided oxides can be an effective barrier to impurity diffusion.

Another benefit to nitrogen assisted oxidation is the control of oxide growth. Since nitrogen severely reduces the oxidation rate, it is much easier to grow controlled thin oxides.

2. EXPERIMENTAL RESULTS

Diatomic nitrogen (AMU ~28) was implanted into half a (100) p-type wafer at 70KeV through a 950 Angstrom screen oxide. The other half of the wafer was then implanted with equal doses of silicon (AMU~28) at the same energy. The doses were 0, 2e13, 1.1e14, 4e14, 9e14 cm². Figure 1 shows the predicted range and straggle of the nitrogen implants.

(Figure 1: TRIM Simulation of N₂ implant.)

Fifteen wafers were used which allowed for five doses, three temperatures, and four times. Once implanted, the oxide was stripped using a buffered oxide etch for 45 seconds. An RCA clean was then done in order to remove any other possible contaminants.

Oxidation was performed on every dose at 850°C, 900°C, and 950°C for times of 5, 10, 15, and 20 minutes in dry O₂. Due to constraints, only one group (consisting of every dose) of wafers could be tested for each temperature. Therefore, in order to obtain thicknesses for the multiple times, the wafers were soaked for 5 minutes, unloaded, measured, and soaked again for another 5 minutes (up to 20 minutes). To decrease the amount of unwanted oxide growth caused by moisture, the wafers were loaded and unloaded at 700°C in N₂.

After each oxide growth, the wafers were measured along 15 sites using ellipsometry. Tables 1 and 2 describe the average values for each wafer on both the silicon implanted side and the nitrogen implanted side.

<table>
<thead>
<tr>
<th>SEC</th>
<th>0</th>
<th>2.0E+13</th>
<th>1.1E+14</th>
<th>4.0E+14</th>
<th>9.0E+14</th>
</tr>
</thead>
<tbody>
<tr>
<td>5min</td>
<td>109</td>
<td>115</td>
<td>109</td>
<td>125</td>
<td>130</td>
</tr>
<tr>
<td>10min</td>
<td>21.2</td>
<td>22.8</td>
<td>23.0</td>
<td>24.0</td>
<td>24.8</td>
</tr>
<tr>
<td>15min</td>
<td>30.4</td>
<td>32.8</td>
<td>33.2</td>
<td>34.1</td>
<td>34.1</td>
</tr>
<tr>
<td>20min</td>
<td>38.8</td>
<td>42.4</td>
<td>42.6</td>
<td>42.9</td>
<td>42.8</td>
</tr>
</tbody>
</table>

Table 1: Oxide Thickness for various Si implants
Table 2: Oxide Thickness

As shown in table 1, the oxide thickness from the silicon implant was about the same as the thickness for the non-implanted wafer for all doses. Minor variation was simply due to wafer placement and furnace error. It can be seen that the silicon implant neither benefited or hindered the oxidation rate. From this, it can be deduced that implant damage and silicon implant prior to oxidation do not effect oxidation.

Conversely, the rate of oxidation was severely impaired by the nitrogen implant when compared to the non-implanted wafer (table 2). When plotted versus time, it can be seen that the oxidation follows a linear trend (Figures 2–4). The model can be best fit by the standard linear equation:

\[ X_{ox} = C_1 t + C_2 \]

Where \( C_1 \) and \( C_2 \) are constant growth rate and initial oxide thickness and \( t \) is time in minutes.

These plots also emphasize the importance of dose. They clearly show a significant reduction in growth rate for doses greater than \( 1.1 \times 10^{14} \) cm\(^2\). This is largely in part of nitrogen's inherent properties, which are still under investigation. It should also be noted that the best fitting lines occurred at the \( 9 \times 10^{14} \) cm\(^2\) dose. And further more, the slope (oxidation rate) doubled after each temperature increase.

The statistical program RS/1 was used to derive a model equation for \( C_1 \) and \( C_2 \) from the gathered data. It determined that constant \( C_1 \) was dependent on dose, temperature, dose*temperature, and temperature\(^2\). The \( r^2 \) value was calculated to be 0.99. The \( C_2 \) value was found to be dependent upon dose\(^2\). However, it was a very poor fit, having a \( r^2 \) of 0.44. Table 3 shows the corresponding values for \( C_1 \) and \( C_2 \).

Table 3: \( C_1 \) and \( C_2 \) for \( N_2^+ \) Oxidation

<table>
<thead>
<tr>
<th>Dose (cm(^2))</th>
<th>( C_1 )</th>
<th>( C_2 )</th>
<th>( C_1 )</th>
<th>( C_2 )</th>
<th>( C_1 )</th>
<th>( C_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.5E+4</td>
<td>21</td>
<td>3.9E+4</td>
<td>57</td>
<td>6E+4</td>
<td>1.2E+4</td>
</tr>
<tr>
<td>( 2.0 \times 10^{13} )</td>
<td>1.5E+4</td>
<td>1</td>
<td>4.0E+4</td>
<td>39</td>
<td>7.6E+4</td>
<td>1.0E+5</td>
</tr>
<tr>
<td>( 1.1 \times 10^{14} )</td>
<td>1.5E+4</td>
<td>-56</td>
<td>3.5E+4</td>
<td>-63</td>
<td>7.3E+4</td>
<td>-2.4E+7</td>
</tr>
<tr>
<td>( 4.0 \times 10^{14} )</td>
<td>0.57E-4</td>
<td>-11</td>
<td>1.3E+4</td>
<td>-405</td>
<td>5.2E+4</td>
<td>-3.4E+4</td>
</tr>
<tr>
<td>( 8.0 \times 10^{14} )</td>
<td>0.21E+6</td>
<td>0.15</td>
<td>0.40E+4</td>
<td>-35</td>
<td>0.8E+6</td>
<td>-0.8E+3</td>
</tr>
</tbody>
</table>

Figure 2: Oxide Thickness versus time for different \( N_2 \) implant doses at 850°C

Figure 3: Oxide Thickness versus time for different \( N_2 \) implant doses at 900°C

Figure 4: Oxide Thickness versus time for different \( N_2 \) implant doses at 950°C
Surface charge analysis was performed upon a 4e14 cm⁻² doped wafer. It concluded that there was a rise in flatband charge, density of interface traps, and carrier lifetime on the nitrogen implanted side (Figures 5-7).

3. SUMMARY

The effect of silicon implant prior to oxidation was negligible, as was the effect of implant damage. The effect of the nitrogen was profound. It relied heavily upon dose and temperature to a certain extent. A medium dose of 9e14 cm⁻² of nitrogen grew 4.3 Angstroms after 20 minutes at 850°C compared to 38.8 Angstroms from the undoped sample. The model was best fit by a simple linear relationship. There is some discrepancy in the C₂ value. Surface charge analysis revealed that implanting with nitrogen increases flatband charge, density of interface traps and lifetime.
Plasma Induced Damage to Thin Gate Oxides

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Abstract - Two mechanisms of plasma processing damage to thin gate oxide structures were studied. Thin 17.5 nm oxide on Si substrate structures were studied after direct exposure to a oxygen plasma environment with surface charge analysis and breakdown voltage measurements. A second antenna structure was used to study the charging effects of an oxygen plasma on 17.5 nm gate oxides through breakdown voltage measurements. A correlation was found between duration of plasma exposure and the extent of damage in terms of decreased dielectric strength and changes in oxide charge levels for both experiments.

INTRODUCTION

IC fabrication has become dependent on plasma processes for the anisotropic etching of polysilicon, aluminum, oxide, and polymers/photoresist (ashing). Within a plasma, wafers are exposed to charged particles, in the form of reactive ions and electrons, as well as high energy photons. Both of these have been determined to cause damage to CMOS processes with sub-micron geometries.

CMOS designs are most vulnerable to damage in the area of the thin gate oxides. One source of damage is a result of direct exposure of the gate oxide to the plasma. UV radiation and charged particles in the plasma induce dangling bonds and trapped charges in the oxide in regions which are directly exposed to the plasma ambient [1]. Damage can also result when the gate oxide is not exposed directly to the plasma by a mechanism referred to as “charging”. Charging is the condition where gate conductors collect a charge from the plasma which in turn forms electric potentials across the wafer [2,3,4]. If the voltage at the gate is sufficiently high, then the current will discharge through the gate oxide by Fowler-Nordheim tunneling or, at the highest voltage levels, will result in breakdown of the oxide.

Antenna structures have been used in previous studies to investigate the effects of charging [2]. In their simplest form antennas are large metal or polysilicon features on the surface of the wafer which cover a smaller gate region.

The charge is then collected over the entire antenna area while discharge is focused through a smaller gate area.

This damage results in several negative effects for CMOS devices including; shifts in threshold voltage [5], increased gate leakage current[3], decreased oxide breakdown voltage[2], and general yield loss. Increased leakage current and oxide breakdown can both be studied with simple capacitor devices which employ antenna ratio structures [6]. Furthermore, if the metal layer completely covers the thin gate oxide, the device will be protected from damage caused by UV radiation and ion bombardment and the effects of charging can be isolated [1,2].

Damage is believed to occur primarily during the over-etch period of plasma processing [2]. For photoresist ashing, this is the time when the metal gates are directly exposed to the plasma. For polysilicon and metal etching, the devices are also most vulnerable during over-etching because at this time the gate structures become isolated from each other.

EXPERIMENTAL DESCRIPTION

Two experiments were designed to test for charging and direct exposure damage using the RIT GEC plasma cell. First the effects of charging were studied by building capacitor like antenna devices (see figure 1a). These devices required two lithography steps to open holes in the field oxide for gate oxide growth and to pattern the Al antennas. A second device which uses only a thin oxide with no field oxide was fabricated to study direct exposure effects (see figure 1b).
The charging test device was subjected to plasma processing (100 W, 200 mT, 30 sccm O₂) after fabrication was completed. This plasma was not intended to perform any function in device construction, its purpose was to simulate over etching conditions. Breakdown voltage was then measured using an HP4145B parameter analyzer.

The direct exposure test device were subjected to the experimental plasma (40 W, 200 mT, 30 sccm O₂) after the gate oxide growth. Surface charge analysis was performed using a Semitest SCA2500 before and after the plasma. These devices were then returned to processing to add the capacitor plates and back side aluminum. Finally, breakdown voltage was determined using the HP4145B parameter analyzer.

**EXPERIMENTAL RESULTS**

The antenna structure devices used in the ‘charging’ experiment were tested for shifts in breakdown voltage shifts. A linear decrease in average $V_{bd}$ from 25 V at 0 minutes of exposure to 23 V at 20 minutes of exposure was observed as illustrated in figure 2.

The ‘direct exposure’ devices were also tested for changes in breakdown voltage. Given the planar structure of these devices, applied voltage can easily be converted into electric field by dividing by the oxide thickness of 17.5 nm. The theoretical maximum for applied field before breakdown for SiO₂ is 10 MV/cm. A histogram of the measured values for devices tested on each wafer for 0 min, 2 min and 20 min plasma exposures is presented in figure 3. A control sample, labeled as ‘no plasma’ is also listed which yielded at approximately the theoretical maximum. The 0 min sample was placed in the plasma chamber for 10 min with gas flow but no power. A 10 min sample was also prepared but was destroyed during aluminum processing.
number of failures at low electric fields in the 1 to 5 MV/cm range. Finally, the 20 minute sample showed the greatest number of devices breaking down in the low range.

The direct exposure devices were also measured after plasma processing with the Semitest SCA2500 surface charge analyzer to detect for changes in oxide charge concentrations. The control sample, 0 min., 2 min., and 10 min. plasma exposure duration samples all averaged +3E10 charges/cm². The 20 min. exposure duration sample, however, showed shifts toward −4E11 charges/cm² in a ringed pattern around the center of the wafer’s radius (see figure 4).

![Figure 4. Output from surface charge analyzer for the 20 minutes of direct plasma exposure sample showing the shift from +2E10 at the center and edges of the wafer to −4E11 in ringed pattern at mid-radius.](image)

This pattern can be explained by the non-uniform electric fields believed to be generated in the plasma system.

**CONCLUSION**

Plasma damage occurring through a ‘charging’ mechanism was found to result in a lower breakdown voltages which decreased linearly with increased plasma exposure duration. Plasma damage occurring through a ‘direct exposure’ mechanism was found to result in both lower breakdown voltages and a shift in oxide charge density for the sample with the greatest plasma exposure duration (20 min). Therefore, plasma processes during CMOS fabrication should be optimized to minimize these negative effects on gate oxides.

**ACKNOWLEDGMENTS**

The author wishes to thank Dr. Jackson and Dr. Kurinec of RIT for their assistance in preparation and in processing of this experiment.

**REFERENCES**


Oxide Passivated Nanocrystalline Silicon Trap-Controlled Memory Devices

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Abstract - An alternative to the single floating gate on a standard EEPROM device could be a continuous semi-insulating layer in which the distribution of charge can be controlled. By partial oxidation of porous silicon, a new material named Oxide Passivated Nanocrystalline Silicon (OPNSi) is formed, which has embedded Si nanocrystals in a porous glass structure. With oxide barriers between silicon nanocrystals, carriers can be confined to the silicon crystallites or trapped at interface states on the surface of these nanocrystals. With the assistance of an electric field, carriers can undergo direct tunneling through the very thin barriers and alter the charge distribution within the OPNSi layer. The placement of charge within the layer will determine the field-effect on the underlying silicon substrate. A nondestructive read would take place at low control-gate bias, and possibly result in faster write/erase cycles compared to traditional EEPROM. Another fundamental limitation of today's flash EEPROM is that each memory cell requires a pass-gate and a 3-terminal transistor structure, which limits the size of each cell. The OPNSi Diode will also be investigated as a possible candidate for a 2-terminal X-point array memory device.

I. Objective

The purpose of this project was to investigate the feasibility of two different kinds of memory devices which use OPNSi as the "memory material". One of the memory devices studied was a traditional EEPROM-like structure, which focused on the effect of altering the charge distribution within the 0.4μm thick OPNSi film. The second approach involved investigating a two terminal cross-point array concept by investigating the effect of charge transport through the film.

II. Introduction

Traditional EEPROM memory devices involve Fowler-Nordheim (F-N) tunneling through a thin oxide layer (100 Å). A control gate, which is placed above the floating gate separated by an oxide layer, controls the source to drain current and the electric field across the tunnel oxide (Figure 1). A high voltage on the control gate, such as 15V is used to increase the electric field close to 10MV/cm, which creates a steep bend in the SiO2 energy band, forming a triangular potential barrier. Electrons then tunnel through this thinned potential barrier, upwards to the polysilicon floating-gate. Electrons are transferred back and forth between the floating gate and the substrate in order to store information. This information is read by applying a much lower voltage bias on the gate and measuring the resulting transistor current.

Figure 1. EEPROM - F-N tunneling

The idea behind replacing the floating gate and the thin oxide layer with OPNSi would involve the shifting of charges between silicon nanocrystals. The formation of porous silicon material introduces lots of surface area and trap sites due to the electrochemical anodization of silicon. The passivation of porous silicon with SiO2 results in a high density of interconnected silicon crystallites, separated by very thin oxide layers (Figure 2). With the assistance of an appropriate electric field, electrons tunnel through this very thin oxide (~10-15Å) layer and can transfer between the silicon crystallites. Shifting the charge distribution within this film will influence the field effect on the underlying substrate, thus controlling the threshold voltage (C-V shift) in the transistor (capacitor) structure.

Figure 2. OPNSi Diode Structure
A high voltage is used to write/erase the device, whereas a low bias (or zero bias) can be used for a read operation. A high positive voltage (write-bias) will shift electrons up towards the OPNSi/LTO interface, causing the capacitor to remain in inversion once returned to a zero-bias condition. A high negative voltage (erase-bias) will shift the distribution of electrons toward the OPNSi/silicon interface, causing the capacitor to remain in accumulation once returned to a zero-bias condition.

Since the direct tunneling takes place at a much lower electric field as opposed to F-N tunneling, this type of structure may result in lower operating voltages and faster write/erase cycles. An OPNSi gate EEPROM may also eliminate "over-erase" problems because of self-limiting charge redistribution due to Coulombic forces.

An OPNSi capacitor was fabricated, as shown in figure 3. A high voltage is used to write/erase the device, whereas a low bias (or zero bias) can be used for a read operation. A high positive voltage (write-bias) will shift electrons up towards the OPNSi/LTO interface, causing the capacitor to remain in inversion once returned to a zero-bias condition. A high negative voltage (erase-bias) will shift the distribution of electrons toward the OPNSi/silicon interface, causing the capacitor to remain in accumulation once returned to a zero-bias condition.

III. Experimental Procedure

A series of experiments was designed to investigate the effects of surface disorder prior to anodization, film porosity, film thickness, passivation and the anodized substrate type on the current transport in the diode structure. Figure 5 illustrates a sample I-V curve for one of these samples. The voltage at 100mA and the differential conductance were recorded. After the analysis of the resulting data, the following conditions were determined to be the optimized values for the responses:

- **Substrate Preparation**
  - Induced surface disorder prior to anodization
  - $1E14$ ions/cm$^2$ BF$_2$ implant
  - 900°C, 7 hours of steam oxidation
- **Anodization Conditions**
  - Time: 2 min.
  - Current: 135mA. ($J = 3.5mA/cm^2$)
- **Porous silicon anneal (to form OPNSi)**
  - 900°C for 15min.

The cross point array concept is the idea of making a 2 terminal (gate & substrate) memory device as opposed to a 4 terminal (drain, gate, source & substrate) memory device. This concept would require an I-V hysteresis as opposed a C-V hysteresis. A reversible change in resistance may result from an adjustable level of trapped charge, resulting in different levels of charge screening, thus effecting transport in conductive pathways (Figure 4). The cross point array memory device could be programmed and read through the same two terminals, thus providing an increase in the packing density of memory cells. A change in resistance for OPNSi diodes (structure shown in figure 2) was initially observed after applying a high forward or reverse bias (see figure 5).
Voltage Sweep

Figure 7. C-V Hysteresis

Another very important observation was at “zero bias” testing. After “writing” the device was programmed to inversion (capacitance ~ 80pF), followed by erasing which programmed the device to accumulation (capacitance ~ 110pF), immediately followed by a zero-bias stability test. After pulling up the capacitance to 110pF, zero volt “read” was performed. The purpose of this “read” was to quantify the charge holding capacity of this device. After about 6 minutes of “zero bias”, the capacitance relaxed back down to about 80 pF (Figure 8). This was a key issue for this device. It was possible to store information, however, the information was lost due to the relaxation/redistribution of charge within the OPNSi film.

These results were consistent with observed behavior during the I-V analysis fabricated OPNSi diodes (without the LTO). A voltage shift of around 2V at 100mA forced current was induced by a +/-20V bias prior to the measurement. A voltage between 7.5V and 9.5V could be observed at the same current level, depending upon the preceding bias. Although measureable, this effect was very short-lived.

V. Conclusion

The charge distribution in the OPNSi film was determined to be unstable which caused the variation in the voltage shift and capacitance values. OPNSi was also determined to be a leaky material. It took 6 minutes to discharge the capacitor and bring it to an equilibrium state (Figure 8). Also the write/erase voltages were too high (+/-25V). Writing and erasing was too long (1 min.) OPNSi does not seem feasible as a non-volatile memory device because of the unstable charge distribution nature, however, a dynamic two-terminal memory device may be feasible in the future. Fabricating more capacitor samples with an organized design of experiment will help explore the secrets of this material. Also investigating the effects of the porous silicon size on the C-V curves may be a strong lead in manufacturing these devices.

VI. Acknowledgements

I would like to thank Prof. Karl Hirschman and the department of Microelectronic Engineering at Rochester Institute of Technology for their continuous support.

VII. References

Burcay Gurcan is from Ankara - TURKEY. He cooped for ATMEIL Corporation- Colorado Springs, Advanced Vision Technologies- Rochester, and National Semiconductor- South Portland. He is a proud member of the RIT Men's Waterpolo team for 5 years, which won the New York State Championship in 1996. Burcay, will be working for National Semiconductor, South Portland, Maine after graduation.
Integration of SiGe Resonant Interband Tunneling Diodes with RIT CMOS

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Abstract- This study investigates the integration of SiGe resonant interband tunneling diodes (RTD) with a standard silicon p-well CMOS process. It is feasible to build the RTD devices on the MOS source/drain regions if the RTD process did not degrade MOS devices. Besides, some etch selectivity issues need to be addressed. MOS transistors were subjected to the thermal cycling of the molecular beam epitaxial growth process and the rapid thermal anneal used in the fabrication of RTDs prior to contact formation. No destructive effects on the operation of NMOS and PMOS devices were observed. NMOS devices exhibited a positive shift of about 100mV in threshold voltage, while transconductance was reduced by about 5%. PMOS devices exhibited under 5% change in both threshold voltage and transconductance. The CMOS devices were proven to be compatible thermally with the RTD device fabrication process.

INTRODUCTION

Tunnel diodes were first discovered by Leo Esaki in 1958 while studying bipolar transistors.[1] Tunnel devices exhibited multi-valued I-V characteristics as well as negative differential resistance and high-speed transient response. These properties made them very interesting, but due to the lack of a Si-based manufacturing process, they have seen little commercial exposure. To date III-V material systems are the only ones which realize fully integrated tunnel diodes and transistors.[3]

In the early 1990s Si/SiGe resonant tunneling devices were demonstrated. In the last few years further improvements in the manufacturing of these devices has been made. Peak-to-valley current ratios for these devices have been measured at 1.54 at a peak current density of 3.2 kA/cm² [2]. These devices were fabricated using molecular beam epitaxy (MBE) followed by a thermal anneal. This process is compatible with current Si-based CMOS manufacturing, unlike the previously mentioned III-V RTDs.

PROPOSED INTEGRATION

Due to the high sensitivity of the RTD devices to thermal steps it was decided that the fabrication of these RTD devices should occur after the bulk of the CMOS devices were completed, but before metallization. The aluminum used in the wiring of the transistors would not be able to withstand the temperatures that the MBE process uses. While the RTD device mesas were being etched, the CMOS devices would also need some sort of protective layer. With this in mind, the decision was made to present an integration scheme that involved the CMOS wafers being taken right before the contact cut etch step. The wafer would be completely encased by CVD deposited low temperature silicon dioxide (LTO) which should provide adequate protection for the CMOS devices from the RIE step necessary for RTD mesa formation. Also there would be no metal on the wafers.

RIE would be used to open up windows in the LTO for the formation of the RTD mesas. MBE growth would follow, covering the entire wafer with the Si/SiGe/Si stack. It has been noted that over the LTO the Si/SiGe/Si epitaxial stack would not grow as single crystal stack. After the MBE growth a refractory metal etch mask would be deposited and patterned to delineate the areas where the mesas would be. Following this step the contact cuts would be etched, still using the refractory metal mask to protect the RTD devices. After contact-cut etch the refractory metal would be removed as it would be no longer necessary. The final CMOS steps of metallization, photo and sinter would then be performed as usual. A final cross-section can be seen in Figure 1.
A thermal study of the impact of RTD device fabrication was performed on the p-well CMOS process (PW-3) developed at the Microelectronic Fabrication Facility of the Rochester Institute of Technology. A completed CMOS wafer was taken and three NMOS as well as three PMOS devices were tested. The wafer was then stripped of aluminum and RCA cleaned to insure a clean surface for the subsequent steps. The aluminum was removed from the wafer due to the fact that Al would melt and diffuse into the silicon at the temperatures to be used in the subsequent thermal steps. A rapid thermal furnace was used to simulate the RTD growth and anneal processes. The simulation consisted of a 320 °C for 30 minutes, followed by 500 °C for 5 min, and finally 700 °C for 1 minute. All of the thermal steps were performed in a N₂ ambient so that the wafer surface would remain unchanged. After the thermal treatments, Al metal was deposited on the wafer using evaporation. The wafer was patterned using a GCA Mann g-line stepper and wafertrac, and then developed. Finally the wafer was placed in a furnace for 15 minute at 450 °C in H₂/N₂ (5%/95%) ambient for sintering. The same transistors were then retested and the results were recorded.

Table 1: Thermal Simulation Results

<table>
<thead>
<tr>
<th>Site 1</th>
<th>Before</th>
<th>After</th>
<th>Δ</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS VT (mV)</td>
<td>427</td>
<td>547</td>
<td>120</td>
</tr>
<tr>
<td>NMOS gm (1/Ω)</td>
<td>2.65E-05</td>
<td>2.68E-05</td>
<td>3.00E-07</td>
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<tr>
<td>PMOS VT (mV)</td>
<td>-424</td>
<td>-442</td>
<td>-18</td>
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<tr>
<td>PMOS gm (1/Ω)</td>
<td>9.11E-06</td>
<td>9.16E-06</td>
<td>5.00E-08</td>
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<th>Site 2</th>
<th>Before</th>
<th>After</th>
<th>Δ</th>
</tr>
</thead>
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<td>670</td>
<td>102</td>
</tr>
<tr>
<td>NMOS gm (1/Ω)</td>
<td>2.51E-05</td>
<td>2.40E-05</td>
<td>-1.10E-06</td>
</tr>
<tr>
<td>PMOS VT (mV)</td>
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<td>-841</td>
<td>-8</td>
</tr>
<tr>
<td>PMOS gm (1/Ω)</td>
<td>1.10E-05</td>
<td>1.06E-05</td>
<td>-4.00E-07</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Site 3</th>
<th>Before</th>
<th>After</th>
<th>Δ</th>
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<tr>
<td>NMOS VT (mV)</td>
<td>363</td>
<td>467</td>
<td>104</td>
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<tr>
<td>NMOS gm (1/Ω)</td>
<td>2.52E-05</td>
<td>2.30E-05</td>
<td>-2.20E-06</td>
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<tr>
<td>PMOS VT (mV)</td>
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<td>-717</td>
<td>25</td>
</tr>
<tr>
<td>PMOS gm (1/Ω)</td>
<td>8.13E-06</td>
<td>7.98E-06</td>
<td>-1.50E-07</td>
</tr>
</tbody>
</table>

Table 1 shows the results obtained before and after for the three wafer sites tested. Site one corresponds to the center of the wafer, while site 2 and site 3 correspond to...
the right and left sides of the wafer respectively. For the tests the flat was oriented away from the probe operator. The PMOS devices remain largely unchanged, with a few mV shift in \( V_T \) and a few \% decrease in transconductance. The NMOS devices exhibited about a 100mV shift in \( V_T \) and under 10\% decrease in transconductance.

**CONCLUSION**

The thermal simulation on CMOS devices has proved that the RTD device fabrication process is not destructive, and can be integrated with standard Si-based CMOS processes. A small degradation in CMOS performance should be expected, but this can be accounted for in previous CMOS thermal processes, and perhaps the \( V_T \)-adjust implant step for NMOS devices.

**FUTURE WORK**

In the future, a plasma etch chemistry and appropriate etch stop should be investigated. The selectivity of the Si/SiGe/Si to LTO and the barrier metal used should also be investigated. A thermal study on the impact of the sinter step should also be done on the RTD devices. Finally masks and a circuit utilizing integrated CMOS and RTD devices should be created.

**REFERENCES**


**ACKNOWLEDGMENTS**

I would like to thank Santosh Kurinec, my advisor for this study. Special thanks are due to Karl D. Hobart, and Paul R. Berger for their work on RTD devices and suggesting this study and to Phillip E. Thompson for providing MBE information and samples.

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Development of an Anisotropic, Highly Selective Tungsten Silicide Dry Etch Process

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Abstract—The development of an anisotropic Tungsten Silicide etch that will provide good selectivity to photoresist as well as an underlying oxide has been studied. It has been found that by reducing the amount of fluorine (SF₆) in the system and increasing the chlorine concentration, slightly tapered sidewalls can be achieved without the use of a polymer forming gas. An optimum process was developed on an Applied Materials P-5000 MxP system. A condition of 10 sccm SF₆, 40 sccm Cl₂, 20 sccm HeO₂ at 30 mTorr, and 400W presents slightly tapered sidewalls with within wafer uniformity of 4.85%. The selectivity of Tungsten Silicide to photoresist and oxide is 0.89, and 3.07 respectively.

An experiment was also conducted in which comparable etch rates of 57Å/sec were obtained using a first order approximation of power densities between the P-5000 MxP and a GEC Plasma Cell located at the Rochester Institute of Technology.

1. INTRODUCTION

Refractory metal silicides have become increasingly important materials in the ULSI era. Materials such as TiSi₂, MoSi₂, WSi₂, and TaSi₂ have found uses in semiconductor manufacturing due to their low resistivity, high temperature stability, good electromigration resistance, and excellent optical and electrical properties. Refractory metal silicides have now found applications in a wide variety of technologies ranging from CMOS and BiCMOS to CCD applications. With silicides finding a wider range of applications in the semiconductor industry, new processes need to be developed for these materials. The development of an anisotropic WSi₂ dry etch process that would provide high selectivity to oxide was the focus of this experiment.

A considerable amount of work has been done in developing etch processes for WSi₂ using a wide variety of process conditions [1-3]. This project was restricted to a limited subset of useful process gases. It has typically been reported that the use of polymer forming gases (e.g. C₂F₆, CF₄), in a WSi₂ etch process is the easiest way of achieving an anisotropic, highly selective etch. This experiment was designed using gas sources that did not contain polymer-forming agents. SF₆, Cl₂, HBr, and HeO₂ were the gases that were available. The initial experiment was processed on an Applied Materials Precision-5000 MxP Magnetically Enhanced RIE system (MERIE). A two level screening experiment was designed in which the etch rates and uniformities of photoresist, WSi₂, and SiO₂ was determined as well as selectivities of the WSi₂ to the photoresist masking layer and the underlying oxide. Following the initial experiment, runs were selected based on the selectivities, and uniformities, and were etched to endpoint and the critical dimension and uniformity was measured and an optimum process determined. A process translation was then attempted between the P-5000 and the GEC Plasma Cell at the Rochester Institute of Technology (RIT).

2. PROCEDURE

The initial screening experiment was a six factor two level fractional factorial design for the P-5000 to examine the effect of gas flow, power, and pressure on a number of output responses. Table 1 below shows the experimental design. The design was created using the statistical software JMP. Three center point runs, (35sccm SF₆, 20sccm Cl₂, 15sccm HBr, 10sccm HeO₂, 90mTorr, 300W), were added to evaluate experimental error. Etch experiments were run at all of

<table>
<thead>
<tr>
<th>Input Parameters</th>
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<th>Output Responses</th>
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<tr>
<td>Gas Flows</td>
<td></td>
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<tr>
<td>SF₆</td>
<td>10,60 sccm</td>
<td>WSi₂ Etch Rate</td>
</tr>
<tr>
<td>Cl₂</td>
<td>0,40 sccm</td>
<td>WSi₂ Uniformity</td>
</tr>
<tr>
<td>HBr</td>
<td>0,30 sccm</td>
<td>Photosresist Etch Rate</td>
</tr>
<tr>
<td>HeO₂</td>
<td>0,20 sccm</td>
<td>Oxide Etch Rate</td>
</tr>
<tr>
<td>Power</td>
<td>200,400 W</td>
<td>Oxide Uniformity</td>
</tr>
<tr>
<td>Pressure</td>
<td>30,150 mTorr</td>
<td>WSi₂ : Photoresist</td>
</tr>
<tr>
<td>Time</td>
<td>60 sec fixed</td>
<td>WSi₂ : Oxide</td>
</tr>
<tr>
<td>Cathode Temp</td>
<td>10°C fixed</td>
<td></td>
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</tbody>
</table>

Table 1: Experimental Design for the P-5000
the given process conditions on patterned resist masked samples of 6000Å of WSi₂, sputtered on top of 5000Å of oxide formed from a TEOS precursor. Pre-etch step heights were measured at 25 sites using a KLA Tencor P-22 profilometer. With the initial step heights measured

With the screening experiment analyzed, conditions which showed acceptable selectivity, and uniformity were chosen for endpoint detection. Wafers were run under the chosen process conditions for 400 sec. which allowed for endpoint detection. The endpoint detection system incorporated with the P-5000 was used. The endpoint system monitored by changes in intensity at a given wavelength. Previous work showed that the optimum wavelength to monitor the endpoint for WSi₂ was a W line at 4010Å. Endpoint algorithms were established for each process condition based on the endpoint curve generated by the endpoint monitoring system. After an endpoint algorithm was established for each process. The conditions were repeated but stopped at endpoint with a fixed over etch time. CD measurements, (2µm opening), were collected on the selected wafers before and after each etch and strip. From this CD bias, or widening of the opening, and CD bias uniformity was determined. Oxide thickness measurements were also collected before and after each etch to examine the selectivity of each etch. SEM cross sections were also taken to determine the degree of anisotropy of each condition. The wafer that showed the best selectivity, and cross sectional profile with the minimum CD change was chosen as the optimum process which was then used in a higher level experiment that is discussed further in this report.

Based on optimum process conditions obtained on the P-5000 work was done to translate the etch process to a GEC Plasma Cell located at RIT. There is a considerable difference in the chamber design of the two tools which will result in a significant difference in the performance of the etch between the two tools. The P-5000 supports 6" wafer processing while the GEC has an electrode designed for 3" wafer processing. The brief list below shows some design variables that should be taken into account when either designing an etch process or trying to translate a process from one tool to another.

- Distance between electrodes
- Electrode Area
- rf power ramp rates
- Process pressure ramp rate(s)
- Gas flow ramp rates
- Electrode temperature
- Wall temperature (chamber)
- Shower head temperature
- Shower head pattern (gas distribution)
- Wafer cooling (He flow)

The etches were run for 60 sec. each and the step heights were remeasured. Knowing that the etch would actually remove some photoresist a second step height measurement was made after the samples were stripped in an O₂ plasma. The samples were again measured on the P-22, and now the etch rates of both the WSi₂ and the resist were measured as well as the uniformity of each etch and the selectivity of WSi₂ to photoresist for each process condition

The main differences that need to be accounted for in this work were the distance between the electrodes, and the electrode area. The difference between the electrode in the GEC cell is 1". The distance between the electrode spacing in the P-5000 is 3¼". The difference in electrode spacing between both tools will impact an etch with all other factors similar. The shorter the distance between electrodes the greater the average ion energy of the ions incident on the wafers. This will enhance the reactivity of the etch increasing the etch rate. Since this difference in the two tools was known it could be accounted for when performing the experiment and again will be addressed when the results are discussed. Since the electrode area exposed to the plasma could not be determined on the two tools due to the complexity of the two chambers, a method had to be devised to obtain comparable power densities in order to acquire equivalent etch rates between the two tools. It was thought by simply holding the gas flows and pressure constant and only varying the power it would be possible to extrapolate equivalent etch rates on the two tools. This was attempted by assuming that there is a linear relationship between etch rate and power. By running two conditions at two different powers on the GEC and obtaining etch rates for both conditions a straight line could be fitted to the data through the origin. A single condition could then be run on the P-5000 and the etch rate acquired from that run could be interpolated onto the line generated from the GEC data. The power needed to obtain an etch rate on the GEC comparable to the P-5000 could then be extracted. Figure 1 illustrates this procedure. The gas sources supplied to the two tools was another significant difference. SF₆ was the only common gas supplied to the two tools, therefore a complete process could not be translated once comparable etch rates had been achieved. Since SF₆ etches WSi₂ isotropically, a process could not be developed in which SF₆ is the only gas supplied to the chamber and achieve the desired output. SF₆ is useful only with biased masks or when large ΔCD’s do not pose a problem. However, the approach used to find the power needed on the GEC to give the
necessary etch rate found on the P-5000 work could be used to develop a process in which other gases like a fluorocarbon gas and some oxygen could be added to the system. Using a polymer forming etch would minimize the lateral etching nature of SF$_6$ alone, and provide better selectivity to underlying oxide layers.

Figure 1 Relationship between etch rate and power, and proposed extraction of equivalent etch rates between the P-5000 and GEC.

3. EXPERIMENTAL RESULTS

A.) P-5000 Screening Experiment

With the design issues addressed, the initial screening experiment was done on the P-5000. Table 2 shows the process conditions run in this screening experiment. The process conditions were run on samples with photoresist patterned on 6000Å WSi$_x$ on 5000Å TEOS oxide, and on samples with only 5000Å of TEOS. All samples had patterned 1.9μm resist masks to allow for accurate step height measurements. Etch rates, uniformity, and selectivity were determined for each process condition. Table 3 below shows the average etch rates for WSi$_x$, photoresist, and TEOS oxide as well as the selectivity between WSi$_x$ and photoresist and WSi$_x$ and oxide. It can be seen from Table 3 that there are

<table>
<thead>
<tr>
<th>Condition</th>
<th>SF6</th>
<th>Cl2</th>
<th>HBr</th>
<th>He:O2</th>
<th>Pressure</th>
<th>Power</th>
<th>GP</th>
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<td>20</td>
<td>15</td>
<td>10</td>
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<td>1</td>
</tr>
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significant variations in etch rates of the three films. This is due to a number of factors, and the statistical software package JMP was used to see what effect each input parameter had on the output responses defined in the beginning of this report. Table 4 shows the impact the increase in each input factor has on each output response. From the screening experiment, conditions were selected for endpoint detection.

A) Endpoint Detection and CD Bias Analysis

Nine process conditions were selected based on selectivity and uniformity. These conditions are shown in bold font in Table 2 as well as Table 3. These conditions were run for 400sec, while the endpoint monitoring system on the P-5000 monitored the intensity of the plasma at a specified wavelength, of 4010Å. With the endpoint traces obtained, seven process conditions were chosen for CD bias measurements. These conditions can be found in bold and italic font in Table 2. Conditions 7 and 8, in Table 2, were removed from the original nine because they showed no signs of endpoint in the 400sec.

Table 3: Etch rates and Selectivity

<table>
<thead>
<tr>
<th></th>
<th>WSix ER</th>
<th>PR ER</th>
<th>Oxide ER</th>
<th>WSix: PR</th>
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<td>6.81</td>
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etch time. Due to possible throughput issues an etch that exceeds 400sec. is not considered a viable process. Therefore, with the seven conditions chosen endpoint algorithms were created for each. The process programs were then set up to etch to endpoint instead of for a given time. This allows for the etch to automatically stop when each condition reaches what the programmed endpoint algorithm defines as endpoint. With the endpoint algorithms established pre-etch CD measurements were taken on a Hitachi S-6200H scanning electron microscope. Figure 2 below is a sample SEM of a CD that was measured.

Wafers were etched under each process condition until the endpoint algorithm determined endpoint. A short over etch was done but was not optimized sample to sample. The resist was then removed, and post-etch CD measurements were taken. Oxide loss measurements were also taken using a KLA Tencor UV-1280. Table 5 below shows the CD bias, CD bias uniformity, and the oxide loss for each sample.

It can be seen in Table 5 that there is a considerable amount of variation in the CD bias for the various etch conditions. This is due in a large part to the chemistries used for the different process conditions. The byproduct formations that occur during the etch have extremely different volatilities, which play a major role in etch rates and CD bias. Fluorine-based plasmas have a significantly higher volatility of reaction products than chlorine-based plasmas do, allowing for increased etch rates and a much more chemically reactive etch [4][5]. To promote the desorption of the silicon chlorides and tungsten chlorides so etching can occur, ion assisted reactions are necessary in chlorine-based plasmas which will effectively decrease the etch rate and make for a much more physical etch process. However, this enhances the etching anisotropy, since the sidewall of the etched film is not subjected to energetic ion bombardment. Oxygen is often added to enhance the etch rates of these gases [4].

Table 5: CD bias, CD bias uniformity and oxide loss
This phenomena can be seen in the selected cross-sectional SEM micrographs found in Figure 3 a-c. It can be seen that the CD bias was relatively low in Fig. 3b and 3c. This is most likely due to the fact that chlorine was added to the system. Figure 3a shows the effect of a predominately fluorinated plasma. It can be seen that there was severe lateral etching resulting in a CD bias of ~1.25μm. Although this sample was etched in a mostly fluorinated plasma it should be noted that this sample was also run at a fairly high pressure, (150mTorr), which will also aid in the isotropic nature of the etch. Figure 3c is what was determined to be the optimum etch process for the experiment presented. As can be seen a slightly tapered sidewall has been obtained with relatively good selectivity to the underlying oxide; only losing ~647Å. It is important to point out that this etch was processed in a plasma that contained a only 10sccm of SF6 while 40sccm of Cl2 was added with 20sccm of HeO2. By examining the Fig. 3c it can be seen that by flowing more Cl2 than SF6, that an anisotropic profile was obtained. This is due to the fact that the more chloride compounds were formed requiring more ion assisted reactions, which as described above allows for a more anisotropic etch. However, since a predominately chlorine based plasma was used, the time needed to reach endpoint was lengthened. However, since HeO2 was added, the oxygen was able to speed up the etch rate and result in only a 30 sec. difference in etch time. The HeO2 also allowed for the tapered sidewall due to the fact the erosion of the photoresist by the its oxygen component. This is important because the etch time needed to endpoint was kept to the point where throughput would not be an issue. Since throughput is sufficient and an optimum etch profile was now obtained on the P-5000 the next phase of the experiment was initiated.
B.) Process Translation from P-5000 to GEC Cell

To begin the process translation the differences in chamber design of the two tools needed to be understood. The many variables that needed to be addressed were previously listed in the Procedure section of this report. Again the main differences that needed to be understood and accounted for were the electrode spacing in the two tools and the exposed electrode area. In both cases these variables could not be controlled and were fixed for the experiment. Since the GEC has a much shorter distance between the electrodes, and a smaller electrode surface area it was clear that the power density would be significantly higher on the GEC at equal powers. This is due to the fact that a shorter distance between electrodes leads to a higher plasma potential, or higher ion energy. It should also be noted that a smaller area leads to a higher current or power density. With these differences in mind, it was determined that the way to achieve comparable power densities was to obtain comparable etch rates. To do this all parameters were held constant and only the power varied. As previously described there should be a linear relationship between etch rate and power. Gas flows, and pressure was chosen at 35 sccm of SF$_6$ and 150mTorr. Again only SF$_6$ could be used due to the fact that it was the only common gas supplied to both tools. This process condition was run on the P-5000 at 150W for 60sec. and rendered an etch rate of 57.3Å/sec was obtained. Two samples were then run on the GEC at 200W and 300W for 60 sec. yielding etch rates of 98.6Å/sec and 100.3Å/sec, respectively. As can be seen there was not a significant difference in etch rates found on the two samples processed in the GEC. This is due to the fact that the reactivity of the etch was so high under each process condition that the WSi$_x$ was completely removed before the 60 sec. etch time was completed. It therefore, etched through the WSi$_x$ and was slowly reacting with the underlying oxide making it impossible to calculate an accurate WSi$_x$ etch rate. It was therefore determined that the power and time of the etches on the GEC needed to be lowered. A 20 sec. etch time at 150W and 50W was randomly selected to ensure that endpoint was not reached before the etch timed out. After the etches were run under the new conditions etch rates were calculated. For the 150W etch an etch rate of 102.3Å/sec was obtained while the 50W etch yielded an etch rate of 56.75Å/sec. The data from these two etches are shown in Figure 4. With the etch rates determined for the two conditions run on the GEC Cell, the power needed on the GEC to give an etch rate of 57.3Å/sec found on the P-5000 was estimated. To do this a line was fit using the two GEC etch rate data points. The etch rate from the P-5000 was then placed on that line and the power needed on the GEC was extrapolated. Coincidentally, it was found that to obtain an etch rate of ~57Å/sec on the GEC it needed to be run at 50W which was one of the original process conditions. With equivalent etch rates found on two tools it is now possible to run a comparable etch on the two tools provided the gas chemistry and pressure remain constant.

Following the approach used to obtain similar etch rates determined it would now be possible to extend the experiment completely onto the GEC and develop an etch process which would yield comparable etch profiles and selectivities as the optimum process described in the previous section. However, with the gas sources supplied to the two tools being different this is not possible. The GEC would require the addition of Cl$_2$ or a polymer forming gas (i.e. CF$_3$F, CF$_4$), to allow for anisotropic etching, and acceptable selectivity to the underlying oxide. By adding the polymer forming gas to the system the addition of oxygen is then required to remove the organic polymer from the sidewalls so an organic etch stop is not formed.

4. CONCLUSION

An in depth study of plasma etching for Tungsten Silicide has been presented. An optimum etch process for tungsten silicide was developed on a P-5000 MxP and the factors that control the process were explained. The etch yielded tapered sidewalls as well as good uniformity, (i.e. 4.85%), and good selectivity to the underlying oxide, (i.e. WSi$_x$:oxide=3.07). It was found that the addition of chlorine plays a significant role in allowing for an etch to be anisotropic as well as highly selective to the underlying oxide, especially when not using a polymer forming gas.

An initial experiment was also completed in which ion energies and power densities of both the P-5000 and the GEC were matched, to a first order, allowing for similar etch rates to be obtained. This experiment showed that chamber design plays a major role in the design of an etch process, and a process transfer from one tool to another.

Future work is planned to further optimize the process on the P-5000 MxP. The use of the magnetic field capabilities on the etch process will be evaluated; as well as the implementation of alternate focus rings to improve the etch uniformity. A Focus ring is a glass "cup" that surrounds the cathode and allows for a uniform distribution of the gas species over the substrate surface.
A process will be proposed for the GEC in which C\textsubscript{2}F\textsubscript{6} or CF\textsubscript{4} will be used to generate anisotropic sidewalls as well as improve selectivity to an underlying oxide, by forming a polymer on the sidewalls.

Table 4: Two level screening experiment results generated in JMP
5. REFERENCES


5. ACKNOWLEDGMENTS

The author would like to acknowledge the Faculty and the 1999 graduating class at Rochester Institute of Technology for helpful comments and criticisms. The author would also like to acknowledge the Microelectronic Technology Division at Eastman Kodak Company for allowing access to the resources necessary for this project, as well as the insight and support in the research.

Thomas J. Schulte, originally from Batavia, NY, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 1999. He attained co-op work experience at Eastman Kodak Company, Rochester, New York.
Electrolytic Plating of Copper for Advanced Interconnects

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Abstract- There is great interest in the semiconductor industry to move to copper for advanced interconnect processing. The purpose of this study was to develop an electroplating process so further studies in copper processing can be undertaken at R.I.T. Electroplating was performed using the facilities available at the University of Rochester. This system utilizes a copper sulfate based electrolyte and an 8" wafer holder. In order to use the electroplating tool for four-inch wafers, a fixture was designed. Plating was performed on Si wafers coated with adhesion and seed layer of copper at varying current densities. Plated films were characterized for sheet resistance. A 7% standard deviation in sheet resistance of the electroplated layer has been achieved with this wafer fixture design. This variation can be explained in terms of the electric field distribution in the electrolytic cell. The bulk resistivity for the plated copper was found to be 2.06E-6 Ω-cm. Powder X-ray diffraction analysis showed that the plated films had (110) preferred orientation.

I. INTRODUCTION

Interconnect resistance and capacitance has become increasingly important in determining packing density, reliability, and the manufacturing cost of ICs. Copper's low resistivity and excellent thermal conductivity makes it a good candidate for the next generation conducting material for interconnects in ICs. Copper can also handle higher current densities which allows for smaller line dimensions. Copper also has superior resistance to electromigration compared to aluminum. Lower manufacturing costs can be expected because a dual damascene requires 20-30% less process steps. Due to a higher level of integration per level, fewer levels of metal are needed (about half required compared with aluminum). Some issues that are associated with moving to copper processing include the inability of copper to be patterned using plasma etching due to the lack of volatile halide by-products. This requires the implementation of the dual damascene process which takes a while to develop. Another issue is that copper is a known fast diffuser through Si and SiO₂.

II. BACKGROUND

A basic copper interconnect process contains three layers that includes a barrier layer, seed layer, and a copper electrofill layer. A typical cross-section is shown in Figure 1. The first layer is the barrier layer. This layer prevents copper from diffusing through oxide and silicon. If the copper diffusion is not blocked, copper atoms can reach the substrate and cause devices to fail. This layer must provide good step coverage during deposition, be a good adhesion layer for copper deposition, and must also be easy to remove during the chemical mechanical polishing (CMP) step. Tantalum deposited by sputtering was used for this layer. Tantalum was chosen because it has excellent step coverage properties and it is a highly reactive with other metals. The second layer of the process is a copper seed layer, which was also deposited by sputtering. This layer offers a low-resistance path for conduction. It also provides a nucleation layer for initiation of the plated copper film growth. The main copper layer was deposited with an electroplating process. The last layer is a Si₃N₄ cap. This layer prevents diffusion of copper between metal levels. It also acts as an etch stop during the dual damascene process.
absence of any secondary reactions, the current delivered to a conductive surface during electroplating is directly proportional to the quantity deposited. Using Faraday's law and Faraday's constant the following relationship can be derived to find the theoretical deposited weight:

\[
\text{Weight Deposited} = \frac{63.546 \text{g/mol} \times (\text{Amps} \times \text{time})}{2 \times 96,500}
\]

**III. EXPERIMENTAL**

In order to use the electroplating tool at the University of Rochester a 100-mm wafer fixture was designed and constructed. Figure 3 shows a bottom view of the fixture. A constant current flows from a power supply to a copper rod and gets distributed to six copper clips. The current flows onto the wafer and makes it into a cathode. The clips hold the wafer in place with compression springs. Plating was performed on silicon wafers coated with adhesion and seed layers using varying current densities. Various currents and plating times were tested to obtain a uniform film and to determine a deposition rate.

**IV. RESULTS**

The following is a plot of sheet resistance as a function of the theoretical deposited weight. This plot shows that as the deposited weight is increased the sheet resistance decreases as expected. This was used to verify the wafer fixture is working properly.

The next plot shows that the standard deviation of the sheet resistance increases as the amount of copper deposited increases.

The following is a sheet resistance contour plot of a wafer plated with 2 amps of current. Higher deposition of copper is visible at the edge of the wafer. This is due to a higher current density existing at the edge of the wafer. The wafer fixture was simulated using a field simulation program called Maxwell. Simulations show that with the current wafer fixture design a higher current density is expected at the edges.

The next sheet resistance contour plot is of a wafer plated with 0.2 amps. When using a low current there are less current density effects. This current yielded a standard deviation of 7%.
Knowing the sheet resistance of the sample and the thickness, the resistivity can be calculated and is found to be $2.07 \times 10^{-6}$ ohm cm. The actual resistivity for bulk copper is reported to be $1.6 \times 10^{-6}$ ohm cm.

X-ray diffraction analysis revealed a stronger peak corresponding to the (220) planes ($d = 1.27 \, \text{Å}$) indicating a (110) preferred orientation of the plated films.

V. CONCLUSION

An electroplating wafer fixture was constructed and a process was characterized for plating 100mm wafers. Plated films were characterized for sheet resistance. A 7% standard deviation in sheet resistance of the electroplated layer has been achieved with this wafer fixture design. Variation can be explained in terms of the electric field distribution in the electrolytic cell. The bulk resistivity for the plated copper was found to be $2.06 \times 10^{-6}$ Ω·cm. Further studies in copper processing are planned using the optimum plating process that was determined.

VI. ACKNOWLEDGEMENTS

The author would like to thank Dr. Jome and Rajib Ahmed of the University of Rochester for providing access to their plating facility and their help. Special thanks are due to Tom Locke and Jim Greanier for help in machining the plating fixture. The author is grateful to Sara Widlund, Birender Singh, Ivan Puchades, Scott Blondell, Richard Battaglia and Dr. Lynn Fuller for their support. Finally, the author acknowledges the guidance of Dr. Santosh Kurinec for this study.

VII. REFERENCES


Pattern Density Effects on the Chemical Mechanical Planarization of an Interlevel Polymer Dielectric

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Abstract—Chemical Mechanical Planarization is quickly becoming a standard in microelectronic processing. CMP can decrease the depth of focus constraints in photolithography, resolve topography issues for multilevel interconnects, improve metal step coverage, and be used as an alternative etch process. The recent break-through in the copper damascene process has invoked a large number of studies focused on the planarization of oxides and metals. The research has proven beneficial for other applications where oxides are used as an interlevel dielectric material. It has also shown the need for further studies in the polishing of other dielectric materials. The purpose of this experiment was to study the effects that pattern density had on both the polish rate of the polymer and changes the pattern density made to the improvement of planarization. Interactions, if any, between the pattern density and the other factors were also to be studied.

1. BACKGROUND

Polymers are involved in the IC process in many ways including as an interlevel dielectric material. Because of this, modeling the chemical mechanical planarization of polymers can prove to be very useful. Numerous factors and resulting effects are involved in the CMP process. Listed below are some of the known factors.

- Applied downward pressure
- Rotating speed of the table and wafer carrier
- Time of polishing
- Polishing tool used
- Type of slurry
- Density of slurry
- Type of wafer carrier
- Pattern variation on the wafer
- Wafer size

Because of the large number of variables it would not be realistic to model all of the effects in one study.

2. PROCEDURE

The first process in designing the experiment was to decide upon the factors and responses. They are shown in the following table. The experimental design was then laid out in the statistical software RS/1©.

<table>
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<table>
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<th>Responses</th>
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<td>Polish Rate</td>
<td>Δ thickness / polish time (um/min)</td>
</tr>
<tr>
<td>Planarization Improvement</td>
<td>Δ variance(normalized) (%)</td>
</tr>
</tbody>
</table>

* Definitions of pattern density will be given in the procedure

RS/1© generated an experimental worksheet defining the variable settings for each run. Twenty-five wafers were coated with a photosensitive polyimide, patterned, and cured. The wafers were then measured on a TENCOR® P-2 Long Scan Profiler for initial thickness and uniformity. There were three different areas measured on each wafer, one for each pattern density setting. Dense patterning was defined as 43% raised topography. Local patterning was similarly defined as 86% raised topography. Global patterning was defined as an overview look at the entire 4” wafer. Below are photos of both localized areas (dense and local).

Each localized area was observed in a 300 X 300-micron window. After the pre-polish measurements were obtained the wafers were polished using the Strasbaugh 6DS-SP-polishing tool, following the polishing parameters set in the RS/1© worksheet. After polishing the wafers were cleaned utilizing a megasonic cleaning unit and a rinser/dryer. The wafers were again measured on the
TENCOR® for thickness and planarization. An EXCEL spreadsheet was used to calculate the responses. The results were entered into RS/1® and insignificant terms were removed from the model design. The program revealed the table speed as statistically insignificant. Because of this the table speed was set at a constant value of 125 rpm for the graphical analysis. Three graphs, one for each pattern density, were made for the individual responses.

3. ANALYSIS

For the analysis of the results 3-D plots were obtained. In each graph the X-axis represents the polish time, the Y-axis represents the downward pressure and the Z-axis is the observed response. Again it should be noted that the table speed was set at a constant of 125rpm. The results for Polish Rate can be seen below:

![Dense Pattern](image1)
![Local Pattern](image2)
![Global Pattern](image3)

For each pattern density there is a linear relationship between the downward applied pressure and the polishing rate. This is an expected result, as the pressure is increased the polishing rate increases slightly. What is more interesting is the effect that the polishing time has between the three pattern densities. In the dense pattern there is a negative exponential relationship. This is most likely due to the initial polishing of ridges formed during the curing of the polyimide.

The local pattern graph also displays this initial high rate of polish. Again the ridges can explain this because they are formed in both the dense and local areas. As defined the local area has less patterning and therefore has less ridges formed during the curing process. In the local pattern results there is a secondary increase in the polish rate. This may be due to dishing effects in the densely patterned areas. When the densely patterned areas have dished an amount greater than the planarization length of the table pad the local areas essentially become the high spots on the wafer and begin polishing at this increased rate. This oscillation between the polishing of dense areas and local areas can explain the sinusoidal pattern seen in the graph. The global pattern appears to be simply a combination of the two localized areas.

The results for Planarization Improvement are:

![Dense Pattern](image4)
![Local Pattern](image5)
![Global Pattern](image6)

As with the polishing rate graphs there is still a linear relationship with the response throughout each pattern density, although in this case the contributing factor is the polishing time not the downward pressure. The downward pressure has a parabolic effect on the planarization improvement. The dense and local patterns again present the sinusoidal patterns seen in the polishing rate graphs. This suggests that the rate in which the polymer is polishing plays a role in the planarity of the area. The global view does not appear to simply be a combination of the two localized areas as before. The graph shows that with increased polishing time the improvement in planarization decreases.
4. CONCLUSIONS

The graphical analysis shows that the downward pressure applied has a positive linear effect on the polish rate. An increase in polish time shows an oscillation in the polishing rate most likely due to ridge polishing and dishing effects between the localized areas. The global view of polish rate is an “averaged” rate of the two local areas.

The improvement in planarization also appears to be connected to the ridging and dishing effects. The alternation in the graphs is clearly visible throughout both the dense and local pattern. The global view suggests that improvements in planarity decrease with increased polish time and that the downward pressure plays only a same role in the planarity.

The possible correlation between the polish rate and the improvement of planarization suggests there may be an interaction amongst the two responses. Because of this a second experiment should be performed with an expanded design space – namely increased polish time. This will allow for further insight into the oscillations seen throughout each graph.

5. APPENDIX

Some constants in the experiment:

<table>
<thead>
<tr>
<th>Polyimide</th>
<th>Probimide 7520 – from Olin Microelectronic Materials</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slurry</td>
<td>882G Al oxide – from Ferro Corp.</td>
</tr>
<tr>
<td>Polishing Tool</td>
<td>Strasbaugh 6DS-SP</td>
</tr>
<tr>
<td>Table Pad</td>
<td>Rodel IC1000P</td>
</tr>
<tr>
<td>Wafer Carrier</td>
<td>4” carrier, 36 holes, no holes plugged</td>
</tr>
<tr>
<td>Spindle Speed</td>
<td>100 rpm</td>
</tr>
<tr>
<td>Slurry Flow Rate</td>
<td>300 ml/min</td>
</tr>
<tr>
<td>Back Pressure applied to Wafer</td>
<td>-5 psi</td>
</tr>
</tbody>
</table>

6. REFERENCES


7. ACKNOWLEDGEMENTS

The author would like to thank Dr. Fuller, Dr. Kurinec, Dr. Lane, Dr. Calistri-Yeh, Karl Hirschman, Gene Fauz, David Holden, and Jason Neidrich for their support and insight, and Xerox Corporation for the use of their equipment and materials.

Teresa M. Evans, originally from Springwater, New York, received a BS in Microelectronic Engineering from Rochester Institute of Technology in 1999. She attained co-op work experience at Advanced Vision Technologies and the Xerox Corporation. She is joining the Xerox Corporation as a Chemical-Mechanical Planarization Engineer starting June 1999.
Abstract- The purpose of this study is to present and characterize an 8 bit AD converter implemented with flash architecture. Flash architecture provides one of the fastest and easiest ways to convert analog input signals to digital outputs. Analog-to-digital conversion is the process in which a continuously varying analog signal is transformed into a multilevel digital signal. Analogue electrical waveforms are applied to the converter and are sampled at a fixed rate. Sample values are then expressed as a binary number consisting of 0's and 1's. The resulting digital code can be used to encode digital audio, applications in video and image processing systems. The more bits that are used to represent the amplitude of the original signal, the higher the quality of the output. 8 bit sampling is typically used to encode speech, 16 bit to encode music.

I. INTRODUCTION

A. Flash-Type Converter

Sampling levels for an 8 bit ADC are 256. Sampling frequency should be twice that of the highest frequency in the sampled waveform, if it is to be represented correctly when digitized according to the signal sampling Nyquist theorem.

The input voltage of the ADC can range from 0 to Vref. The voltage reference is used to set the range of conversion of the converter. If the input to the ADC is equal or larger than Vref then the converter will output all ones. For inputs between these two voltage levels, the A/D converter will output binary numbers corresponding to the signal level. Because of the numerous output levels there is inherently noise in the quantized output signal. The key to reducing the effects of the noise is to maximize the input signal level. A good rule of thumb is to keep Vref at least as large as the maximum digital signal.

The most straightforward method to perform Analog to Digital conversion is to compare the sampled analog signal with different levels implementing the Flash AD architecture Fig.1. An 8 bit AD converter was implemented in CMOS, the number of comparators required using simple flash architecture is \(2^{N} - 1\) comparators, number of transistors 6200. We assigned a full scale input level of 10 V between positive and negative rails for Vcc and Vss supplies to the comparator, the LSB voltage level is \(10/255 = 39\) mV. The input signal was first sampled by the circuit, the comparator made a decision whether or not the sampled value is greater or smaller than the reference voltages. Each reference level in the series of resistors ladder needs to be one Least Significant Bit apart from each other. The offset of the comparator needs to be less than the least significant bit level of 39 mV. The converter ladder resistance was assigned a value of 2550 Ohms. In CMOS, this offset requirement is difficult to achieve.

Some special circuit techniques are required to reduce the offset of the comparator, which requires large amounts of power because of its fast conversion rate, this limit the family of flash converters to 8 bit or less resolution. The fundamental block of the design for this project is the 32 level sampling output element, the total number of comparators is 255 and total number of resistor is 256.

![Figure 1. Flash AD architecture](image-url)
Reyes, A.

17th annual Microelectronic Engineering Conference, May 1999

The comparator circuit is displayed in Fig. 2, it is implemented in CMOS technology, the transistors

Figure 2. The comparator

geometries are balanced to conduct the same amount of current, taking into account the difference in carriers mobilities between NMOS and PMOS.

B. The Combinational Logic

Figure 3. The combinational logic array

The combinational logic array of Fig. 3 geometries have been set up according to the number of inputs N:

\[(W/L)_n = N/2 \times (W/L)_p\]

for NMOS and PMOS transistors. The logic used is NAND to NAND. This logic was selected to save silicon area. For the present case the outputs produced will be inverted. The decoder combinational usual logic is AND to NAND. NAND logic replacing the OR logical output. A set of two trees of NAND gates with 64 inputs each has been used to implement the binary code. The number of input is half the sampling level or two to the power eight, in this case 256/2 = 128 inputs.

1. DC Bias Analysis

The comparator is biased to make the pull-down network conductive and turn the current mirror transistor, assuming the transistors are working in the saturation regime, we can use the following approximation to obtain the bias voltage, using transistor M8, M9 and M10.

\[I_{ds} = \frac{kW}{L} (Vgs - Vt)^2\]  [1]

\[I_{ds8} = I_{ds10} = I_{ds9}\]

The sum of all potentials from the positive rail to the negative rail is given by:

\[20 \, V = V_{sg10} + V_{sg9} + V_{gs8}\]

\[20 \, V = 2 \, V_{sg9} + V_{bias}\]

\[V_{bias} = 20/2 = -V_{sg9}\]

The voltage drop at Vgs8 will produce the Vbias needed to turn the current mirror transistor

From equation [1] we obtain:

\[K \frac{W9}{L9} (Vgs9 - Vt)^2 = k \frac{W8}{L8} (Vgs8 - Vt)^2\]

\[\frac{W9}{L9} \left( -V_{bias}/2 + 20/2 - Vt \right)^2 = \frac{W8}{L8} \left( V_{bias} - Vt \right)^2\]

\[\frac{W9}{L9} = \left( V_{bias} - Vt \right) / \left( -V_{bias}/2 + 20/2 + 1 \right)\]

\[\frac{W9}{L9} = \frac{W8}{L8}\]

\[\frac{W9}{L9} = 0.264\]

\[\frac{W8}{L8} = 3.77 \times \frac{W9}{L9}\]

This gives an approximate ratio of four to one for the PMOS and NMOS transistors of the Vbias circuit.

2. Differential Pair

The saturation currents for the differential pair transistors and the current load transistors are given by:

\[I_{ds} = u \, W \, Cox/2 \times (Vgs - Vt)^2\]

Assume \(I_{ds} = 15 \, uA\)

\[I_{ds1} = I_{ds2} = I_{ds3} = I_{ds4} = 7 \, uA\]
Reyes, A.

17th annual Microelectronic Engineering Conference, May 1999

IdsatM1 = 600 * 30/20 Cox' / 2 (1.5-1) ^2 = 900 cm^2 / V sec * (1.5 - 1 V)^2 * (6.9E-8 F/cm^2) / 2 = 7.85 uAmps for NMOS transistor

IdsatM3 = 300 * 40/20 Cox' / 2 (1.6-1) ^2 = 3000 cm^2 / V sec * (1.6 - 1 V)^2 * (6.9E-8 F/cm^2) / 2 = 7.58 uAmps for PMOS transistors.

IdsatM5 (current mirror) = 600 * 40/20 Cox' / 2 (1.6-1) ^2 = 1200 cm^2 / V sec * (0.6 V)^2 * (6.9E-8 F/cm^2) / 2 = 14.9 uAmps

2. Output stage

The output stage calculation of Idsat is done taking into consideration the channel length modulation parameter lambda of 0.02

Idsat = uW Cox’ / 2 L (Vg- Vt)^2 (1 + lambda Vds) [2], lambda = 0.02 and Vout near zero so Vds should be ~10 V

From equation [2] we obtain for M7 PMOS transistor:

Idsat = (300) (80/20) * (6.9E-8/2 F/cm^2) * (1.6-1)^2 * (1.0 + 0.02 * 10V) = 15.2 uAmps

M6 NMOS transistor Idsat:

Idsat = (600/2) (40/20) * (6.9E-8 F/cm^2) * (1.6 - 1 ) ^2 * (1 + 0.02 * 10V) = 15.3 uAmps

4. Differential amplifier small signal analysis

Gm = W u Cox’ / L (Vg - Vt) = 2 Id / (Vg - Vt) ; rds = 1 / ( lambda Id)

Gm = 2 * [7.5E-6 u Amps / (1.6 - 1 )] = 30.24 umho

rds = 1 / ( 7.5E-6 * 0.02 ) = 6.66 M

Vo / Vin = 2 * gm / rds / [ rds] = 2 * 30.24 umho * 6.66 M / 6.66 M = 201.6 (differential pair gain)

M1 and M2 differential pair
M3 and M4 are current source loads

5. Output stage small signal analysis:

Transconductance Gm

Gm = W u Cox’ / L (Vg - Vt) = 2 Id / ( Vg - Vt) ; rds = 1 / lambda Idsat

Gm = 2 (15.07 uAmps) / (1.6 -1) = 50.2 umho

rds = 1 / (lambda Id) = 1 / ( 0.02 *15.07 uAmps) = 3.31 umho

Output gain = Vout / VM4 = Gm rdsPMOS / rdsCMOS = 50.2 umho * 3.31 M / 3.31 M = 83

6. Differential mode gain

Acm = common mode gain = - Gm rdsPMOS / (1 + 2 gm Ro ) = - 50.2 E-6 (3.1E6) / ( 1 + 2 * 50.2E-6 * 1.65 E6 ) = - 0.99

Avd = differential mode gain = 201.6 * 83 = 16,732.8 or 84.47 dB

CMRR = |Avd/ Acm| = 16565.47 = 20 log16565.47 = 84 dB

CL = Area * Cox’ = 80 pF/cm^2

Gain Band Width Product

GBW = gm / 2 pi CL = 99.86 KHz

Slew Rate = Id / CL where CL = CL min (parasitic load capacitance) + CL ' (nominal load capacitance) .The output of an ideal op-amp has the ability to change instantaneously. In a real op-amp the rate of change of the output, expressed in volt/ unit time should never exceed the slew rate value

SR = 15 uAmps / 80 pF = 0.187 V/usec

Table of the comparator parameters

<table>
<thead>
<tr>
<th>Comparator Specs</th>
<th>Output Resistance</th>
<th>1.65 Mohm</th>
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</thead>
<tbody>
<tr>
<td>Avd= 200.1 * 83</td>
<td>16732</td>
<td></td>
</tr>
<tr>
<td>Common Mode Gain</td>
<td>-0.99</td>
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</tr>
<tr>
<td>CMRR = 16732* 0.99</td>
<td>16565</td>
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<tr>
<td>CMRR= 84.3 dB</td>
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<tr>
<td>Vcc/Vss= 10 V</td>
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<td></td>
</tr>
<tr>
<td>Gain Bandwidth</td>
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<tr>
<td>Product</td>
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<td></td>
</tr>
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</table>

Slew Rate = 0.187 V/usec
III. RESULTS

Figure 4 shows the converter output obtained and presented in this study, the performance of the converter is measured in terms of digital synchronous outputs. Future work will include the improvement of the model and refinement of the A/D circuit.

ACKNOWLEDGEMENT

The author of this study would like to acknowledge the support of Dr. Lynn Fuller, head of the department of microelectronic engineering and Dr. Pawel Sniatala of the department of computer engineering at the Rochester Institute of Technology.

REFERENCES


Fabrication and Development Of a Charge Injection Device Imager

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Abstract- As Rochester Institute of Technology (RIT) brings into production i-line capabilities with a new Canon stepper, resolution beyond 2μm will be possible. The present project prepares one of RIT's most novel and successful processes for this transition. The process for a Charge Injection Device Imager (CID) has been entirely developed at RIT through the work and collaboration between the Imaging Science and Microelectronic Engineering Departments. After the initial success in the design and fabrication of 8X8 and 32X32 imager, a more challenging 54X40 process was developed employing 6-micron PMOS technology. The goal of this project is the successful fabrication of an imager that will allow for the capture of real images. All this exclusively fabricated at RIT. This project recalls on the latter design and which transitions the ClD) process in preparation for 2-micron technology. The device transistors has been tested and characterized and the results are compared to simulated transistor data obtained using SUPREM-IV.

I. INTRODUCTION

Charge Coupled Devices (CCD's) dominate the digital imager industry today. They are found in many different applications such as High Definition TV (HDTV), astronomy, space based imaging [1] and the widely used hand-held video camera. However, there are some low light level imaging and harsh conditions applications where Charge Injection Devices (CID's) provide a distinct advantage over the CCD. Furthermore, Charge Coupled Devices, still present some challenges that are avoided with the use of CID's, such as charge transfer problems, non-random readout, and expensive and complex fabrication techniques since it cannot be integrated with CMOS technology.

The CID approach, on the other hand, has the main advantage of its total compatibility with CMOS fabrication techniques. This makes them cheaper to manufacture and it also allows for electronic components to be integrated in the chip. Other advantages are its avoidance of charge transfer losses, minimized blooming and random non-destructive readout.[2]

This paper reports on the basic CID structure, readout mechanism and process fabrication at RIT.

II. DESCRIPTION

A basic description of how light is collected and stored by the CID follows. Then, figures and an explanation of the readout mechanism of the device, provide an insight of the operation and some of its advantages. Finally noise reduction techniques are taken into consideration when selecting a pixel design.

A. Light Integration and Charge Collection

It is important to understand how light is collected by the device and what considerations are taken when fabricating the structure. The basic element of a CID imager is a MOS capacitor. This operation is portrayed in figure 1. Basically, light is collected by bringing a MOS capacitor to a deep depletion state. Photons will enter the Silicon creating electron/hole pairs. Light with short wavelengths will travel a shorter distance, depending on the absorption coefficient of Si, figure 2. Holes created by shorter wavelength light will be directly collected by the potential well. Holes produced by light with longer wavelengths, which absorption coefficient is larger than the depletion length, may or may not be collected in the potential well. It will depend on their characteristic diffusion length. A lightly doped substrate will allow for a larger depletion width, thus a larger sensing area is possible. Charge is integrated on the Si/SiO2 interface of the collection MOS capacitor.[3]

![Figure 1. Light Collection and Charge Integration](image-url)
B. Pixel Operation

Figure 3 sequentially represents the basic pixel operation and readout mechanism utilized in this design. Two capacitors are utilized for a random X-Y selection a pixel. Both capacitors are biased to a negative potential but the column or collection capacitor is biased to a larger negative potential, all charge is stored here. Then, the row or sense capacitor is left floating and its potential, which should be near the potential of its source, is read. All the stored charge is then moved to the potential well of the sensing capacitor by biasing the collection capacitor to a lower negative potential. After this transfer operation the potential of the sensing capacitor is read again. The potential difference between these two readouts of the sensing capacitor is proportional to the collected charge. As an advantage this readout technique is not destructive and can be repeated as many times as necessary. This results in a reduction of noise. Finally the charge is cleared by injection into the substrate. Consequently another pixel can be selected and read on a similar way.

C. Active vs. Passive Pixel Design

The CID structure allows for two different kinds of pixels, active and passive. A passive pixel uses most of its area for light collection. After storing the collected charge, this is sensed and transfer to the output stage where its amplified and read. The active pixel has a smaller collection area since it includes a pre-amplifier in the pixel are itself. This group of transistors will amplify the sensed charge before its transfer to the output stage. Although the active pixel has a smaller sensing area, the resulting noise reduction of this design makes it advantageous over that of the passive pixel.
resistive Phosphorous implant was performed next to act as transistor load. Due to the uncertainty of the characteristics of the Polysilicon deposited a pre-screening implant is necessary to determine the necessary dose. After the pre-screening five different doses were used: 1e14/cm^2, 2e14/cm^2, 3e14/cm^2, 4e14/cm^2, and 5e15/cm^2. The remaining of the polysilicon is doped to a low resistivity level and etched. Then, another series of implants follow. These include a p+ drain/source for the PMOS transistors, a pinning implant to avoid surface inversion in the exposed gate oxide areas and an n+ substrate contact. Finally a thick layer of oxide is deposited via LPCVD and metal contacts and routing are deposited and patterned.

**IV. SIMULATION**

The preceding process flow was simulated using the software package SUPREM-IV. The resulting structure is presented in figure 4. This allowed for the simulation of the PMOS transistor characteristics as well as obtaining information about the resistance characteristics of our films.

![SUPREM-IV simulated structure](image1)

**Figure 4.** SUPREM-IV simulated structure

The simulation results showed a threshold voltage of the PMOS transistor of —1.2Volts. It was inconclusive on the resistivity values of the polysilicon films since no specific grain boundary properties could be established for the modeling.

**V. RESULTS**

As it can be seen in figure 5, good PMOS transistors were fabricated. The two sub-threshold curves correspond to transistors fabricated at Poly1 and Poly2 respectively. The difference observed in threshold represents the difference in thickness of about 200Å. An excellent gain is observed out of this two curves. Unfortunately, as seen in figure 6, the load resistance tested in the fabricated devices proved to be too low. Represented here is the device which received the lowest implant dose at the resistor level. The values obtained were too low and prevented the PMOS-transistor-based logic from operating properly.

![Sub-threshold Plots for Poly1 and Poly2 PMOS](image2)

**Figure 5.** Sub-threshold Plots for Poly1 and Poly2 PMOS

![Load resistance is too low](image3)

**Figure 6.** Load resistance is too low

**VI. CONCLUSION**

An Active Pixel Charge Injection Device has been fabricated at Rochester Institute of Technology. The process flow has proven solid but with room for improvement. A better qualitative characterization of the polysilicon layer is necessary if PMOS transistors are to be used. CMOS utilization could avoid some of these issues.
REFERENCES


ACKNOWLEDGMENTS

The author would like to thank Ph.D. candidate and advisor George Lungu for his contribution, dedication, designs and knowledge and Dr. Lynn Fuller, head of the Microelectronic Department at Rochester Institute of Technology.

Ivan Puchades, originally from Barcelona, Spain, received his B.S. in Microelectronic Engineering from Rochester Institute of Technology in 1999. He attained co-op work experience at Advanced Vision Technologies and National Semiconductor. He is Semiconductor. He is currently pursuing an M.S. in Electrical Engineering at Rochester Institute of Technology.

17th Annual Microelectronic Engineering Conference, May 1999
Oxide Passivated Nanocrystalline Silicon LED Optimization

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Abstract- The objective of this project was to create an optimized, repeatable process for integrated PSI (Porous Silicon) LEDs. Porous Silicon is a light-emitting version of silicon, formed by electrochemical etching in an HF-containing solution. This material becomes stable once passivated with oxygen at high temperatures (900°C) and maintains its light-emitting properties. This study systematically investigated the process effects on electroluminescence (EL) and electrical transport characteristics. The relationship between fabrication conditions and the structural and electronic properties of porous silicon have been subsequently examined. It was discovered that pre-anodization substrate preparation had a dominant influence on the device characteristics. Analysis of the designed experiments (ANOVA) has been used to quantify the influence of factors under study; details of which will be presented.

I. Introduction

With silicon as the dominant semiconductor in the microelectronic industry, the realization of silicon LEDs would greatly enhance the capabilities of integrated optoelectronic systems. Such devices could provide a cost-effective alternative to hybrid technologies for use in display devices and optical interconnects. Silicon, however, is an extremely inefficient light-emitter, and for this reason had not been able to achieve the desired levels of dominance in optical applications. Fortunately, porous silicon, an optically efficient silicon-compatible material has been developed. Porous silicon is a network of nanometer-sized silicon regions surrounded by void space, resulting in a light-emitting material. A porous silicon film is typically prepared by electrochemical anodization of the surface of a silicon wafer.

The fabrication of these devices involves multiple factors that require optimization, each of which have significant effects on electroluminescence (EL) and transport characteristics. The selection of process factors was influenced by background process knowledge of porous silicon materials and the requirements for "working" LEDs (uniform light-emitters, with good transport properties).

II. Theory and Device Fabrication

In order to interpret optical properties of porous silicon, it is necessary to understand why bulk silicon, which is an indirect-bandgap semiconductor, has a low optical efficiency.

Band-edge light emission from a semiconductor involves the excitation of an electron from the filled valence band to the empty conduction band and subsequent recombination of the electron with an empty state (or hole) back in the valence band. Light emission occurs when the recombined energy is given off as a photon. In silicon, this process of photon emission is unfavorable, meaning the laws of physics do not allow it to happen very often.[1] However, if the silicon material is modified from a bulk solid to small crystals of silicon, as in the case of porous silicon, radiative recombination events become much more favorable. Here, electrons, in the conduction band and holes in the valence band are confined spatially by potential barriers, such as nanocrystal surfaces. As a result of the confinement of both these electrons and the holes, the lowest energy optical transition from the valence to the conduction band increases in energy, effectively increasing the bandgap and pushing the emission wavelength into the visible region. The pure quantum confinement model was initially proposed by Canham [2].

Porous silicon is a material formed by electrochemical etching of crystalline silicon using an HF/Ethanol solution. Porosity and PSI thickness are dependent on the variations in the anodization process, and effect the silicon structure size as well as the mechanical stability. [See Figure 1].

![Fig 1: Porous Silicon Cross Section](image-url)
The basic fabrication process for OPNSi bulk film devices developed at RIT goes as follows:

First, 10 Ω-cm p-type (100) oriented crystalline silicon wafers, with a BF₂⁺ implanted surface layer, go through a steam oxidation to intentionally induce stacking faults. They are then etched and anodized in a 1:1 HF/Ethanol solution. The current density during anodization was approximately 3.5mA/cm². The wafers were anodized for two minutes. Anodization transforms the silicon into a nanoporous layer (porosity ~70%) that is ~.4um thick. The current density during anodization is then deposited to passivate the porous silicon with oxygen. A polysilicon film is then deposited using LPCVD, and then selectively doped n+ to form the device cathode. Aluminum contacts were then sputtered on the polysilicon and on the backside in order to form an ohmic contact to the substrate for device testing purposes.[3] [See Figure 2 below.]

![Fig 2: Schematic cross section of porous silicon light-emitting diode, capable of light emission at visible wavelengths.](image)

III. Experiments and Evaluation

Process development for this project included a total of three separate designed experiments. The experiments focused on the relationship between fabrication conditions and the electronic properties of porous silicon. The first experiment investigated the relationship between the amount of pre-anodization surface stress, film thickness, and passivation temperature. The second experiment investigated the amount of lattice damage, surface stress and the anneal method. The third experiment investigated lattice damage and pre-anodization surface stress.

In the first experiment a 900°C steam oxidation time was systematically varied between 2, 4, and 6 hours. This was to see if time really played a key role in producing desired stacking faults. The anodization time was varied between 1.5, 2, and 2.5 minutes. This was used to measure importance of film thickness. Lastly, the anneal temperature was varied between 850, 900, and 950°C to measure the degree of passivation. The transport characteristics were not very good, and there was minimal to no light emission on these devices. However, this helped design the second experiment, where implant dose and steam oxidation, as well as Rapid Thermal Process versus furnace anneal were investigated.

The second experiment varied implant dose, steam oxidize, and anneals. The implant was 1E14 cm⁻² vs. 1E15 cm⁻². This was used to evaluate how lattice damage affects responses. The steam oxidize was varied by whether or not to do a seven hour 900°C steam oxidation or not. This was to evaluate how the degree of surface stress on the wafer effects light emission and transport characteristics. Both the implant dose and the steam oxidation were performed to induce stacking faults on the wafer surface. Finally, the anneal method was varied between RTP and furnace. This was performed to see if RTP was as effective as the furnace in passivating the anodized wafers.

The third experiment was designed with the process information discovered from the second DOE. The implant dose was varied between 1E15 cm⁻² and 1E16cm⁻² and the steam oxidation between 900°C and 950°C. The seven-hour steam oxidation was performed on all wafers and the wafers were annealed in the furnace, not the RTP, per DOE #2 results. The strategy for the experiment was to fabricate repeatable devices while optimizing the process.

IV. Results

After analysis of each designed experiment, it was discovered which factors influenced light emission and transport characteristics of the devices.

Each device was tested for light emission, which at this point is purely a visible test for light, and transport characteristics. [See Figure 3.]

![Fig 3: “Good” and “Poor” Transport Characteristics](image)
The desired characteristic curve is described by W1. This has "Good" Transport, this means the device displays small variation in device behavior, and uniform EL over the entire cathode area. W2 represents a typically "Poor" Transport curve, this typically has inconsistent device behavior, and pinpoint EL spots at the aluminum edge. The voltage was measured at 100mA for all devices.

The first experiment, except of one treatment combination, did not have light emission, and several devices had "poor" transport. During the analysis, it was seen that none of the factors had a real impact on the experiment by themselves, and only a transformed quadratic version of the factors impacted the outcome of the experiment. Figure 4 shows the anodization time vs. voltage, and the steam oxidation vs. the voltage.

The horseshoe effect is a result of the transformed factors, and shows their quadratic behavior. In this experiment only 74% variation is accounted for. This raises the question as to how influential these factors are.

However, from this experiment, and prior porous silicon knowledge, the second experiment was designed. In this experiment, 82% of the variation was accounted for and two wafers emitted substantial (very bright) light. Both of these wafers went through the seven-hour steam oxidation and were annealed in a furnace. Figures 5 and 6 show the single effect relationship of implant dose and steam oxidation on the electrical response (voltage at 100mA). The implant dose is shown to have a linear effect in relationship to the voltage of the device. The steam oxidation shows that the wafers that received a steam oxidation have minimal voltage variation in comparison to the wafers not receiving the steam oxide.
Both of these factors influenced the third designed experiment, where it was decided to process all the wafers with the steam oxidation, (varying temp from 900°C to 950°C) and to vary the implant dose between $1 \times 10^{14}$ cm$^{-2}$ and $1 \times 10^{15}$ cm$^{-2}$.

V. Conclusions

An optimized porous silicon LED was not achieved, in the first two designed experiments, however, the third DOE is still being analyzed and current data looks promising. It was discovered that lattice damage from ion implantation and induced stacking faults from the steam oxidation, are both significant influencing process factors in 'good' transport characteristics and EL device behavior. More work still needs to be completed to ensure repeatability and optimization of the process.

VI. Acknowledgements

The author would like to give special thanks to all the help and support from Karl Hirschman and Burcay Gurcan.

Tina M. Wheaton, originally from Fair Haven, NY, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 1999. She obtained co-op experience at Eastman Kodak and Motorola. She is joining Motorola, Austin, TX, as a Device Engineer in June 1999.

Investigation of a Silicon Bulk Etched Incandescent Light Source

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Abstract - An attempt of fabricating an incandescent light source was made at Rochester Institute of Technology. Filament length, width, material and shape as well as encapsulation method were under investigation in the experiment. Due to a design flaw, the devices could not be tested for functionality. This has since been fixed and another attempt will be made to fabricate the devices.

PURPOSE

For many years, methods of producing light from a silicon wafer have been investigated. These methods have included trying to make LED's, using Porous silicon but few have succeeded. With the radical change in thinking brought about with the fabrication of Microelectromechanical devices (MEMs), a new method has been realized. Using a sacrificial oxide layer covered with silicon nitride, a hollow cavity can be created. If a metal or polysilicon line is run through this cavity, then it may be possible to produce an incandescent light source. This source is a way of integrating a light source with standard CMOS processes. This may lead to the advent of optoelectrical circuits at an integrated circuit level. If such devices can be fabricated the speed of circuits may increase dramatically, since the limiting factor would be the speed the light can travel through a medium.

EXPERIMENTAL DESIGN

This experiment investigated the light emission from polysilicon and tungsten lines spanning the cavity. It also investigated the effects of filament length, width, shape, and encapsulation method.

The structure depicted in Figures 1 and 2 were fabricated in the lab at RIT. Figure 1, shows the final cross-section of the encapsulated filament sealed at a pressure of 5mT. The metal lines will be comprised of either silicon or tungsten depending on the run. The length of the filament will be varied at 300, 400 and 500μm while the width is varied at 5 and 10μm. Filaments will also be created that have a 90° bend in them but are identical in every other aspect.

Since the filament is coated with silicon nitride, it may not be necessary to encapsulate the filament with a vacuum. Therefore, a second process flow was investigated which will not enclose the filament inside mini-chamber. The cross-section is depicted in Figure 2.

PROCESS FLOW

The following section will describe the processes which were used to fabricate the devices. All processing was done starting with <100> silicon wafers.

The first step is to grow a 1500Å silicon nitride film. This film will be used to protect the silicon substrate during subsequent processing. It is important that this layer is low in stress so that it will not fracture and crack during later thermal steps. The nitride was grown with the following recipe.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setpoint</th>
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</thead>
<tbody>
<tr>
<td>Temperature</td>
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</tr>
<tr>
<td>Gas(es)</td>
<td>SiH4:Cl2/NH3</td>
</tr>
<tr>
<td>Flow(s)</td>
<td>60/150sccm</td>
</tr>
<tr>
<td>Pressure</td>
<td>430 mT</td>
</tr>
</tbody>
</table>

Table 1: Nitride CVD process

Following the Nitride etch, the first sacrificial oxide layer is grown. This oxide layer should be 1μm thick. This thickness was chosen so that the filament will be free standing. The process used to grow this oxide is shown in Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setpoint</th>
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</thead>
<tbody>
<tr>
<td>Power</td>
<td>50 W</td>
</tr>
<tr>
<td>Gas(es)</td>
<td>SF6</td>
</tr>
<tr>
<td>Flow(s)</td>
<td>30 sccm</td>
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<tr>
<td>Pressure</td>
<td>300 mT</td>
</tr>
</tbody>
</table>

Table 2: Nitride etch process

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setpoint</th>
</tr>
</thead>
<tbody>
<tr>
<td>Push/Pull</td>
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</tr>
<tr>
<td>Ramp up</td>
<td>30Min</td>
</tr>
<tr>
<td>Soak</td>
<td>1100°C/210Min</td>
</tr>
<tr>
<td>Ambient</td>
<td>Wet O2</td>
</tr>
<tr>
<td>Ramp Down</td>
<td>60Min</td>
</tr>
</tbody>
</table>

Table 3: Sacrificial Oxide process
Following the oxide growth, a second nitride layer is grown on top if it. This nitride layer is deposited under the same conditions as the previous one. This layer is going to be the bottom layer of the protective coating surrounding the filament. Figure 4 show the resulting cross sections.

The next step is to deposit a metal layer to be used as a filament. This experiment used both polysilicon and a titanium/tungsten alloy as the filament. The polysilicon was grown under the following conditions.

<table>
<thead>
<tr>
<th>Parameter</th>
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</thead>
<tbody>
<tr>
<td>Temperature</td>
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<tr>
<td>Gas(es)</td>
<td>SiH₄</td>
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<tr>
<td>Flow(s)</td>
<td>90 sccm</td>
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<tr>
<td>Pressure</td>
<td>350 mT</td>
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</tbody>
</table>

Table 4: Polysilicon CVD process

The poly should be doped p-type using a spin on dopant. The boron was driven into the poly for 10 min at 1050°C in Wet O₂. The resulting sheet resistance should be approximately 50 Ω/square.

The TiW film was deposited at CVC products using the recipe in Table 5. The resulting film thickness was approximately 2000 Å and had a sheet resistance of 3Ω/square.

<table>
<thead>
<tr>
<th>Parameter</th>
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<tr>
<td>Flow(s)</td>
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<td>Bias Power</td>
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<tr>
<td>Target - Wafer Distance</td>
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</tbody>
</table>

Table 5: TiW Sputter process

Following the deposition of the metal film, the filament pattern should be etched using the process in Table 6. Both the polysilicon and the TiW films will be etched using the same process.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setpoint</th>
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</thead>
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<tr>
<td>Gas(es)</td>
<td>SF₆</td>
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<tr>
<td>Flow(s)</td>
<td>42 sccm</td>
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<tr>
<td>Pressure</td>
<td>300 mT</td>
</tr>
</tbody>
</table>

Table 6: Metal etch process

Following the metal etch process, a third nitride layer is deposited. This layer is repeat of the first two processes and it will act as the top filament protective layer. The cross sections in Figure 5 show the device at this stage of processing.

After the nitride is grown, the wafers are again patterned and the nitride is etched off. This will expose the sacrificial oxide under the filament but will leave the metal filament isolated from the outside world (see Figure 6). At this point, a 3µm Oxide is grown on the wafer. This is done using a Tetra-ethyl-ortho-silicate (TEOS) process. This layer will act as a top sacrificial layer and will help suspend the filament inside the mini-chamber (see Figure 7).

After the oxide is grown, the wafer must be patterned and etched. This etch will provide an anchor hole for the nitride cap layer. After the etch is done, a capping nitride layer is deposited. This layer needs to be thick enough to preserve the vacuum integrity of the device. On average, the thickness should be on the order of 2-3µm (see Figure 8).

The capping nitride must then be patterned and etched with holes in which the sacrificial oxide can be etched. Once the holes are etched in the capping nitride, the wafers are placed in a Buffered Oxide Etch (BOE) solution that will remove the sacrificial oxide layers. The etch rate of the BOE is on the order of 1000Å/min so the wafers need to be left in the solution for a few hours so that all of the oxide can be removed. Following the BOE etch the wafers are places in a KOH etch solution. This solution is a 20% by weight solution at 75°C. This solution will etch the silicon substrate in a V shape. This V shape will redirect any light that is emitted down and shine it to the surface (see Figure 9).

The next step is sputter Aluminum. This time the aluminum will be used for two purposes. The obvious reason is to create a good electrical contact to the filament. The second reason is to seal the cavity underneath the filament. When the aluminum seals the cavity, the pressure inside the cavity will be the same as the pressure at which the Aluminum is sputtered (see Figure 10).

Finally the Aluminum should be patterned and etched. The final cross sections are shown in Figure 11. After the Al is etched, the devices can be tested by attaching a power source to either side of the filament.

**PROCESSING ISSUES**

Quite a few issues were come across while trying to fabricate the device. One of the biggest issues is that the time allowance to fabricate this device was short. The proper attention could not be paid to each of the individual processes. In many cases, the previous work was used as a basis for these processes but there were a few that there had been no previous testing.

For instance, there had been no interest in optimizing a dry etch process for TiW. There had been some work with TiW but it was all for CMP related research. A process was found in some papers and it was utilized at RIT. Wafers were not available at the time to check the process prior to the need for it. This caused an issue in and of itself. When the TiW was etched (to define the filament) there was shadowing around the features. In other words,
the nitride around the edges of the features was etching as well so the features were not as defined as they should be.

In the process of modifying the stepper program, the offsets were changed by 1mm. This made the overlay between levels shift by 2mm. This took several days to pinpoint the problem and correct it. Once the source of the problem was found it was easy to correct but the time table in which to complete the processing grew even tighter.

The final and most crucial issue came when the protective layer was to be etched. The etch was designed to remove approximately 4000Å of nitride. This would have etched the nitride back down to the sacrificial oxide layer. However, when this etch was done the probe contacts were not protected with photoresist. Therefore, the process etched the 1500Å of nitride on top of the filament and then it etched through the metal filament back down to the underlying nitride layer. Due to this process miscalculation, the device could not be manufactured beyond this point since there was no way to test the filament. At the time the mask was designed, the etching chemistry was not known. Therefore, this level was designed improperly.

CONCLUSIONS

Several important things can be learned from this project. First of all, never trust other people to leave your recipes alone. Somehow, the stepper recipe was tampered with which caused a major delay in processing. The fix was simple but the downtime could have seriously impeded the research.

The second lesson learned was that recipes that are proven in other labs do not necessarily transfer to this one exactly. Some monitor wafers should have been coated with TiW along with the device wafers. This would have enabled the process to be optimized prior to the etching of the device wafers. Therefore any harmful side effects resulting from the shadowing would be eliminated.

Finally, the use of an etch stop is extremely important. If an etch stop was used surrounding the metal filament then the etching of the contact pads could have been prevented. There would need to have a slight process modification, which would be to deposit a low temperature oxide (LTO) just prior to the metal for the filament. After the filament is etched then the etch stop should be deposited again. This would prevent the accidental over etching of one film into the next film.

Another way to prevent this from happening would be to correct the mask level so that the probe contacts are protected during the protective layer etch. This is only a band aide because over etching is still a problem at other levels.

All in all, this experiment was troubled from the start. Given the numerous issues with this investigation, it was a great learning tool. After all, how many devices are completely fabricated and function properly the first time.

REFERENCES


ACKNOWLEDGEMENTS

The author would like to thank Dr. Santosh Kurinec for her guidance with the project, Kathy Hesler for her assistance with the stepper program and overlay issues, Dave Yackoff for keeping the stepper in an operational state for the duration of the project and everybody at CVC for allowing me to process wafers on an R&D machine.

APPENDIX

Figure 1 : Final Encapsulated Cross Section
Figure 2 : Final Cross Section Non-Encapsulated
Figure 3 : Cross Section # 1
Figure 4 : Cross Section #2
Figure 5 : Cross Section # 3
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Silicon Based Light Emission
by
Avalanche Breakdown of Shallow p+/n+ Junctions

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Abstract—The objective of this study was to develop and demonstrate a technology for producing optical signals on a VLSI chip using only standard silicon processing techniques. The design of the process requires shallow p+/n+ junctions to minimize the high absorption inherent in silicon for \( \lambda < 850\text{nm} \) and to obtain low reversed biased voltages for avalanche breakdown due to impact-ionization. The effects of doping and device geometry on the visible luminescence of reverse biased Si p+/n+ junction diodes has been investigated. Each diode designed has a unique design incorporating sharp edges that promote high fields that aid the onset of breakdown. The p+-doping was varied while other processing parameters were held constant. All vertical junction diodes had excellent diode characteristics but no light emission was observed. Lateral junction diodes had typical reverse breakdown voltages of between 6 and 7 volts while certain devices of set geometry broke down rather sharply at 4 volts with light emission. Intensity and breakdown characteristics seemed to correlate with magnitude of p+ dose and device geometry.

I. INTRODUCTION

The use of Silicon light emitting structures promises to be a strong contender in the future as an effective electro-optical source in opto-electronic integrated circuitry. This study is the collaboration between Dr. David V. Kerns of Vanderbilt and RIT. In the past the intensity obtained was typically low with quantum conversion efficiencies of \( 5 \times 10^{-8} \) [1,2]. Because of the high absorption coefficient for wavelengths below 850nm it is not surprising that intensity of visible light in this range suffers. This study and others that have preceded it minimize light absorption by optimizing the device design [3]. Here in this study both co-planar controlled and electric field confinement devices were fabricated to assist in increasing quantum conversion efficiencies. On going challenges for integrating these devices into CMOS technology are: (1) increasing the adaptability of device design and fabrication procedures for standard bipolar or CMOS processes, (2) increasing both the electrical-to-optical power and quantum conversion efficiencies associated with silicon LEDs, (3) increasing the lateral uniformity in emissions from LED’s surfaces, especially the avalanche-type diodes, and (4) lowering the operating voltages and currents associated with these diodes [4].

II. FABRICATION

The device wafers were n-type (100) silicon with an average resistivity of 5.7\( \Omega \cdot \text{cm} \). Of the 13 wafers, 10 were allocated for device wafers and 3 were used as control wafers. The 10 wafers were scribed: PR1-10 and the control wafers were scribed: D1-3.

An implant with Phosphorus at a dose of \( 3 \times 10^{14} \) P\(_3\) ions/cm\(^2\) with an energy of 100keV followed n+ lithography for all wafers. Wafer PR-10 was chosen for a blanket implant of 4 different doses, each occupying one quarter of the wafer surface. Supreme-3 simulations gave junctions depths of \( x_j = 0.254, 0.325, 0.349 \) and 0.370\( \mu \text{m} \) for the doses: 4, 5, 6 and 7\( \times 10^{15} \) BF\(_2\) ions/cm\(^2\) respectively. Actual junction depths for these for doses were: \( x_j = 0.345, 0.299, 0.409 \) and 0.449\( \mu \text{m} \) respectively and were obtained using the "groove and stain" technique. Surface concentrations ranged between 1.9\( \times 10^{20} \) to 2.8\( \times 10^{20} \) BF\(_2\) ions/cm\(^2\).

During the p+ implant it was found that the lateral devices received insufficient dopant through a large oxide of about 2600 \( \AA \). This necessitated a split in the device wafers so that lateral devices could be recovered. The split consisted of wafers D1,PR-1,3,5 and 7 for continued processing for vertical diodes and was designated "lot-1." Wafers D2, PR-2,4,6 and 8 were called "lot-2" and re-worked by etching the oxide over the p+ regions for the vertical and lateral structures. These vertical regions experienced a second implant since they originally received p+ dopant through a masking oxide of about 980 \( \AA \). This was designed to help achieve a more shallow junction. While etching the oxide it was found that since BF\(_2\) was present the etch rate decreased.
from the normal rate of 900 Å/min. down to 180 Å/min. Initially the etch was done in a buffered oxide etch (BOE) which after the second p+ implant and resist ash was found to be severely over etched. An RIE etch would have been more appropriate for removing this oxide since it is highly an-isotropic. The doses and energy determined in Supreme-3 were: 7x10^{14}, 1x10^{15}, 3x10^{15} and 4x10^{15} BF_2 ions/cm^2 at an energy of 120kev. For the anneal a wet oxide was used since no oxide was present for contact isolation and was best in this case to keep the implant from being driven in too deep.

Both lots next received contact cut lithography and since BF_2 was present an RIE etch was used. The gases used were: 25 sccm CF_4, 10 sccm CHF_3 and 80 sccm of Argon with power and pressure set at 100 watts and 200 mT respectively. The masking resist was then removed in a Plasma-line asher for 50 minutes then RCA cleaned. An HF dip was included to help reduce residual oxide before sputtering of the alloy Al/Si in the CVC601 sputter tool. The sputter was done in an Argon ambient with a base pressure of 1.4x10^{-5} Torr. A pre-sputter was done before the actual sputter to help reduce any contaminants that might have been present on the Al/Si target. An average aluminum thickness of 0.887µm was measured using the Tencor "alpha step" tool.

Finally photo level four for metal patterning was done. This step was followed by an aluminum etch. The etch time was approximately 1.5 minutes per wafer. A sinter at 450 Celsius in H_2N_2 was done to help improve ohmic contact and the 1% silicon in the aluminum helps to alleviate migration of silicon into the aluminum that can cause spiking and eventual shorting at the junctions. The following page shows the device chip.

III. RESULTS

All testing was performed using an HP4145, probe station and voltage source. Lot 1 was tested for vertical device behavior. All I-V curves were very symmetric with a reverse breakdown voltage (V_{BR}) of 3 volts and forward turn on voltage (V_{F}) of about 3 volts. These devices emitted no light. Both forward and reverse characteristics were sharp, showing no sign of series resistance.

Lateral devices from lot 2 gave good results. All devices that had an I-V curve also emitted light. Wafers tested from lot were PR-2,4,6 and 8 with doses: 7x10^{14}, 1x10^{15}, 3x10^{15} and 4x10^{15} BF_2 ions/cm^2 respectively. Table 1 shows a summary of light emission observed by dose and device geometry. It is clear from table 1 that in the F-series of devices F5-9 emitted light across all 4 doses tested. This is no surprise since these devices are virtually identical in geometry and are the simplest in design. They are constructed such that the p+ material lies in a circular plain surrounded by an n+ ring concentric around the p+ material. Under reverse bias light was first seen around the aluminum contact over the n+ ring at 7.5 volts and 10mA for the lowest dose and was 6 volts for the highest. The light observed extended through the whole circumference as the current exceeded 20mA at 12 volts regardless of dose. Series resistance in the reverse characteristic was observed to be worst with lower dose. Considerable improvement in the lack of series resistance was observed in the same device at the highest dose of 4x10^{15} BF_2 ions/cm^2. All devices had a V_{F} of between 2.5-3 volts with the exception of device D8, which had a V_{F} of about 1 volt and only functioned on the wafer with the highest dose. Device D8 had very sharp forward and reverse characteristics and its geometry consisted of three rows of sharp zig-zag like p+ structures centered across a square n+ plain. Devices F1-4 only functioned and emitted light at the highest dose tested with the exception of F3, which also functioned on the third highest dose of 1x10^{15} BF_2 ions/cm^2. Device F3 is a made up of a crescent shape n+ region over a circular p+ region. When under reverse bias the crescent shape was highly defined by the outline of a bright yellow/orange luminescence. Device F4 also showed bright light defined by its coil like n+ structure concentric about a p+ circular plain.

The second best series of devices tested that emitted light was the E-series. E5 and E6 emitted light over all doses. Their geometry resembles two sine like patterns superimposed over each other running 180 degrees out of phase, each pattern being of opposite doping. There are three rows in this pattern and when under reverse bias a grid of pin point light is seen through the microscope and is well defined. Again all operating characteristics are the same as that described for the F-series. All the C-series devices failed to operate and it is not understood why at this time. Their geometry is not unlike that described above for the D-series devices.

The lowest breakdown voltage of less than 5 volts was observed in one device among the B-series. Device B1 is made up of n+ wedge shapes placed concentrically over a circular p+ plain. Although it had the lowest V_{BR} its light emission was rather weak and the device could not withstand currents above 30mA at 15 volts where as all the other devices could be reversed biased as high as 30 volts at 200mA before failure occurred. See figure 2 and 5 for device B1 and its matching I-V curve. Figures 3 and 4 show a typical device E3 and its I-V curve. Devices like E3 and B1 are a good example of a field confinement type devices. An electric field confinement was created at the p'n tips when biased.
Table 1: Light emission observed by dose and device geometry.

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</table>

* = Breakdown is ≤ 5.0 volts

** = Light Observed for Wafer Id. PR-2, Dose = 7x10¹⁴ BF₃ ions/cm²

▼ = Light Observed for Wafer Id. PR-4, Dose = 1x10¹⁵ BF₃ ions/cm²

♦ = Light Observed for Wafer Id. PR-6, Dose = 3x10¹⁵ BF₃ ions/cm²

A1.....F9 = Device Types.

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Figure 2: Device B1

Figure 3: Device E3

Figure 4: Characteristic curve for device E3

Figure 5: Characteristic curve for device B1
IV. SUMMARY

The objectives of observing light under relatively low reverse bias voltages and low currents was realized. It was found that higher doses most likely are of interest for field confinement type devices. Co-planar surface devices such as in the F and higher E series devices worked over a wider dose range. Geometry is important but process technique and materials is a key factor in achieving devices that can be integrated into the CMOS process. Of principle importance is the quantum efficiency and photonic yield that results from silicon light emitting structures. These parameters are important in that they help to determine the viability of these devices as electro-optical sources to be used in opto-electronic integrated circuitry.

REFERENCES


ACKNOWLEDGMENTS

The author would like to thank Prof. D.V. Kerns, Jr. of Vanderbilt University for his guidance and support. Special thanks are due to George Lungu for chip design and other help. The help and support from all RIT clean room technicians, especially Richard Battaglia and David Yackoff is highly appreciated. The author acknowledges the advice of Dr. Santosh Kurinec for the project, Dr. Karl Hirschman, Dr. Mike Jackson, Dr. Richard Lane, Dr. Lynn Fuller and the staff of Advanced Vision Technologies, Inc. for their valuable input. Finally, the author is grateful to Dr. Renan Turkman for providing mentorship throughout his studies.

Peter I. Ritchie, originally from Rochester, NY, received B.S. in Microelectronic Engineering form Rochester Institute of Technology in 1999. He attained internships at Quantum Corp. and Intel Corp.