Investigation of Reactively Sputtered Titanium Oxide Memristors

Wilkie Olin-Ammentorp

Follow this and additional works at: http://scholarworks.rit.edu/theses

Recommended Citation
Investigation of Reactively Sputtered Titanium Oxide Memristors

by

Wilkie Olin-Ammentorp

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Materials Science and Engineering

Department of Materials Science and Engineering
College of Science

Rochester Institute of Technology
Rochester, NY
August 20, 2015
Investigation of Reactively Sputtered Titanium Oxide Memristors

By Wilkie Olin-Ammentorp

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Materials Science and Engineering

Approved by:

Dr. Santosh K. Kurinec, Professor (Advisor) August 20, 2015

Dr. Karl D. Hirschman, Professor August 20, 2015

Dr. Michael A. Jackson, Associate Professor August 20, 2015

Dr. Casey W. Miller, Associate Professor August 20, 2015

Department of Materials Science and Engineering
College of Science
Rochester Institute of Technology
Acknowledgments

I’d like to thank the following people for their invaluable assistance:

The members of my committee: Dr. Santosh Kurinec, Dr. Karl Hirschman, Dr. Michael Jackson, and Dr. Casey Miller.

The members of the SMFL staff: Patricia Meller, Sean O’Brien, Rich Battaglia, Scott Blondell, Tom Grimsley, John Nash, Bruce Tolleson, and Dave Yackoff.

My fellow students: Karine Florent, Matt Filmer, and Eric Pethybridge.

Jim Carroll of Photomask Portal and David MacMahon of Micron

Lastly, I’d like to dedicate this work to my family.
Abstract

Over the previous decade, flash memory has made massive gains in storage density and market share. However, due to fundamental scaling limits being reached, a replacement memory device must be found. Resistive random access memory (RRAM) is a leading candidate to replace flash memory as a storage-class memory. RRAM is a broad classification of devices, all of which share the commonality that their information is stored in the resistance of a material. These devices are often described as being memristive.

The objective of the study performed was to develop a process for fabricating microelectronic structures to investigate the memristive behavior of materials. The first approach taken was to explore a self-aligned fabrication process that relies on angular deposition of electrodes to create crossbar structures. These structures consist of a bottom electrode, the material being characterized, and a top electrode. Issues related to access to contacts were encountered while using the self-aligned process, and it was refined into an improved process. This process used conventional lithography and patterning techniques to replace the angular self-aligned deposition.

The improved process successfully demonstrated memristive switching of a titanium oxide film, with on/off ratios of $4.25 \cdot 10^5$ at 1 V observed. Set voltages of 3 V were used to switch the memristors into a low-resistance state. Large variations in resistances between devices were observed, and are commonly encountered in memristors at microscales due to stochastic nature of filament formation. Further work using shaped electrodes to improve characteristics has been proposed, and a shaping etch which could be applied towards this goal was demonstrated.
Contents

1 Introduction 1
   1.1 The Memory Hierarchy ................................. 1
   1.2 Flash Memory ....................................... 3
   1.3 Emerging Memories .................................. 5

2 Resistive Random Access Memory 6
   2.1 The Memristor ...................................... 6
   2.2 Resistance Change in Transition Metal Oxides .............. 9
   2.3 Titanium Dioxide as a Memristive Material .................. 11

3 Self-Aligned Crossbars 14
   3.1 Goals and Motivation .................................. 14
   3.2 Crossbar Test Structure ............................... 14
   3.3 Self-Aligned Shadow Deposition ......................... 15
   3.4 Reactive Sputtering of Titanium Oxides ..................... 19
   3.5 Experimental Deposition of Titanium Oxide Films ............ 19
   3.6 Results ............................................. 23
   3.7 Conclusions ......................................... 24

4 Conventional Crossbars 25
4.1 Fabrication ......................................................... 25
4.2 Aluminum Electrode Memristors ................................. 29
4.3 Platinum Electrode Memristors .................................. 31
  4.3.1 Initial Electrical Testing .................................. 32
  4.3.2 Sequential Reading and Resistance ......................... 34
  4.3.3 Erasure Difficulty and Device Size ....................... 35
  4.3.4 Slow Set .................................................. 36
4.4 STEM Analysis .................................................... 38
  4.4.1 Introduction to STEM and EELS ......................... 38
  4.4.2 STEM Images of Platinum Crossbar Stack ............... 39
4.5 Challenges in Reactive Sputtering .............................. 42
4.6 Conclusions ...................................................... 44

5 “Lightning-Rod” Crossbars ........................................ 45
  5.1 Fabrication ..................................................... 45
  5.2 Experimental Shaped Silicon Etch ............................ 48
  5.3 Conclusions ..................................................... 51

6 Conclusions and Future Work .................................... 52

A Processing Steps .................................................. 54
  A.1 Preparation .................................................... 54
  A.2 Shaped Etch .................................................... 54
  A.3 Bottom Electrode .............................................. 55
  A.4 ILD and Contacts .............................................. 56
  A.5 Top Electrode .................................................. 56
  A.6 Pad Clearout .................................................... 57
# List of Figures

1.1 Illustration of the memory hierarchy ........................................... 2  
1.2 Types of memory and their mechanisms ........................................ 3  
1.3 Overview of a flash memory cell ................................................ 3  

2.1 The six relationships between the four fundamental circuit variables, completed by the memristor ......................................................... 7  
2.2 An illustration of the switching behavior of an ideal memristor .......... 8  
2.4 Illustration of the formation of conductive pathways in a TiO$_2$ device. 12  

3.1 A crossbar test structure ............................................................. 15  
3.2 Illustration of shadowing effects causing selective deposition (dark areas will not be deposited on). The source in this image is in the lower-right hand corner. 16  
3.3 Illustration of the memristive film over the bottom electrode creating two memristors in series. ......................................................... 17  
3.4 Illustration of misalignment causing deformation of the desired shadow pattern 18  
3.5 A 10° misalignment disrupting electrode deposition .......................... 18  
3.6 Optical constants ($n$ & $k$) extracted from VASE data, $\lambda = 500$ nm .. 22  
3.7 Crossbars fabricated by the self-aligned process .............................. 23  
3.8 Slight switching behavior in self-aligned memristor .......................... 24  

4.1 Overview of the photomask layout ................................................ 26
4.2 Layout of individual crossbar

4.3 Layout of passive crossbar matrix

4.4 A side profile of devices during fabrication, with all patterning done by lift-off

4.5 A current-voltage characteristic as applied bias is swept up

4.6 Switching of a \((1.7 \, \mu m)^2\) conventional aluminum - titanium oxide crossbar

4.7 Cross section of the conventional platinum - titanium oxide memristor

4.8 Micrograph of finished devices

4.9 Forming and reading several devices

4.10 Current-voltage sweeps of low-resistance (upper) and high-resistance (lower) states. An average on/off ratio of \(4.25 \cdot 10^5\) at 1 V was observed.

4.11 Influence of sequential reads on device resistance

4.12 Resistance and current data for device reset attempts

4.13 Resulting average resistance vs. the voltage level used in a long set pulse

4.14 STEM image of the cross-section of a platinum crossbar

4.15 STEM cross-section, labeled with materials

4.16 Atomic profile of crossbar, calculated by fitting to EELS data

4.17 Energy spectra of inelastically scattered electrons at the top and bottom of titanium oxide film

4.18 Diagram showing the sputter process inputs and their effects on the sputter

5.1 Illustration of a silicon dry etch

5.2 Illustration of the shaping etch process

5.3 Micrographs of the shaped silicon structures, filtered by a polarizer
List of Tables

3.1 Conditions of reactive sputter experiment ................................................. 20
3.2 Results of reactive sputter experiment ....................................................... 22
4.1 Data on the degradation of sputtering rates over sequential runs ................. 43
5.1 Conditions used in the LAM 490 for a shaped silicon etch .......................... 49
5.2 Conditions used in the Drytek Quad for a shaped silicon etch ...................... 49
5.3 Photoresist (PR) etch results for the two processes .................................... 49
5.4 Silicon etch results for the two processes .................................................. 49
Chapter 1

Introduction

The capacity of computer memory has increased exponentially in the previous decades, following a trend similar to Moore’s Law. This increase in capacity has been seen in many different types of memory, such as static random-access memory (SRAM), dynamic random access memory (DRAM), flash memory, and hard disks. Memory scaling has enabled computers to grow vastly in both their capabilities and applications. However, as is the case in both memory and logic technologies, the extreme scaling of devices into the nanometer regime makes continued planar scaling of historically successful devices impossible for a multitude of reasons. For solid-state memory in particular, a suitable successor to flash memory must be scalable below flash’s lower size limit of approximately 14 nm.

1.1 The Memory Hierarchy

Modern computers use a wide variety of different types of memory. Each is assigned a certain purpose based on its speed, cost, and durability. The fastest memory, SRAM, is reserved for CPU memory caches and registers. For practical purposes, this memory has no endurance limit. It is very fast, but also very expensive as each unit cell requires six
transistors. DRAM is not as fast as SRAM, but is much less costly, using one transistor and one capacitor per unit cell. DRAM is employed as the primary memory of a computer, where programs and moderate amounts of data are stored and accessed by the CPU. However, SRAM and DRAM are volatile, requiring power to retain data; a non-volatile storage memory is required to store data when a computer is shut down. Traditionally, the hard disk drive has served this purpose, as it is a non-volatile magnetic storage media with a low cost-per-bit. However, access times are very long on a hard disk, and unlike SRAM and DRAM, hard disks are not a solid-state memory; this limits their lifetime due to wear on drive bearings and other components [1],[2]. Figure 1.1 gives a graphical comparison of different memory types and their properties, including cost and latency. Figure 1.2 shows more information on the types of memory and their mechanisms.

Figure 1.1: Illustration of the memory hierarchy
1.2 Flash Memory

The combination of SRAM, DRAM, and a hard drive to form a typical computer was standard practice from approximately the 1980s into the early 2000s. However, flash memory became an alternative to hard disk drives as its density increased and costs dropped. Flash memory has much faster access times than hard disks and is solid-state, making it more rugged. However, the continued planar scaling of flash memory is not possible below approximately 14 nm [1].
Flash memory consists of a single transistor with an additional element, the floating gate, placed in an oxide between the transistor channel and the control gate. This physical arrangement is illustrated in figure 1.3. By using Fowler-Nordheim tunneling to ‘push’ electrons off the floating gate, and using hot carrier injection to charge it, the number of electrons on the floating gate can be controlled. If the floating gate is charged, this shifts the threshold voltage of the transistor. By controlling the charge on the floating gate, the threshold voltage can be shifted to represent different logical levels. Single-level cell (SLC) flash uses a charged and uncharged state to represent a ’1’ and ’0,’ but multiple-level cell (MLC) flash technology uses multiple charge levels (4 or 8) to store multiple bits (2 or 3) in one cell [1].

Through a combination of transistor scaling, improvements in MLC techniques, and advanced memory controllers, flash memory has become preferable over hard disks in a wide variety of applications. Smart phones, laptops, and desktop computers are all likely to have a flash memory component. Some hard disk drives now incorporate a smaller cache of flash memory to store the programs and data which are most often accessed, improving computer start-up times.

However, planar scaling of flash memory has reached its limits. Parasitic capacitances between adjacent memory cells has grown as the transistors have shrunk, making it more difficult to read the difference in threshold voltage created by the floating gate. The oxides which isolate the floating gate have also been thinned to enable scaling, but this negatively impacts endurance; a thinner oxide degrades more quickly as the floating gate is programmed and erased [1]. The combination of parasitic capacitances and endurance issues places a hard limit on the planar scaling of flash memory, which is approximately 14 nm. Memory manufacturers such as Samsung and Micron are switching to flash memory structures which can be scaled vertically to continue increasing memory density [3],[4]. However, even 3D scaling is limited; to reach ultimate scaling densities, a practical memory which operate at
dimensions less than 14 nm must be found.

1.3 Emerging Memories

There are many different physical mechanisms which can be utilized to create a computer memory. The 2013 International Technology Roadmap for Semiconductors (ITRS) Emerging Research Devices table identifies several avenues which are being widely pursued [2]. These include ferroelectric memories which store information through a stable electric polarization, spin-torque transfer magnetoresistive memory, using the giant magnetoresistive effect to store information in small magnetic domains, and phase-change memory, which changes resistance by modifying the material phase of a chalcogenide. However, the subject of this work is resistive random access memory, which has been heavily investigated over the past decade.
Chapter 2

Resistive Random Access Memory

Resistive memory is an emerging category which stores information encoded into the resistance of a material or device. When the resistance of a passive device changes based on its electrical biasing conditions and previous resistive state, then this device is termed a ‘memristor.’

2.1 The Memristor

Memristors are a circuit element which was first proposed by Chua on theoretical symmetry arguments. Between the four basic circuit variables, current, charge, voltage, and magnetic flux, combinatorially six possible relationships exist. Charge is the differential of current, and magnetic flux is the differential of voltage, which gives two relationships.

\[ dq = I \cdot dt \]  \hspace{1cm} (2.1)

\[ d\phi = v \cdot dt \]  \hspace{1cm} (2.2)

The three traditional passive electronic components, the resistor, capacitor, and inductor,
create an additional three relationships between the four variables.

\[ dv = R \cdot dI \]

\[ dq = C \cdot dv \]

\[ d\phi = L \cdot dI \]

It was argued that to complete the set of six possible relationships, there was one missing passive element which would relate magnetic flux and charge [5]. Figure 2.1 illustrates these six relationships and highlights the missing relation.

\[ d\phi = M \cdot dq \]

Figure 2.1: The six relationships between the four fundamental circuit variables, completed by the memristor
This element was given the name ‘memristor,’ a portmanteau of ‘memory’ and ‘resistor.’ An ideal memristor displays a hysteresis in a current-voltage sweep, switching between high and low resistances as the voltage is swept up and down. This produces a pinched hysteresis loop on a current-voltage characteristic, as shown in figure 2.2. The magnitude of this behavior shown will be dependent on the value $M$, the “memristance.”

![Figure 2.2: An illustration of the switching behavior of an ideal memristor](image)

One application of the memristor is to store digital information. In this case, a high-resistance state can be used to store a 0, and a low-resistance state, a 1. While a memristor can be used to store digital information, their unique behavior also creates many alternative applications. This includes a physical implementation of advanced learning techniques such as neural nets. Neural networks physically implemented by a matrix of memristors has recently been demonstrated, showing future possibilities for low-power computers with deep learning capabilities [6].

When a memristor is being used as a digital memory, there are several key metrics which it must meet in order to be accepted as a mainstream memory. These include endurance,
on/off ratio, power usage, data retention, cost, and yield. While several of these properties are difficult to measure (endurance measurements can take months), others are not. On/off ratio is easily measurable through electrical testing, and power usage is related to the voltages needed to read and program the devices.

One other consideration for device operation is the polarity of the memristor. Bipolar memristors require a voltage of one polarity to switch to the low resistance state, and the opposite polarity to reset to the high resistance state. In unipolar memristors, only the current levels matter; a lower current level can set the device into a low-resistance state, and a higher current level will reset it into the high-resistance state.

![Diagram](a) A unipolar device, with set and reset independent of polarity ![Diagram](b) A bipolar device, with set and reset dependent on polarity

Many resistance-change memories are described as memristors. They may not meet the ideal definition of a memristor as it was first proposed, but the term has been broadly accepted to mean a type of memory which can switch resistance from electrical biasing.

### 2.2 Resistance Change in Transition Metal Oxides

A phenomenon where the resistance of transition metal oxides (TMOs) shifts from a high-resistance state to a low-resistance state after applying an electric field has been known
for some time. It has been found that the migration of defects through these films creates conductive pathways which change the resistance of the material. Electrical current and electric fields can cause these pathways to shift and reform, which results in a resistance state which is dependent on how the film has been biased [7].

The use of TMOs to create memristive devices is a concept which has seen great interest over the past decade. These devices have the potential to be stable, high-endurance, low-latency, and have been demonstrated at sizes under 5 nm [8, 9]. Resistance switching has been observed in many different transition metal oxides: TiO$_2$, HfO$_2$, ZrO$_2$, ZnO, Ta$_2$O$_5$, NiO, and many others have been used to form RRAM devices [10, 11]. In these materials, vacancies or interstitials in the materials’ lattices can increase the nearby concentration of free electrons. This increases the local conductivity of the material. [12] As a result, if enough mobile defects can gather to form a pathway of the material’s conductive phase, the overall resistance appears to decrease by orders of magnitude.

Each material has a unique set of characteristics and may have a certain advantage in endurance, programming voltage, and endurance. These parameters are also determined by each material’s interaction with its surroundings, normally the electrodes used to bias the device (though substrates have also been shown to influence device parameters). Electrode material also has a significant effect on determining the device’s stability and polarity [13].

Several different mechanisms can be responsible for the movement of defects through these materials. Drift, electromigration, Fick diffusion, and thermophoresis (electric fields, electron kinetic energy, concentration gradient, and temperature gradient, respectively) can all influence vacancies to move [9]. These effects can be used on defects with the end goal of changing the resistivity of a material, but their complex interactions makes fully understanding RRAM’s mechanisms a challenge. Titanium dioxide (TiO$_2$) has been focused on as a material for RRAM devices for several reasons: abundance of materials, CMOS compatibility, and good device characteristics. As a result, the resistance switching mechanisms in
TiO<sub>2</sub> are better understood than in many other transition metal oxides.

### 2.3 Titanium Dioxide as a Memristive Material

In TiO<sub>2</sub>, it is generally agreed that oxygen vacancies are responsible for creating the conductive titanium oxide phase [10]. In a stoichiometric TiO<sub>2</sub> film, an initial high-voltage forming (“electroforming”) step is required to create the vacancies. Equation 2.7 shows the reaction which drives creation of vacancies in TiO<sub>2</sub> in Kröger-Vink notation. In short, it expresses that an oxygen atom can leave its lattice site, creating oxygen gas, a double positively-charged vacancy, and two electrons. The oxygen vacancies can then be moved through the film by the previously mentioned mechanisms (drift, electromigration, etc.).

\[ O_o \leftrightarrow \frac{1}{2}O_{2,\text{gas}} + V_O^- + 2e^- \quad (2.7) \]

This reaction drives the formation of vacancies, but also creates gaseous oxygen which can build up and cause damage to the devices by rupturing electrodes. To avoid this, under-stoichiometric TiO<sub>x</sub> films are deposited under a thin stoichiometric layer to create a film which already has defects when deposited. This avoids the need for an electroforming step. Sputter conditions to create under-stoichiometric TiO<sub>x</sub> films were investigated in this work, with the goal of depositing films which would not require an initial electroforming step.

When a vacancy forms, it influences the valence cloud of nearby titanium atoms, which increases local conductivity. As a result, when positive vacancies are pushed by electric fields towards the low-potential electrode, the vacancies can effectively extend it into the insulating film. This changes the topology of the electric field, creating sites which have higher electric fields, and which draw in more vacancies. This self-sustaining effect grows with the filament, and results in filaments which usually grow to be conical in shape [14, 15].
Figure 2.4: Illustration of the formation of conductive pathways in a TiO$_2$ device.

Frame 1 in figure 2.4 shows a filamentary RRAM device in the high-resistance state. No conductive filaments exist between the top and bottom electrodes. In frame 2, a positive voltage is applied to the top electrode.

In frame 3, vacancies pushed to the cathode have begun to form into cohesive filaments. The conductive filaments extend a small distance from the bottom electrode, but do not yet touch the top electrode. As a result, there is no low-resistance pathway to take through the cell, and resistance remains high. However, partially extended conductive filaments can slightly increase device current by assisting tunneling.

The filaments continue to grow with the applied voltage. Once a conductive filament extends between the electrodes, current flows through it and drops the voltage applied between the electrodes. The device is then in the low resistance state, and is said to be ‘set.’ This is shown in frame 4 of figure 2.4. This low-resistance state is stable, and its contrast to the high-resistance state can be used to store information.

However, a working memory needs to be both writable and erasable. To return to the high-resistance state, large current densities traveling through the filament cause Joule heating, which can overwhelm the electronic effects keeping the vacancies in place, causing the filament to dissipate. This returns the material to a high-resistance state. However, vacan-
cies still exist inside the film. An applied bias can again cause these vacancies to form a conductive filament, returning the material to a low-resistance state. Through the disruption and reformation of these filaments, the material is programmed and depogrammed, or “set” and “reset.”

However, the filaments responsible for conduction are on the order of 10 nanometers in diameter. As a result, each time the device is set into the low-resistance state, a different filament with a unique resistance and forming voltage may be created [9]. Potential solutions include doping memristive materials to assist pathway formation and reducing device size to the same size as a filament [10]. An alternative mechanism investigated in this work is to use electrode geometry to make a smaller effective device area.
Chapter 3

Self-Aligned Crossbars

Initial investigations used a self-aligned process to create crossbar structures which would explore electrical properties of TMO films. The self-aligned fabrication method, described in this chapter, had several issues. To create better devices, this process was modified to use more conventional patterning methods, discussed in the next chapter.

3.1 Goals and Motivation

Due to the promising nature of resistive memory, it was desired to begin an investigation at RIT to fabricate and characterize these devices. The goal of this investigation was to establish a process which could be used to fabricate memristive devices, to electrically characterize the resulting devices, and to propose and investigate refinements to the fabrication process to improve electrical results.

3.2 Crossbar Test Structure

A crossbar is a simple test structure which can explore the electrical properties of a material. In a crossbar, a bottom electrode is deposited first, patterned by either lift-off or
etch. Next, the material which will be electrically characterized is deposited, followed by the top electrode. These two materials are then usually patterned by lift-off, to obviate the need to characterize a chemical etch for every deposited material. The upper and lower electrodes can then be separately biased, creating a voltage across the material being investigated and allowing current to flow. A 3D side profile illustrates the crossbar structure in figure 3.1.

3.3 Self-Aligned Shadow Deposition

To first investigate memristive switching of metal oxide films, an existing process created by another student was utilized to create crossbar structures [16]. In this process, a single layer of photoresist is patterned into a cross: two lines which intersect at a right angle to one another. By using shadow evaporation, this single layer can then be used to create a separate top and bottom electrode with a dielectric layer in between.

The self-aligned process takes advantage of the shadows generated by features. Inside an evaporator, the metal being deposited is heated in vacuum past its melting point, giving it a vapor pressure larger than the vacuum around it. This causes metal atoms to enter the gas phase, and because the vacuum level inside the evaporator is very large, the mean free path of the atoms is long. Effectively, this means the evaporation source can be thought of as a point-source of material.

To create a bottom electrode which only goes in a single direction, a wafer with the cross
pattern in photoresist is loaded into an evaporator. The wafer is oriented so that either the horizontal or vertical lines point towards the evaporation source. The lines pointed towards the source have a line-of-sight to it, and so material will reach the surface and adsorb. The other set of lines will be shadowed, and the deposition will be blocked, leaving no feature behind. Figure 3.2 illustrates shadowing from a light source, which is similar to the shadowing of material across the structure.

Using this self-aligned shadow deposition process, it is fairly simple to create a crossbar structure. First, the bottom electrode is created by the first shadow deposition. The wafer then receives a blanket sputter deposition of the memristive film being investigated. Then, the top electrode is deposited by shadow deposition over this film, creating the desired crossbar structure. Lastly, thick metallic bond pads are deposited and patterned over the ends of the electrodes to provide good sites for electrical contact. Using this method, alignment is not an issue, and there is a well-defined, small area where memristive film is being stressed by electric fields.

During the development of this process, there was an oversight in that the bottom electrode is entirely covered by the memristive film. This confounds testing, as it effectively an extra memristor between the bond pad and bottom electrode, as illustrated in figure 3.3. As
Figure 3.3: Illustration of the memristive film over the bottom electrode creating two memristors in series.

As a result, high voltages are needed to drive current through the structure, and if one device is set or reset, it may not be individually observable because it is in series another memristor.

It is possible to also use shadow deposition to pattern the memristive film so that it only sits under the top electrode, and not on top of the bottom electrode. However, this means that only memristive materials deposited by evaporation can be investigated. The films being investigated in this work were created by reactive sputtering, so a new process was needed to allow for blanket deposition of the memristive film.

There are also multiple issues found in the directional deposition created by the structure of evaporators. The evaporators used were bell jars which have a structure for holding the wafer towards the top of the machine, and a source at the bottom which can melt the desired material under vacuum (either by an incident electron beam or direct contact of the metal to a hot surface). Because of the size and layout restrictions of the system, wafers which are being placed at a grazing angle with respect to the source must be placed fairly close to the source. The density of evaporated material follows a rule similar to the inverse square law, and as a result, sections of the wafer which are closer or farther away from the source receive greatly differing amounts of deposited material. Measurements show that the electrodes at the top of the wafer and the bottom of the wafer differ by approximately 60 nm, or 12% of the total height.
Non-desired shadowing effects were also found across the wafer. Towards the side of the wafer, shadows created by the source not being directly centered on the cross creates shadows from the side of the structure. Additionally, if the wafer is not loaded with the proper angle (within $10^\circ$), so that the desired electrode is pointing directly towards the source, the sides of the structure will create unwanted shadowing on the electrode. This non-desired shadowing is illustrated in figure 3.4, and devices which exhibit electrode deformity due to rotational misalignment are shown in 3.5. Loading was done by hand, and this made it a step which was extremely susceptible to error.

Figure 3.4: Illustration of misalignment causing deformation of the desired shadow pattern

Figure 3.5: A $10^\circ$ misalignment disrupting electrode deposition
3.4 Reactive Sputtering of Titanium Oxides

The best available process to create a memristive transition metal oxide was reactive magnetron sputtering. In a normal sputter process, a non-reactive noble gas, usually argon, is used to strike a plasma. An electric field causes ions to collide with a target, composed of the material which is to be deposited. The incident ions knock some of the atoms off the target, which then diffuse away and can adsorb on the substrate which is receiving the deposition. In magnetron sputtering, the target includes magnets which cause electrons in the plasma to take a circular path around the target’s center, increasing the chance that they can ionize neutral gas atoms, increasing plasma density and deposition rates [17].

In most sputtering processes, the material which is desired for deposition is the same as the material which the target is composed of. However, by changing the composition of the sputtering ambient to include a reactive species, the composition of the deposited material can be changed. The reactive species colliding with the target, or sputtered material traveling through the ambient, can combine to form a new compound. In this case, oxygen is introduced into the argon ambient during a titanium sputter to create titanium oxides. Unlike atomic layer deposition, the stoichiometry of a reactively sputtered film cannot be tightly controlled [18],[19]. It is dependent on factors such as the energies of colliding atoms, the plasma density, and the amount of reactive gas present. All of these factors are controlled with some degree of precision, but experimental tolerances and changing energy and gas kinetics through a sputtering process make precise control challenging. The reactive sputter of titanium oxides proved to be the most challenging and problematic step of fabrication.

3.5 Experimental Deposition of Titanium Oxide Films

An experiment was carried out to characterize titanium oxide films deposited under different reactive sputter conditions. This information would then be used to determine
Table 3.1: Conditions of reactive sputter experiment

<table>
<thead>
<tr>
<th>Run</th>
<th>Argon (mT)</th>
<th>Oxygen (mT)</th>
<th>Argon (sccm)</th>
<th>Oxygen (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-sputter</td>
<td>12.0</td>
<td>0</td>
<td>18.0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>12.0</td>
<td>0</td>
<td>18.0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>11.8</td>
<td>0.2</td>
<td>17.6</td>
<td>1.37</td>
</tr>
<tr>
<td>3</td>
<td>11.6</td>
<td>0.4</td>
<td>17.3</td>
<td>1.48</td>
</tr>
<tr>
<td>4</td>
<td>11.4</td>
<td>0.6</td>
<td>17.0</td>
<td>1.83</td>
</tr>
<tr>
<td>5</td>
<td>11.2</td>
<td>0.8</td>
<td>16.6</td>
<td>2.38</td>
</tr>
<tr>
<td>6</td>
<td>11.0</td>
<td>1.0</td>
<td>16.2</td>
<td>3.04</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Run</th>
<th>Time, Closed\Open (s)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-sputter</td>
<td>0 \ 300</td>
<td>300</td>
</tr>
<tr>
<td>1</td>
<td>0 \ 200</td>
<td>300</td>
</tr>
<tr>
<td>2</td>
<td>20 \ 200</td>
<td>300</td>
</tr>
<tr>
<td>3</td>
<td>20 \ 200</td>
<td>300</td>
</tr>
<tr>
<td>4</td>
<td>20 \ 200</td>
<td>300</td>
</tr>
<tr>
<td>5</td>
<td>20 \ 200</td>
<td>300</td>
</tr>
<tr>
<td>6</td>
<td>20 \ 200</td>
<td>300</td>
</tr>
</tbody>
</table>

optimum process conditions to deposit under-stoichiometric TiO$_x$ and near-stoichiometric TiO$_2$ films. To achieve this, the partial pressure of oxygen in the sputtering ambient was varied from 0% to 9% of the total combined pressure of oxygen and argon. Other experiments have used similar partial pressures [20]. The system used for sputtering was a CVC 601 DC sputter system.

During the pre-sputter run, a shutter is moved over the target. The target is sputtered for 300 seconds to remove any native oxides or surface contamination. This shutter is then opened to start the deposition onto the stationary substrate. In the experiment, the partial pressure of oxygen was increased over six levels. For each level, a new substrate was rotated into place and received a blanket deposition. For each run which contained oxygen, an initial pre-sputter was done with the shutter blocking deposition - this allowed sputter conditions to reach a steady-state before the film was deposited onto the substrate, and prevented arcing.

One additional phenomenon found during reactive sputters is that the partial pressure of oxygen in the ambient appeared to gradually increase by 0.2 millitorr throughout the
sputter, while gas flow remained constant. This may be due to several causes; sputtering targets are subject to high electronic fields, and the process creates large amounts of heat. As a result, targets can become quite hot, and generally use water cooling on the target’s backside to prevent overheating. However, residual heat in the target can assist chemical reactions with the gas ambient, creating surface oxides. Initial heating of the target after the sputtering plasma is struck may cause an initial increased uptake in oxygen, which plateaus after the steady-state target temperature or surface reaction is reached. This creates another factor which must be considered in order to reactively sputter films with a specific chemical composition.

The deposited films were characterized by profilometry and ellipsometry. A section of Kapton tape was placed over the substrates before deposition. After deposition, the tape is removed. The step height between the bare silicon which is left and the film is measured by physically moving a stylus across the step, while measuring its position. This gives a physical measurement of the thickness of the film.

In ellipsometry, measuring the change in polarization of light is used to deduce the optical properties of a film by solving Maxwell’s equations. By varying the angle of incident light and its wavelength, additional information is collected which can give more details about a film’s properties. This method is known as variable-angle spectroscopic ellipsometry (VASE). However, fitting a model to solve for the optical properties from VASE data can be extremely challenging. By using the data collected by profilometry to provide an approximate film thickness, a starting point for the models is provided, and gives a better fit for the models’ solutions to the data. Figure 3.6 and table 3.2 show the results of these depositions. For comparison, the refractive index of stoichiometric TiO$_2$ at $\lambda = 500$ nm is 2.71 [21].
<table>
<thead>
<tr>
<th>Run</th>
<th>Argon (mT)</th>
<th>Oxygen (mT)</th>
<th>n, λ=500 nm</th>
<th>k, λ=500 nm</th>
<th>Deposition Rate (Å/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12.0</td>
<td>0</td>
<td>1.49</td>
<td>1.52</td>
<td>11.5</td>
</tr>
<tr>
<td>2</td>
<td>11.8</td>
<td>0.2</td>
<td>1.73</td>
<td>1.68</td>
<td>10.5</td>
</tr>
<tr>
<td>3</td>
<td>11.6</td>
<td>0.4</td>
<td>1.72</td>
<td>1.92</td>
<td>11.0</td>
</tr>
<tr>
<td>4</td>
<td>11.4</td>
<td>0.6</td>
<td>1.64</td>
<td>1.75</td>
<td>12.3</td>
</tr>
<tr>
<td>5</td>
<td>11.2</td>
<td>0.8</td>
<td>2.33</td>
<td>0.002</td>
<td>12.2</td>
</tr>
<tr>
<td>6</td>
<td>11.0</td>
<td>1.0</td>
<td>2.48</td>
<td>0</td>
<td>13.0</td>
</tr>
</tbody>
</table>

Table 3.2: Results of reactive sputter experiment

Figure 3.6: Optical constants (n & k) extracted from VASE data, λ = 500 nm

The transition between a oxygen-rich metallic film and a under-stoichiometric dielectric can be seen as partial pressure passes 7%, and the extinction coefficient drops to nearly zero. Visually, this is seen when the film changes from a shiny or cloudy metallic coating and a transparent coating. To create an under-stoichiometric TiO$_x$ film, an ambient of 0.8 millitorr of oxygen and 11.2 millitorr of argon was selected. Conversely, a higher oxygen content of 1.0 millitorr oxygen and 11.0 millitorr argon was selected to create the near-stoichiometric TiO$_2$ film.
3.6 Results

Despite processing challenges, the initial self-aligned process gave results which confirmed the memristive behavior of the TiO$_x$ (20 nm) and TiO$_2$ (60 nm) film stack between aluminum electrodes. Figure 3.7 shows a micrograph of the self-aligned crossbar structures which were fabricated. Electrical results are shown in figure 3.8.

![Crossbars fabricated by the self-aligned process](image)

Figure 3.7: Crossbars fabricated by the self-aligned process
These electrical results were unsatisfactory; set and reset voltages were on the order of 30 V, which is very high, and current levels were very low. An average on/off ratio of only 15.6 at 5 V was seen, which is orders of magnitude too low to be of use. The high set voltage was necessary to overcome the film between the bottom electrode and bond pad, which made a single structure into two serial memristors. Despite this, several state changes between high-resistance and low-resistance states were observed, encouraging further work.

3.7 Conclusions

To overcome the issues found in the self-aligned process, a new process to fabricate crossbar structures was devised, and is discussed in the next section. The revised process requires only a few more steps than the self-aligned process, but removes all the issues which were discovered with the self-aligned process.
Chapter 4

Conventional Crossbars

A new process was designed to create crossbar test structures without relying on shadow deposition. This would give greater control over the end structures and make devices more structurally uniform across the wafer.

4.1 Fabrication

The self-aligned steps used previously were replaced by traditional patterning methods. Bottom and top electrodes, as well as contacts and the memristive material, can be patterned in photoresist in both positive and negative tones. As a result, either a chemical etch process or physical lift-off process can be used to define any layer. To achieve this capability, a new layout and photomask were created. This design includes individual crossbar structures which vary in size from 0.5 \( \mu \text{m} \) to 10 \( \mu \text{m} \). Passive matrices of 6 by 6 memristors are also included to create a large number of samples with one size, from 0.5 \( \mu \text{m} \) to 2.0 \( \mu \text{m} \). Large capacitors are also included to allow for the collection of capacitance data. Figure 4.1 gives an overview of the mask’s layout, and figures 4.2 and 4.3 show zoomed-in detail of an individual crossbar and crossbar matrix, respectively.
An insulating substrate is normally desired to create isolation between devices. Bare silicon wafers are cleaned, and then a 500 nm SiO$_2$ layer is grown by thermal oxidation in a pyrogenic steam ambient. The first lithographic layer etches alignment marks into this oxide to allow for good registration between layers. Next, the bottom electrode is patterned; the process flow at this point depends on whether a chemical etch or lift-off will be used to pattern the electrode.

If a chemical etch is being used, the metal is deposited by whatever method is desired (PVD, ALD, etc.). A photoresist layer on top of the metal is patterned with positive tone; resist will be left where the electrode is desired, and protects the underlying material during the chemical etch. After the etch, the photoresist can be removed by an oxygen plasma or solvent strip.

If instead lift-off is being used to pattern the metal, the photoresist is patterned onto the wafer first. In this case, a negative tone is used; resist will be left where metal is not desired.
Then, the desired metal is deposited on top of the photoresist. After deposition, the wafer is placed into acetone and sonicated. Acetone causes the photoresist to dissolve, and the metal on top of it lifts off into the solvent. Once the lift-off is complete, metal is left in the regions where there was no photoresist underneath it.

To reduce the chance of leakage paths or defects creating a short between the top and bottom electrode, an inter-layer dielectric can be deposited. A contact layer will open a window in this material, restricting electrical interaction to the lithographically-defined area. However, if an etch is used to pattern this dielectric, it must be carefully chosen to not etch the underlying bottom electrode.

The most critical step of fabrication is the deposition of the memristive material; this,
more than anything else, will define the characteristics of the resulting devices. The sputter conditions selected after the investigation detailed in section 3.4 were used to deposit titanium oxides. It was assumed that deposition rates would remain constant under the same conditions, but this was later found to not hold true for reactive sputtering. Lift-off is used to pattern the memristive layer and the top electrode simultaneously, so that a selective etch does not have to be investigated for the memristive material. In this work, reactive sputtering was used to deposit the memristive film.

The top electrode is then deposited on top of the memristive layer, and the underlying lift-off resist is used to pattern both the memristive layer and top electrode simultaneously. This creates the crossbar structure.

Lastly, if an inter-layer dielectric was used, a photoresist layer is patterned which opens a window over the bottom electrode bond pads. The dielectric is etched away over this area, and the resist is removed, allowing for good electrical contact to the bottom electrode. A summary of this processing, using lift-off, is given in figure 4.4. Detailed information on processing is given in the appendices.
4.2 Aluminum Electrode Memristors

To verify the new process, pilot devices using aluminum electrodes and a titanium dioxide memristive film were fabricated. An etch was used to define the bottom layer, and lift-off was used to define the memristive layer and top electrode.

To create electroforming-free devices, a stack of non-stoichiometric TiO$_x$ (30 nm) and stoichiometric TiO$_2$ (5 nm) were deposited with the same reactive sputtering conditions which had been previously used. Thickness was reduced to investigate its influence on forming voltage.

An initial test to see if the devices were viable quickly swept the applied bias from 0 to 6 V in 0.1 V increments. Several current spikes were observed on the milliamp level, as shown

Figure 4.4: A side profile of devices during fabrication, with all patterning done by lift-off
Figure 4.5: A current-voltage characteristic as applied bias is swept up

in figure 4.5. It was found that when no current compliance level is set, this can “burn out” the device into a permanently high-resistance state. This is likely due to the high current densities which travel through a filament causing undue heat and permanently changing the device. For this reason, electrical testing of memristors usually employs a current compliance to prevent this. Current compliance was set to 100 nA and further devices were tested.

After this change was made, a 1.7 by 1.7 µm device was tested and demonstrated switching between a high and low resistance state, shown in figure 4.6. Devices showed an average on/off ratio of $1.46 \cdot 10^4$ at 1 V. This first test of the new process confirmed that memristors were successfully created, and further experimentation was validated.
4.3 Platinum Electrode Memristors

In many works, platinum is used as the electrode of choice for reference devices. This is because platinum is a noble metal, unlikely to have any chemical interactions with whatever material is being tested. For this reason, platinum electrodes were chosen for the next investigation.

Processing was carried out using lift-off patterning for top and bottom electrodes. A titanium adhesion layer was first deposited, followed by platinum. A TiO$_x$ (60 nm), TiO$_2$ (20 nm) film stack was deposited to replicate conditions used in another experiment using electroforming-free devices [22]. A platinum top electrode, followed by more titanium, was deposited last, forming the crossbar. An illustrative cross-section is shown in 4.7, and a
4.3.1 Initial Electrical Testing

Electrical testing of the devices quickly showed memristive behavior. Figure 4.9a shows the initial reading sweep of the devices in a high-resistance state. After a sweep to higher voltages, increases in current up to compliance level were seen, shown in figure 4.9b. Devices
then retained this low-resistance state for the next reading sweep, in figure 4.9c. Devices achieved a good on/off ratio of $4.25 \cdot 10^5$ at 1 V, shown in figure 4.10.

Figure 4.9: Forming and reading several devices
Figure 4.10: Current-voltage sweeps of low-resistance (upper) and high-resistance (lower) states. An average on/off ratio of $4.25 \times 10^5$ at 1 V was observed.

4.3.2 Sequential Reading and Resistance

One phenomenon which was observed was an apparent change in resistance after several read sweeps were done immediately after one another in a single device. This causes heating in the element, which temporarily raises resistance until it can cool again, shown in figure 4.11.

(a) Current-voltage characteristics of the sequential sweeps
(b) Average fitted resistance of the sequential sweeps vs. time

Figure 4.11: Influence of sequential reads on device resistance
This could be an issue in applications where rapid, sequential memory reads may be carried out on a single element. Engineering devices to have better thermal connections to the substrate could help fix this issue, but element heating is also important to reset devices. An equilibrium which allows devices to reset but prevents overheating should be found.

4.3.3 Erasure Difficulty and Device Size

Although it was observed that heat was likely influencing device resistance, the devices remained very hard to reset into a high-resistance state (a process assisted by heating). Several attempts were made to erase a $(1.5 \, \mu m)^2$ device. This was only successful when very high current levels were used; a $0.1$ A pulse finally succeeded in resetting the device to a high-resistance state (figure 4.12).

![Figure 4.12: Resistance and current data for device reset attempts](image)

In larger devices, the number of possible filaments which can carry current through the device is very large. Multiple filaments begin to form in a device, but the first one to carry current drops the voltage across the memristive film, halting the filament formation process. In a slow, high voltage and current erasure attempt, a single filament may be quickly disrupted by high current levels. This restores the voltage across the memristive
film, which can cause other filaments to grow, causing another connection. For this reason, a good erasure technique would likely need to use a short current pulse to cause the filament to reset, before the applied voltage can cause other conductive pathways to form.

This is supported by the fact that the smaller devices were sometimes disrupted by a low voltage read sweep into a high-resistance state. In the smaller devices, fewer possible paths can restore a low-resistance state. The reading sweep was also conducted more quickly than reset attempts for the large device.

Additionally, aluminum electrode devices were easier to disrupt into high-resistance state. This may be due to the aluminum electrode assisting in reactions. Electrostatic effects created by using different metals have been known to influence forming voltages and device resistance, and could be used to optimize erasure as well [11]. Smaller devices were also easier to reset into a high-resistance state. More investigation into the time-dependency of filament formation and the influence of the electrode materials could give more supporting information about device operation.

4.3.4 Slow Set

In most electrical testing of memristors, a parameter analyzer is used to quickly sweep the device through a range of applied voltages. However, time-dependency is an important factor in the change from a high-resistance to low-resistance state which is often ignored as a factor. Instead of using a parameter analyzer to characterize forming voltages, a pulse generator which gives a controlled burst of a single voltage for a defined amount of time can give important information.

Although many papers report on set voltage variation, few investigate or mention time-dependent forming of the devices. In the testing done on the platinum-titanium oxide devices, it was found that by using a long current pulse at a single voltage, most devices could be formed using a single voltage level. This is shown in figure 4.13.
Figure 4.13: Resulting average resistance vs. the voltage level used in a long set pulse

For the majority of devices, a 3 V pulse lasting 1 second was more than sufficient to form a low-resistance state. A longer pulse at a single voltage was more effective at reliably switching devices, and is simpler to implement as well. Additionally, it suggests that there is a critical field which has to be passed to allow defects inside of the film to become mobile and form conductive pathways.

Although this set operation is uniform in voltage, it appears to have no effect on the resulting resistance of the device, which still displays large variations. This fits in with the current understanding, which holds the variation in shape and size of the conductive pathway to be responsible for a device’s resistance.

One solution to improving device on-state resistance is to introduce a thin layer of an insulator, such as alumina, above the memristive film stack. This film serves as a well-defined series resistor, whose controlled resistance can become the dominant term in the total resistance of the film stack once the memristive layer has entered a low-resistance state. This gives improved uniformity between devices at the cost of on/off ratio.

A replicate of the successfully tested platinum-titanium oxide devices with an additional alumina layer was created, but due to an error in deposition, the alumina layer was too thick.
This prevented a low-resistance state from being seen at all.

### 4.4 STEM Analysis

Samples of the platinum crossbar structure were sent for analysis by scanning transmission electron microscopy (STEM) and electron energy loss spectroscopy (EELS). These two techniques together give a great deal of information on the physical, chemical, and electronic properties of a sample.

#### 4.4.1 Introduction to STEM and EELS

STEM microscopy is very similar to regular transmission electron microscopy; the probability that free electrons encountering the sample can tunnel through without being absorbed or scattered creates contrast, forming an image. In the case of STEM, however, a beam only exposes a very small portion of the sample at once, similar to scanning electron microscopy. The beam is then rastered across the sample to create a full image.

The advantage of STEM over TEM is that the electron beam only interacts with a small region of the sample at once. The material composition of the sample which is being investigated will have a dramatic effect on the electrons which emerge from the sample. If these electrons are sorted by energy, information about what scattering events the electrons have encountered can be extracted. Inelastic scattering events can be directly related to interactions with characteristic atomic energy levels, and this signature energy loss can be measured in the distribution of observed electron energies. The elements which the electrons have scattered off of can then be determined [23].

This technique is known as EELS, electron energy loss spectroscopy. It is sensitive enough to determine not only elements, but different forms of elements through their bonding energies. Techniques like EELS are not possible with traditional TEM, as the electrons travel
through the entire sample at the same time, confounding the energy spectra of different interactions.

### 4.4.2 STEM Images of Platinum Crossbar Stack

Images of the sample were taken on a Hitachi HD-2300A STEM, equipped with a Gatan Enfina Parallel EELS system.

![STEM image of the cross-section of a platinum crossbar](image)

Figure 4.14: STEM image of the cross-section of a platinum crossbar

Comparing figure 4.14 to the desired cross section, illustrated in figure 4.7, it can be immediately seen that the titanium oxide layer is much thinner than was desired, and that the titanium electrodes are also quite rough. Figure 4.15 shows a zoomed-in cross-section with the materials labeled.
The thickness of the deposited titanium oxide film is on the order of 10 nm, although this varies across the device due to the electrode roughness. This is one-eighth of the thickness which was targeted using previous deposition rates; it is quite evident that the deposition rates determined in section 3.4 did not remain constant. Several tested devices which appeared as permanent shorts are likely to be due to metallic peaks from the bottom or top electrode contacting one another.

However, the composition of the memristive film as a titanium oxide was confirmed. Figure 4.16 shows the composition of the film along a line, as determined by EELS. Significant levels of carbon were also detected inside the film, which could be due to the reactive sputter etching the lift-off photoresist introducing carbon into the sputter environment.
The electron energy spectrum at points at the top and bottom of the titanium oxide layer are shown in figure 4.17. The spectra are similar to, but do not match precisely, the reference spectrum for titanium dioxide. This could be due to the desired under-stoichiometry of the film, or the carbon contamination influencing the titanium oxides.
4.5 Challenges in Reactive Sputtering

At first glance, reactive sputtering can appear to be a simple modification to traditional sputtering. However, with further investigation the kinetics of the reactions inside the sputtering system are revealed to be complex.

In the sputtering system used (a CVC 601 DC sputter system), the user controls four basic inputs: the gas flows used to create the ambient, the pressure of the gas ambient, the plasma power, and the sputtering time. Other factors, such as substrate rotation and radiative heating, are controllable but were not investigated.

These four inputs exert control over the pressure and composition of the sputtering ambient, as well as how fast it is being replenished by incoming gases. Plasma power and time control the degree of ionization in the ambient, the creation of reactive free radicals, and the ion energy. This, in turn, influences the composition, temperature, and sputter...
yield of the target. As a reactive sputter proceeds, these factors can all change, giving a deposited film and sputter process with different characteristics. Figure 4.18 illustrates how these factors feed into one another.

![Diagram showing the sputter process inputs and their effects on the sputter](image)

Figure 4.18: Diagram showing the sputter process inputs and their effects on the sputter

The significant drop in deposition rates of the reactive sputter may be due to a change in the target itself. A 4 inch titanium target was used in the system for a reactive sputter. As the sole user of that target, sequential reactive sputter runs may have saturated its surface layer with oxygen, turning it into titanium dioxide. A five-minute pre-sputter with pure argon gas was run before each deposition, but this may not have been effective in removing the titanium oxides from the target’s surface. As time built up, the surface oxide thickness may have kept growing, and reduced sputter yield to the point where no material was deposited; the next reactive sputter under the same conditions had no detectable material deposited, even by ellipsometry. Table 4.1 shows how much the sputter rates decreased over several sequential runs.

The current and voltage used to create the sputtering plasma could give insight into how

<table>
<thead>
<tr>
<th>Deposition</th>
<th>Deposition Rate (Å/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Experimental Run</td>
<td>12-13</td>
</tr>
<tr>
<td>Platinum Crossbars</td>
<td>0.53</td>
</tr>
<tr>
<td>Shaped Crossbars</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 4.1: Data on the degradation of sputtering rates over sequential runs
the process changed over successive runs, however, these values were not recorded. Future processing with reactive sputters should record these values to give one indication of process changes. If a target becomes more insulating, the voltage will rise, indicating a greater target resistance. Additionally, switching to an RF sputtering system could also be preferable over using a DC plasma sputter when attempting to deposit an insulating oxide.

4.6 Conclusions

The fabrication of platinum-titanium oxide memristors successfully demonstrated resistive switching in a large number of devices. Fast, sequential reads to a single device caused the observed resistance to increase. The interaction of device size on the current levels required to reset to the high-resistance states was noted. The duration of the pulse used to erase a device was also suggested as an important factor. It was observed that this was very much the case for device set operation, which could be done for most devices with a single voltage pulse of long duration. Through TEM and EELS analysis, significant issues with the stability of the reactive sputter deposition method were discovered.
Chapter 5

“Lightning-Rod” Crossbars

The creation of a conductive filament through a material is somewhat analogous to a lightning strike; electric potentials induce a change in a material, creating a conductive pathway. As is well-known, lightning tends to strike areas which are higher in elevation, as this decreases the amount of material which must be broken down. By introducing a conductive structure elevated above its surroundings, lightning can be induced to strike in a certain location, causing it to take a safe, defined pathway.

By altering the geometry of an electrode in a crossbar, it may be possible to create one shorter pathway through the material which is confined to a small location. This could cause filament formation to be restricted to a smaller area, making devices more uniform and better-behaved, as well as reducing set voltages.

5.1 Fabrication

To create an electrode with a structure that can create high fields in a small location, several approaches are available. Two investigations on this topic have used lateral memristor devices, patterning electrodes using lithography in a top-down manner [24],[25]. However,
lateral implementations of RRAM generally display worse characteristics than in vertical devices, as the devices have a much larger gap between electrodes. A simple method to create a number of sites with vertical topography is to distribute nanoparticles across an electrode. However, due to the random distribution of nanoparticles across a surface, this process cannot be controlled exactly.

In order to create uniform, vertically-integrated memristors with shaped electrodes, a different approach must be used. Dry etching techniques are one method which can be used to create shaped features in a material. In this case, an etch is started to remove the desired material.

Dry etching is a technique which uses gas-based chemistries to chemically remove a material. In a chamber which is pumped down to a rough vacuum, a gas, often a fluorocarbon, is introduced into the ambient. A plasma is struck in the system, usually with 13.56 MHz RF power. This has several effects: some atoms and molecules are ionized, but more often molecules disassociate into their components, creating free radicals. These radicals are electrically neutral, but extremely reactive. As they disperse through the system, they can adsorb onto the material being etched and react, forming a new volatile compound which desorbs and can be pumped out of the system. In this manner, the material is etched in a plasma, hence the name “dry” etch [17]. The process of a silicon dry etch is illustrated in figure 5.1.
Dry etches with low-density plasmas are isotropic, as free radicals are not influenced by electric fields. This means that the sidewalls of a valley-like structure will be etched roughly as much as the bottom. This is an advantage in the creation of pointed shapes to create localized fields.

To create an elevated structure, a photoresist layer is deposited over the desired area. A dry etch which removes the silicon substrate is carried out, but additional oxygen is added into the etching gas. As an organic compound, photoresist is readily etched by oxygen radicals. As a result, the photoresist will shrink laterally as the oxygen attacks it, exposing more area to the silicon etch. When the etch finishes, a vertically-shaped structure remains. Figure 5.2 etch illustrates this technique.
By depositing electrode materials over this structure, the first layer of the memristor is created. A conformal deposition is desired in this case to transfer the geometry created in the silicon substrate to the conductive electrode material. Next, deposition of the memristive oxide of choice must be carried out. However, on this layer a conformal deposition of material is not desired; the top of the memristive material will ideally be flat, creating a small active area which conductive pathways will favor. Lastly, the top electrode is shaped and patterned to create the crossbar.

5.2 Experimental Shaped Silicon Etch

Two different etch systems were used in an attempt to create shaped silicon features: a LAM 490 plasma etch tool and a Drytek Quad reactive ion etch tool. Tables 5.1 and 5.2 show the etch conditions used in the tool to attempt this process. The recipe for the LAM 490 was created by modifying an existing silicon etch, and the recipe from the Drytek was a
pre-existing etch designed to create shaped structures.

<table>
<thead>
<tr>
<th>SF$_6$ Flow (sccm)</th>
<th>O$_2$ Flow (sccm)</th>
<th>Pressure (mT)</th>
<th>Gap Height (cm)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>40</td>
<td>325</td>
<td>0.90</td>
<td>140</td>
</tr>
</tbody>
</table>

Table 5.1: Conditions used in the LAM 490 for a shaped silicon etch

<table>
<thead>
<tr>
<th>SF$_6$ Flow (sccm)</th>
<th>O$_2$ Flow (sccm)</th>
<th>Pressure (mT)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>50</td>
<td>150</td>
<td>200</td>
</tr>
</tbody>
</table>

Table 5.2: Conditions used in the Drytek Quad for a shaped silicon etch

To establish the etch rates of the two different processes, two samples were patterned with the contact layer from the crossbar photomask. This left photoresist squares over the sections of the devices which would go on to form the active area of the memristors. Each sample was then etched for 60 seconds to establish the etch rate of the photoresist. This etch rate was then used to calculate the amount of time needed to etch through 110% of the photoresist thickness. Etching slightly past the endpoint is not harmful, as once the photoresist is gone the entire surface should be etched at an equal rate. The step at the edge of the die was then measured with profilometry to determine the vertical etch rate of silicon. Tables 5.3 and 5.4 show the measured etch rates for photoresist and silicon.

<table>
<thead>
<tr>
<th>Tool</th>
<th>Initial PR Thickness (nm)</th>
<th>PR Etch Rate (nm/s)</th>
<th>Total Etch Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drytek Quad</td>
<td>938.5</td>
<td>7.61</td>
<td>130</td>
</tr>
<tr>
<td>LAM 490</td>
<td>939.2</td>
<td>2.47</td>
<td>397</td>
</tr>
</tbody>
</table>

Table 5.3: Photoresist (PR) etch results for the two processes

<table>
<thead>
<tr>
<th>Tool</th>
<th>Silicon Etch Depth (nm)</th>
<th>Silicon Etch Rate (nm/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drytek Quad</td>
<td>75.2</td>
<td>0.578</td>
</tr>
<tr>
<td>LAM 490</td>
<td>1123.0</td>
<td>2.83</td>
</tr>
</tbody>
</table>

Table 5.4: Silicon etch results for the two processes
In the case of this shaped etch, a process with poor selectivity is desired in order to make the structures short enough that thin films can continuously cover them. For this reason, the etch performed in the Drytek Quad is preferable over the one in the LAM 490 as it is much shorter.

Characterizing these structures can be difficult, as the profilometry tool used did not have the spatial resolution to directly measure the slope of the features created (the radius of curvature on the installed stylus is 10 \( \mu \text{m} \)). Assuming a relatively isotropic photoresist etch, the width of the shaped feature created would be approximately the same as the depth of photoresist etched, on the order of 1 \( \mu \text{m} \). As a result, the structures were too small to measure by profilometry.

Dark field microscopy would be a useful tool to observe these structures, but unfortunately this feature was broken on both optical microscopes available at the time of writing. Instead, the polarizer was used to obtain pictures which had a small degree of edge highlighting, but at the expense of greater image noise.

![Shaped silicon feature created in the Drytek Quad](image1)  
![Shaped silicon feature created in the LAM 490](image2)

Figure 5.3: Micrographs of the shaped silicon structures, filtered by a polarizer
As seen in figure 5.3, the taller structure created in the LAM 490 scatters much more light than the shorter one created in the Drytek Quad, which is only visible with the aid of image processing.

A metal layer was deposited on top of these structures and an attempt was made to deposit the titanium oxide memristive film. However, due to the difficulties in reactive sputtering, discussed in section 4.5, deposition rates were essentially zero and no material was deposited, making the structures electrical shorts. Future work using a more reliable memristive film deposition techniques and shaped electrodes could possibly create devices with improved characteristics.

5.3 Conclusions

It was demonstrated that by using a dry silicon etch with poor selectivity, structures with inclined sides could be created. Using this method, future memristors could have smaller effective areas and display improved characteristics.
Chapter 6

Conclusions and Future Work

The memristor is an extremely promising device with multiple potential applications. To begin the exploration of this device at RIT, the creation of memristors using a self-aligned process was investigated. Titanium oxide was chosen to be used as the memristive oxide, with aluminum electrodes. Fabrication was successful, but issues were encountered and the resulting devices only showed an on/off ratio of 15.6 at 5 V. Additionally, high voltages were needed to observe any change in resistance.

A new process using conventional patterning methods was designed to create memristors with better characteristics. A pilot run of this process using aluminum electrodes and a titanium oxide film displayed improved characteristics: an on/off ratio of $1.46 \cdot 10^4$ at 1 V, requiring 3 V to switch resistance. Devices which used platinum electrodes were then created, showing the best on/off ratio of $4.25 \cdot 10^5$ at 1 V, and also requiring 3 V to switch resistance. However, STEM analysis revealed that the titanium oxide film used in these devices was much thinner than anticipated.

Future work on memristors at RIT should concentrate on developing good deposition methods for memristive oxide films, either by reactive sputtering or another method such as e-beam evaporation. Shaped electrodes offer one potential path to improving device
uniformity, and the dry etch recipe demonstrated could be used to create shaped features in new devices. The inclusion of a thin insulating layer to make device resistances more uniform has also been shown to have beneficial effects [11], and this could be investigated in future devices as well.
Appendix A

Processing Steps

A.1 Preparation

The wafers must first be cleaned and prepared for lithography.

1. Standard RCA Chemical Clean - MOS Clean Bench

2. 5 k Å Oxidation - Bruce Tube #1, Recipe #350 (if a good insulating layer is not already present).

3. Zero mark lithography - ASML Stepper, job WilkieXBAR, ZERO level

4. Zero mark etch - 5.2:1 Buffered Oxide Etch, etch until backside pulls dry.

5. Remove resist - Wet solvent strip or ashing.

A.2 Shaped Etch

If shaped bottom electrodes are desired, the silicon is etched to provide a template for the metal.
1. Coat photoresist - Standard coating on SSI track.

2. Pattern photoresist - ASML Stepper, job WilkieXBAR, CONTACT_N level.

3. Develop photoresist - Standard develop on SSI track.

4. Etch silicon/photoresist - Drytek Quad. See section 5.2 for recipe used in the Drytek Quad. Etch 110% of resist thickness.

A.3 Bottom Electrode

Next, the bottom electrode is deposited and patterned. If platinum or another heavy metal is being used as an electrode, all further wet chemical processing must be done in metal-contaminated dishes and approved tools. If using the lift-off process:

1. Coat photoresist - If using thin metals, OiR 620 on the SSI track suffices.

2. Pattern photoresist - ASML Stepper, job WilkieXBAR, BOTTOM_N level.

3. Develop photoresist - Standard develop for the resist being used.


5. Lift-off - Ultrasonic wet bench, sonicate in acetone until patterns are clear.

Alternatively, if a chemical etch is being used to pattern the metal:

1. Deposit metal - Any PVD method

2. Coat photoresist - Standard coating on SSI track.

4. Develop photoresist - Standard develop for the resist being used.

5. Chemical etch - Appropriate etch station and chemistry.

6. Remove resist - Wet solvent strip or ashing.

A.4 ILD and Contacts

If desired, deposit and contact the interlayer dielectric to prevent shorts. Selective etch between ILD and top/bottom electrode metal is needed.

1. Deposit ILD - Any PVD/CVD method

2. Coat photoresist - Standard coating on SSI track.

3. Pattern photoresist - ASML Stepper, job WilkieXBAR, CONTACTS_P level.

4. Develop photoresist - Standard develop for the resist being used.

5. Wet/Dry etch - Appropriate etch to remove ILD but not underlying metal. Dry etch ok for aluminum electrodes, HF ok for platinum if contaminated etch is available.

6. Remove resist - Acetone/IPA in contaminated dishes if heavy metals being used.

A.5 Top Electrode

The top electrode is then deposited and patterned, along with the memristive film. Chemical etch cannot be used for the top electrode/memristive film unless it is selective against the bottom electrode.

1. Coat photoresist - If using thin metals, OiR 620 on the SSI track suffices.

2. Pattern photoresist - ASML Stepper, job WilkieXBAR, TOP_N level.
3. Develop photoresist - Standard develop for the resist being used.


5. Deposit metal - Any PVD method: CHA e-beam evaporator for platinum, CHA flash evaporator for aluminum.

6. Lift-off - Ultrasonic wet bench, sonicate in acetone until patterns are clear.

A.6 Pad Clearout

If the interlayer dielectric was deposited, it needs to be etched off of the bottom bond pads.

1. Coat photoresist - Standard coating on SSI track.

2. Pattern photoresist - ASML Stepper, job WilkieXBAR, CLEAROUT_P level.

3. Develop photoresist - Standard develop for the resist being used.

4. Wet/Dry etch - Appropriate etch to remove ILD but not underlying metal. Dry etch ok for aluminum electrodes, HF ok for platinum if contaminated etch is available.

5. Remove resist - Wet solvent strip or ashing.
References


