A Charge Pump Architecture with High Power-Efficiency and Low Output Ripple Noise in 0.5 μm CMOS Process Technology

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A Charge Pump Architecture with High Power-Efficiency and Low Output Ripple Noise in 

0.5 µm CMOS Process Technology

by

Primit Modi

A Thesis Submitted in Partial Fulfillment of the 

Requirements for the Degree of 

Master of Science 

in 

Electrical and Microelectronics Engineering

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Modern integrated microsystems have several functional blocks which require different voltages to operate adequately. Charge pump circuits are used to generate different voltage domains for different functional blocks on large integrated microsystems. Charge pump is an inductorless DC-DC converter which generates higher positive voltage or lower negative voltage from the applied reference voltage. The thesis presents a high power-efficiency charge pump architecture with low output ripple noise in AMI 0.5 µm CMOS process technology. The switching action of the proposed charge pump architecture is controlled by a dual phase non-overlapping clock system. In order to achieve high power-efficiency, the power losses due to the leakage currents, the finite switch resistance and the imperfect charge transfer between the capacitors are taken into consideration and are minimized by proper switching of the charge transfer switches. The proposed charge pump can operate over the wide input voltage range varying from 3 V to 7 V with the power conversion efficiency of 90%. The loading current drive capability of the proposed charge pump ranges from 0 to 45 mA.
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Introduction

1.1 Background and Motivation

Portable consumer electronic devices have become inseparable parts of people’s lives in recent times. The demand for portable, thin, lightweight and multifunctional consumer electronic devices (i.e., mobile phones, laptops) is growing day-to-day. Portable devices are powered from single battery and they should be able to operate for an extended period of time. These devices typically have a large number of circuit sub-systems which require different voltage domains to operate. Therefore, the requirement for multiple voltage generation from a single voltage battery-operated power supply imposes design challenges to achieve high power-efficiency, low output ripple voltage and low leakage power.

Charge pumps are inductorless DC-DC power converters which step up or step down the voltage level of the input power supply to generate secondary constant voltages. They use charge transfer switches and capacitors to deliver the charge packets to the loading circuit. Charge pumps use switches and capacitors only so they can be easily implemented with conventional integrated circuit technology.

Charge-pump-based architectures are generally designed fully on-chip or partially on-chip depending upon their applications to support portability. If the charge pump is used to drive a light load current, capacitors used in the architecture have low values and are integrated on-chip. On the other hand, external ceramic capacitors may be used to handle heavy load currents in the charge-
pump-based DC-DC converter architecture. Charge pumps are mostly employed in CMOS-based microsystems (i.e., flash memory, display driver, RS-232 transceivers) as they are cost-efficient, portable and do not emit significant EM radiation.

One idea behind using charge pumps in large microsystems is to generate several voltage supply levels according to requirements from different functional blocks. The most crucial challenge is to achieve high power-efficiency for the wide range of output load currents. Charge pump circuits with low power efficiency restrict the power conversion benefit of the chip and the power loss results in the dissipation of heat.

The output ripple voltage is another important design parameter. The variation in the output voltage at the operating clock frequency should be minimized if a charge pump circuit is used to drive supply-sensitive analog circuits like a bandgap reference or high-speed circuits. Moreover, large output ripple voltage has a negative effect on the circuits powered by the charge pumps.

The startup/rise time of a charge pump circuit is another significant parameter. Slow startup time limits the performance of other functional blocks and delays startup of the portable device. On the other hand, fast startup time reduces the power consumption during startup and enhances the power conversion efficiency.

A high-performance charge pump should be able to generate a wide range of output voltages and be able to drive heavy load currents and light load currents with adaptable high power efficiency. In automotive and telecommunication applications, the operating line voltage supply
range varies from 10 V to 55 V. It is not feasible to design a new charge pump every time when
the operating voltage changes according to the requirements from the customers. Moreover, the
customers also prefer a high performance all-in-one charge pump to avoid the high manufacturing
cost. Most of the charge pump circuits that are commercially available are optimized at one
operating point while they typically give poor performance at another operating point. This
concept can be proved by analyzing the plots of the power conversion efficiency versus the load
current for two commercially available charge pumps shown in Fig. 1-1. It is quite noticeable that
the power conversion efficiency varies by 20-25% over the input voltage range in both the cases.
Linear Technology’s LTC3200® charge pump is optimized to provide approximately 90% power
efficiency for the load current higher than 10 mA and it is noticeable in Fig. 1-1(a) [1]. Maxim’s
MAX679® charge pump is designed to provide 80% to 90% power conversion efficiency for the
load current less than 10 mA. In modern CMOS processes, smaller device dimensions have
reduced the breakdown voltages and increased the oxide leakage current. This has restricted the
maximum voltage that can be handled on the chip. The switching power loss also dominates at
high input voltage.
Figure 1-1. The plot of the power conversion efficiency versus the output load current for (a) LTC3200 IC (adapted from [1]) and (b) MAX679 IC (adapted from [2]).
1.2 Research Objectives

The research work presented in this document focuses on the implementation, design and mathematical analysis of the proposed charge pump architecture. The charge-pump-based DC-DC converter is designed in the AMI 0.5 µm n-well CMOS process. The purpose of this work is to explore an innovative approach to design a new charge pump architecture which can provide high power efficiency and low output ripple noise.

Objectives of this research work include:

- Develop a new charge pump architecture which has high power efficiency and low output ripple voltage over a wide range of input voltage and load current.
- Derive mathematical model for the proposed charge pump and use the model to predict the performance of the proposed charge pump.
- Design the proposed charge pump architecture in the AMI 0.5 µm n-well CMOS process and simulate extensively to prove the concept.

1.3 Thesis Organization

This thesis is comprised of six chapters:

Chapter 1 provides the scope and motivation for this research work.
Chapter 2 reviews the inductor-based and charge-pump-based DC-DC converters. It also compares the output noise, cost and portability between them. Also, the existing topologies of the charge-pump-based converters are briefly summarized. The most commonly used regulation schemes for the charge pump circuits are categorized and described to give better insight.

Chapter 3 proposes a new architecture for the charge pump and its design specifications for battery-powered applications. Also, the transient operation of the proposed charge pump is explained in detail along with the auxiliary circuits which are used to drive the charge pump architecture. They are also beneficial in reducing unwanted power loss.

Chapter 4 provides a mathematical analysis of the charge pump architecture and derives the output voltage equation and the transfer function for the same. Different power losses are taken into consideration and mathematically derived to analyze their effect on power conversion efficiency, output voltage regulation, and output ripple noise.

Chapter 5 discusses the simulation data over fifteen temperature and process corners. Moreover, the effect of different input parameters on power conversion efficiency, output voltage and output ripple voltage is analyzed to prove the concept.

Chapter 6 concludes the current research work and also elaborates on future enhancements that can be made for the proposed charge pump circuit. It also discusses the buck converter topology using the same concept proposed in the current research work.
References


Overview of Existing DC-DC Converter Circuits

2.1 DC-DC Converter Topologies

2.1.1. Inductor-based DC-DC converter

The conventional inductor-based DC-DC converter architecture has dominated moderate and high-power integrated circuit applications. The typical configuration of an inductor-based DC-DC converter architecture is shown in Fig. 2-1(a). It generally uses an inductor, a switch, a diode and a load capacitor which is used to store the energy required to be delivered to the load [1]. Different topologies of DC-DC converter (i.e., buck converter, boost converter, inverting converter) can be derived by placing the inductor in different ways in the circuit. One such topology of an inductor-based boost converter is shown in Fig. 2-1(b).
The inductor-based boost DC-DC converter, shown in Fig. 2-1(b), has two operating phases which are the charge phase and discharge phase. During the charge phase, the switch is open, the inductor current flows through the diode and charges the load capacitor. The load capacitor is charged to the value equal to input voltage. When the switch closes during the discharge phase, the diode is reverse-biased and the energy to the load is provided by the load capacitor. The timing diagram of the inductor-based boost DC-DC converter is depicted in Fig. 2-1(c).
2.1.2. Switched-Capacitor (SC) based DC-DC converter

The switched-capacitor (SC)-based DC-DC converter is another widely-used alternative to the inductor-based DC-DC converter in the medium power and low power handling applications. As its name suggests, it uses switches and capacitors and is also called a charge pump. The switches used in charge pump circuits fulfill the purpose of energy transfer from one stage to another. Unlike the inductor-based DC-DC converter, charge pump architectures use capacitors for energy transfer. These charge pump capacitors are known as flying or reservoir capacitors. Depending upon the power handling requirement, the charge pump architectures are integrated fully on-chip or partially on-chip since the sizes of capacitors are determined by the loading requirement.

Like the inverter-based DC-DC converter, various voltage converter topologies (i.e., voltage doubler, tripler, step-down, negative converter) can result in SC-based architectures for different orientations of the flying capacitors and switches. In Fig. 2-2, the architecture of a basic voltage doubler is depicted where $V_{in}$ is the input supply voltage, $V_{out+}$ is the stepped-up output voltage, $C_f$ is the flying capacitor and $C_L$ is the load capacitor. The charge transfer action of the voltage doubler shown in Fig. 2-2 is controlled by a dual-phase clock system.

![Figure 2-2. Architecture of a basic voltage doubler.](Image)
The most commonly used charge pump circuit, known as the Dickson charge pump and its timing diagram are shown in Fig. 2-3(a) and (b), respectively. Assuming the charge on the flying capacitors \( C_1, C_2, \) and \( C_3 \) is zero during the start-up condition, diode \( D_1 \) is forward-biased when ‘clk’ signal is low and ‘clk_bar’ signal is high. The flying capacitor \( C_1 \) charges to \( VDD \) voltage. When ‘clk’ signal is high and ‘clk_bar’ is low, the voltage at the anode terminal of \( D_2 \) diode becomes \( 2*VDD \) and \( D_2 \) is forward-biased. The charge stored in \( C_1 \) capacitor is shared with \( C_2 \) capacitor and the voltage across \( C_2 \) capacitor becomes \( 0.5*VDD \). When ‘clk_bar’ signal goes high in the next half cycle, diode \( D_3 \) is forward biased and \( D_2 \) is reverse-biased. The voltage across \( C_2 \) is shared with \( C_3 \) capacitor. The voltage across \( C_3 \) capacitor after charge sharing is \( 0.25*VDD \). In the next half cycle, ‘clk’ signal goes high and diode \( D_4 \) is forward-biased and \( D_3 \) is reverse-biased. The output voltage \( V_O \) with respect to ground is \( 1.25*VDD \). Eventually, the output voltage \( V_O \) becomes \( 2*VDD \) due to the sequential charge sharing action between the flying capacitors.
Selection between the architectures of a DC-DC converter is often debatable and is made based on the power requirement of an application. The knowledge of the advantages and disadvantages of both the architectures is also important for selection. The inductor-based DC-DC converter architecture is less area-efficient compared to the charge-pump-based DC-DC converter. The former uses a bulky inductor which is 5-10 times larger than the flying ceramic capacitors used in the charge pump architecture. Even though the switching rate in modern systems has increased and the size of inductor used in DC-DC converter has been reduced, the integration of an inductor on the chip is still difficult compared to a capacitor. Moreover, the cost of an inductor is also 5 to 10 times higher than a flying capacitor used in the charge pump. If an analog designer chooses to use a low quality inductor to reduce cost, the power conversion efficiency of an inductor-based DC-DC converter degrades due to power dissipation.

Figure 2-3. (a) Dickson charge pump architecture and (b) its timing diagram.
The charge pump architecture is also an alternative to the inductor-based DC-DC converter in high power density applications due to the use of off-chip capacitors in the former [1]. Generally, an inductor-based converter uses only one switch in a single stage of conversion. The charge pump architecture has more than one switch depending upon its structure. Therefore, the path from input to output is more resistive in the charge pump architectures. When the load current requirement is higher, the conduction loss in the switches also increases. Due to power loss, the output voltage degrades and power conversion efficiency also decreases. However, the research in advanced process technology has made MOSFET switches available which exhibit less resistance per unit chip area.

Another important metric for comparison between both types of DC-DC converters is the output noise. There are a number of noise sources inherent in switch-mode power supplies. The intrinsic noise generated by the DC-DC converter itself is dominant compared to noise generated by external sources. The switching behaviors of the inductor-based voltage converter and charge pump are very different. Their energy storage elements are also different. According to [3], inductor-based and charge pump DC-DC converters generate noise at their switching frequency and around its harmonics. Moreover, in an inductor-based DC-DC converter, additional output noise is evident around its LC resonant frequency. The noise profiles of both types of voltage converter are shown in Fig 2-4.
In modern DC-DC converters, the switching frequency can be quite high and in the range varying from KHz to several MHz [4]. In inductor-based DC-DC converters, the inductor acts as an antenna and emits electromagnetic signals at such high switching frequency. Other circuit parts on the board may fail due to the Electro-Magnetic Interference, which is a big issue. Use of a shielded inductor to avoid EMI only increases cost and area of the system. Thus, the use of inductor-based DC-DC converters is avoided in the high switching frequency (RF) application.

Finally, the comparative analysis of the switched-capacitor DC-DC converter and the inductor-based DC-DC converter shows that the former architecture is smaller in size and lower in cost and generates less noise compared to the latter. The power conversion efficiency of the charge pump architecture is on par with the inductor-based architecture.
(A) Topologies of Switched-Capacitor Based DC-DC Converter / Charge Pump

Charge pump circuits are often used as voltage doublers to fulfill the purpose of generating higher bias voltages. As mentioned earlier, the flying capacitors are core elements used for voltage conversion. The transfer of charge into and out of the flying capacitors is performed by MOSFET switches at frequencies between KHz to tens of MHz, typically. Fig. 2-5 depicts four different boost type charge pump architectures which are basic cascaded voltage doubler, ladder, Fibonacci and multi-phase voltage doubler. Each of them has different orientation of the charge transfer switches and capacitors and different charge transfer sequence. Their advantages and disadvantages are explained in [5] and [6]. Each architecture has a voltage doubler as a basic cell shown in Fig. 2-2 and the switches are turned on and off by two non-overlapping clocks having 50% duty cycle. The selection of charge pump topology is based on their respective characteristics.

(a)
Figure 2-5. (a) Dual phase cascaded voltage doubler (adapted from [6] and [7]) (b) Ladder charge pump architecture (adapted from [5]) (c) Fibonacci charge pump architecture (adapted from [6]) and (d) Multiphase cascaded charge pump architecture (adapted from [6] and [7]).
(1) Dual Phase Voltage Doubler: The orientation of the transfer switches and capacitors in the dual phase cascaded voltage doubler is shown in Fig. 2-5(a). $V_{in}$ is the input DC power supply and $V_{out+}$ is the stepped up output voltage. As its name suggests, the charge transfer action in the voltage doubler is controlled by two non-overlapping clocks. The ideal voltage gain for the dual phase voltage doubler with $N$ stages is $A = 2^N$ [7]. In order to perform switching action, an $N$-stage dual phase voltage doubler involves $4^N$ charge transfer switches. As the charge pump architecture is designed fully on-chip or partially on-chip with external capacitors, the available silicon area and the number of pins are critical constraints for an analog designer. For the dual phase voltage doubler with $N$ stages, the optimal performance can be achieved by using $2^N$ capacitors with equal capacitance value [7].

(2) Ladder Charge Pump Architecture: The organization of the charge transfer switches, the flying capacitors, and the load capacitor for the ladder charge pump architecture are shown in Fig. 2-5(b). Its switching action is also controlled by dual phase non-overlapping clocks. Ideally, the ladder charge pump architecture with $N$ stages has gain $A = 2^N$. An $N$-stage ladder charge pump requires $4^N$ charge transfer switches. To optimize the performance, $2^N$ capacitors with equal capacitance value are required for the ladder charge pump architecture with $N$ stages.

(3) Fibonacci Charge Pump Architecture: During his study of the switched-capacitor voltage multipliers, Makowski developed a new orientation of the switch-capacitor charge pump which has voltage gain related to the Fibonacci numbers and is shown in Fig. 2-5(c) [7]. An $N$-stage Fibonacci charge pump architecture has $3^N+1$ charge transfer switches and has gain equal to $(N+3)^{th}$ number of the Fibonacci sequence (i.e. An 5-stage Fibonacci charge pump architecture has
voltage gain equal to 13). Thus, the voltage gain of an N-stage Fibonacci charge pump is higher or equal to that of an N-stage cascaded voltage doubler.

(4) Multiphase Charge Pump Architecture: A modern orientation of the multiphase charge pump architecture is shown in Fig. 2-5(d). An N-stage multiphase charge pump architecture can provide $2^N$ voltage gain with $4*N$ charge transfer switches and $(2*N+1)$ capacitors of equal value. However, it requires $2*N$ clock signals which can be easily generated by a frequency division scheme [7].

(B) Unregulated Charge Pump and Regulated Charge Pump

In portable device applications like mobile phones, the system power supply voltage should be stable and should not be affected by discharging the battery input voltage. In the unregulated charge pump, the output voltage follows input voltage and is always a multiple of input. Such behavior of the output voltage is not desirable in mobile phone devices. To maintain the output voltage at a stable value, several regulation schemes have been implemented. The most commonly used regulation methods involve current regulation, voltage regulation, and frequency regulation.

(1) Current Mode Regulation: A basic switched-capacitor charge pump, shown in Fig. 2-6 employs the current mode regulation scheme in which the current flowing through either single MOS switch or multiple switches is controlled by a feedback voltage. Thus, the regulated MOS switch acts as a current source [8]. If the output voltage goes below a certain voltage level, the difference between the feedback/output voltage and the reference voltage is amplified by an error amplifier. The output of the error amplifier regulates the MOS switch to increase the current
through it. Due to the rise in the current flowing through the switch, the flying capacitor ($C_{fly}$) charges quickly and the output voltage returns to its stable level. The regulated MOS switch can be either in the charging path or in the discharging path. The duty cycle of both the charging and discharging phase should be set to 50% [8], [9].

![Charge pump architecture with current mode regulation method](adapted from [8]).

Figure 2-6. Charge pump architecture with current mode regulation method (adapted from [8]).

(2) Voltage Mode Regulation: In this regulation method, the on-switch resistance of single or multiple MOS switches is controlled by a feedback voltage as shown in Fig. 2-7. The regulation of on-switch resistance of the switch also controls the voltage drop across it [9], [10]. If the load
current is high or the input battery voltage goes low, the output voltage decreases and it is compared against a stable reference voltage by an error amplifier. An error signal generated by the error amplifier reduces the on-switch resistance and the voltage drop across the regulated switch also goes down. If the battery voltage increases or the load current goes low, the output voltage of the charge pump architecture increases. In this case, the error signal amplified by the error amplifier increases the on-switch resistance and the voltage drop across the controlled MOS switch also increases. The voltage mode regulation scheme can be employed in either the charging or discharging path. Like the current mode regulation scheme, the duty cycle of non-overlapping clock signals should be maintained at 50% and their frequency should be fixed.

Figure 2-7. Implementation of voltage mode regulation scheme (adapted from [9]).
(3) Frequency Regulation:

(A) Fixed Frequency Regulation (Pulse Width Modulation Technique):
In the fixed frequency regulation scheme, the duty cycle of the clock signal is modulated to regulate the output voltage. The duty cycle modulation of the clock signal depends either on the input voltage or on the load requirement [11]. The block diagram of pulse width modulation control for charge pump architecture is shown in Fig. 2-8. If the input voltage increases or the load current goes low, the output voltage of charge pump increases and it is fed back to an error amplifier. The output of the amplifier is compared against a saw tooth waveform using a comparator. For higher output voltage, the duty cycle of the clock signal becomes narrow and the average power delivered to the load during each clock cycle goes down. In case of low output voltage and high loading requirement, the output voltage decreases which causes an increase in the duty cycle of the clock signal. Thus, the average energy delivered to the load during each clock cycle rises as well as the output voltage [11].
Figure 2-8. Schematic of buck charge pump with pulse width modulation technique (adapted from [11]).

(B) Variable Frequency Regulation:

B.1. Pulse Skip Regulation Method: In the pulse skip control scheme, the output voltage of the charge pump is maintained at the desired value by omitting the unnecessary clock pulses [12]. The regulated charge pump architecture with the pulse skip regulation method and the switching signals are shown in Fig. 2-9. When the output voltage goes lower than the reference voltage, the output load capacitance is charged continuously during each clock cycle. When the output voltage is higher than the reference voltage, some clock pulses are skipped and the charge pump stops providing energy to the load. During the pulse skipping, the average input current is quite low, which is advantageous. However, the output ripple voltage in the pulse skip regulation scheme and
large frequency variation in the clock signal are disadvantages compared to the fixed frequency regulation method.

Figure 2-9. (a) Block diagram of pulse skip regulation method (adapted from [13]) (b) Skipping of the clock signal for high load current requirement (adapted from [12]).
B.2. Linear Skip Regulation Method: The linear skip control method is more complex than the pulse skip regulation method and helps in enhancing the output ripple voltage performance of the charge pump. The linear skip regulation scheme uses three phases of operation, which are wait state, transfer phase, and charge phase [14]. When the load current is high, there is no wait state and the current supplied to the output load is regulated by charge and transfer phases. When the output voltage increases due to either high input voltage or low load current, the wait time increases and the operation of the charge pump stops. During the wait state, the charge delivered to the load is supplied by the load capacitor. Fig. 2-10 depicts the switching clock signals for the linear skip regulation method employed in the switched-capacitor DC-DC converter.

![Diagram](image_url)

Figure 2-10. Clock signals for different loading current requirement in linear skip regulation method (adapted from [14]).
References:


3.1 Design Specifications

The worst-case performance goals of an unregulated switched-capacitor charge pump doubler circuit are established in Table 3-1 which will be beneficial in investigating the proposed charge pump architecture. These specifications are typical for display subsystems in modern portable products such as cell phones and other mobile devices.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification Goal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>3 V – 6 V</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>2X</td>
</tr>
<tr>
<td>Load Current</td>
<td>2 mA – 45 mA</td>
</tr>
<tr>
<td>Power Conversion Efficiency</td>
<td>90%</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>6 V – 12 V</td>
</tr>
<tr>
<td>Output Ripple Voltage</td>
<td>25 mV</td>
</tr>
<tr>
<td>Startup Time</td>
<td>2 ms</td>
</tr>
</tbody>
</table>

Table 3-1. Design specifications for the proposed charge pump architecture.
As mentioned earlier, modern integrated circuit systems manufacturers demand high-efficiency power converters. Most of the discrete charge pump ICs available in the market offer conversion efficiency ranging from 80% to 99%. High power conversion efficiency implies that the ratio of the power delivered to the load to the input power provided to the system by the charge pump architecture should be close to unity. Typical integrated charge pump architectures consume several milliamperes under no-load condition. As a consequence, the charge pump architecture exhibits low power conversion efficiency at light load current. The switched-capacitor charge pump architecture presented in this thesis is designed to drive load currents ranging from 2 mA to 45 mA with efficiencies greater than 90%.

Figure 3-1. Block diagram of the proposed charge pump architecture.
The proposed charge pump architecture, shown in Fig 3-1, is comprised of the charge pump core and auxiliary circuits which include a non-overlapping clock generator, level shifters, and well-switchers or well-managers. These auxiliary circuits are required to optimize the performance of the charge pump core by minimizing the power losses (i.e., conduction loss, reversion loss). The block diagram of the proposed charge pump architecture is depicted in Fig. 3-1.

3.2 Design of Auxiliary Circuits

3.2.1. Well-Switcher Circuit

The proposed step-up charge pump architecture is designed in the 0.5 µm n-well CMOS process technology. During the startup condition, the internal node voltages of the charge pump can swing from ground to any voltage less than $2V_{in}$. The body of the NMOS switch is connected to ground voltage which is the lowest possible voltage in the circuit. The body of the PMOS switch should be connected to the highest voltage in the circuit to avoid the forward biasing of the source-body diode [1]. However, as mentioned earlier, the voltages at source and drain terminals of PMOS switches can modulate between ground and $2V_{in}$. It is not viable to connect the body of PMOS directly either to its source or to its drain. The auxiliary circuit shown in Fig. 3-2 helps in avoiding the forward biasing of the source-body diode.
As depicted in Fig. 3-2, the body of charge transfer PMOS switch PM is connected to the bodies of two auxiliary PMOS switches WP1 and WP2. The bodies of WP1 and WP2 are further connected to their source terminals. The gate terminals of WP1 and WP2 are connected to the source and drain terminals of the charge transfer switch PM, respectively. The source and drain terminals of the PM switch are designated by P1 and P2, respectively. When the voltage at the P2 terminal of the PM switch is lower compared to the voltage at the P1 terminal, the WP1 switch turns on and the WP2 switch turns off. The voltage of the P1 node of the PM switch is directly applied to its body via the WP1 switch. A similar explanation can be given when the P1 voltage of PM is lower than the voltage at P2. Thus, the body (n-well) connection of the charge transfer switch PM is connected either to its source terminal or its drain terminal. Moreover, neither WP1 nor WP2 contribute to the reverse charge transfer or any leakage current. The well-switcher circuit does not consume any considerable amount of current.
3.2.2. Clock Pair Generator Circuit

The choice of clocking frequency has a direct relationship with the size of flying capacitors, the load current, and the output ripple voltage. Depending upon the output ripple voltage and the load current specifications, the clocking frequency should be chosen such that it is higher than the operating frequency of the loading circuit. In the proposed charge pump architecture, the clocking frequency is 10 KHz +/- 20%. If many charge pumps are connected in parallel and each of them is designed to deliver a fraction of the total load current, the sizes of flying capacitors will decrease in each charge pump. In this case, the capacitors can be integrated on-chip. However, an on-chip integrated capacitor has stray capacitance with respect to ground. Eventually, it results in less power conversion efficiency. The model of the on-chip integrated capacitance with the parasitic capacitances and its equivalent circuit model are depicted in Fig. 3-3 (a) and (b), respectively. According to one study, the maximum possible power conversion efficiency of the charge pump was 50% with the on-chip poly-metal capacitor. On the other hand, the same charge pump architecture exhibited 97% efficiency with external ceramic capacitors under certain load conditions [2]. The block diagram of the clock pair generator circuit is shown in Fig 3-4.
Figure 3-3. (a) Graphical description of on-chip poly-poly capacitor along with parasitic capacitance. (b) The equivalent circuit model of the on-chip poly-poly capacitor.

where $C_{\text{poly-poly}}$ is desired on-chip capacitance and $C_A$, $C_B$, $C_C$, and $C_D$ are parasitic capacitances.
The proposed charge pump architecture uses non-overlapping clock phases to turn MOS switches on and off, which prevents the short circuit condition between the high voltage node and the low voltage node. The gate level schematic of the non-overlapping clock signal generator and the clock signals are depicted in Fig. 3-5. The circuit shown in Fig. 3-5(a) operates in ‘break-before-make’ manner [3]. The phase difference between clock signals $\phi_1$ and $\phi_2$ is 180° and their amplitude is $V_{in}$. 

(A) Non-overlapping Clock Generation
Figure 3-5. (a) Transistor Level Schematic of the Non-Overlapping Clock Signal Generator Circuit. (b) Input Clock Signal (top) and Output Clock Signals clk_a (middle) and clk_b (bottom).

The non-overlapping period between both the clock signals can be varied by adding more inverter delays. However, the large non-overlapping period keeps MOS switches in an open state for a long time, which further causes leakage current glitches in input current. One such event of the input current glitch during the non-overlapping period is shown in Fig. 3-6.
Figure 3-6. The input current glitch during the non-overlapping period of $\Phi_1$ and $\Phi_2$.

(B) **Level Shifter**

When the output voltage of the charge pump increases beyond the input voltage, $V_{in}$, the gate drive voltage of PMOS charge transfer switches should be equal to or higher than the output voltage to turn them off properly. The complement is true for the NMOS switches where the gate drive voltage should be equal to or higher than the output voltage to turn them on. Otherwise, the charge transfer switches do not turn on or off properly and it results in short circuit power loss. Thus, the gate voltages of the charge transfer switches are required to be level shifted.
The level shifter used in the proposed charge pump architecture is shown in Fig. 3-8. The conventional level shifter, shown in Fig. 3-7, offers large propagation delay [4]. The propagation delay is caused due to pull-up and pull-down action of PMOS transistors and NMOS transistors, respectively. The simultaneous action of pull-up and pull-down also gives rise to the switching power which creates large current spikes on the supply rails. The simultaneous action of pull-up and pull-down is mitigated in the level shifter used in the charge pump clocking scheme. The quasi-inverters formed by PMOS transistors and stacked NMOS transistors help in pulling up or pulling down the nodes A and B faster to their final values, which further reduces the dynamic power consumption.
Figure 3-8. Contention Mitigated Level Shifter used in the Clocking Scheme of the Proposed Charge Pump.

The clock signal which is level shifted to the $V_{DDH}$ voltage level is shown in Fig. 3-9. $V_{DDH}$ is the voltage fed back from the output of the charge pump and $V_{DDL}$ is the input voltage to the charge pump. $V_{DDH}$ voltage is swept from 0 to $2V_{DDL}$ to analyze the transient response of the level shifter.
3.3 Operation of the Proposed Charge Pump Circuit

The transistor level design of the proposed charge pump DC-DC converter is shown in Fig 3-10. The design contains six PMOS and two NMOS switches for the charge transfer and three capacitors for the charge storage. The switches are turned on and off by two non-overlapping level-shifted clock signals, $\phi_1$ and $\phi_2$, and their level-shifted complimentary signals, $\phi_{1n}$ and $\phi_{2n}$, which are generated by the clock-pair generator circuit. The proposed charge pump voltage converter is composed of two equal switched capacitor circuits which are mirrored across the load.
capacitor as shown in Fig 3-10. The body of PMOS switch is connected to the well-switcher circuit. As the proposed charge pump architecture is designed in 0.5 µm CMOS n-well technology, the well-switcher circuit ensures that the body of PMOS transistor is always connected to the highest voltage during the active state of the charge pump. The body of NMOS switch is always connected to the ground.

The architecture of the proposed charge pump is based on continuous current pumping technique. In general, a charge pump is required to provide the load current, $I_L$, all the time. The input power supply should deliver enough charge during each clock cycle to fulfill the load current requirement. A typical charge pump has two clocking phases: 1) Charge phase – during which the charge is transferred to the load capacitor. 2) Discharge phase – during which the charge pump stops pumping charge. The load current is provided by discharging the load capacitor during the discharge phase. In the proposed architecture, the energy required to be delivered to the load is continuously provided by either the top half or the bottom half of the charge pump to the load capacitor. During a full cycle of the clock signal, there is no explicit discharge phase for the load capacitor. However, the load capacitor discharges a small amount of charge to fulfill the load current requirement during each half cycle which results in the output ripple voltage.
Figure 3-10. Schematic of the Proposed Charge Pump Circuit
Figure 3-11. The timing diagram of the proposed charge pump when it is operating in the steady state condition.

When $\phi_1$ goes low and $\phi_2$ becomes high logic during $N^{th}$ half cycle, their corresponding complimentary signals $\phi_{1n}$ and $\phi_{2n}$ become high and low, respectively. The timing diagram is shown in Fig. 3-11. The top half of the circuit is in charge phase and the bottom half of the circuit is in discharge phase as shown in Fig 3-12. In top half of the charge pump architecture, PM1 and NM1 switches are closed and PM1 switch allows the current to flow. The flying capacitor, $C_{fly1}$, charges to the input voltage, $V_{in}$, ideally. During this half cycle, the transistor switches PM2, PM4, PM5 and NM2 are open. The PMOS switches, PM3 and PM6, are turned on in the bottom half of
the circuit. The charge stored in the flying capacitor, $C_{fly}$, during $(N - 1)^{th}$ half cycle is transferred to the load capacitor, $C_{load}$. In other words, $C_{fly}$ is ideally charged to the input voltage, $V_{in}$, during $(N - 1)^{th}$ half cycle. During $N^{th}$ half cycle, the voltage across the flying capacitor, $C_{fly}$, appears across the load capacitor. The output voltage, $V_{out}$, is given by:

$$V_{out} = V_{in} + V_{load}$$  \hspace{1cm} (3-1)

During the $(N + 1)^{th}$ half cycle, $\phi_1$ goes high and $\phi_2$ goes low. The bottom half of the circuit is in the charge phase and the top half of the circuit is in the discharge phase. The transistor switches PM2, PM4, PM5 and NM2 are closed and the rest of the charge transfer switches are turned off during this half cycle as shown in Fig 3-13. If the voltage drop across MOS switches is
considered to be negligible, the flying capacitor, $C_{fly2}$, is charged to the voltage $V_{in}$. In the top half of the charge pump architecture, $C_{fly1}$ and $C_{load}$ become parallel and the output voltage is given by (3-1).

![Schematic of the proposed charge pump](image)

Figure 3-13. The Schematic of the proposed charge pump when $\phi_1$ goes high and $\phi_2$ goes low.

References:


Analysis of the Proposed Low Noise High-Efficiency Charge Pump

4.1 Mathematical Model of the Proposed Charge Pump Architecture:

Ideally, the voltage conversion efficiency of any single-stage charge-pump-based DC-DC converter is given by:

$$\eta = \frac{V_{out}}{K \cdot V_{in}}$$  \hspace{1cm} (4-1)

where $K$ is the gain multiplier of the single-stage charge pump architecture and it depends upon the topology of charge pump (e.g., for voltage doubler cell, the value of $K$ is 2). Equation (4-1) does not consider conduction losses, switching voltage loss and quiescent voltage loss. The voltage conversion efficiency of the single-stage charge pump is 100% without those voltage losses.

Figure 4-1. Simplified DC model of charge pump (adapted from [1]).

A simplified DC model of DC-DC converter is shown in Fig 4-1. $R_{loss}$ component causes power loss or dissipation in the charge-pump-based DC-DC converter and is comprised of the on-
switch resistance of MOS switches, ESR of capacitors and parasitic resistances [1]. $I_L$ is the load current. From the DC model, the output voltage of the DC-DC converter model can be given by:

$$V_{out} = K \cdot V_{in} - I_L \cdot R_{loss} \quad (4-2)$$

The load current is required to be supplied all the time. The input power should supply enough charge to fulfill the load current requirement during each half cycle. The charge required to be delivered to the load during full clock cycle is given by:

$$Q_{load} = I_L \cdot T \quad (4-3)$$

During each half cycle, the charge supplied by the input power supply can be calculated by:

$$Q_{in} = 2I_L \cdot \frac{T}{2} = Q_{load} \quad (4-4)$$

Thus, twice the load current flows through the flying capacitors, $C_{fly1}$ and $C_{fly2}$ during each half cycle.
Assuming that the charge pump is operating in steady-state condition and not in start-up state, the control signals $\phi_1$ and $\phi_2$ are low and high, respectively, during $N^{th}$ half clock cycle. A simplified RC model of the proposed charge pump during $N^{th}$ half clock cycle is shown in Fig. 4-2. PMOS transistor PM1 and NMOS transistor NM1 are in the ON state in the top half of the circuit and $C_{fly1}$ charges to $V_{c1}$ due to the loop current flowing through the charge transfer
switches. As mentioned earlier, the loop current is twice the load current during half clock cycle. Applying KVL in loop 1 as shown in Fig. 4-2, the voltage $V_{C1}$ can be derived as follows.

\[
V_{DD} = 2I_L R_{ON} + 2I_L R_{ON} + 2I_L R_{ESR} + 4I_L R_{bump} + V_{C1} \quad (4-5)
\]

\[
V_{C1} = V_{DD} - 4I_L R_{ON} - 2I_L R_{ESR} - 4I_L R_{bump} \quad (4-6)
\]

where $R_{ON}$ is the ON switch resistance of MOS charge transfer switch, $R_{ESR}$ is equivalent series resistance of the external ceramic capacitor and $R_{bump}$ accounts for the metal pin resistance and the PCB route resistance. During the same phase, PMOS transistors PM3 and PM6 are also turned on in the bottom half of the circuit. The flying capacitor, $C_{fly2}$, is charged to voltage $V_{C2}$ during $(N - 1)^{th}$ half cycle. The positive output voltage $V_{OUT+}$ can be derived by using KVL for loop 2 shown in Fig. 4-2.

\[
V_{Cload} - V_{C2} + 2I_L R_{ON} + 2I_L R_{ON} + 4I_L R_{ESR} + 2I_L * 4R_{bump} = 0 \quad (4-7)
\]

\[
V_{Cload} = V_{C2} - 4I_L R_{ON} - 4I_L R_{ESR} - 8I_L R_{bump} \quad (4-8)
\]

\[
V_{OUT+} = V_{DD} + V_{Cload} \quad (4-9)
\]

Substituting $V_{Cload}$ from (4-8) into (4-9)
\[ V_{OUT^+} = V_{DD} + V_{C2} - 4I_L R_{ON} - 4I_L R_{ESR} - 8I_L R_{bump} \] (4-10)

The value of \( V_{c2} \) across \( C_{fly2} \) during \( N - 1 \)th half cycle is similar to that of \( V_{c1} \) during \( N \)th half cycle. Therefore, the positive output voltage \( V_{OUT^+} \) can be given by:

\[ V_{OUT^+} = V_{DD} + V_{DD} - 8I_L R_{ON} - 6I_L R_{ESR} - 12I_L R_{bump} \] (4-11)

\[ V_{OUT^+} = 2V_{DD} - 8I_L R_{ON} - 6I_L R_{ESR} - 12I_L R_{bump} \] (4-12)

Figure 4-3. Simplified RC model of the proposed charge pump when \( \phi_1 \) is high and \( \phi_2 \) is low. (\( V_{in} = V_{DD} \)).
During \((N + 1)^{th}\) half cycle, \(\varphi_1\) goes high and \(\varphi_2\) becomes low. PM1 and NM1 transistors turn off first and then PM2 and PM5 transistors turn on to avoid the reversion loss. In the bottom half of the circuit, PM4 and NM4 turn on and the flying capacitor, \(C_{fly}\), is charged to \(V_{C2}\). A simplified model of the proposed charge pump is shown in Fig. 4-3 during \((N + 1)^{th}\) half cycle. The output voltage \(V_{OUT+}\) during \((N + 1)^{th}\) half cycle can be derived in the same way as it is calculated for \(N^{th}\) half cycle. The timing diagram the proposed charge pump is shown in Fig. 4-4.

![Figure 4-4. The timing diagram of the proposed charge pump (a) \(\varphi_1\), (b) \(\varphi_2\), (c) \(V_{in}\), (d) \(V_{C1}\), (e) \(V_{C2}\), and (f) \(V_{OUT+}\) (from top to bottom).](image-url)

Thus, the load current is delivered to the load by input supply during both half cycles...
continuously. There is no discharge phase during the operation of the charge pump. The continuous current pumping technique is beneficial in achieving low ripple output voltage.

### 4.2 Design Considerations:

The definition of the power conversion efficiency given by (4-1) applies to an ideal DC-DC converter system. In reality, there are several power losses in the DC-DC converter which play a significant role in worsening the power efficiency. Taking power losses into account, the power conversion efficiency, $\eta$, is given by [1]:

$$
\eta = \frac{\text{output power}}{\text{input power}} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} \quad (4-13)
$$

where $P_{\text{OUT}}$ and $P_{\text{IN}}$ are output power and input power, respectively. Input power also includes total power loss due to the conduction loss, the charge redistribution loss, the reversion loss and the switching loss. In order to achieve high efficiency, all power losses should be minimized [2]. The charge redistribution loss is due to charge transfer between capacitors. The conduction loss is caused by non-ideal charge transfer due to resistive voltage drop across the transistor switches. The reversion loss takes place due to back transfer of the charge from high voltage to low voltage. The switching power loss is due to gate drives and parasitic capacitors and it is unavoidable to some extent [2].
4.2.1 Conduction Power Loss:

The conduction power loss originates due to the ON resistance of MOSFET switches and the equivalent series resistance (ESR) of the flying capacitors and the load capacitor. In the proposed dual phase charge pump, MOSFET switches are used to connect and disconnect the flying capacitors and the load capacitor with input supply and load [2]. According to (4-12), the ON resistance of the switch plays a significant role in determining the output voltage. In steady-state condition of the charge pump, these charge transfer switches operate in the linear region. The ON switch resistance can be given by [4]:

\[ R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{GS} - V_T} \]  \hspace{1cm} (4-14)

In order to achieve high power efficiency, it is worth mentioning that low ON switch resistance is mandatory. Furthermore, \( R_{ON} \) depends largely upon the aspect ratio of MOSFET switches. By choosing proper aspect ratio for both NMOS and PMOS switches, the ON switch resistances of both NMOS and PMOS switches can be made equal and low.

\[ R_{ONPMOS} = R_{ONNMOS} = R_{ON} \]  \hspace{1cm} (4-15)

Moreover, \( R_{ON} \) also depends upon the threshold voltage of the device. To keep the ON switch resistance low, threshold voltage should be kept low [4]. The threshold voltages of long channel NMOS device is given by:
\[ V_{T_{NMOS}} = V_{TO} + \gamma(\ \frac{V_{SB}}{V} + 2\varphi - \frac{2\varphi}{F}) \] (4-16)

In order to keep threshold voltage low, the body voltage in NMOS should be held at the lowest possible voltage which is the ground signal in the circuit [4]. Similarly, the body terminal in PMOS should be connected to the highest possible voltage. The well-switcher circuit, discussed in Chapter 3, helps in maintaining the body voltage of PMOS switches at the highest voltage in the circuit. Thus, the threshold voltage of the PMOS charge transfer switch decreases and it further reduces the ON switch resistance.

Moreover, the Equivalent Series Resistances (ESR) of the flying capacitors and the load capacitor also contribute to the conduction power loss. The on-chip poly-poly capacitor or metal-insulator-metal capacitor offers high ESR compared to the external ceramic capacitor. ESR contributed by the external ceramic capacitor is in the range of several ohms (2 Ω - 4 Ω). The conduction power loss can be calculated by:

\[ P_{cond} = 8R_{ON}I_L + 6R_{ESR}I_L + 12I_L^2R_{bump} \times I_L \] (4-17)

\[ P_{cond} = \frac{8I_L^2}{\mu C_{ox} \frac{W}{L} V_{GS} - V_T} + 6R_{ESR}I_L^2 + 12I_L^2R_{bump} \] (4-18)

4.2.2 Reversion Loss:

Reversion loss occurs due to shorting of the higher voltage to the lower voltage and the
charge is transferred back to the lower voltage node. Reversion power loss can be optimized by implementing the proper gate control scheme for the charge transfer switches [3].

In the proposed charge pump, the ‘break-before-make’ clocking scheme is used to turn the charge transfer switches on and off. This switching scheme ensures that the higher voltage node should not be connected to the lower voltage node to avoid reverse transfer of the charge at any time.

4.2.3 Charge Redistribution Loss:

The charge redistribution loss results from the non-ideal charge transfer between two parallel capacitors. When two capacitors are connected in parallel, charge sharing between two parallel capacitors takes place. This charge sharing event leaves its signature on the output of the charge pump in the form of voltage ripples. Large ripple voltage is certainly an undesirable quantity for systems like display driver, touch, microcontroller, etc.

![Figure 4-5. Output Response of the Proposed Charge Pump in Steady-State Condition.](image)

Figure 4-5. Output Response of the Proposed Charge Pump in Steady-State Condition.
When $\phi_1$ is high and $\phi_2$ is low, $C_{fly1}$ and $C_{load}$ are connected in parallel. The charge $Q_{load}$ is discharged through $C_{fly1}$ and $C_{load}$ and the output voltage changes from $V_{OA}$ to $V_{OB}$ during $N^{th}$ half period as shown in Fig. 4-5. Applying the rule of charge conservation for the loop,

$$Initial \ Charge \ T_{start} = Final \ Charge \ T_{end}$$ (4-19)

$$C_{fly1} + C_{load} \ V_{OA} = I_L T_N + C_{fly1} + C_{load} \ V_{OB}$$ (4-20)

When $\phi_1$ is low and $\phi_2$ is high during $T_{N+1}$ half cycle, $C_{fly2}$ is placed on the top of $V_{DD}$ and the charge across $C_{fly2}$ is redistributed with the load capacitance. At the start of $T_{N+1}$ (i.e., $(N+1)^{th}$) half cycle, the output voltage increases from $V_{OB}$ to $V_{OA}$. Applying the rule of charge conservation for the corresponding loop,

$$2C_{fly2}V_{DD} + C_{load}V_{OB} = C_{fly2}V_{OA} + C_{load}V_{OA}$$ (4-21)

Considering $C_{fly1}$ is equal to $C_{fly2}$ and solving (4-9) and (4-10) for $V_{OA}$ and $V_{OB}$

$$V_{OA} = 2V_{DD} - \frac{C_{load}I_LT_N}{C_{fly1} \ C_{fly1} + C_{load}}$$ (4-22)

$$V_{OB} = 2V_{DD} - \frac{C_{load}I_LT_N}{C_{fly1} \ C_{fly1} + C_{load}} - \frac{I_LT_N}{C_{fly1} + C_{load}}$$ (4-23)

The ripple voltage in the output of the charge pump is given by:
\[ V_R = V_{OA} - V_{OB} = \frac{I_L T_N}{C_{fly1} + C_{load}} \]  \hspace{1cm} (4-24)

Thus, the output ripple voltage is directly proportional to the load current and inversely proportional to the clocking frequency, the flying capacitor and the load capacitor. By choosing the proper capacitor and clocking frequency, the ripple voltage can be reduced to minimal value.

References


Simulation of the Proposed Charge Pump

This chapter discusses the simulation results of the proposed architecture of the integrated charge pump circuit. The key parameters (i.e., power conversion efficiency, output ripple voltage, rise time) are simulated over 45 process, temperature and voltage corners which are listed in Table 5-1 below:

<table>
<thead>
<tr>
<th>Corner Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>-30°C</td>
</tr>
<tr>
<td></td>
<td>27°C</td>
</tr>
<tr>
<td></td>
<td>80°C</td>
</tr>
<tr>
<td>Process</td>
<td>tt → typical NMOS and typical PMOS</td>
</tr>
<tr>
<td></td>
<td>ss → slow NMOS and slow PMOS</td>
</tr>
<tr>
<td></td>
<td>ff → fast NMOS and fast PMOS</td>
</tr>
<tr>
<td></td>
<td>sf → slow NMOS and fast PMOS</td>
</tr>
<tr>
<td></td>
<td>fs → fast NMOS and slow PMOS</td>
</tr>
<tr>
<td>Voltage</td>
<td>3V, 5V and 7V</td>
</tr>
</tbody>
</table>

Table 5-1. List of process, temperature, and voltage corners used for simulating the proposed charge pump architecture.
The clock frequency is chosen to be 111 KHz to meet the design specifications. The clock frequency for the simulation is calculated via (4-24). However, the effect of the clock frequency on the different design specifications is investigated later in this section. Moreover, the effects of the input range, the duty cycle, the clock frequency and the flying capacitor are also simulated and discussed in the chapter over typical process corner and at the room temperature.

5.1 Transient Analysis Results

5.1.1 Start-up time

The start-up time of the proposed charge pump based DC-DC converter is simulated using the transient analysis and is shown in Fig. 5-1 for the loaded and unloaded conditions, respectively. It is depicted as the output voltage of the charge pump with respect to time. The rise time or the start-up time can be defined as the time required for the output voltage to reach 95 % of its final value. The start-up time of the charge pump circuit is a function of the load capacitance, the output resistance and the flying capacitors. The start-up time is evaluated for the input voltage of 5 V and the load capacitor of 4.7 µF. The clock frequency is set to 110 KHz. In order to simulate the start-up time, the voltages across all the capacitors are set to zero. The charge pump is operated in the loaded and unloaded condition. It can be observed that the start-up time for typical process and temperature is 195 µs. The generic test bench for the measurement of the start-up time, the power efficiency and the output ripple voltage is shown in Fig. 5-2.
Figure 5-1. Transient responses of the proposed charge pump in (a) loaded and (b) unloaded condition.
Figure 5-2. Generic test bench for the measurement of the power efficiency, the output ripple voltage, and the start-up time. The metal pin resistances and PCB route resistances, included in the test bench are considered to be 5 Ω.

Moreover, the start-up time is also analyzed over 45 process and temperature corners for the input supply of 5 V and is shown in Fig. 5-3. The worst case start-up time is 255.3 µs for the “npTv” (i.e., slow N process, slow P process, 80°C and 3 V) corner. Low start-up time results due to the high ON switch resistance of the charge transfer switches.
5.2 Steady-State Analysis Results

The steady-state analysis of a charge pump involves the evaluation of the power conversion efficiency, the output ripple voltage, the input power and the output characteristics. The power conversion efficiency of the proposed charge pump is characterized by:

\[
\eta = \frac{P_{out}}{P_{in}} = \frac{1}{T} \int_T V_{out} \times I_{out} \, dt = \frac{1}{T} \int_T V_{in} \times I_{in} \, dt
\]  

Figure 5-3. Start-up time simulation for the proposed charge pump over 45 temperature and process corners. Input voltage = 3 V, 5 V, and 7 V. Temperature = 30°C, 27°C, and 80°C.
where $P_{\text{out}}$ is the output power, $P_{\text{in}}$ is the input power, $V_{\text{out}}$ is the simulated output voltage, $I_{\text{out}}$ is the simulated load current, $V_{\text{in}}$ is the input voltage, $I_{\text{in}}$ is the input current which accounts for the current consumed by the charge pump and the current consumed by the clock generation circuit and the level shifters. $T$ is the time period over which the average of the output power and the input power is measured when the charge pump is operating in the steady-state condition. The power conversion efficiency is simulated over 45 process and temperature corners with input supply of 5 V and is shown in Fig. 5-4. The worst case power efficiency is 90.55% at npTv (slow process, high temperature = 80º C) corner as the slow NMOS and PMOS processes offer the worst case ON switch resistance.

![Residual Plot - power eff](image)

Figure 5-4. The power conversion efficiency of the proposed charge pump over corners. Input voltage = 3 V, 5 V, and 7 V. Temperature = -30ºC, 27ºC, and 80ºC.
Furthermore, the effects of the light loading and the heavy loading on the power conversion efficiency are also analyzed and the dependence of the power efficiency on the load current is depicted in Fig. 5-5. It can be observed that the power efficiency is low at light loading since the charge pump circuit consumes 2.1 mA input current at input supply of 5 V in the unloaded condition. Therefore, the output power is quite low compared to the input power when the charge pump is lightly loaded and it leads to low power efficiency. Moreover, high load current also degrades the power efficiency due to the increase in the conduction power loss according to (4-18). The flying capacitors and the load capacitor are not large enough to store and to deliver the charge required to sustain high load current. It further causes decrease in the output voltage and the output power. Thus, the power conversion efficiency diminishes at the high load current.

![Power Efficiency vs. Output Load Current](image)

Figure 5-5. The power conversion efficiency versus the output load current.
The output ripple voltage can be defined as the difference between maximum output voltage and minimum output voltage when the charge pump is operating in the steady-state condition for a given load condition. The output ripple voltage is depicted in Fig. 5-6 which is an enlarged version of Fig. 5-1. Moreover, the effect of the load current on the output ripple voltage is also examined and shown in Fig. 5-7(a). It can be noticed in Fig. 5-7(a) that the increase in the load current increases the output ripple voltage. In Fig. 5-7(b), the power conversion efficiency and the output ripple voltage are plotted with respect to the output load current to ascertain good operating range of the designed charge pump.

![Graph showing output ripple voltage](image)

Figure 5-6. The output ripple voltage of the proposed charge pump when it is operating in the steady-state condition with $R_{load} = 200 \, \Omega$. 
Figure 5-7. (a) The output ripple voltage versus the load current plot. (b) The effect of the load current on the power efficiency and the output ripple voltage to determine good operating range for the proposed charge pump.
The output impedance of a charge pump circuit can be defined as the change in the output voltage for the given change in the output load current.

\[ R_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \] (5-2)

Increase in the output load current gives rise to the conduction power loss according to (4-18) and it affects the output voltage level according to (4-2). The test bench for the measurement of the output resistance is shown in Fig. 5-8. The output voltage of the proposed charge pump circuit decreases with the increment in the output load current which can be observed in Fig. 5-9.

Figure 5-8. The test bench for the measurement of the output impedance of the proposed charge pump circuit.
5.2.1 Effect of the Duty Cycle of the Control Signals:

The proposed charge pump is designed to be controlled by $\phi_1$ and $\phi_2$ clock signals which have 50% duty cycle. Changing the duty cycle of these clock signal / control signals affects the charge delivered to the load. In Fig. 5-10, it can be observed that the power efficiency of the proposed charge pump is low when ON duty cycle is low. When the duty cycle is low, the non-overlapping period between $\phi_1$ and $\phi_2$ is high which causes the charge pump circuit to stay in the idle (non-operating) mode for a long time. The charge stored in the flying capacitors leaks during this non-operating mode which further causes decline in the power conversion efficiency.
When the duty cycle of the clock signals $\phi_1$ and $\phi_2$ is higher (more than 55%), $\phi_1$ and $\phi_2$ have overlapping period which results in the shorting of the high voltage node to the low voltage node. The reversion power loss increases with the increase in the duty cycle of $\phi_1$ and $\phi_2$. Thus, the power conversion efficiency declines due to high reversion power loss at large ON duty cycle which is shown in Fig. 5-10.

In similar way, the effect of ON duty cycle of the clock signals on the output voltage and the output ripple voltage is also simulated and is shown in Fig. 5-11 and 5-12, respectively. It can
be concluded that the proposed charge pump gives good performance when the duty cycle of the clock signals is set marginally below 50%. It results in a minuscule non-overlapping period which avoids the reversion loss. As mentioned earlier, if the duty cycle of the clock signal is much less than 50%, there is a large non-overlapping period between two clock signals. The charge pump stops pumping charge and the flying capacitors and the load capacitor start to leak the stored charge. If the duty cycle of the clock signal is higher than 50%, the ON periods of two clock signals will overlap each other. It causes the shorting of the output node (i.e., higher voltage node) and the input node. The charge in the output load capacitor is shared with the low voltage node and reversion loss occurs. This undesired event causes large ripple on the output voltage. The output ripple voltage for the duty cycle higher than 50% is shown in Fig. 5-12.

![Output Voltage vs. Duty Cycle](image)

**Output Voltage vs. Duty Cycle**

Input Voltage = 5 V; Load Capacitor = 4.7 µF; Flying Capacitors = 1 µF; Load Resistance = 200 Ω

Figure 5-11. The effect of the duty cycle of the clock signals on the output voltage.
5.2.2 Effect of the Clock Frequency:

Choosing proper clock frequency is an utmost requirement for better performance of the charge pump circuit. The clock frequency has direct effect on the power conversion efficiency, the output ripple voltage and the output voltage. Low clock frequency results in the high output ripple voltage according to (4-24). Increase in the output ripple voltage further reduces average output voltage in steady-state operating condition at low clock frequency. As the power conversion efficiency is directly proportional to the average output voltage, the former declines at low clock frequency, which is shown in Fig. 5-13.
If the operating clock frequency of the charge pump is chosen to be high (i.e., in MHz range), the flying capacitors and the load capacitors of the proposed charge pump are not able to deliver the charge to the loading circuit during half clock cycle due to the RC time constant of the MOS charge transfer switches, which leads to low output voltage. The relationship between the output ripple voltage and the clock frequency is discussed in Chapter 4 and is given by the following equation.

Figure 5-13. The effect of the clock frequency on the power conversion efficiency for the proposed charge pump.
\[ V_R = \frac{I_L}{C_{fly1} + C_{load} \cdot f_{CLK}} \]  

(5-3)

where \( V_R \), \( I_L \), and \( f_{CLK} \) are the output ripple voltage, the load current and the clock frequency, respectively. According to (5-3), the clock frequency is inversely proportional to the output ripple voltage. If the clock frequency is high, the output load capacitor does not have enough time to discharge the stored charge in the proposed architecture. Therefore, the ripple voltage on the load capacitor is quite low at high frequency. The effect of the clock frequency on the power conversion efficiency, the output ripple voltage and the output voltage is analyzed and shown in Fig. 5-14 and Fig. 5-15, respectively.

**Figure 5-14.** The plot of the clock frequency versus the output ripple voltage for the proposed charge pump.

Input Voltage = 5 V; Load Capacitor = 4.7 µF
Flying Capacitors = 1 µF; Load Resistor = 200 Ω
5.2.3 Input Voltage Range:

The power efficiency of the proposed charge pump is simulated over a wide input voltage range. Fig. 5-16 depicts that the power conversion efficiency over the input range is higher than 90% at typical corner. The worst case charge pump efficiency is 86.49% when the charge pump circuit is simulated with slow NMOS process parameters, slow PMOS process parameters, 2.7 V (i.e., 3 V – 10%) at 80°C and it is depicted in Fig. 5-17.
Figure 5-16. The plot of the power conversion efficiency versus the input voltage.

Figure 5-17. The worst case power efficiency simulation over 45 corners. The input supply is 3V.
The simulation of the worst case power efficiency is shown in Fig. 5-17 over 45 process, temperature, and voltage corners. The input voltage corners are 2.7 V, 3 V, and 3.3 V. The temperature and process corners are mentioned in Table 5-1. The worst case power efficiency is 87.46 % at slow NMOS process, slow PMOS process, 80°C, and 2.7 V. In slow NMOS and slow PMOS processes, the charge transfer switches have the worst ON resistance due to higher threshold voltage and it leads to higher conduction power loss. Their turn-on time and turn-off time are also high which increases reversion loss. The proposed architecture is designed for the input voltage ranging from 3 V to 7 V. It gives the power conversion efficiency higher than 90% under full load condition for the input voltage range (i.e., 3 V to 7 V) over temperature and process corners.

5.3 Layout

Proper design of the physical layout is an important requirement for the high-performance and high-power charge pump circuit. The layout size has a direct relationship with the power of the DC-DC converter. The layout size increases with the increase in the power of the charge pump as the charge transfer switches become large to minimize the conduction loss. The metal routes of supply rails and the output signal from pad to the charge pump core should be laid out with enough width to avoid electromigration since currents flowing through these routes are large. The layout size of the proposed charge pump architecture is 936 µm X 229 µm. The physical layout of the proposed charge pump is shown in Fig. 5-18. The layout of the digital circuits containing the non-overlapping clock generator and the level shifter is isolated from the high power analog circuits using the guard rings. Moreover, the supply rails for the digital circuits and the analog circuits are
also laid out separately with wide metal lines and they are connected near output pad. It avoids the coupling of the switching noise from the digital circuits to the analog circuits.

Furthermore, large charge transfer switches are connected in an interdigitated manner and each charge transfer switch is laid out with multiple fingers to avoid parasitic capacitance and parasitic resistance. PMOS and NMOS switches are isolated by guard rings to avoid latch-up.
Figure 5-18. Physical layout of the charge pump.
6.1 Conclusion

The thesis presents a new architecture for a charge-pump-based DC-DC converter with improved performance and higher power conversion efficiency. The proposed architecture uses a conventional two-phase non-overlapping clocking scheme to control the charge pump circuit. The continuous current pumping method is also proposed which is beneficial in enhancing the overall power conversion efficiency, and the drive capability, and improves the output ripple noise performance. As the proposed charge pump used the conventional clocking scheme, its architecture can be scaled to operate at higher frequencies. Moreover, the well-switcher circuit also contributes in reducing the conduction power loss and prevents the source-body junction of MOS switches from being forward-biased during the start-up condition. The continuous current pumping methodology avoids any discharge phase during the operation of the charge pump architecture and prevents a significant portion of the charge from being wasted away in the load capacitor. The prototype of the proposed charge pump architecture is designed using the AMI 0.5 μm CMOS process design kit. The effectiveness of the proposed charge pump architecture and the continuous current pumping method in enhancing output ripple noise performance and in improving overall power efficiency is verified by results obtained from rigorous simulations. Furthermore, the experimental results are in agreement with all the design specifications. The effects of the input parameters of the charge pump architecture on the output parameters are also analyzed to prove the
concept. The worst case simulation results are summarized in Table 6-1 and compared with the specifications.

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>Input Range</th>
<th>Output Load</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3 V – 7 V</td>
<td>2 mA – 45 mA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specification</th>
<th>Simulation Result</th>
<th>Corner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Conversion Efficiency</td>
<td>&gt;90 %</td>
<td>90.14 %</td>
<td>npTv</td>
</tr>
<tr>
<td>Output Ripple Voltage</td>
<td>&lt; 25 mV</td>
<td>6 mV</td>
<td>NPtV</td>
</tr>
<tr>
<td>Start-up Time</td>
<td>2 ms</td>
<td>255.4 us</td>
<td>npTv</td>
</tr>
</tbody>
</table>

Table 6-1. The compliance table for the proposed charge pump architecture

The significant contributions of this research work can be summarized as follows:

- Development of new transistor-level architecture of integrated charge pump.
- Modeling, characterization and optimization of the power efficiency, the output voltage gain and the output ripple voltage of the proposed charge pump architecture.
- Derivation of the mathematical equations of the power losses which are suited for any integrated charge pump.
- Application of the continuous current pumping method to enhance the drive capability, the power conversion efficiency and the output ripple noise performance effectively.
- The prototype of the proposed charge pump is designed in AMI 0.5 μm CMOS process and the simulation results are discussed in details.
To conclude, the charge-pump-based DC-DC converter is a widely preferred circuit for power generation in integrated microsystems compared to the bulky, costly and radiation-emitting inductor-based DC-DC converter. It is also a good solution for applications which require a wide input and output voltage range, high power conversion ratio and a wide range of operating frequency.

6.2 Future Work

In n-well 0.5 µm CMOS process technology, all NMOS transistors share a common p-well substrate which should be connected to a constant voltage during the operation of the circuit. The body terminal of an NMOS transistor can’t be connected to the well switcher in n-well CMOS process technology. This disadvantage precludes the possibility for implementation of the step-down or negative charge pump.

Generally, the stepped up output voltage of the boost charge pump is used as an input supply to implement a negative or step down charge pump. This input voltage is transferred to the load capacitor by proper switching of the charge transfer switches. The top plate of the load capacitor is connected to the ground terminal. The negative output voltage is measured at the bottom plate of the load capacitor as shown in Fig. 6-1. As mentioned earlier, the body terminal of an NMOS transistor should be connected to the lowest possible voltage in the circuit. If the body terminals of NMOS switches are connected to the output voltage of the negative charge pump, the body terminal voltage varies largely during start-up condition which further causes NMOS switches in step-up charge pump to behave erratically. Thus, it affects the overall performance of the step-up charge pump. In case of the twin tub CMOS process technology, each transistor has its
own well. The variation in the body terminal voltage of a MOS transistor does not affect the body terminal voltage of the other transistor. The negative charge pump using the same topology will be designed in the twin tub CMOS process technology as a future improvement.

Figure 6-1. The architecture of step-down charge pump based on the proposed step-up charge pump.

Another major improvement will be the implementation of the power-down circuit to achieve zero reset current when the charge pump is in the reset state. Many applications require that any idle functional block of a microsystem consume little or no power when the microsystem is in the power-down condition.

The proposed charge pump architecture can be enhanced to provide high power conversion efficiency for light loading current. The power efficiency for the low load current is in the range varying from 46% to 85% as shown in Fig. 5-4. The average current consumption in the unloaded condition is 2.1 mA which causes low power efficiency at the light load current. If the ON
resistances of the charge transfer switches are increased when the charge pump is lightly loaded, the input power consumption will decrease and the overall power conversion efficiency will increase at the light load current. By decreasing the aspect ratio of the charge transfer switches, the ON switch resistance can be increased.