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Energy- and Area-Efficient DC-DC Converters Fabricated in Low Temperature Crystalline Silicon-on-Glass Technology

Hans Christian Rotmann

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Energy- and Area-Efficient DC-DC Converters Fabricated in Low Temperature Crystalline Silicon-on-Glass Technology

by

Hans Christian Rotmann

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering

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Energy and Area Efficient DC-DC Converters Fabricated in Low Temperature Crystalline Silicon-on-Glass Technology

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Abstract

The display industry is moving toward the development of system-on-panel (SOP) architectures to make increasingly compact small-format displays and reduce manufacturing cost. Presently, the voltages required by pixel drivers, row scan logic, and timing circuitry, are generated from a single supply voltage using charge pumps fabricated on a high voltage, monolithic integrated circuit mounted off the glass panel.

In this work, a new high-efficiency charge pump architecture for fabrication on display glass substrates is presented. The distinguishing feature of this work is the nested-clock timing scheme used to improve power efficiency and reduce output voltage noise without the use of external capacitors. The circuit is intended for implementation on a novel low-temperature crystalline silicon thin-film transistor technology (SiOG™) that exhibits superior performance compared to other low-temperature fabrication processes. Based on simulation results, the proposed circuit exhibits both smaller ripple voltage (61% smaller) and improved power efficiency (80.6% vs. 67.8%) when compared to previous work.
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<th>Description</th>
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<td>AMLCD</td>
<td>Active Matrix Liquid Crystal Display</td>
</tr>
<tr>
<td>AMOLED</td>
<td>Active Matrix Organic Light-Emitting Diode</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>LC</td>
<td>Liquid Crystal</td>
</tr>
<tr>
<td>LCD</td>
<td>Liquid Crystal Display</td>
</tr>
<tr>
<td>NMOS</td>
<td>MOS Transistor (n-type)</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>OLED</td>
<td>Organic Light-Emitting Diode</td>
</tr>
<tr>
<td>PMOS</td>
<td>MOS Transistor (p-type)</td>
</tr>
<tr>
<td>QVGA</td>
<td>Quarter Video Graphics Array (320 by 240 pixels)</td>
</tr>
<tr>
<td>R.M.S.</td>
<td>Root-mean-square</td>
</tr>
<tr>
<td>SC</td>
<td>Switched-capacitor</td>
</tr>
<tr>
<td>SiOG&lt;sup&gt;TM&lt;/sup&gt;</td>
<td>Silicon-on-Glass</td>
</tr>
<tr>
<td>SOP</td>
<td>System-on-a-Panel</td>
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1 Introduction

1.1 Small Format Displays and the Push Toward On-Glass Integration

Electronic displays have become an integral part of many portable devices in the last decade. The user interfaces in digital cameras, portable media players, cellular telephones and portable navigation systems owe their simplicity to the flexibility that small-format flat panel displays offer: multiple colors, high resolutions, small dot pitch, high contrast ratio, slim profile and low power consumption. Research efforts by the leading display companies today are targeted at improving display performance.

As these display systems become increasingly complex, a large percentage of the display driver electronics is being placed on the glass surface. The process technologies to enable on glass integration continue to evolve. Since the mid 1980s, amorphous silicon (a-Si) TFT technology has been the workhorse of the display industry. It was adopted because of its low cost and low thermal budget (300 °C, critical to the use of low-cost glass substrates), and has enabled the proliferation of flat panel displays of all sizes. However, the performance characteristics of a-Si thin-film MOSFET devices lag behind their monolithic counterparts (for instance, the average electron mobility in a-Si TFT transistors is 600 times smaller than that of monolithic silicon). Recent developments in TFT technology have improved the performance of devices fabricated on glass substrates, to the extent that a trend towards increasing integration of display subsystems onto glass substrates has emerged [1] (devices fabricated using low-temperature polycrystalline silicon, LTPS, exhibit electron mobilities 200 times larger than their a-Si counterparts,
while still maintaining a low temperature budget). This trend towards System-on-Panel (SOP) aims at fabricating a complete display module, including all timing and control circuitry, on the same substrate as the TFT switches found at the pixel sites. A first step in achieving SOP has already been accomplished by successfully integrating gate drivers and analog switches in mass-produced display panels for portable applications. Despite the added processing steps (which can affect display yield negatively), SOP remains an attractive target for display manufacturers interested in providing a one-stop, low-cost solution to display applications. SOP displays require no external integrated circuits, only external connections for video data, timing signals and a single voltage supply.

The objective of this work is to contribute to the advancement of SOP development, by addressing the need for voltage conversion required to power all subsystems in a small-format Quarter Video Graphics Array (QVGA) display module for portable applications.

The small format displays commercially available today can be grouped based on their fabrication technology or emission phenomena. The following sections outline the key aspects of the two dominant display technologies.

1.2 Active Matrix Liquid Crystal Display (LCD) Technology

An Active Matrix Liquid Crystal Display (AMLCD) makes use of the electro-optical properties of liquid crystals, along with thin film transistor (TFT) fabrication technology, to selectively adjust the transmissivity of pixels. A backlight (usually a cold-cathode fluorescent stick lamp or white LED) is added behind the
polarizer and liquid crystal layer to operate the display in transmissive mode, since the light filters absorb most of the visible light [2].

A matrix of switches, fabricated directly on the glass substrate using TFT fabrication technology, is used to charge each pixel to a voltage specified by the display electronics. The non-conductive liquid crystal (LC) material acts as the dielectric of a capacitor, whose electrodes are formed using indium tin oxide (ITO, a transparent, electrically conductive material). The transmittance of the LC dielectric varies depending on the electric field present across it, so a given pixel brightness can be obtained by establishing a controlled voltage across the plates of the capacitor. Figure 1-1 shows the structure of a pixel stack.

Figure 1-1: LCD pixel stack.
The pixel voltages generated by digital-to-analog converters (DACs), are applied to the respective pixel sites through a source bus (also referred to as the data line), which runs vertically across the screen. The gate driver (row driver) bus, runs horizontally across the screen and controls the TFT switches at each of the pixel locations. At each point where the busses cross, the TFT switch connects the data bus to the bottom electrode of the LC capacitor. An ITO common electrode connects the opposite capacitor plate to a common ground plane. The simplified pixel schematics, along with the main electronic blocks of a typical LCD module (excluding the backlight), are shown in Figure 1-2.

![Figure 1-2: TFT LCD module and pixel site block diagram (adapted from [2]).](image-url)
1.2.1 Power requirements of AMLCD subsystems

The functional blocks of the AMLCD shown in Figure 1-2 require multiple supply voltages, due to the different functions they perform and the devices they control. First, the timing controller, which consists mainly of digital logic, uses either a single 3.3 or 5 V supply to minimize power consumption. It serves as an interface between the input data and the source/gate drivers, and provides control of both the source drivers (with timing signals and digital image data) and gate drivers (timing and control signals).

The gate drivers control each row of TFT switches, and require voltage levels between 20 V and -5 V to completely turn them ON and OFF (due to the poor performance of a-Si TFTs and the 10 V range of LC material). In addition, the digital logic blocks present in the gate drivers require a 3.3 V or 5 V supply line, bringing the total number of supply voltages to three (plus ground).

The source drivers contain the digital-to-analog converters and buffers that control the voltage developed at each pixel. Pixel voltages range from 0 to 5 V, to achieve the full range of LC transmittance, while the digital blocks require a 3.3 V or 5 V voltage supply.

Finally, the common reference helps prevent image retention in the LCD display by varying the reference voltage of the LC capacitor. This technique, know as $V_{com}$ modulation, requires a voltage variation between 0 and 5 V. Table 1 summarizes these voltage requirements for a QVGA display (320×240×3 pixels), and provides estimates for load currents.


### Table 1: Power requirements for LCD subsystems in QVGA display.

<table>
<thead>
<tr>
<th>MODULE</th>
<th>VOLTAGE AND CURRENT REQUIREMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing Controller</td>
<td>5.5 V, 100 μA</td>
</tr>
<tr>
<td>Gate Drivers</td>
<td>-5 V, 100 μA</td>
</tr>
<tr>
<td></td>
<td>5.5 V, 10 μA</td>
</tr>
<tr>
<td></td>
<td>20 V, 100 μA</td>
</tr>
<tr>
<td>Source Drivers</td>
<td>5.5 V, 600 - 1000 μA</td>
</tr>
<tr>
<td></td>
<td>10 V</td>
</tr>
<tr>
<td>DAC Reference Voltages</td>
<td>10 V</td>
</tr>
<tr>
<td>Common Reference</td>
<td>5 V</td>
</tr>
</tbody>
</table>

---

### 1.3 Active Matrix Organic Light-Emitting Diode (AMOLED) Technology

Organic light-emitting diode (OLED) displays rely on the emission of photons in the visible light spectrum when electrons and holes (injected from the pixel terminals) recombine. Since each OLED pixel acts as a light source, a backlight is not required for transmissive operation, which can lead to power savings when compared to LCD displays. In addition, OLED displays offer a higher contrast ratio and deeper color saturation than reflective LCD technologies. Figure 1-3 shows a basic OLED pixel stack. Typical display panels manufactured today contain double-stacked OLED structures at each pixel site.
Figure 1-3: OLED pixel stack (adapted from [2]).

Tang et al. [3] first reported the successful fabrication of an electroluminescent (EL) device with improved characteristics over its predecessors. The main advances achieved were high power-conversion efficiency and high brightness with low DC biasing. Figure 1-4 shows the electroluminescent characteristics of a pixel 150 μm long by 50 μm wide (which are typical pixel dimensions), based on data published in the literature [3].

Figure 1-4: EL characteristics of a 150 μm x 50 μm OLED stack (adapted from [3]).
The typical OLED display employs three sub-pixels (red, green and blue) within each macro-pixel location. Each individual pixel is usually made up of two vertical OLED stacks, to achieve higher luminance. Based on the data shown in Figure 1-4, the luminance from a double-stacked OLED pixel responds logarithmically over three orders of magnitude of current \((10^{-9} \text{ to } 10^{6})\), and required a fixed DC bias up to 14 V. Pixels in an LCD display, on the other hand, do not draw a fixed DC current because the LC element looks capacitive. For this reason, the power requirements of the pixel driving circuits in an AMOLED are substantially different from their AMLCD counterparts. Furthermore, OLED structures exhibit aging effects that translate into an increase in turn-on voltage. While the luminance vs. current relationship remains fairly uniform, the voltage required to develop a given current increases as the OLED pixel ages (a right-wise translation of the curves in Figure 1-4). The pixel driving circuits must, therefore, provide ample voltage headroom to accommodate the wide DC range and the aging effects.

A simplified block diagram of the typical AMOLED display is shown in Figure 1-5. Despite the differences in the pixel drivers, much of the surrounding control electronics is very similar to that found in an LCD module. Row drivers control each of the row select lines, while the column drivers contain the DACs responsible for providing the programming currents (or voltages) to each of the pixel circuits.
1.3.1 Power requirements of AMOLED subsystems

As stated earlier, the main difference between AMLCD and AMOLED displays resides in the pixel driving scheme. A typical AMOLED pixel will require enough voltage headroom to sink the full range of currents provided by the DACs, in addition to
the voltage drops across the drive transistors. Based on the results obtained for samples of double-stacked OLED devices, voltages between 10 and 15 V are required to power the pixel OLED stack and the necessary drive circuitry.

An estimate of the DC current required by a QVGA display can be obtained by assuming that the display is white, since all sub-pixels would be turned on. By taking into consideration the total number of pixels in the display \((320 \times 240 \times 3)\) and the current drawn by each (60 nA for 33% luminance), then

\[
I_{\text{total}} = N_{\text{pixel}} \times I_{\text{pixel}} = (320 \times 240 \times 3) \times 60 \text{ nA} = 13.8 \text{ mA} \quad (1-1)
\]

Table 2 provides a summary of the voltage and current requirements of a QVGA AMOLED display.

<table>
<thead>
<tr>
<th>Module</th>
<th>Voltage and Current Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing Controller</td>
<td>5 V, 100 µA</td>
</tr>
<tr>
<td>Row Drivers</td>
<td>10 V, 100 µA</td>
</tr>
<tr>
<td></td>
<td>5 V, 50 - 100 µA</td>
</tr>
<tr>
<td></td>
<td>15 V, 15 mA</td>
</tr>
<tr>
<td>Column Drivers</td>
<td>5 V, 600 - 1000 µA</td>
</tr>
<tr>
<td>DAC Reference Voltages</td>
<td>10 V</td>
</tr>
</tbody>
</table>
1.4 Integrating Electronics on Glass

Display manufacturers continue to seek ways to reduce manufacturing cost and improve performance. The glass surface offers a large area substrate for placing electronics components, but TFT fabrication processes in use by industry today are still a significant distance away from reaching bulk-quality CMOS devices. A major focus of this work is investigating the use of a novel on-glass thin film technology for fabricating display drive circuits called SiOG™, which is covered in greater detail in Section 2.4.

As seen in this chapter, energy and area-efficient DC-DC conversion is a fundamental part of any small-format portable display. Advances in display fabrication technology have allowed the integration of major system components onto glass substrates, thus allowing manufacturers to achieve more compact display solutions for their customers. As the industry migrates towards SOP, the development of improved charge pump architectures becomes an important priority because these provide power for all subsystems in the display.
2 DC/DC Converters and Charge Pumps

Both AMLCD and AMOLED displays require several operating voltages. The demand for modular displays with single voltage interfaces requires that multiple voltages be developed by DC-DC converters on the display. Traditional switched-mode DC-DC converter architectures rely on magnetic components (such as inductors or transformers) and capacitors to boost one DC voltage to a higher DC voltage. These are widely used in board-level designs because of their high energy efficiencies. However, these architectures do not lend themselves to monolithic implementation because high Q inductors and compact transformers are not available in the process technologies.

An alternative better suited to monolithic integration is charge pumps. Charge pumping has been used effectively for a broad array of applications, including EEPROM, sample-and-hold circuits, white LED drivers and RS-232 level shifters. Integrated capacitors are easily fabricated using processes already in use by the display industry, and are often present in the pixel driver circuits for both AMLCD and AMOLED display modules. Like their magnetic counterparts, DC-DC converters based on charge pumps can be highly energy efficient.

The first charge pump developed for DC-DC conversion, the Cockcroft-Walton multiplier [4], was used to generate 800 kV of steady potential required by particle accelerators. The first successful implementation of a solid state charge pump was reported in 1976 by J.F. Dickson, in what is now known as the Dickson multiplier [5]. Like the Cockcroft-Walton multiplier, the Dickson multiplier makes use of capacitors and
rectifiers to charge and voltage boost capacitors in a sequential manner, while keeping the maximum voltage across each capacitor equal to the value of the input drive voltage.

In the typical charge pump, a ‘flying capacitor’ is used to store energy and develop a potential that may be higher or lower than the input voltage. Figure 2-1 shows the schematic of a basic voltage doubler, where switches S1 through S4 control the nodes to which the capacitor electrodes are connected. Switches S1 and S4 are controlled by one clock signal (Φ₁), while switches S2 and S3 are controlled by another clock signal (Φ₂). Both Φ₁ and Φ₂ are anti-phase, non-overlapping clocks, as shown in the timing diagram in Figure 2-2.

![Figure 2-1: Basic voltage doubler.](image)

![Figure 2-2: Timing diagram for the basic voltage doubler.](image)
During the time when $\Phi_1$ is active (Figure 2-3a, the charge phase), capacitor $C$ is connected in parallel to the voltage source. A total charge $Q_{\text{charge}}$ is delivered to the flying capacitor, and thus a voltage $V_{\text{DD}}$ develops across its plates, according to:

$$Q_{\text{charge}} = C \cdot V_{\text{DD}}$$  \hfill (2-1)

![Figure 2-3: Charge (a) and discharge (b) phases of the basic voltage doubler.](image)

When $\Phi_2$ becomes active (Figure 2-3b, the discharge phase), capacitor $C$ is connected in series with the voltage source, so the total charge in the system, $Q_{\text{total}}$ is given by

$$Q_{\text{total}} = Q_{\text{charge}} + Q_{\text{previous}} = C \cdot V_{\text{DD}} + Q_{\text{previous}}$$  \hfill (2-2)

where $Q_{\text{previous}}$ is the charge present in $C_{\text{filter}}$ from the previous discharge cycle under no load conditions. Assuming a voltage $V_o[n]$ develops at the output node, $Q_{\text{total}}$ can be expressed as the sum of the charges stored in $C$ and $C_{\text{filter}}$:

$$Q_{\text{total}} = Q_C + Q_{\text{filter}} = C \times [V_o[n] - V_{\text{DD}}] + C_{\text{filter}} \times V_o[n]$$  \hfill (2-3)
Combining (2-2) and (2-3) yields the following expression for $V_o[n]$:

$$V_o[n] = V_{DD} \times \left( \frac{2 \cdot C}{C + C_{filter}} \right) + \frac{Q_{previous}}{C + C_{filter}}$$

(2-4)

Realizing that $Q_{previous}$ may be expressed as

$$Q_{previous} = C_{filter} \cdot V_o[n-1]$$

(2-5)

yields the final expression for the output voltage:

$$V_o[n] = V_{DD} \times \left( \frac{2 \cdot C}{C + C_{filter}} \right) + \frac{V_o[n-1]}{C_{filter}} + 1$$

(2-6)

Figure 2-4 shows the output of the voltage doubler as it reaches twice the input voltage. The three curves represent different ratios of flying capacitor to filter capacitor. The output voltage has been normalized to the input voltage $V_{DD}$. Increasing the size of the filter capacitor leads to an increase in the rise time of the output voltage, because the amount of charge transferred from the flying capacitor effects a smaller change in $V_{out}$. As discussed later in this chapter, the filter capacitor size cannot be reduced excessively (in favor of reduced circuit footprint and rise time) because it helps reduce output voltage sag brought about by loading the charge pump.
2.1 Charge Pump Performance Characteristics

As shown in Figure 2-4, the output of the voltage doubler remains constant if the circuit is driving a capacitive (high impedance) load. If a resistive load is attached, the mathematical model outlined previously has to be modified to account for the charge being drawn from the system. Assuming the frequency of the clocks is \( f \), equation (2-2) becomes:

\[
Q_{\text{total}} = Q_{\text{charge}} + Q_{\text{previous}} - Q_{\text{drawn}}
\]  

(2-7)

where \( Q_{\text{drawn}} \) is the charge drawn from the system by the load during half a clock period. For a load current \( I_{\text{load}} \),

\[
Q_{\text{drawn}} = I_{\text{load}} \cdot \frac{T}{2} = \frac{I_{\text{load}}}{2f}
\]  

(2-8)
Since the load current also draws a certain amount of charge during the charge cycle, equation (2-5) becomes

\[ Q_{\text{previous}} = C_{\text{filter}} \cdot V_o[n-1] - Q_{\text{drawn}} \]  

(2-9)

For a loaded voltage doubler, the output voltage then becomes:

\[ V_o[n] = V_{DD} \times \left( \frac{2 \cdot C}{C + C_{\text{filter}}} \right) + \frac{V_o[n-1] - \frac{I_{\text{load}}}{f \cdot C_{\text{filter}}}}{C} \]  

+ 1

(2-10)

The right-most term in (2-10) shows that, under resistively-loaded conditions, the filter capacitor behaves as a switched-capacitor resistor. This resistor reduces the multiplication factor of the charge pump – i.e. the ratio of steady-state output voltage to input voltage.

Another important effect of loading is the voltage ripple present at the output node of the charge pump. Ripple occurs as the result of the competition between the pump capacitor feeding charge into the output node, and the load drawing charge from it. Figure 2-5 shows a modified version of Figure 2-3b, showing the discharge cycle of the charge pump, including load resistance and switch resistance. When the switch is thrown, capacitor \( C \) discharges through the switch and causes the voltage at the output node to rise. During the charge cycle, the load draws charge from the filter capacitor and causes the voltage to sag, as shown in the inset of Figure 2-6.
Figure 2-5: Discharge circuit including switch resistance.

Figure 2-6: Output waveform for charge pump with resistive load.
Supply ripple can be problematic for the analog components in the display electronics, especially amplifiers where it can couple into the output. A voltage regulator can be used to remove ripple, but it will reduce the power efficiency of the converter.

Along with multiplication factor and voltage ripple, power efficiency and area are important metrics for charge pumps. Power efficiency, \( \eta \), is defined as

\[
\eta = \frac{P_{\text{out}}}{P_{\text{in}}}
\]

(2-11)

where \( P_{\text{out}} \) is the power delivered to the load, and \( P_{\text{in}} \) is the power drawn from the voltage supply. Maintaining high power efficiency increases battery lifetime in portable products.

Circuit area is of particular concern when integrating display electronics on glass, because maximizing usable display area is a priority. The capacitors used in a charge pump use a substantial amount of area, and therefore it is up to the circuit architecture to use them effectively. As shown in Figure 2-7, capacitors of moderate size can occupy a substantial amount of display area (assuming 5000 Å of silicon dioxide as dielectric).

Figure 2-7: Capacitors overlaid on typical QVGA portable display (to scale).
2.2 Charge Pump Architectures

Integrated charge pumps have been reported since the early 1970s. The first integrated charge pump used for DC-DC conversion was reported by J. F. Dickson [5], and is therefore known as the Dickson charge pump. This design makes use of diode-connected MOSFETs to chain together several pumping stages, as shown in Figure 2-8.

![Diagram of 4-stage Dickson charge pump with clocks](image)

Figure 2-8: 4-stage Dickson charge pump and clocks (adapted from [5]).

The Dickson charge pump works by pushing packets of charge from one node to the other during alternating clock cycles of non-overlapping clocks. Although a simple circuit, this architecture has made its way to a multitude of integrated electronic systems requiring voltage levels above a single input voltage. Neglecting the stray capacitance present at each pumping node, the output voltage for an $N$-stage Dickson multiplier is given by

$$V_{out} = V_{in} - V_T + N \cdot (V_{in} - V_T) - \frac{N \cdot I_{out}}{C_p f}$$ (2-12)

where $V_{in}$ is the input voltage, $V_T$ is the threshold voltage of each diode-connected
transistor, $C_p$ is the pump capacitance, $f$ is the clock frequency and $I_{out}$ is the load current.

One of the biggest drawbacks of the Dickson charge pump is the $V_T$ drop across each of the diode-connected transistors, which is made worse by the body effect increase in threshold voltage toward the latter stages. One therefore reaches a point of diminishing returns, because adding more stages to the charge pump has little impact on the output voltage.

Another limitation of the Dickson charge pump is its high output resistance. Equation (2-13) shows that the Thévenin-equivalent resistance of an $N$-stage Dickson charge pump is inversely proportional to both clock frequency $f$ and pump capacitance $C_p$.

$$R_{th} = \frac{N}{C_p \cdot f}$$  \hspace{1cm} (2-13)

Ideally, the output resistance could be made as low as necessary. However, the constraints placed on the number of pump stages (due to $V_T$ drops and the body effect), the size of the pump capacitance (large area required) and the clock frequency (low carrier mobilities of TFT devices) lead to high output resistance values for this architecture.

Finally, the voltage ripple present at the output node of the Dickson charge pump is inversely proportional to clock frequency and filter capacitance, as shown in (2-14).

$$V_{ripple} = \frac{I_{out}}{C_{fil} \cdot f}$$  \hspace{1cm} (2-14)
This relationship forces the circuit designer to use a high switching frequency and large filter capacitors to achieve small voltage ripple.

The non-idealities associated with silicon implementations of the Dickson charge pump have been thoroughly studied in the literature. The effects of threshold voltage increases in the latter stages of the circuit, along with the effects of parasitic capacitances and leakage currents at each node were studied by Witters et al. [6].

The adverse effects of the threshold voltage increase have been tackled in several ways. Shin et al. [7] propose the implementation of a Dickson charge pump using PMOS devices in triple-well technology, where the body of the charge transfer transistor is connected to two additional PMOS devices. These auxiliary devices are responsible for connecting the body of the diode-connected PMOS to either its anode or cathode, depending on which has the higher potential, thus ensuring that \( V_{BS} \) is zero and that no body effect occurs. This increases the maximum number of stages that can be implemented, but does not alleviate the fact that each diode-connected device still forces a \( V_T \) drop. Furthermore, the two auxiliary devices in each stage add to the parasitic capacitance at each pumping node, thus reducing the power efficiency of circuit.

The approach of disconnecting the body of the diode-connected devices was investigated by Choi et al. [8]. The circuit consisted of a traditional Dickson charge pump, implemented with diode-connected PMOS devices in a 0.5 \( \mu \)m triple-well high-voltage CMOS process. The \( n \)-wells that formed the bodies of each PMOS device were left floating, while the \( p \)-type substrate was grounded, as shown in Figure 2-9.
The authors state that, when a PMOS device is first turned on at the beginning of the charge transfer cycle, the source-to-body potential is positive and equal to the built-in potential of the junction. This leads to a $V_T$ slightly lower than the $V_{th}$ of the device, thus increasing the output voltage and drive strength of the circuit. Leaving the body floating can, however, cause unwanted body currents and charge accumulation.

More sophisticated Dickson-like circuits have been reported in the literature. Hoque et al. [9] utilized silicon-on-insulator (SOI) technology to implement a body diode that exhibits reduced voltage drop and permits a 10% increase in charge pump efficiency. This particular diode was implemented by connecting together the gate, body and drain terminals (diode anode) of an SOI NMOS transistor. Since each transistor is isolated from its neighbors by a buried oxide layer, the body can be tapped independently in each device. As the authors of this work correctly point out, such diode could not be used in a CMOS process because of the risk of turning on the parasitic bipolar formed by the $n^+$-type drain, $p$-well, $n$-epi layer. Based on 2-D device simulations, the authors report that the diode drop is reduced from 0.7 V to 0.4 V. The results measured and reported
reveal a higher DC steady-state output voltage, but only for medium loads at high clock frequencies (5 MHz). The reduced parasitic capacitances offered by SOI technology also contributed to an increase in power efficiency, but at the expense of higher fabrication costs.

An alternative Dickson charge pump without any threshold voltage drops across the charge transfer devices was proposed in the literature [10] (a pump stage is shown in Figure 2-10). The circuit presented uses NMOS transistors to transfer charge from one node to the other. Each clock signal is coupled to the gate of the NMOS switch (M1 and M3) through a capacitor ($C_{gate}$), which has previously been pre-charged. When the clock signal goes high, the gate of the transistor sees a voltage equal to the clock voltage plus the capacitor voltage, which is enough to turn the device on and transfer charge to the next node.

![Diagram of improved charge pump stage without $V_T$ drop](image)

Figure 2-10: Improved charge pump stage without $V_T$ drop (adapted from [10]).
This circuit architecture was implemented using a three-well CMOS process, which also allowed the designers to connect the bodies of the charge transfer switches to their drains, thus creating a PN junction between the drain and the source. The addition of this diode in parallel to the NMOS switch increases the time available for charge transfer and decreases the ON resistance from one node to the other. This body-drain connection is only feasible in a three-well process, because of the isolation provided by the n-well between p-type transistor body and the p-type substrate. Despite the reported increases in drive strength and power efficiency, the latter figure (50%) remains below the ideal for portable applications, where battery life is critical.

Hirata et al. [11] developed a ten-stage positive and a six-stage negative Dickson charge pump for use in TFT-LCD panels, that does not exhibit a $V_T$ drop from one stage to the next. Their circuit makes use of a secondary charge pump to generate the gate control signals for the main charge pump, both of which are implemented using PMOS devices. The negative voltage charge pump was implemented by replacing all PMOS with NMOS devices, and changing the location of the input and output nodes. Both designs make use of four-phase clocks to achieve the correct switching sequence. Like similar designs, the main disadvantage of this circuit is the high number of connections made to each pumping node, which can significantly increase the top-plate parasitic capacitance of the flying capacitors. The use of auxiliary charge pumps to generate the appropriate voltage levels to control transistors translates also to an increase in chip area.

A number of Dickson-like designs that are not susceptible to threshold voltage drops or variations have been reported in the literature [12, 13].
One such work, by Wu et al. [12], replaces the diode-connected transistors in the traditional Dickson circuit by sophisticated charge transfer switches (CTS). These switches make use of the higher voltages generated in the latter stages of the charge pump to control the transistor gates in the earlier stages, thus ensuring complete turn off of the devices and preventing reverse leakage. Unfortunately, the output stage of the charge pump is implemented by using a diode-connected MOSFET, thus reducing the output voltage by a \( V_T \).

In what could be regarded as the *state of the art* in Dickson charge pumps, Ker et al. [13] improve on the Wu et al. design by splitting the charge pump into two branches, each with equal sized capacitors. The new design takes into account the voltage stresses that the gate oxide is subjected to in the more traditional charge pumps, and ensures that the gate-source and gate-drain voltages do not exceed the input voltage. This is of particular importance for circuit reliability and duration, as operating voltage continue to drop and gate oxides get thinner. Measured results, obtained from the implementation of this circuit in a triple-well, 0.35 \( \mu \)m, 3.3 V CMOS process reveal a three-fold reduction in ripple voltage, when compared to the Wu charge pump, and a four-fold reduction when compared to the traditional Dickson charge pump. Output drive strength measurements also indicate a significant increase over the previous two architectures [13].
2.3 Switched-Capacitor Charge Pumps

Dickson charge pumps are a subset of a larger group of voltage converters based on switched-capacitor (SC) circuits. Expanding the possible connection arrangements allows more flexibility when choosing a topology to provide a given conversion ratio (i.e., the ratio of output voltage to input voltage when unloaded). For instance, Makowski et al. [14, 15] determined that a two-phased SC charge pump with \( k \) capacitors can exhibit both positive and negative ideal conversion ratios of the form \( P/Q \), where \( P \) and \( Q \) are integers between 1 and the \( k^{th} \) Fibonacci number. Hence, for an SC charge pump with three capacitors, there are fourteen distinct conversion ratios\(^1\). Which ratio is ultimately chosen depends on the circuit topology and switching pattern.

Starzyk et al. [16] went further into the analysis of SC charge pumps, and presented the benefits brought about by using more sophisticated clocking schemes. By using multi-phase clocks, the maximum attainable conversion ratio is pushed up to \( 2^n \), where \( n \) is the number of capacitors (excluding the filter capacitor) in the charge pump. Reducing the number of capacitors needed to reach a certain conversion ratio leads to a significant area reduction, since integrated capacitors tend to be large.

The main challenge in designing a switched-capacitor voltage doubler is that the MOSFET switches required to implement them need control signals with voltages as high as the doubled voltage. As seen earlier, some designs resort to auxiliary charge pumps to

---

\(^1\) The fourteen conversion ratios are \( \pm \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, 1, 1\frac{1}{2}, 2, 3 \).
develop the voltages needed to control the switches. This leads to higher area and power consumption.

The cross-coupled charge pump featured in Figure 2-11 [17] makes use of two parallel charge pumps, cross connected so that the doubled voltage developed on one side controls the switches on the opposite side.

Clock signals \( \Phi_1 \) and \( \Phi_2 \) are 180° out of phase with amplitude equal to \( V_{in} \). As shown in Figure 2-12, one side of the voltage doubler is charged during the first half of the clock period, and discharged during the second half. The use of PMOS switches instead of diode-connected NMOS devices to connect the capacitors \( C_{p1} \) and \( C_{p2} \) to the output node ensures that there will be no \( V_T \) drop.

Because each side of the voltage doubler is discharged once every clock period, the output filtering capacitor is charged to the doubled voltage twice as often as in the Dickson case. The ripple voltage for the cross-coupled doubler is, therefore, half of that for the Dickson charge pump. For equal ripple voltage requirements, this translates to a substantial reduction in circuit area, since the size of the output filtering capacitor can be halved.
Figure 2-11: Cross coupled charge pump (adapted from [17]).

Figure 2-12: Timing diagrams for cross-coupled charge pump.
Baderna et al. [18] compare the performance of a cross-coupled charge pump and a Dickson charge pump with boosting circuitry, under equal conditions (same fabrication technology, equal number of stages, equal pump and filter capacitor sizes and same clock frequencies). Their results indicate that the cross-coupled structure was 13% more efficient than the Dickson charge pump due to the reduced top-plate parasitic capacitance. The overwhelming majority of researchers working on SOP displays prefers the use of SC charge pumps, over Dickson-type architectures, because of the superior power efficiency, voltage ripple and circuit footprint figures [19-25].

2.4 The Case for On-Glass Integration

Currently, the control electronics for small-format displays is fabricated on bulk silicon and later die-attached to the glass substrate [2]. As seen earlier in this chapter, the implementation of DC-DC converters requires high-voltage, triple-well CMOS processes that can drive the cost of the display up [22]. Bulk-biasing techniques are also required to prevent latch-up and unintended forward-biasing of p-n junctions that can lead to substrate currents [26]. Silicon-on-Insulator (SOI) technology shows excellent performance for SC charge pumps [27], but once again the costs associated with the fabrication technology are high.

Although display manufacturers would prefer to manage all of the fabrication steps in house, it is common practice for them to contract out the design of the display driver circuits to a third party. The third party design house uses monolithic silicon to
implement the complex display electronics, and the resultant silicon die is then inserted into the display module by attachment to the flex-cable (chip-on-flex, COF, technology).

To this day, efforts towards SOP have been limited by the TFT fabrication technology available. The main roadblock has been the low temperature ceiling imposed by the glass substrate (1000 °C), which forbids the use of a high-temperature anneal step. Low-temperature polycrystalline silicon (LTPS) technology makes use of a laser to re-crystallize silicon, and has enabled the integration of certain circuit blocks. Device uniformity and carrier mobilities, however, still suffer from the grain boundaries inherent to the silicon film [28].

This project used a novel TFT fabrication technology targeted for small-format flat panel displays called Silicon-on-Glass (SiOG™) [28]. Devices fabricated on SiOG™ substrates exhibit carrier mobilities comparable to those of monolithic silicon, and are vastly superior to those obtained using LTPS. They exhibit very low off-state currents, thus permitting the fabrication of good switches (instrumental to high-efficiency charge pumps). As a demonstration of SiOG™ potential, Choi et al. [29] report the successful implementation of an QVGA 2.4”AMOLED display, with gate drivers, level shifters and column multiplexers integrated onto the glass substrate. SiOG™ offers many of the advantages of SOI technology (latchup-free operation, low parasitic capacitance, high carrier mobilities and isolated transistor mesas for body-biasing of individual devices), at a lower manufacturing cost and without any additional fabrication steps aside from those already used to make TFT switches at each pixel site.
The current state of SiOG™ technology is not without its limitations. SiOG is a 5-mask process, which limits the number of metal layers to two. The minimum gate length is 2 µm, metal-to-silicon contacts are 4 µm by 4 µm with an overlap of 2 µm, metal-to-metal contacts are also 4 µm by 4 µm with an overlap of 4 µm, and the minimum metal width is 6 µm. The minimum-sized transistor that meets the design rules is shown in Figure 2-13. Excluding the separate gate to metal contact, the device dimensions are 28 µm by 12 µm. This illustrates the overhead in area that exists as a result of the large size contacts and wide metal requirements. Said requirements affect the area efficiency of circuits designed in the SiOG™ process. A monolithic silicon process offers more metal layers, thinner metal traces and carefully-controlled threshold voltages, which can improve circuit performance and footprint significantly. These shortcomings will be improved as the SiOG™ process matures.

![Diagram of SiOG™ technology](image)

Figure 2-13: Minimum size device in SiOG™ technology.
3 Proposed High-Efficiency Charge Pump

The cross-coupled voltage doubler is a simple circuit. However, the cross-coupled architecture faces two leakage paths which limit its performance [30]. These paths can best be observed by assuming that the charge pump in Figure 3-1 has reached steady state, and that its clocks are about to undergo a transition. In this situation, $\Phi_1$ is going high and $\Phi_2$ is going low. The first of the leakage paths (output leakage) occurs when PMOS switch M4 has not turned off completely before $\Phi_2$ goes low. Under these circumstances, a leakage current can flow from the output node back to node 2, thus reducing the voltage at the output. Similarly, M1 allows a current to flow from the output back to node 1 because it starts turning on before $\Phi_1$ is high. Timing diagrams for both of these cases are shown in Figure 3-2.

![Figure 3-1: Leakage paths in cross-coupled voltage doubler.](image-url)
The second leakage path (rail leakage) occurs when transistor M3 allows a certain current to flow back to the input rail from node 2. Rail leakage also occurs when transistor M2 has not completely turned off before $\Phi_1$ goes high, thus reducing the voltage developed across $C_{pi}$ and, hence, the output voltage. The converse situation takes place when $\Phi_1$ goes low and $\Phi_2$ goes high. As seen in the timing diagrams, the effects of output leakage are greater, due to the longer time window available for current to flow back.

Both leakage paths have negative effects on power efficiency and R.M.S. output voltage, because of the constant amount of charge wasted during each clock edge. If multi-phase techniques [19] are used to further reduce ripple, the reduction in power efficiency becomes worse. The glitches that such leakage paths create also contribute to
greater high-frequency noise at the output node of the charge pump, which can be detrimental to the performance of analog electronics. The focus of this work is, therefore, to find the optimal timing sequence for the cross-coupled charge pump to eliminate these leakage paths and implement it to see the resulting charge pump performance.

3.1 The Nested-Clock Timing Scheme

In order to eliminate the conditions that give rise to output and rail leakage, switch timing is critical. The correct sequence to achieve voltage doubling and eliminate leakage is illustrated in Figure 3-3. The figure shows two sides of a cross-coupled charge pump. The right hand side is entering the charge phase, and so M4 has to be turned off first. Once M4 is completely turned off, \( \Phi_2 \) goes low (this ensures the elimination of output leakage). Once \( \Phi_2 \) is low, M3 is turned on to recharge \( C_{p2} \) (this eliminates rail leakage). Conversely, the left hand side of the circuit is in the discharge phase, and so M2 must be turned off completely before \( \Phi_1 \) goes high to ensure no rail leakage occurs. Once \( \Phi_1 \) is high, M1 is turned on (this eliminates output leakage). The resulting timing diagram for \( \Phi_1, \Phi_2 \) and the gate signals of M1 through M4 reflect the nested nature of the timing scheme: the on-time of M1 is nested within the high-time of \( \Phi_1 \), which is nested, in turn, within the off-time of M2. Similarly, the on-time of M3 is nested within the off-time of \( \Phi_2 \), which is nested within the off-time of M4. Close observation of the timing diagrams indicate that such a clocking arrangement cannot be obtained by using only delay elements, because of the sequence at which the signal edges take place. A timing diagram showing several cycles of the proposed clocking scheme is shown in Figure 3-5.
Figure 3-3: Switch activation sequence.

Figure 3-4: Nested-clock timing diagram for (a) discharge and (b) charge phases.
As seen in Figure 3-5, the falling edges of the gate signals of M2 and M3 precede the transitions that take place in the nested clocking scheme. The transitions of clocks \(\Phi_1\) and \(\Phi_2\), as well as those of gate signals \(V_{G1}\) and \(V_{G4}\), can therefore be triggered by these falling edges. Figure 3-5 also reveals that \(V_{G2}\) and \(V_{G3}\) are two non-overlapping clock signals, which can be generated from an external clock. This also ensures proper startup of the charge pump, because the rail switches are activated first. A block diagram of the timing electronics for the proposed charge pump is shown in Figure 3-6.
3.2 Proof Of Concept

In order to verify the improvements brought about by the use of the proposed nested-clock timing scheme in a voltage doubler, a charge pump with individually controlled gates was simulated using Spectre™. For comparison purposes, a cross-coupled charge pump was simulated under the same conditions, using non-overlapping clocks to reduce shoot-through currents [20]. Timing signals were generated using ideal clocks. Details on the circuit components are shown in Table 3.

<table>
<thead>
<tr>
<th>Table 3: Circuit comparison details.</th>
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<tr>
<td>Clock frequency</td>
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<td>Input Voltage</td>
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<td>Flying capacitor size</td>
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<tr>
<td>Filter capacitor size</td>
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<tr>
<td>PMOS switch sizes (W/L)</td>
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<tr>
<td>NMOS switch sizes (W/L)</td>
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The circuit simulations revealed the presence of both rail and output leakage current spikes, resulting from the simultaneous conduction problem outlined at the beginning of this chapter. Figure 3-7 shows the currents coming in (positive) and out (negative) of the transistor terminals connected to the flying capacitors (drain of M1 and source of M2) in the cross-coupled and nested doublers, during one clock cycle (1 μs) under a 100 μA load. Leakage currents are highlighted for clarity.

The current through the drain of M1 (orange curve in Figure 3-7) in the cross-coupled charge pump presents a 500 μA current spike at the beginning of the clock
transition (25.5 µs), as shown in dotted region labeled (a). The dotted region (b) in Figure 3-7 shows another current spike at the next clock transition (26.0 µs). A third current spike occurs at the source of M2 during the first clock transition, as shown by the green curve in the dotted region (c) of Figure 3-7. All of these spikes reduce the amount of charge being transferred from the flying capacitors to the output, thus increasing ripple and reducing R.M.S. output voltage.

The nested-clocking scheme eliminates the conditions that give rise to these spikes, as shown by the blue (M1 drain) and purple (M2 source) curves in Figure 3-7. Figure 3-8 provides a close-up of the spikes highlighted in Figure 3-7. The reduction in leakage currents is evident, and it contributes directly to the improvements in circuit performance shown in Table 4.

<table>
<thead>
<tr>
<th>Table 4: Proof of concept simulation results.</th>
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<td>Output Voltage (V_{rms})</td>
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<td>Ripple Voltage (mV)</td>
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<td>Power Efficiency</td>
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Figure 3-7: Leakage currents in cross-coupled and nested charge pumps.

Figure 3-8: Highlighted output (a, b) and rail (c) leakage spikes from Figure 3-7.
3.3 Clocking Scheme Implementation

The implementation of the nested clocking scheme is an area that deserves significant attention. Improvements that may be obtained by using such a scheme may be offset by the complexity of the circuits needed to generate it. Since SiOG technology permits the fabrication of both NMOS and PMOS devices, the timing electronics were implemented using CMOS logic. An expanded version of the timing electronics block diagram from Figure 3-6 is shown in Figure 3-9.

![Timing electronics block diagram](image)

Figure 3-9: Timing electronics block diagram.

As stated in Section 3.1, the signals to control the rail switches M2 and M3 can be generated from a system clock using a non-overlapping clock generator. The outputs from the non-overlapping clock generator (CLK₁ and CLK₂ in Figure 3-9) have to be level shifted to drive the gates of the NMOS transistors (rail switches). As discussed in
Section 3.1, these signals are also responsible for triggering the correct sequence of transitions to ensure nested operation, and are therefore used as inputs to the transition control electronics that will generate the required signals. Finally, these signals are conditioned (i.e., buffered to provide enough drive strength, or level-shifted to the appropriate voltage) and used to drive the gates of the PMOS switches ($V_{G1}$ and $V_{G4}$) and the bottom plates of the flying capacitors ($\Phi_1$ and $\Phi_2$).

The non-overlapping clock generator is the first element in the timing electronics block. One such circuit is available in the literature [31] and is shown in Figure 3-10. The delay between clock pulses (the dead time) depends on the number of delay elements present in the feedback loops of the NOR gates.

![Non-overlapping clock generator diagram](image)

Figure 3-10: Non-overlapping clock generator.

Level shifters are of particular importance to the charge pump, because they are required to ensure that the PMOS switches are completely turned off and that the NMOS transistors are on. A total of four level shifters are therefore required. The traditional level shifter (shown in Figure 3-11) is poorly suited to low-power applications because every time that the input shifts logic levels a low impedance path between the upper rail and
ground exists. This path disappears after the level shifter reaches steady state, but can nonetheless severely affect the performance of a charge pump.

![Traditional level-shifter diagram](image)

**Figure 3-11: Traditional level-shifter.**

An alternative design for a level shifter is presented in Figure 3-12. The new design makes use of a capacitor, located between the gates of NMOS and PMOS transistors, to provide the additional voltage needed to turn off the PMOS device when the input is high. The diode-connected PMOS transistor charges the capacitor up to $V_{DD} - V_{TP}$ whenever the input is logic low. An inverter is placed at the output so that the level shifter is logically transparent (i.e., the output is high when the input is high) and to provide buffering. Based on simulations of both level shifters, the new design consumes 66.3% less power.
Two negative edge detectors are needed to trigger the appropriate signal transitions when either of the non-overlapping clock signals goes low. The traditional edge detector circuit (shown in Figure 3-13) lends itself well to this application. This circuit outputs a brief pulse every time the input experiences a falling edge. The duration of the pulse depends on the number of delay elements present in the circuit.

The outputs from the edge detectors are connected to the transition control circuit, shown in Figure 3-14 along with its corresponding timing diagram. The circuit is
composed of two pairs of SR latches, which are either set or reset based on the input from the edge detectors and the output of the opposite latch.

At time $t = 0$, the outputs from the edge detectors are both low. $Q_1$ and $Q_4$ are high, while $Q_2$ and $Q_3$ are low. At $t = t_1$, CLK$_1$ goes low and therefore the topmost edge detector generates a pulse. This pulse forces SR$_2$ and SR$_3$ to be set, thus making $Q_2$ and $Q_3$ high (which, consequently, makes $V_{G4}$ and $\Phi_1$ high, as needed). Once $Q_2$ and $Q_3$ are high, SR$_1$ and SR$_4$ are reset (because both inputs of the AND gates are now logic high), thus forcing $Q_1$ and $Q_4$ low (which makes $V_{G1}$ and $\Phi_2$ low). Before $Q_1$ and $Q_4$ become low, however, the output signals from SR$_2$ and SR$_3$ have to travel through the delay of an AND gate and a SR latch. This ensures that the transitions occur in the correct order.

At $t = t_2$, CLK$_2$ goes low and therefore the bottom edge detector generates a pulse. This pulse forces SR$_1$ and SR$_4$ to be set, thus making $Q_1$ and $Q_4$ high (hence making $V_{G1}$ and $\Phi_2$ high, as needed). Once $Q_1$ and $Q_4$ are high, SR$_2$ and SR$_3$ are reset (because both inputs of the AND gates are now logic high), thus forcing $Q_2$ and $Q_3$ low (which makes $V_{G4}$ and $\Phi_1$ low). As in the previous case, the delay through the AND gate and SR latch ensure correct transition order.

The final circuit diagram for the timing electronics is shown in Figure 3-15.
Figure 3-14: Transition control circuit and timing diagram.
Figure 3-15: Final design of timing electronics.
3.4 Signal Timing Considerations

The SR latches in the control electronics have precise timing requirements that must be met to ensure proper operation. As seen in Figure 3-15, the duration of the pulse generated by the edge detector must be sufficient to meet the hold time requirements of the SR latch. Secondly, the dead-time of the non-overlapping clock generator must be long enough to accommodate all the signal transitions that must take place.

Timing calculations were performed based on the propagation delay of an inverter made with transistors of the same size as those used in the digital blocks. At the time this work was developed, accurate SiOG™ device models did not exist, and therefore a modified SPICE model file for a 0.5 μm process was used. The simulations revealed an average propagation delay of 587.5 ps for such inverter. The delay through an AND gate, such as the one used in the transition control block, was found to be 2.054 ns (3.496 inverter delays). The delay between the S input and Q of the SR latch was 2.044 ns (3.479 inverter delays), and the delay between the R input and Q was 1.079 ns (1.834 inverter delays). Based on these figures, the pulse generated by the edge detector must have a duration longer than 8.809 inverter delays, as shown in Figure 3-16.
Since there is no upper limit on the duration of the clock pulse (other than half the period of the input clock), the edge detector was configured to produce a pulse approximately four times larger than the minimum pulse duration calculated earlier. Based on simulations of the edge detector circuit, the duration of the pulse was found to be 19.82 ns, or 33.7 inverter delays. This is roughly 3.83 times larger than the minimum calculated duration.

As stated in the beginning of this section, the dead-time between the clock pulses (i.e., the time during which both clocks are low) must be long enough to accommodate all of the required signal transitions. Figure 3-17 shows a pictorial representation of the delay paths involved in this calculation. Based on the delays for the level shifter and buffers found in simulation, signal transitions take a total of 20.91 inverter delays to complete. The non-overlapping clock generator was therefore designed to provide a dead-time of 40 inverter delays, to ensure correct operation.
Figure 3-17: Delay paths during one transition.
3.5 Device Characterization

As stated earlier, accurate device models for SiOG™ were not available at the time this work was realized. It was necessary, therefore, to gain an understanding of the electrical characteristics of circuit elements that are required in charge pumps, namely switches and capacitors. Several test structures were fabricated for this purpose, and the results obtained are outlined in this section.

3.5.1 Capacitors

The SiOG™ process offers two possible dielectric materials for capacitive structures: a 5000 Å field oxide for metal-insulator-metal (MIM) capacitors, and a 500 Å gate oxide for metal-oxide-semiconductor (MOS) capacitors. MOS stacks offer the highest capacitance per unit area, but their capacitance is affected by the bias voltage across the plates, and the frequency at which the capacitor is charged and discharged. This can be overcome by maintaining the capacitor in the accumulation region at all times during the operation of the charge pump. For an MOS capacitor with n-type contacts on a p-substrate, this translates to negative gate-body voltage bias. A 50 µm by 54 µm MOS capacitor of these characteristics was fabricated and tested, and exhibited a capacitance of 2.06 pF at -2 V bias (The C-V plot is shown in Figure 3-18). Assuming a 500 Å gate-oxide dielectric, an MOS stack of the above stated dimensions should exhibit a capacitance of 1.86 pF, which agrees with the reading obtained.
By extrapolating linearly from the above results, a 972 µm by 400 µm capacitor should exhibit 296.6 pF of capacitance. The C-V plot for such structure, shown in Figure 3-19, reveals that the added resistance of the substrate material and the contacts surrounding it limits the speed at which charge is moved into and out of the capacitor plates.

Figure 3-18: $C_{gb}$ vs. bias curve for a 50 µm x 54 µm MOS capacitor (1 MHz).

Figure 3-19: $C_{gb}$-V plot for 972 µm by 400 µm MOS capacitor.
By breaking up a large MOS capacitor into smaller unit cells, connected in parallel, the resistance of the plates can be reduced and thus the switching speed of the capacitor can be increased. Figure 3-20 shows the C-V plot for a capacitor made up of 144 unit cells, each with an area of 50 µm x 54 µm, with a frequency of 1 MHz. The results obtained indicate that a faster switching speed for the charge pump can be used as long as the capacitors are laid-out using smaller unit cells. Figure 3-21 shows the layout of such a capacitor.

![C-V plot for 144 unit-cell (50 µm by 54 µm) MOS capacitor at 1 MHz.](image)

**Figure 3-20:** C-V plot for 144 unit-cell (50 µm by 54 µm) MOS capacitor at 1 MHz.
The reduction in series resistance can be predicted by using a simplified 2D model of the silicon mesa that acts as the bottom plate of the capacitor. The bottom plate of the MOS capacitor is split into a grid of $N$ by $M$ smaller capacitors, each at a location $[x,y]$ in Figure 3-22. A computer algebra system was used to calculate the resistance of the three perpendicular paths from every grid location to the three surrounding metal contacts. The total resistance from a given point in the grid to the outside is then given by the parallel combination of all three resistance values. The resistance of the metal lines and contacts was ignored because the sheet resistance of the silicon mesa is significantly higher.
Figure 3-22 shows the contour plot for the resistance of a single unit cell capacitor (50 μm by 54 μm). As expected, the zones closes to the metal layer show the least resistance (blue), while the areas furthest away from it exhibit the highest resistance (dark red).

![Figure 3-22: 2D resistance model and resistance contour for silicon mesa.](image)

This model was intuitive and was preferred over a more elaborate 2-dimensional device model. The purpose of this analysis was to obtain a qualitative handle of the improvements offered by splitting the pump and filter capacitors into smaller units, and not specific series resistance measurements.

The results obtained show that for the 144 cell MOS capacitor from Figure 3-21, the maximum series resistance from any given point in the bottom plate is 1.4 kΩ. A single MOS capacitor of equivalent area shows 21.2 kΩ of maximum series resistance (the contour plot is shown in Figure 3-24). The improvement in series resistance is evident, and accounts for the difference in C-V curves obtained earlier.
3.5.2 Switches

Switches are instrumental for high-efficiency charge pumps. If the MOSFETs fabricated on SiOG™ technology exhibit high leakage currents, then accurate gate control will not realize the expected benefits in power efficiency or voltage ripple. Choosing the right geometry for the switches becomes important, because of the tradeoff associated with large drive strength and low reverse leakage. A high ON resistance also
reduces the power efficiency of the charge pump, one of the most important performance figures.

The rail switches, which connect the flying capacitor to the input voltage during the charge phase, are implemented using NMOS devices. During the charge cycle, when the NMOS switch is in the ON state, the drain sees the input voltage (5 V) while the gate is held at the doubled voltage (10 V). The source terminal, connected to the top plate of the flying capacitor, will see a voltage between 0 and 5 V. During the discharge cycle, the NMOS device must remain off, hence its gate is held at 0 while the source experiences voltages between 5 and 10 V.

Four different SiOG™ NMOS transistors, with a channel width of 24 µm and lengths of 6, 4, 3 and 2 µm, were subjected to conditions above specified, in order to measure ON resistance \( R_{on} \) and reverse leakage current \( I_{leak} \). Test schematics are shown in Figure 3-25, and the results obtained are shown in Figure 3-26 and Figure 3-27.

![NMOS Device Under Test (DUT)](image)

(a) Charge Phase          (b) Discharge Phase

Figure 3-25: Test schematics for NMOS switches.
The ON resistance data in Figure 3-26 shows that the switch resistance decreases for shorter channel lengths, as expected. The OFF state data shows that, under maximum stress conditions (a drain-source voltage of -5 V), the shortest device experiences 37.8 µA of leakage current. The difference with the longer channel length devices is substantial.
(2 or 3 orders of magnitude), and indicates the need for such long channel devices when implementing switches. An NMOS switch with channel length of 4 μm offers a fair balance of low ON resistance and low OFF leakage, plus it offers some protection against metal over-etching issues observed in processing.

The output switches, implemented using PMOS devices, connect the top plate of the flying capacitor to the output node. As in the NMOS case, leakage and drive strength are both important, but their operating conditions are different. During the discharge phase, when the transistor is ON, the voltage difference between the drain (connected to the flying capacitor) and source node will usually be small (except under heavily loaded conditions or during the time the charge pump is starting). When the transistor is OFF, its source still sees a voltage close to the doubled voltage (10 V), while the drain falls below 5 V. In order to minimize leakage between the output and the drain, a high OFF resistance switch is necessary. Figure 3-28 shows the test schematics for the discharge (a) and charge (b) phases outlined above.

![Diagram of PMOS switches](image)

**Figure 3-28:** Test schematics for PMOS switches
The ON resistance and OFF leakage data shown in Figure 3-29 and Figure 3-30 indicate that, as expected, the device with shortest length offers the least ON resistance and the largest OFF leakage. A PMOS switch with a channel length of 4 μm presents, therefore, the best combination between low ON resistance (below 2.5 kΩ for $V_{DS}$ under 2 V) and low OFF leakage (below 2.5 μA for $V_{DS}$ above -6 V).

![Figure 3-29: PMOS switch ON resistance, for different drain-source voltages.](image)

![Figure 3-30: PMOS switch leakage currents, for different drain-source voltages.](image)
3.6 Physical Layout

The complete layout for the charge pump is shown in Figure 3-31. To test the need for unit-cell based capacitors, an identical charge pump was laid out with large single-cell capacitors. The circuit in Figure 3-31 occupies an area of 2.89 mm².

In addition to the charge pump, the individual elements used in the timing circuitry were also laid out for testing. This helps verify that the individual charge pump components are functioning properly.

Figure 3-31: Charge pump layout.
4 Circuit Simulations and Results

4.1 Charge Pump Performance

In order to simulate the charge pump and timing electronics, a BSIM3 device parameter file was modified to approximate the data measured from test structures. The simulated charge pump had 100 pF pump capacitors, a 200 pF filter capacitor, and a 1 MHz input clock. Figure 4-1 shows the output of the simulated charge pump for a 100 µA load. The slight dent in the curve when the charge pump reached 6 V was attributed to the level shifters used in the circuit.

The simulation shows that the charge pump achieves a R.M.S. voltage of 9.29 V, with 46 mV ripple. Table 5 shows a summary of the charge pump performance under three different load conditions.

![Figure 4-1: Charge pump output.](image-url)
Table 5: Circuit simulation results for nested-clock charge pump.

<table>
<thead>
<tr>
<th></th>
<th>Unloaded</th>
<th>Light loading (50 µA)</th>
<th>Heavy loading (100 µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage ($V_{rms}$)</td>
<td>9.97</td>
<td>9.68</td>
<td>9.29</td>
</tr>
<tr>
<td>Ripple Voltage (mV)</td>
<td>7.73</td>
<td>23.7</td>
<td>46.4</td>
</tr>
<tr>
<td>Power Input (mW)</td>
<td>0.15</td>
<td>0.63</td>
<td>1.15</td>
</tr>
<tr>
<td>Power Output (mW)</td>
<td>0</td>
<td>0.48</td>
<td>0.93</td>
</tr>
<tr>
<td>Overall Power Efficiency (%)</td>
<td>NA</td>
<td>73.9</td>
<td>80.6</td>
</tr>
</tbody>
</table>

The power efficiency figure reported in Table 5 is defined as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\int V_{out} \times I_{load} \cdot dt}{\int (V_{in} \times I_{in} + V_{clk} \times I_{clk}) \cdot dt}$$

(4-1)

where $V_{out}$ is the voltage measured at the output node, $I_{load}$ is the load current, $V_{in}$ is the input voltage, $I_{in}$ is the input current, $V_{clk}$ is the input clock voltage, $I_{clk}$ is the input clock current and $T$ is input clock period. At first glance, the results reported in Table 5 show that the nested-clock charge pump exhibits ripple voltage and R.M.S. voltage figures in agreement to what was obtained in the proof-of-concept simulation of section 3.2 (the voltage ripple in the unloaded case is the exception, because the level shifters draw a certain current when in operation). The main discrepancy between Table 4 and Table 5 is power efficiency, since the latter incorporates into its calculation the power consumed by the timing electronics, and thus provides a more realistic estimate. In spite of this, the nested charge pump remains highly efficient across a wide range of load currents, as
shown in Figure 4-2. Under light-loading conditions, the efficiency of the charge pump drops because the load is drawing less power. The charge pump consumes 150 μW of power when unloaded.

![Graph showing power efficiency vs load current]

**Figure 4-2: Loading effects on power efficiency.**

Figure 4-3 shows the variations in ripple voltage and R.M.S. output voltage as a function of load current. A 20% change in load current about a nominal load of 100 μA produces a change in output voltage of only 1.5% (i.e., variation of 140 mV from 90 to 110 μA). Voltage ripple remains below 80 mV for loads up to 140 μA.
4.2 Timing Electronics

The correct operation of the timing electronics was verified by observing the gate signals for the charge and discharge cycles of the charge pump. Figure 4-4 shows the results for $V_{G4}$ (red, top), $\Phi_2$ (pink, center) and $V_{G3}$ (blue, bottom) during the charge cycle. Similarly for the discharge cycle, Figure 4-5 shows the results for $V_{G1}$ (blue, top), $\Phi_1$ (red, center) and $V_{G2}$ (green, bottom) during discharge cycle.
Figure 4-4: $V_{G4}$ (top), $\Phi_2$ (center) and $V_{G3}$ (bottom) during charge cycle.

Figure 4-5: $V_{G1}$ (top), $\Phi_1$ (center) and $V_{G2}$ (bottom) during discharge cycle.
4.3 Charge Pump Comparison

A comparison of this design with others reported in the literature is a complicated task because authors do not always report the same set of performance figures. In many instances, authors exclude certain important details, such as the nature of the capacitors used (external or internal), intended load, and power efficiency definition (efficiency of the pump or overall efficiency, including timing circuitry). In some cases, measured results are not available. Table 6 shows the results obtained from multiple charge pump circuits for small-format portable displays reported in the literature. Brief observations are included for each reviewed design, to clarify any important points.

<table>
<thead>
<tr>
<th>Power Efficiency (%)</th>
<th>Yeh(^1)(^2) [25]</th>
<th>Lin(^1)(^2) [21]</th>
<th>Yoo [19]</th>
<th>Ying [20]</th>
<th>This Work(^1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>79(^3)</td>
<td>80(^3)</td>
<td>67.8(^3)</td>
<td>65.3(^3)</td>
<td>75</td>
<td>54</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Input Voltage, (V_{in}) (V)</th>
<th>5</th>
<th>2.8</th>
<th>6</th>
<th>6</th>
<th>2.5</th>
<th>2.5</th>
<th>5</th>
</tr>
</thead>
</table>

| Output Voltage \((V_{rms})\) | 8.5 (1.7\(V_{in}\)) | 5.1 (1.8\(V_{in}\)) | 11.5 (1.9\(V_{in}\)) | 11.4 (1.9\(V_{in}\)) | 9.48 (3.8\(V_{in}\)) | 9.06 (3.6\(V_{in}\)) | 9.29 (1.9\(V_{in}\)) |

<table>
<thead>
<tr>
<th>Ripple Voltage (mV)</th>
<th>N.A.</th>
<th>N.A.</th>
<th>123</th>
<th>135</th>
<th>4(^4)</th>
<th>10(^4)</th>
<th>46</th>
</tr>
</thead>
</table>

| Load Current (μA) | N.A. | < 30 | 100 | 100 | 100 | 100 | 100 |

| Fabrication Technology | LTPS | LTPS | LTPS | LTPS | CMOS | CMOS | SiOG |

**Notes:**
1. Simulated results.
2. No information about capacitors (internal/external).
3. Efficiency calculation does not take into account clock generation.
4. 4X charge pump with output regulator and external capacitors.
As seen in Table 6, the charge pump reported in this work compares favorably to the other reported designs. The power efficiency improvements obtained by using a nested clocking scheme are apparent, as the overall efficiency of the circuit (80.6%) is notable higher. Only two charge pumps [21, 32] in the table have efficiency figures in the vicinity of 80%, but their overall efficiency (which includes the power consumed by the clock generators) is expected to be lower. If the power consumption of the timing electronics is ignored, this figure reaches 94.2%.

The circuit presented could be implemented using LTPS fabrication technology, but the low carrier mobilities would reduce the maximum switching frequency of the charge pump (since a larger switch resistance increases the time needed for the pump capacitors to charge). A lower frequency of operation extends the rise time of the charge pump output and limits the maximum current that the charge pump can deliver. In order to deliver the same amount of current, several pumps would have to operate in parallel, thus increasing circuit footprint.

With respect to voltage ripple, the charge pump presented exhibits the lowest figure among those circuits without a voltage regulator at the output. The charge pump by Ying [20] achieved very low ripple figures by adding a regulator at the output, but this affected its power efficiency substantially. The nested charge pump offers low output ripple without the use of a regulator.
5 Conclusions and Future Work

This work focuses on improving the power efficiency, drive strength, and output noise (ripple) figures of a charge pump, by means of carefully controlling the device switching sequence. The performance attributes of SiOG™ (CMOS structures, high switching speeds, low parasitic capacitances, effective electrical isolation between individual devices) were used to develop clocking circuits for the signals needed to activate the charge pump switches in the correct sequence.

The tradeoff between performance and circuit simplicity limits the possibility of developing highly-efficient, fully integrated DC-DC converters on glass. The benefits offered by SiOG™ technology, however, allow the fabrication of relatively complex circuits that perform adequately for the purpose of controlling charge pump switches. As a result, the power efficiency, ripple voltage and drive strength improvements outweigh the drawbacks of implementing the gate control scheme outlined in this text. This project also shows the potential of SiOG™ for implementing more sophisticated digital electronics, such as timing interfaces and DACs, in the future.

The adoption of a nested clock timing scheme successfully eliminated those conditions where charge was being lost, and hence helped increase the power efficiency of the overall circuit. Since SiOG™ is still under development, certain approximations had to be made to obtain a reasonable circuit model that could predict the behavior of the circuit during operation. A careful analysis of the timing requirements of the control electronics was performed to minimize the possibility of design-level defects and thus
reduce the number of process runs before obtaining a charge pump with the expected performance. The simulation results disclosed here need to be compared to the measurements taken from the SiOG™ wafers to corroborate the expected improvements in performance. Discrepancies between the two could mainly be attributed to the process-to-process variations (since SiOG™ is still an ongoing project), and to the absence of circuit models that adequately predict the performance of the devices obtained. As a first step, a SiOG™ wafer with various test structures needed in charge pumps was successfully measured, and the results were used to provide better insight on the design considerations.

Based on the simulation results, the nested-clock charge pump exhibits significant improvements over designs implemented using both LTPS (on glass) and CMOS (bulk).

5.1 Future Improvements

One advantage of the timing circuit implementation is that it uses a single pulse train to generate all other signals. The frequency of the gate control signals depends on the frequency of the input clock, thus allowing the addition of a voltage-to-frequency circuit to vary the clock frequency according to loading demands. Power efficiency is uniformly high from medium to heavy loads, however it drops off as the charge pump becomes unloaded. By slowing down the input clock during low-load conditions, power efficiency can be increased, thus improving the performance of the pump with respect to other designs.
A second area of improvement is the capacitive structure used in the circuit. In a charge pump, capacitors occupy large areas because of the low relative permittivity of silicon dioxide, even as gate oxides become thinner. By utilizing a high-k dielectric material compatible with the display manufacturing process, the area of the circuit could be reduced drastically. A research project is currently underway to investigate the use of either hafnium oxide or tantalum oxide for this purpose. Such capacitors could use the aluminum and molybdenum interconnect layers as plates, thus steering away from the C-V dependency of MOS capacitors and the need to use unit-cell capacitors to minimize their series resistance.
6 References


7 Appendix

7.1 Test chip schematics

Figure 7-1: Level shifter schematic diagram.
Figure 7-2: Edge detector schematic diagram.
Figure 7-3: Non-overlapping clock generator schematic diagram.
Figure 7-4: Transition control circuit schematic diagram.
Figure 7-5: Nested-clock charge pump top-level schematic diagram.