An Ultra Low Power Digital to Analog Converter Optimized for Small Format LCD Applications

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An Ultra Low Power Digital to Analog Converter Optimized for Small Format LCD Applications

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Abstract

Liquid crystal displays (LCDs) for mobile applications present a unique design challenge. These “small format” displays can be found primarily in cell phones and PDAs which are devices that have particularly stringent power requirements. At the same time, the displays are increasing in resolution with every generation. This is creating demand for new LCD display technologies. The predominant amorphous thin film transistor technology is no longer feasible in the new high resolution small format screens due to the fact that the displays require too many connections to the driver and the aperture ratios do not allow high density displays.

New technologies such as low temperature polysilicon (LTPS) displays continue to shrink in size and increase in resolution. LTPS technology enables the display manufacturer to create relatively high quality transistors on the glass. This allows for a display architecture which integrates the gate driver on the glass. Newer LTPS LCDs also enable a high level of multiplexing the sources lines on the glass which allows for a much simpler connection to the display driver chip.

The electronic drivers for these display applications must adhere to strict power and area budgets. This work describes a low-power, area efficient, scalable, digital-to-analog conversion (DAC) integrated circuit architecture optimized for driving small format LCDs. The display driver is based on a twelve channel, 9-bit DAC driver. This architecture, suitable for ¼ VGA resolution displays, exhibited a 2 MSPS conversion rate, less than 300 μW power dissipation per channel using a 5 V supply, and a die area of 0.042 mm² per DAC. A new performance standard is set for DAC display drivers in joules per bit areal density.
Table of Contents

Acknowledgements iii
Abstract iv
Table of Contents v
List of Figures vi
List of Tables viii
List of Publications and Patents ix

Chapter 1: Introduction 1
1.1 Liquid Crystal Material Properties 2
1.2 Liquid Crystal Displays 4
  1.2.1 Amorphous Silicon Active Matrix Displays (AMLCD) 6
  1.2.2 Low Temperature Polysilicon (LTPS) Displays 8
  1.2.3 High Multiplex Ratio LTPS Displays 10
1.3 Source Driver Proposed Solution 13
  1.3.1 Performance Requirements 13
  1.3.2 Final Specifications 15
1.4 Literature Search: DAC Architectures for Use as Display Source Drivers 16

Chapter 2: Source Driver Architecture 19
2.1 DAC Architecture 20
2.2 Self Refresh Buffer Method 26
2.3 Multiplexer Architecture 28
2.4 Operational Amplifier Architecture 33
  2.4.1 Basic Operational Amplifier Architecture 34
  2.4.2 Slew Rate Enhancement 39
2.5 DAC Simulation Results 46
2.6 Physical Implementation 50

Chapter 3: Experimental Results 53
3.1 DAC Measurements and Results 55
3.2 Operational Amplifier Buffer Measurements and Results 58
3.3 DAC Performance Summary and Comparisons 60

Chapter 4: Conclusions and Future Work 63
4.1 Improvements to this Work 64
4.2 Future Work 64

References 66

Appendix 68
Output Buffer Offset Calculation 68
2006 ISSCC Paper 72
Test Chip Schematics 76
### List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>No electric field applied to LC [1].</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>Electric field applied to LC [1].</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>LC transmissivity versus voltage [1].</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>Simplified LCD system diagram.</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>Typical amorphous silicon LCD architecture.</td>
<td>7</td>
</tr>
<tr>
<td>6</td>
<td>Typical LTPS LCD architecture.</td>
<td>9</td>
</tr>
<tr>
<td>7</td>
<td>Possible high multiplex ratio LTPS LCD architecture.</td>
<td>11</td>
</tr>
<tr>
<td>8</td>
<td>Checkerboard LCD pattern.</td>
<td>12</td>
</tr>
<tr>
<td>9</td>
<td>Typical high multiplex ratio LTPS timing diagram.</td>
<td>12</td>
</tr>
<tr>
<td>10</td>
<td>Panel parasitics along signal path.</td>
<td>14</td>
</tr>
<tr>
<td>11</td>
<td>DAC architecture.</td>
<td>20</td>
</tr>
<tr>
<td>12</td>
<td>Basic structure of DAC reference circuit.</td>
<td>21</td>
</tr>
<tr>
<td>13</td>
<td>Impedance looking into R-String.</td>
<td>22</td>
</tr>
<tr>
<td>14</td>
<td>Power versus load capacitance and number of folds.</td>
<td>25</td>
</tr>
<tr>
<td>15</td>
<td>Sample and hold from reference [13].</td>
<td>26</td>
</tr>
<tr>
<td>16</td>
<td>Refresh timing diagram.</td>
<td>27</td>
</tr>
<tr>
<td>17</td>
<td>Conventional multiplexers, full decode on left and tree decode on right [8].</td>
<td>28</td>
</tr>
<tr>
<td>18</td>
<td>Folded R-string multiplexer (diagram from [8]).</td>
<td>29</td>
</tr>
<tr>
<td>19</td>
<td>Three dimensional 6-bit analog multiplexer (modified 2D diagram from [8]).</td>
<td>30</td>
</tr>
<tr>
<td>20</td>
<td>Circuit for approximating $V_{out}$ settling time.</td>
<td>33</td>
</tr>
<tr>
<td>21</td>
<td>Buffer amplifier with folded cascode 1\textsuperscript{st} stage and class AB output stage.</td>
<td>35</td>
</tr>
<tr>
<td>22</td>
<td>Block diagram of bias boost method.</td>
<td>40</td>
</tr>
</tbody>
</table>
Figure 23: Block diagram of the load boost technique.

Figure 24: Operational amplifier with a slew rate enhancement circuit.

Figure 25: Slew detect circuit.

Figure 26: Complete operational amplifier with a slew rate enhancement circuit

Figure 27: Top level test bench.

Figure 28: DAC settling from step 64 to step 448.

Figure 29: Output buffer DC simulation results.

Figure 30: SRE simulation results.

Figure 31: DAC layout.

Figure 32: Die photo.

Figure 33: Block diagram of test setup.

Figure 34: Digital signals before (left) and after (right) series resistors.

Figure 35: DAC linearity results

Figure 36: INL of the reference resistor.

Figure 37: DAC performance with and without self refresh.

Figure 38: SRE amplifier (red) vs. non-SRE amplifier (yellow)

Figure 39: Output buffer offset versus input voltage.

Figure 40: DAC figure of merit comparison.

Figure 41: Output buffer offset contributors.

Figure 42: Output buffer Monte Carlo simulation results.
List of Tables

Table 1: Sample LCD transmissivity curve. 5
Table 2: DAC architectural comparisons. 16
Table 3: Architecture comparisons of several 9-bit multiplexers. 31
Table 4: Output buffer offset results. 59
Table 5: DAC performance metrics. 61
Table 6: Output buffer offset summary. 70
List of Publications and Patents

   Accepted for presentation (See Appendix)

2. Patent applied for “Ultra Low Power Scalable DAC Architecture”

3. Patent applied for “Slew Rate Enhancement for Two Stage Amplifiers”
Chapter 1: Introduction

Portable electronic devices pose a challenge because they require displays that are small in size, relatively high in resolution and low in power dissipation. The electronics that drive small format displays must also occupy a small footprint, operate at low power and minimize external component count. The ideal display driver needs to be flexible because a large number of different types of liquid crystal materials exist with different drive requirements. A relatively high resolution data converter is necessary to drive the liquid crystals with adequate resolution since displays are highly non-linear. As the displays industry continuously improves upon its technology, reuse of intellectual property (IP) is essential for fast time to market. The ideal display driver architecture should be easily expandable in the number of outputs and resolution to accommodate displays as they become larger with higher resolution. A final limitation on the display driver is business related. Due to the extreme price pressure on display modules, the display driver is limited to a basic CMOS process technology. A basic CMOS process does not contain low threshold voltage transistors, high sheet resistance poly resistors, or poly to poly capacitors. Integrated display drivers must be designed around these limitations.

This thesis will examine and develop electronic circuits for driving small format LCD technology commonly found in portable devices. Display technologies of at least ¼ VGA resolution (320 x 240 pixels) are considered. Several technologies are being employed to create displays of this resolution. This thesis will examine and develop a display driver for the latest generation of LCD technology currently in production.

This work is organized in the following manner: The remainder of this chapter will introduce the operating characteristics of liquid crystal technology and the architectures of LCDs. The source driver architecture developed in this work will be described in detail in
Chapter 2, including circuit design, simulation and physical implementation. Chapter 3 contains the experimental results with respect to the DAC design and the output buffer design. Chapter 4 draws conclusions from the work and offers suggestions on future work and enhancements to the DAC and testing environment. The last two sections contain the references and appendix.

1.1 Liquid Crystal Material Properties

Liquid crystals (LCs) are molecules which, under the influence of an electric field, align according to the field polarity. Liquid crystals are a type of dielectric where local regions polarize in an electric field as shown in Figure 1 and Figure 2. Birefringence is the property that enables the LC to twist light as it passes through it. The birefringence of the LC material is independent of the polarity of the voltage applied; it depends only on the RMS value of the voltage applied. Polarizers are placed above and below the LC. Light is passed through the polarizers and the LC. The polarizers are arranged such that they are at a 90 degree angle to each other. When the LC is unenergized, it rotates the light passing through such that its direction matches that of the top polarizer, letting all the light through. When a voltage is applied, light is unaffected while it passes through the LC and the two polarizers block all light.
Crossed polarizers 45 degrees to the director (Normally White)

Without rotation, light is blocked by crossed polarizers

LC retardation provides 90 deg rotation, unenergized

No LC retardation results in no rotation, when energized

Figure 1: No electric field applied to LC [1].

Figure 2: Electric field applied to LC [1].

When driving an LCD, DC voltages are not used. A DC voltage on a liquid crystal can cause electroplating of ion impurities on the electrodes. This electroplating is the major cause of image retention. To avoid this condition the LC needs to be driven with negative and positive voltages to ensure the average voltage on a liquid crystal is equal to zero. The RMS level of the voltage applied will determine the transmissivity. Shown in Figure 3 is a graph of an LC’s transmissivity versus the applied voltage.

Figure 3: LC transmissivity versus voltage [1].

It can be seen from Figure 3 that the LC’s response to voltage is extremely non-linear. This voltage to transmissivity relationship is often referred to as the gamma curve. It can also be
seen that the LC material has the same transmissivity whether the voltage applied to it is positive or negative, however this is not necessarily always the case.

Taking linear steps in transmissivity, it can be seen that some steps in transmissivity near the center of the range require small steps in voltage while the steps in transmissivity near the ends require larger steps in voltage. A digital to analog converter, which is designed to drive an LC, must be able to resolve the small voltage steps required near the center of the transmissivity curve. The slope of the tangent near this area will determine the resolution required by the converter.

1.2 Liquid Crystal Displays

The LCD technology discussed in this paper pertains to the architectures most commonly found in portable electronic devices. To create an amorphous silicon display, liquid crystal cells are arranged in a matrix to create an image. Pixels are arranged in columns and rows. A pixel contains three cells (also called subpixels), one to display each of the three primary colors - red, green and blue. To illuminate a display, white light (usually using a white LED) is shown through the display. Cells can output different colors since a red, green or blue film is deposited onto each cell in a pixel to filter the white light. Active matrix LCDs have transistors integrated on the glass to perform the row select.

![Figure 4: Simplified LCD system diagram.](image)
The system processor in Figure 4 sends video commands or image data to the display driver. The display driver drives the analog voltages onto the LCD, which will create the images. The system processor expects a linear relationship between the video data and the brightness on the display. Therefore, the display driver must create a nonlinear digital to analog conversion to obtain the linear response in transmissivity that is required. This is typically referred to as gamma correction.

A typical LC material can only resolve approximately 64 steps in brightness, therefore 6 bits are used for each color (red, green and blue) for a total of 18 bits. There are two ways to perform the digital to analog conversion (DAC). The first is to use a nonlinear DAC with 6 bits of resolution which mimics the inverse of the response curve. The second is to use a high resolution DAC (approximately 8 to 10 bits) and a look up table (LUT) to create the inverse response curve. The LUT approach is the more flexible of the two options and easily accommodates varying liquid crystal responses. To determine the resolution needed for a linear DAC, the transmissivity of the LCD needs to be examined. A sample transmissivity curve is shown in Table 1 [1].

Table 1: Sample LCD transmissivity curve.
It can be seen in Table 1 that the minimum step is 18.1 mV, which corresponds to 277 steps over the entire 5 V range. The resolution of 277 steps across the voltage range implies that a 9-bit converter is necessary.

1.2.1 Amorphous Silicon Active Matrix Displays (AMLCD)

Amorphous silicon (or active matrix) LCDs are currently the most common because large sheets of it are easily and cheaply manufactured. Silicon is deposited on the glass, but it ends up only in an amorphous state because the glass cannot withstand the temperatures required for
annealing. These transistors are too slow to form logic and other complex circuits because their charge carrier mobility is so low. Fortunately, transistors fast enough to switch a pixel in and out can still be created. Figure 5 is a diagram of an LCD system.

![Figure 5: Typical amorphous silicon LCD architecture.](image)

As shown in Figure 5, LCDs require many connections to the row and column drivers. The most common display driver configuration attaches the silicon driver circuits directly to the glass using a "flip-chip" technique. Both the source driver and the gate driver are connected directly to the glass. The required components and system controller are connected to the glass using a flexible circuit board.

It can be seen in Figure 5 that the gate driver selects an entire row of pixels at a time. The gate driver steps the control signal through all the lines in succession down through the display. The LC cell is represented by the capacitor attached to the pass transistor. When a pixel
(one site across the line) is selected, its transistor connects the LC site to the associated column line. Then the source driver applies the appropriate voltage onto the pixel. The other terminal of the LC cells (basically a capacitor) are all connected to a common backplane. The backplane is commonly referred to as $V_{\text{COM}}$, the common voltage. To avoid electroplating as mentioned in Section 1.1, a driver voltage signal needs to be applied to the LC, where the time average value for successive write patterns is zero volts (no dc content). Each pixel will be driven with a positive voltage during one write and with a negative voltage during the successive write. Driving a positive voltage is done by applying 0 V to the common plate and driving 0 – 5 V onto the column lines. Raising the common plate voltage to approximately 5 V and then applying a voltage range of 0 – 5 V on the columns achieves a negative voltage on the LC without any negative voltages in the display driver subsystem. This enables simpler and cheaper process technology to be used in the manufacturing of the source driver.

Amorphous silicon displays typically require much higher drive voltages than provided by standard CMOS integrated circuit processes. The pass transistors typically need to be driven to +15 V to turn the transistors on and need to be driven to –10 V to turn them fully off. Connection configurations become more complex as the display resolution increases. A quarter VGA display (320x240) would require 960 connections by the source driver IC and 320 connections by the gate driver IC. This connection arrangement is not feasible for higher resolution small format displays due to pad number limitations and the space on the LCD required to route drive signals.

1.2.2 Low Temperature Polysilicon (LTPS) Displays

In LTPS displays, the thin layer of amorphous silicon is heated up to create polysilicon. An excimer laser is used to locally heat up the silicon, while keeping the display temperature
under the 450 °C glass limit. The annealed silicon has a charge carrier mobility which can reach up to 90% of the mobility of traditional silicon [2]. In addition, the annealing process enables CMOS devices to be fabricated directly on the glass. This technology allows for a wide array of circuits to be integrated on the display surface, including most of the gate driver. Therefore, only one external chip is required to drive the LTPS LCD. Figure 6 shows a typical LTPS architecture.

![Figure 6: Typical LTPS LCD architecture.](image)

In this LTPS architecture, the gate driver is integrated onto the glass. The gate driver is a simple register chain which passes a token down through the chain at the line rate. This will select one line and turn the rest off. The LTPS architecture saves one entire piece of silicon – the
gate driver. Another benefit of LTPS LCD displays is the reduced voltage requirement to drive the LCD, making it possible to use a cheaper or more advanced process. The final benefit is the ability to use a three to one multiplexer for every column. This reduces the number of connections to the glass required by the source driver to one third of what is required by the amorphous LCD displays. Unfortunately, this also requires the column driver to be three times as fast since three groups of sub-pixels must be driven during every line.

1.2.3 High Multiplex Ratio LTPS Displays

High multiplex ratio LTPS displays promise an even higher level of integration. This process, pioneered by the Sharp Corporation, creates transistors which are about 600 times faster than amorphous polysilicon based devices and approximately three times faster than LTPS [3]. Refinements in LTPS technology allow for an even higher level of multiplexing, which allows for an architecture with even fewer connections to the LCD due to better transistors and reduced parasitics on the glass. The use of better transistors enables the LCD makers to create smaller and higher resolution displays.
In the high multiplex ratio LTPS LCD architecture, the connections to the glass have been reduced to approximately a few dozen. Signals that are needed include the power supply, control signals for the gate driver/multiplexer function and the analog outputs. One advantage of the high multiplex ratio LTPS architecture is that it is now possible to attach the source driver to the LCD using a flexible circuit board. By not having to mount the chip on the glass, glass area can be saved resulting in more LCDs per manufacturing sheet and a smaller bezel area. In Figure 7 only one set of red, green and blue (RGB) cells is connected to the glass to simplify the figure. In actual high multiplex ratio LTPS displays, there can be four or more sets of RGB lines multiplexed on the glass to decrease the speed requirements of the DAC in the source driver.
Figure 8 is an example of a checker board pattern to be used on the display. This keeps RGB voltage the same within a pixel, but voltages will be continuously toggling both in the horizontal and vertical directions on a pixel by pixel basis.

The example employs line inversion to keep the DC voltage on the pixels equal to zero. Positive voltages will be driven onto the pixels on one line (when $V_{COM}$ is low), then negative voltages are driven onto the display on the next line (when $V_{COM}$ is high). The type of glass used in this example is “normally black,” which means that the LCD does not let light through when the LC is not energized. Figure 9 is a sample diagram showing operation of a generic CGS LCD with the checkerboard pattern.
In Figure 9 there is a negative voltage on the first white pixel on the first line (line 0) and there is a positive voltage on the second pixel (also white) on the second line (line 1). Both pixels display white, but the second pixel's voltage is the opposite of the first pixel's voltage.

1.3 Source Driver Proposed Solution

For this work, high multiplex ratio LTPS LCDs, the most challenging current display technology, will be considered as the design target. CGS displays require by far the fastest DACs due to the high multiplexer ratio on the glass. High speed DACs which can drive a non-trivial capacitative load are high power. This work will seek to identify the architecture best suited to meet the needs of high multiplex ratio LTPS LCDs and then to minimize the power consumption of the DAC architecture.

1.3.1 Performance Requirements

The speed of the DAC required to drive a state of the art high multiplex ratio LTPS display will be calculated in this section. It will be assumed that the display has four sets of RGB lines multiplexed on the glass, with a display size of 320 by 240 (quarter VGA), and a refresh rate of 60 frames per second. The line rate and available pixel time can be calculated to help estimate the expected required performance of the DAC source drivers. Traditional LCD technologies such as amorphous silicon, have the source driver connected to the short side of the glass to minimize connections. Due to the high level of multiplexing achievable, the long side of the LCD can be driven to minimize the column line parasitics. The line rate is given by,

\[
line\_rate = \frac{1}{f_{\text{rate}} \times N_{\text{lines}}} = \frac{1}{60 \cdot 240} = 69.4\mu\text{s}
\]

where \( f_{\text{rate}} \) is the frame rate (update rate) and \( N_{\text{lines}} \) is the number of lines in the display. Because we are driving the long side of the LCD, the multiplexer ratio is 80 to 1, which results in:
pixel time = \frac{T_{\text{line}}}{N_{\text{mux}}} = \frac{69.4 \mu s}{80} \approx 870\text{ns} \tag{2}

where $T_{\text{line}}$ is the line time and $N_{\text{mux}}$ is the multiplexing factor. The multiplexing factor is simply the total number of column lines on the display divided by the number of column lines driven by the source driver, which in the case of the above example is four. In the actual display system, the line time may be shorter than (1). Typical video signals include horizontal and vertical blanking time which will reduce the pixel time calculated in (2).

Taking the parasitics along the column line and the sub-pixel switch resistance into consideration, there is some additional settling time required before the multiplexer can switch to the next column to make sure the LC voltage has settled. Figure 10 is a simplified $R$-$C$ load which describes the panel parasitics.

![Figure 10: Panel parasitics along signal path.](image)

The dotted line signifies the partition of the chip and the LCD. Column line resistance and capacitance are the major contributors to delay. Here it is broken down into a three $R$-$C$ network to better simulate the actual load which looks much like a transmission line.

Because of these parasitics, there is a trade off between the number of columns multiplexed on the glass and the source driver’s power. There is also an intrinsic limitation due to panel settling time. For example, the settling time to charge the pixel furthest away from the source driver might take 200 ns. Therefore, only having one set of columns on the glass is
impractical due to the fact that the source driver’s outputs would have almost no time at all to settle. This is the reason a typical high multiplex ratio LTPS LCD will have four sets of RGB columns multiplexed for a total of 12 analog drivers. Due to the $R-C$ delay, approximately one third to one half of the total pixel settling time should be used as the settling time requirement for the DAC. A settling time of approximately 400 ns which results in a conversion rate of 2.5 MHz, is a reasonable conservative specification.

### 1.3.2 Final Specifications

- 9 bit resolution
- 12 Channels
- 1 LSB matching between channels
- 400 ns conversion rate (2 MSPS)
- 100 pF load
- 50 µA power consumption per channel (250 µW at 5V supply)

The 100 pF load requirement is an estimation, since actual panel parasitics are not available. Typical column line capacitances in an amorphous LCD panel are approximately 20 to 40 pF. The second major contributor to parasitic capacitance is the multiplexer bus, which has a parasitic capacitance to the panel in addition to the parasitic capacitance of approximately 60 switches connected to it that can add up to 20 pF. Finally, the flex connector from the panel to the driver IC can also exhibit about 10 pF of capacitance. The final total adds up to approximately 70 pF, which is increased to 100 pF to allow for errors in the estimations and robustness in the circuit.
1.4 Literature Search: DAC Architectures for Use as Display Source Drivers

An extensive literature search was conducted to determine the optimal converter architecture taking into consideration the many requirements and restrictions of driving CGS LCD displays. Table 2 contains a summary of DAC architecture comparisons found in literature that might be suitable candidates. DACs were evaluated with the following criteria: power, area, channel to channel matching, speed and resolution.

Table 2: DAC architectural comparisons.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Pros</th>
<th>Cons</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclic (Algorithmic)</td>
<td>easy to get resolution, auto calibration possible, compact</td>
<td>might be too high power due to need to run at high speed</td>
<td>[4,5,6]</td>
</tr>
<tr>
<td>Pipelined</td>
<td>high speed, easy to modify resolution</td>
<td>high power, possibly high area</td>
<td>[8,10]</td>
</tr>
<tr>
<td>Sigma Delta</td>
<td>simple circuit, architecture small area potentially low power at our resolution</td>
<td>potentially high power due to over-sampling rate</td>
<td>[8,11]</td>
</tr>
<tr>
<td>R-String</td>
<td>low power, simple</td>
<td>might be too slow</td>
<td>[4,12]</td>
</tr>
<tr>
<td>R-2R</td>
<td>low power, simple</td>
<td>might be too slow, possible matching issues</td>
<td>[8]</td>
</tr>
<tr>
<td>R-C Hybrid</td>
<td>low power</td>
<td>Possibly too much area due to many components, might be too slow</td>
<td>[8,9]</td>
</tr>
</tbody>
</table>

The first architecture that was considered was the cyclic DAC. The cyclic DAC is compact because it can be built using two capacitors and an amplifier. The cyclic DAC also has the potential to be low power because of the low component count. Channel to channel matching has the potential to be excellent because offset nulling can be performed during the conversion cycles. The downside to the cyclic DAC is that the number of conversion cycles is proportional to the resolution of the converter. The conversion rate is multiplied by the
resolution to determine the final clock frequency. This inflated clock frequency puts a heavy settling time requirement on the operational amplifier and results in high power.

The second converter considered was the pipelined architecture. This architecture is similar to the cyclic architecture, but each conversion cycle is handled by a unique sample and hold stage in the converter. The pipelined architecture solves the speed problem, but power is still a concern since each stage requires an operational amplifier. This requirement also creates other problems including the fact that the converter will be large and it must be completely duplicated to create multiple channels.

The next converter considered was the sigma delta converter. This converter is potentially simple and can be mostly implemented in digital logic. The DAC conversion rate requirement of 2.5 MSPS is very high for a sigma delta converter and could result in a very high speed system clock depending on the over sampling rate. This architecture does not lend itself to multiple channels and channel to channel matching, because the entire converter has to be replicated. Also, a buffer amplifier would still have to be used.

The resistor string (R-String) or voltage divider architecture is the simplest of the options. Its strengths include good channel to channel matching due to a common reference and small area. It is a simple DAC with minimal logic required and only one buffer amplifier per output. The main concern about the architecture is the need for a low impedance R-String to meet high conversion rate requirements or multi channel requirements. This can significantly increase the power consumption.

The next DAC considered is the R-2R. This DAC is very compact, but it must be completely duplicated to support multiple channels. The concern of channel to channel matching
is raised because the reference is not shared as in the R-String DAC. In addition, due to the fact that each channel has its own R-String, the quiescent power will increase.

The last DAC on the list is the R-C hybrid DAC which is a combination of an R-String DAC and a binary weighted switched capacitor DAC. As a switched capacitor DAC, it offers offset canceling to null the buffer amplifier’s offset. Also aiding the channel to channel matching is the fact that all channels can operate from the same R-String as a common reference. The main downside of this architecture is the necessity for many capacitors, depending on how the reference voltages are split up. The capacitors have to be duplicated for each channel, therefore they will put a large capacitative load on the reference R-String and will take up a large amount of area.

The decision was made to use the R-String DAC architecture. This work will focus to improve the three major areas of deficiency in this architecture. The first area of concern is the output impedance of the reference R-String which needs to drive all of the channels. The solution presented here is a systematic method to buffer the reference R-String to minimize power consumption while still meeting the settling time requirements. The second area of concern is the multiplexer. Due to the moderate resolution required, the multiplexers will be large and they will contribute a considerable amount of parasitics. A new multiplexer is developed in this work to minimize the effects of parasitics and to be as area efficient as possible. The final area for optimization is found in the operational amplifier. The output buffer is the main source of power consumption in the DAC, therefore work needed to be done to reduce the bias current consumption of the operational amplifier.
Chapter 2: Source Driver Architecture

This chapter will detail the development of the source driver architecture. As outlined in the literature review, there are three major areas for improvement over previous data converters based on this architecture. Two major time constants limit performance in resistor string DACs. The first time constant consists of the reference resistor string and the parasitic capacitances that must be driven. The second time constant consists of the multiplexer parasitic resistances and capacitances. The final area for improvement is to reduce the power consumption of the output buffer.

Each of these three areas will be considered and optimized independently. The final design simulation results are shown for the entire DAC. The new DAC architecture will be compared and contrasted to the conventional architecture to emphasize the benefits of the improvements developed in this work.
2.1 DAC Architecture

![Diagram of DAC Architecture]

Figure 11: DAC architecture.

The DAC architecture utilized in this design is based on a simple resistor divider voltage reference. Reference voltages are selected from the reference resistor string through a multiplexer. The reference voltage is buffered so that a large load can be driven with the digital to analog converter’s output. There can be $M$ unique and independent DACs created from the single voltage reference. The advantages of this architecture include its inherent low power, easy scalability to $M$ channels, built-in gamma correction using non-uniform value divider resistors, and reduction of DAC channel matching to within the offset for two amplifiers.

To minimize the power dissipation of the classical resistor voltage divider reference, the composite string resistance, $R$, is made relatively high. However, a large R-String impedance compromises settling time. A method to reduce the driving point impedance of the resistor string is to buffer the resistor string at binary fold points (Figure 11). Each time a buffer is added to a
fold point, the worst case impedance, seen looking into the resistor string, will be cut in half. For example, dividing the string into four equal segments requires three buffers and reduces the driving source impedance from R/4 (in the case of a single fold) to R/16 (Figure 12). The load is comprised of the parasitic capacitances of routing, multiplexer devices, and the input capacitance of the operational amplifier.

![Diagram](image)

**Figure 12: Basic structure of DAC reference circuit.**

Shown in Figure 12 is a reference circuit which has a buffered R-String architecture. Each time a fold is created, a buffer is inserted at the center point of the unit resistors, $R_U$. The point in a resistor string with the highest effective impedance is the center point between two buffers or a buffer and a supply rail. Therefore, it is logical to place the buffer at this center point to reduce the impedance. The number of segmented or unit resistors is equal to $2^F$, where $F$ is the number of folds and the total number of amplifiers is $2^F - 1$. $R_S$ is the total series resistance of the multiplexer from Figure 11. To ensure adequate settling time, a general expression for minimizing power and achieving settling time will be derived. The total system power is:
\[ P_{\text{tot}} = P_{\text{buf}} + P_{\text{res}} \]  

The power dissipated in the composite resistor, \( R \), is:

\[ P_{\text{res}} = \frac{V^2}{R} \]  

The buffer power is:

\[ P_{\text{buf}} = V \cdot I_b \cdot (2^F - 1) \]  

\( I_b \) is the buffer amplifier bias current consumption. It is important to include this in the power calculations since buffer power will have an effect on how many folds are used. Finally, the total reference power is equal to the power dissipated in the resistor and the amplifiers.

\[ P_{\text{tot}} = \frac{V^2}{R} + V \cdot I_b \cdot (2^F - 1) \]  

The next step is to calculate the worst case settling associated with driving the load capacitor. Figure 13 is a more detailed diagram of the highest impedance point on the R-String.

![Diagram of R-String](image)

**Figure 13: Impedance looking into R-String.**

The worst case output impedance is naturally the center point of the unit resistor between two buffer amplifiers. This is because the buffer amplifiers have a much higher output
impedance than the power supplies. Therefore, the worst case impedance will not be found on
the upper or lower unit resistors. The expression for \( Z_{IN} \) is found to be:

\[
Z_{IN} = \frac{r_o + \frac{R_U}{2}}{2} = \frac{r_o}{2} + \frac{R_U}{4}
\]  

(7)

Referring to Figure 12, the time constant is seen to be

\[
\tau = (Z_{IN} + R_{SW}) \cdot C_{INT}
\]  

(8)

\( \tau \) is specified by considering the settling time requirement. For a 9-bit DAC, a total settling time
of \( 6\tau \) is required to settle to an accuracy of one least significant bit (LSB). Settling time must
also be allotted to the output buffer. Once the maximum settling time for the reference is
determined, it can be divided by 6 to find \( \tau \). Substituting (7) into (8), and solving for \( R_U \) give the
following equation

\[
R_U = 4 \left( \frac{\tau}{C_{INT}} - R_{SW} \right) - 2 \cdot r_o
\]  

(9)

The number of unit resistors, \( R_U \) can be related to the total resistance, \( R \) by:

\[
R = 2^F \cdot R_U
\]  

(10)

Solving for \( F \) gives:

\[
F = \frac{\log \left( \frac{R}{R_U} \right)}{\log 2}
\]  

(11)

After inserting \( R_U \) derived from (9), an expression for \( F \) with only one unknown, \( R \), is the result:
\[
F = \log \left( \frac{R}{\frac{4\tau}{C_{\text{INT}}} - 2 \cdot r_o - 4 \cdot R_{SW}} \right) \log 2
\]

(12)

Similarly (but by using (10)), another useful expression can be found for \(2^F\):

\[
2^F = \frac{R}{\frac{4\tau}{C_{\text{INT}}} - 2 \cdot r_o - 4 \cdot R_{SW}}
\]

(13)

Plugging the above (13) into the expression found for total reference power (6), gives:

\[
P_{\text{tot}} = \frac{V^2}{R} + V \cdot I_b \cdot \left[ \frac{R}{\left( \frac{4\tau}{C_{\text{INT}}} - 2 \cdot r_o - 4 \cdot R_{SW} \right)} - 1 \right]
\]

(14)

Now that the number of folds have been expressed in terms of R-String resistance and other constants, it is possible to arrive at an expression with one variable: \(R\). The minimum total power can be found by differentiating \(P_{\text{tot}}\) with respect to \(R\), setting the result to zero and solving for \(R\):

\[
\frac{\partial P_{\text{tot}}}{\partial R} = - \frac{V^2}{R^2} + \frac{V \cdot I_b}{\left( \frac{4\tau}{C_{\text{INT}}} - 2 \cdot r_o - 4 \cdot R_{SW} \right)} = 0
\]

(15)

Finally, the \(R\) that results in minimum system power can be found to be

\[
R = \sqrt{\frac{V \cdot \left( \frac{4\tau}{C_{\text{INT}}} - 2 \cdot r_o - 4 \cdot R_{SW} \right)}{I_b}}
\]

(16)

Once \(R\) is calculated from system constants and requirements, the number of folds and unit resistance can easily be calculated using the above expression for \(F\) (12).
Having expressions to determine the optimal number of folds to be used for lowest power is very useful in a multi-channel DAC where scaling to $M$ DACs is a crucial feature. Figure 14 shows how increasing the number of folds as the load capacitance ($C_{INT}$, directly proportional to $M$) increases will lower power.

![Figure 14: Power versus load capacitance and number of folds.](image)

The load capacitance $C_{INT}$ represents the number of channels, $M$, using the resistor string as a reference. It is interesting to note that as $C_{INT}$ increases, it becomes more important to use folds. For a load capacitance of 10 pF, it is shown that power can be reduced by a factor of approximately 3 by adding two folds. This is a large power savings over the conventional arrangement.
2.2 Self Refresh Buffer Method

A unique feature of the DAC architecture in this work is the method used to buffer the reference voltage generating resistor string. A switched capacitor circuit is used to sample the voltages on the resistor string during a quiescent period of the conversion cycle. Then during the driving portion of the conversion cycle, the reference resistor string is driven by the buffer. Figure 15 shows the sample and hold circuit used from [13].

![Sample and hold circuit](image)

Figure 15: Sample and hold from reference [13].

$V_{IN}$ is the same point on the resistor string that $V_{OUT}$ is driving. The advantage of this sample and hold circuit is that clock feed-through and charge injection are canceled. This cancellation occurs when the sampling switches controlled by $V_{samp}$ (Figure 15) are turned off, causing the extra charge to be stored in the feedback capacitor as well as the holding capacitor. An offset in the feedback loop is thereby introduced, which cancels the voltage error on the
holding capacitor. The use of very small holding capacitors, $C_h$, are then allowed, which saves space. The timing diagram in Figure 16 describes the control signal sequencing.

![Timing diagram](image)

**Figure 16: Refresh timing diagram.**

During the first part of the conversion cycle, the resistor string is buffered. This will lower the effective output impedance of the resistor string and allow it to drive the multiplexers much faster. The buffers are then disconnected during the second half of the conversion cycle. At the end of the conversion cycle when the resistor string is settled, the reference voltage can be sampled back into the sample and hold. Since a CMOS amplifier is used, the only leakage path which will cause droop is the reverse biased drain to bulk diodes of the input switch. This is a very low leakage path, therefore, it may only be necessary to sample the reference voltage once every few hundred conversions. Regardless of the leakage, errors in sampling or offsets in the refresh amplifiers, it will not affect DAC accuracy. The refresh amplifier only drives the reference resistor string for part of the conversion cycle. As soon as the buffer amplifier is disconnected, the intrinsic drive of the resistor string will return the nodes to the proper voltage by the end of the conversion cycle.

It is also possible to save additional power by powering down the buffer amplifier when it is not driving the resistor string. Potentially 75% of the power may be saved in the buffer amplifiers, depending on the duty cycle of $V_{drive}$. Unfortunately, for high speed conversion, the
power saving is not always possible due to long time constants involved in powering up an amplifier. However, it may be possible to put the amplifier into a "low power" mode with the quiescent current greatly reduced to approach the 75% theoretical maximum power savings with a $V_{\text{drive}}$ duty cycle of 25%.

2.3 Multiplexer Architecture

There are several ways to implement the multiplexer (or decoder). The two most common architectures are the full decode and the tree decode [12] shown in Figure 17:

![Multiplexer Architectures](image)

**Figure 17:** Conventional multiplexers, full decode on left and tree decode on right [8].

The advantages of the full decode is that it is unit cell based, easy to copy and replicate when designing the circuit and layout, and it has minimal series resistance. The disadvantage is the large amount of output capacitance due to all of the device junctions connected to the output. The large output capacitance will place a large burden on the R-String which will slow down the multiplexer. The full tree multiplexer solves this problem (and uses almost no decode logic), but the series resistance is increased to the resolution of the multiplexer multiplied by the switch resistance. An intermediate solution was developed to provide a compromise (Figure 18).
Figure 18: Folded R-string multiplexer (diagram from [8]).

The folded multiplexer architecture from [14] is analogous to a standard memory address decode architecture. The switches are arranged in rows and columns to address a reference voltage and connect it to the output. Splitting up the busses greatly reduces the output capacitance, series resistance and the logic required. But this is still not the optimal solution. Another level of folding is possible to create a three dimensional structure. Three sets of decoders would then be required, one each for the x, y and z dimensions. The circuit diagram for such a three dimensional six bit multiplexer can be found in Figure 19.
Figure 19: Three dimensional 6-bit analog multiplexer (modified 2D diagram from [8]).

Using this architecture, parasitic capacitances are further minimized in the signal path, as compared to a 2 dimensional folded multiplexer. Unfortunately, at the same time, the series resistance is increased. Another advantage of the three dimensional multiplexer is the logic required to decode the digital input code is also greatly reduced.
The number of dimensions is denoted by \( D \) (not to be confused with folds in the reference R-String) and \( B \) denotes the resolution (or number of bits). The full decode multiplexer has 1 fold, whereas the tree decode has \( D=B \) folds. It is interesting to note that as \( D \) is increased from 1 to 2, the folded architecture will be arrived at and as we continue increasing \( D \) to \( B \), the decoder will transform into a tree decoder.

Table 3 summarizes the series resistance, parasitic capacitance (sources and drains) and logic required for each of the architectures to implement a 9-bit multiplexer. The logic is calculated by the number of equivalent 4-bit AND gates required for the decoder blocks. The subscript \( D \) is used to identify a specific dimension of folding. For example, a 3-D folded 8-bit DAC might have three bits of resolution (\( B \)) in the first dimension, three bits in the second and two bits in the third.

Table 3: Architecture comparisons of several 9-bit multiplexers.

<table>
<thead>
<tr>
<th>Multiplexer Dimension (( D ))</th>
<th>Multiplexer Resistance</th>
<th>Total number of Junction Capacitances</th>
<th>Equivalent Logic Gates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tree Decode (( D=\text{N} ))</td>
<td>( 9 \cdot R )</td>
<td>( 3 \cdot (N + 1) - 1 = 29 )</td>
<td>0</td>
</tr>
<tr>
<td>Full Decode (( D=1 ))</td>
<td>( 1 \cdot R )</td>
<td>( 2^N = 512 )</td>
<td>( \left( \frac{2^N \cdot N}{4} \right) = 1,152 )</td>
</tr>
<tr>
<td>( D=2 )</td>
<td>( 2 \cdot R )</td>
<td>( (2^4 + 1) + (2^5 + 1) - 1 = 49 )</td>
<td>( \left( \frac{2^4 \cdot 4}{4} \right) + \left( \frac{2^5 \cdot 5}{4} \right) = 56 )</td>
</tr>
<tr>
<td>( D=3 )</td>
<td>( 3 \cdot R )</td>
<td>( 3 \cdot \left( \sqrt{2^N} + 1 \right) - 1 = 26 )</td>
<td>( \left( \frac{2^{N/3} \cdot N/3}{4} \right) = 18 )</td>
</tr>
<tr>
<td>( D=4 )</td>
<td>( 4 \cdot R )</td>
<td>( (2^3 + 1) + (2^2 + 1) + (2^2 + 1) + (2^2 + 1) - 1 = 23 )</td>
<td>( \left( \frac{2^3 \cdot 3}{4} \right) + \left( \frac{2^2 \cdot 2}{4} \right) + \left( \frac{2^2 \cdot 2}{4} \right) = 12 )</td>
</tr>
<tr>
<td>( D=K )</td>
<td>( D \cdot R )</td>
<td>( \sum_{K=1}^{D} \left( 2^{N_K} + 1 \right) - 1 )</td>
<td>( \sum_{K=1}^{D} \left( \frac{2^{N_K} \cdot N_K}{4} \right) )</td>
</tr>
</tbody>
</table>
Assuming the impedance looking into the reference resistor string is much greater than the switch resistances, the parasitic junction capacitances can be lumped into the load capacitance. The load capacitance is usually a buffer tied to $V_{\text{out}}$. Table 3 shows that the total number of parasitic junction capacitances is minimized in the 3-D case.

Adding folds to the multiplexer becomes more important as the resolution increases. For example, in a 9-bit multiplexer, using a full decode scheme will result in 512 junction capacitances at the output in addition to the load of the amplifier’s input devices. A 2-D folded architecture will require a 4-bit and a 5 bit dimension. This will result in 49 junctions effectively tied to the output. In a three dimensional folded multiplexer, the number of junctions that must be driven is reduced to 26. An additional benefit of the 3-D architecture is that the number of equivalent logic gates for decoding the control signal is reduced to 18 from 56 in the 2-D case.

Note the expressions in Table 3 above exclude the effects of interconnect parasitics. Parasitic resistance can rightfully be excluded since it is a small percentage of the total resistance in comparison to the switch resistance. The parasitic interconnect capacitances can be lumped with the parasitic junction capacitances and the sources and drains. Typically, the junction capacitances will dominate the capacitance per node.

Using the expressions for resistance and capacitance in Table 3 for an $N$ dimensional folded architecture, the ideal number of folds to minimize settling time can be found. Approximating the time constant of the output of the multiplexer can be done using the open circuit time constant approach [15]. The approximation circuit is shown in Figure 20.
From Figure 20 it is shown that $R_{SW}$ (from Figure 12) is equal to

$$R_{SW} = \sum_{i=1}^{N} R_i$$

(17)

and $R_{ref}$ is the maximum effective impedance of the reference resistor string. Therefore,

$$\tau \approx \sum_{i=1}^{N} \left[ (R_{ref} + N \cdot R_{SW}) \cdot \left( 2^i + 1 \right) \cdot C_{junc} \right] + \left( R_{ref} + N \cdot R_{SW} \right) \cdot C_{load}$$

(18)

where $C_{junc}$ is the parasitic drain and source to bulk capacitance. Unfortunately, no closed form solution for $\tau$ exists since not every fold in the multiplexer has the same resolution. For example, a 9-bit multiplexer with one fold can have four bits of resolution in one dimension and five in the other. However, (18) can be used to make a decision on how many folds results in a minimum settling time. For a small number of dimensions, $D \cdot R_{SW}$ is small compared to $R_{ref}$ so the junction capacitances can be lumped with $C_{load}$. For a large number of folds, the total switch resistance will approach the voltage reference impedance, which will result in an inefficient solution.

### 2.4 Operational Amplifier Architecture

A low power, high slew rate buffer amplifier is required to drive the panel capacitance. The output buffer is the main source of power consumption in each channel of the DAC, thus it is important to keep the quiescent current as low as possible. Considering a load of 100 pF, an output voltage swing of 5 V and a slewing time of 200 ns, use:
\[ i = C \frac{dV_{\text{out}}}{dt} \]  

(19)
to calculate the necessary output current for the amplifier. A simple operational transconductance amplifier is out of the question because the necessary output current is 2.5 mA and this would necessitate at least as much bias current.

An operational amplifier with some sort of class B or class AB output stage is required to generate the necessary output current. Operational amplifiers require compensation. The compensation capacitor will have to be driven by the input stage. Assuming a compensation capacitor of 1 pF and using (19), a tail current of 25 \( \mu \)A will be necessary. The rest of the operational amplifier can easily use four to five times as much bias current. This results in at least 100 \( \mu \)A of bias current for the operational amplifier, which does not fit in the 250 \( \mu \)W power budget given in Section 1.3.2. A slew rate enhancement (SRE) method is developed to alleviate these limitations.

2.4.1 Basic Operational Amplifier Architecture

A current efficient buffer amplifier capable of driving large capacitive loads is shown in Figure 21.
Figure 21: Buffer amplifier with folded cascode 1st stage and class AB output stage.

The first stage of the amplifier is a folded cascode with a dual polarity front end. The second stage is a class AB common source stage which was first described in [22] and further refined in [17] and [18]. The compensation method employed in this amplifier is cascoded Miller compensation. The compensation capacitors are formed using PMOS devices with their gates tied to the current mirrors and the sources, drains and bulks tied to the output. Using gate capacitors for compensation saves space because of the high capacitance per unit area. Unfortunately, the capacitance will not be the same through the entire common mode range.

The first section of the amplifier is the folded cascode section. This architecture was chosen because it is simple, high in gain, and offers the input stage flexibility. The folded cascode opamp has a PMOS and an NMOS differential input pair providing true rail to rail input
common mode range. The input stages are operated in weak inversion to save power. The input
devices need to be kept relatively large to maintain a low offset. Because there is no constant $g_m$
circuit in the input stage, $g_m$ will vary over the entire common mode range. The input pairs were
sized so that they will both have the same transconductance. Therefore, the effective
transconductance of the input will be twice as large in the middle range of the input voltages as it
will be near the rails. This will reduce the gain of the opamp near the rails and it will also affect
the quiescent current in the output stage. These reasons, in addition to the compensation
capacitor varying are all reasons why the phase margin of the operational amplifier must be
evaluated in the three main regions of operation. The three regions of operation are:

$$V_{IN-LOW} < V_{th-n} + 2 \cdot V_{ds-sat} < V_{IN-MID} < V_{th-p} + 2 \cdot V_{ds-sat} < V_{IN-HIGH}$$ (20)

The second stage, the output stage, is a class AB amplifier. It is comprised of two
common source amplifiers driving a common point. This type of output stage was chosen
because it is high gain and can source and sink a large amount of current in comparison to its
quiescent current. Referring to Figure 21, the output stage is biased by devices $M9a$ and $M9b$.
These two devices along with the output devices form a translinear loop with their respective
bias devices. The bias devices for $M9a$ are simply two stacked diode connected devices which
are not shown here. These two devices in parallel will form a floating voltage source in the
summing node of the folded cascode. The voltage source is designed to keep a minimum
quiescent current through the output stage.

Considering the case where the quiescent current through the diode stacked bias devices
is the same as $M9a$, and the bias devices are the same size as the respective devices in the
operational amplifier, then the quiescent current in $MoP$ will also be the same. It is possible to
set the bias current in the output stage to any arbitrary value using the following expression:
\[
\sqrt{\frac{I_{D-MOp-bias}}{W}} + \sqrt{\frac{I_{D-M9a-bias}}{W}} = \sqrt{\frac{I_{D-MOp}}{W}} + \sqrt{\frac{I_{D-M9a}}{W}}
\]

(21)

The NMOS output device is biased in the same manner with the same bias current. It is important to note that during operation in the \(V_{IN-LOW}\) region, the quiescent current in the output stage will be lower than that during operation in the other regions. This is due to the fact that when the input voltage is above \(V_{IN-LOW}\), the NMOS differential input pair is operating and consuming some of the current from the current sources (\(M3a,b\)). Less current will then be left for the bias devices \(M9a\) and \(M9b\), which in turn will reduce their \(V_{GS}\). Reducing the \(V_{GS}\) voltage will increase drive on the \(ndrive\) and \(pdrive\) nodes since the bias voltages (\(PBiasQ\) and \(NBiasQ\) in Figure 21) generated by the stacked diode devices remains the same. Increasing the gate to source voltages of the output devices will obviously increase the quiescent current in the output stage, which will in turn increase \(g_m\) and decrease the output impedance.

During operation, the floating voltage source will move up and down to drive the output stage (Figure 21). Considering the small to mid signal case, let \(M3b\) act as one current source and \(M6b\) as the other. In-phase input signals coming from the differential pairs into the drains of \(M3b\) and \(M6b\) will control the floating voltage source. Consider the case for a positive input step where current \(\Delta I\) is pulled from the current sources. \(M1N\)'s current is increased by \(\Delta I\) whereas \(M1P\)'s drain current decreases by approximately the same amount. The gate voltages of the output devices will then move down. This is because the gate to source voltage \(M9a\) decreases due to the decreased current, but its gate voltage remains constant. The opposite action occurs for \(M9b\); an increase in its current will cause its gate to source voltage to rise. The current through \(MoN\) will start to decrease and increase the current through \(MoP\), causing the opamp to source current. The process will continue until all of the current flows through \(M9b\). At this
point a minimum current will flow through MoN which is set up by the sizes of the devices in the translinear loop. If all of the devices are in saturation, equation (21) can be used to calculate the minimum current.

The total gain of the operational amplifier operating in the $V_{\text{IN-MID}}$ region is given by

$$A_V = (g_{m1N} + g_{m1P})(g_{m-oN} + g_{m-oP}) \cdot \left( g_{m4b} r_{o4b} (r_{o3b} \parallel r_{o1N}) || (g_{m5b} r_{o5b} (r_{o6b} \parallel r_{o1P})) || r_{o-oN} \parallel r_{o-oP} \right)$$  \hspace{1cm} (22)

Equation (22) is also valid for the other regions of operation as long as the appropriate input device transconductance is set to zero. The other parameters will also have to be reevaluated at the new operating point. A DC gain of 120 dB is easily achieved with this architecture.

The frequency response of the amplifier is dominated by the following poles [24]:

$$p_1 \approx -\frac{1}{g_{m-out} r_{out} r_1 C_C}$$  \hspace{1cm} (23)

$$p_2 \approx -\frac{C_C g_{m-out}}{C_1 C_L}$$  \hspace{1cm} (24)

$G_{m-out}$ is the transconductance of the output stage, $r_{out}$ is the output impedance of the amplifier, $r_1$ is the output impedance of the folded cascode first stage, $C_C$ is the compensation capacitor, $C_1$ is the parasitic capacitance found at the output of the folded cascode first stage and $C_L$ is the load capacitance.

The dominant pole, $p_1$, is found at the output of the folded cascode first stage. It is due to the resistance and total capacitance at that node. The resistance can be found by a standard calculation of the output impedance of a folded cascode amplifier. The capacitor is simply the Miller capacitance at the node which is the gain of the output stage multiplied by the compensation capacitor.

The second pole, $p_2$, is the same as that of a standard class A output stage, except that it has been shifted up in frequency by the ratio of the compensation capacitor to the parasitic
capacitance at the output of the folded cascode. The amplifier in this work has relatively small output devices, therefore this ratio can be on the order of three to five. This additional pole splitting feature of cascoded Miller compensation increases phase margin.

A second advantage of cascode Miller compensation is the right half plane zero associated with traditional Miller compensation is avoided. The cascode device breaks the feed-forward path and the zero is not created. A useful zero is created, however, by the resistor in series with the load capacitance. This is a left half plane zero with a value of $-1/R_LC_L$. The resistor can be sized to bring the zero down in frequency to supply more phase margin; however, care must be taken that the resistor does not adversely affect slew rate by limiting the output current.

### 2.4.2 Slew Rate Enhancement

Low power and speed are mutually exclusive terms when it comes to CMOS operational amplifiers. Two stage amplifiers are required in this application to provide accurate buffers. Two stage amplifiers require a compensation scheme, which is usually a capacitor tied from the output of the amplifier to a high impedance internal node. Due to the fact that the node is high impedance, charging the capacitor during a transient is a slow and usually limiting process. If the slew rate of the amplifier is limited by the time required to charge the compensation capacitor rather than the time it takes for the output stage to charge the load, then the amplifier is said to be internally slew limited. Removing the slew limitation is key to achieving low power and relatively high speed.

Much work has been done to enhance slew rate in single stage OTA's [16,19-21]. Two general approaches have been taken. The first is to increase the tail current in the diff pair during slewing [19,21]; this approach will be termed “bias boost” in this work (Figure 22). The second
approach is to add current directly into the load [16,20], to help the OTA drive the output capacitance. This approach will be termed “load boost.” Both of these approaches are less than desirable in two stage CMOS amplifiers.

The bias boost method is deficient because it is not compatible with some commonly used architectures. For example, boosting the tail current only serves to enhance the slew rate in one direction in a folded cascode amplifier. The folded cascode amplifier is the basis for nearly all low power amplifiers because it is easy to add a buffer stage for driving large capacity loads, it has a very high gain, and it is easy to add a second complementary differential input stage for rail to rail operation.

The load boost method fails because positive feedback into the amplifier’s output can easily lead to oscillations if the slew detect circuit is too slow to turn off, or has too small of a differential trigger voltage. Even when properly compensated, this type of boosting scheme can lead to excessive overshoot from which it takes time to recover. This is a very uncontrolled manner in which to drive the load. A block diagram of Load Boost is shown in Figure 23.
Figure 23: Block diagram of the load boost technique.

An architecture has been developed which will attack the problem at its root in a two stage amplifier. The internal slew rate of a two stage operational amplifier is determined by the speed at which the amplifier can slew its compensation capacitor(s). By directly attacking this problem, the architecture can be simplified and a slew rate enhancement circuit that has the least effect on the dynamic characteristics of the operational amplifier can be employed. A conceptual operational amplifier with a slew rate enhancement circuit is shown in Figure 24.
Figure 24: Operational amplifier with a slew rate enhancement circuit.

The slew detect circuit takes the inputs to the amplifier and if a large difference (on the order of a few hundred millivolts) is detected, a signal is sent to turn on either current source, depending on the polarity of the input transition. For example, if $V_p$ encounters a fast high transition, indicating a positive input step, $V_n$ will lag behind. The slew rate detector sees that $V_p > V_n$, and it turns on the current source at the bottom to help charge $C_I$. Similarly, on a negative going transition, the slew rate detector will turn on the current source at the top. The slew rate detector that was used is shown in Figure 25.
Figure 25: Slew detect circuit.

The slew detect circuit is based on the one developed in [19]. Ms4 and Ms5 are biased as current sources with $\frac{3}{4} I_B$. Ms3 is biased with a current of $I_B$. At equilibrium, when $Vn = Vp$, Ms4 and Ms5 are current starved and operating in the triode region. This causes them to pull their drains to the power supply rail because they are “stronger” than Ms3, which turns off the current injectors Ms6 and Ms7. During a slew condition, such as $Vp > Vn$, all of Ms3’s current wants to go through Ms2. Now the equilibrium condition is reversed, and Ms2 and Ms3 go into the linear region and pull the $Vboostp$ node down, which in turn drives Ms7 to turn on. The exact same action, only involving Ms1, Ms4 and Ms6, occurs for a negative going transition.

This slew detect circuit has several advantages – it is very fast, compact, tolerant to process variations, low power and it does not require any resistors. The circuit is low power because its bias current can easily be scaled down from the main bias current. The limitation on power is whatever current is required to slew $Vboostn$ and $Vboostp$ much faster than the intrinsic slew rate of the amplifier. Ms6 and Ms7 (and interconnect parasitics) constitute the capacitance on the $Vboostn$ and $Vboostp$ nodes. A “SRE-slew to operational amplifier-slew” ratio of approximately 5 was found to work well through simulation. A downside to this slew detect
circuit is the limited input common mode range. The circuit will not malfunction, since turning off \( Ms3 \) will only serve to enhance \( Ms4 \) and \( Ms5 \)'s ability to pull the \( V\text{boostn} \) and \( V\text{boostp} \) nodes high.

There are several options to connect the SRE circuit to the operational amplifier. Connecting the boost circuit for negative going transitions is straightforward – simply connect node \( X \) to the compensation capacitor \( C0 \), i.e. the summing node at the drain of \( M3b \) (Figure 24). The first option for connecting node \( Y \) for positive edge slew rate enhancement is to sum the boost current into the tail of the PMOS diff pair. This would work similarly to solutions based on the approach found in [16], but it has the major drawback that it does not work near the top of the common mode range. Referring to Figure 24, it can be seen that for a positive step close to the power supply rail, \( M1P \) is immediately cutoff. The node \( \text{tailp} \) will follow \( Vn \) to the final value. Once \( \text{tailp} \) gets within \( V_{th}+V_{DS-ON} \), \( M2P \) will be off and the boost current can no longer help because there is no path to the compensation capacitor \( C1 \). The second option is to add an NMOS turnaround for the current coming out of \( Ms7 \) and summing it into the drain node of \( M6b \). This solves the common mode problem, but the circuit has a very slow turn off time and can result in significant overshoot. If node \( Y \) is connected to a turn-around current mirror, there is quick path to discharge node \( Y \) when \( Ms7 \) is turned off after the positive going slew condition is gone. The ideal solution is to sum \( Ms7 \)'s current into the drain of \( M6a \). This solution yields the benefits of both the aforementioned solutions since any current added into \( M6a \) will be mirrored to \( M6b \). This is the same as adding a current source in parallel with \( M6b \). The completed operational amplifier is shown in Figure 26.
Figure 26: Complete operational amplifier with a slew rate enhancement circuit

Key metrics for low power circuits for portable applications are low power, compactness, simplicity, robustness (yield), and offset. SRE greatly speeds up amplifiers with minimal bias current cost. Since internal slew rate limitations are mitigated, the class AB output stage can be sized to accommodate driving various loads. SRE is robust and does not change the small signal dynamics or the offset of the amplifiers because it is off during quiescent operation. SRE is very compact and low power, the circuits can be scaled to use minimum power. An additional bonus of this architecture is that larger compensation capacitors may be used to increase phase margin without detriment to internal slew rate.

Using this SRE circuit, a new benchmark for power vs. slew rate for two stage CMOS operational amplifiers with real driving capability can be achieved. At this point it is undetermined what the maximum improvement factor is. These results were found in a somewhat ad hoc manner through simulation, but analysis will follow to determine the exact
sizing of the boost devices to give a maximum improvement in the slew rate. The analysis will relate the speed of the slew rate circuit, the current of the boost devices and dynamics of the operational amplifier (such as how hard to drive the ndrive and pdrive nodes).

2.5 DAC Simulation Results

The entire test chip is large enough that not all of the verification is possible at the highest level of the hierarchy. The major blocks were all verified separately and then simulated together in a top level test bench. The top level test bench is shown in Figure 27.

![Figure 27: Top level test bench.](image)

The chip is represented by the symbol called “top” in the center of the test bench. The chip has twelve DAC outputs, however, there are only four sets of digital inputs. This is due to a limitation in the pad frame available for the test chip and the matching test hardware. DACs one through three are wired in parallel to the first nine bit digital input, the next three DACs are wired to the next digital input, etc. If all of the DAC inputs were used, over 130 pins would have
been required. Independent control of every DAC is not important to testing the chip; rather it is more important to have all of the DACs present to load the common reference circuit with their parasitics.

Referring to Figure 27, the transistors in the upper left simply set up the bias current. Each DAC has an R-C load at the output of the chip. Three blocks labeled “stim” were used as the digital stimulus. The stimulus was implemented in Verilog-A which is an analog behavioral language similar to Verilog. This provided the flexibility to drive the DACs with digital input words without having to perform mixed signal simulations.

Figure 28 shows the improvement in settling time when stepping all of the outputs in parallel from step 64 to step 448. This is the worst case situation for settling time, since it connects all of the internal loads ($C_{INT}$ as shown in Figure 11) to the point of highest equivalent output impedance on the reference R-String. Settling time to 10 mV (one LSB) was simulated to be 725 ns without the reference R-String buffered and 366 ns with the R-String buffer enabled.
Figure 28: DAC settling from step 64 to step 448.

Figure 29 details the output buffer biasing. In this case the bias current, $I_B$ is set to 6 $\mu$A. The current sources in the folded cascode stage ($M3a$ and $M3b$) are biased to $I_B$ and the differential input pairs are biased with $7/8 I_B$. In general, the value of $V_{DS,SAT}$ is not crucial for the folded cascode devices since the output voltage is kept constant, but they were designed to be approximately 200 mV. $V_{DS,SAT}$ of the output devices was designed to be approximately 100 mV to provide good accuracy nearly all the way to the power supply rails. The folded cascode’s large signal characteristics can be improved by biasing the differential input pair with less current than the current mirror. This is due to the fact that the operational amplifier will recover
from large input steps quicker if the current mirror is not starved during the slewing condition. The current through the translinear loop bias devices ($M9a$ and $M9b$) is $7/16\ I_B$ during the $V_{MID}$ and $V_{HIGH}$ ranges of operation. Approximately $2.5\ I_B$ of current in the output stage will result. During the $V_{LOW}$ portion of operation the NMOS input pair is off, therefore, $M9a$ and $M9b$ receive the full $7/8\ I_B$ which will in turn reduce the current in the output stage. $M9c$ was included to protect the drain of $M4a$ from high voltage. This will dramatically reduce hot carrier injection and it will reduce the systematic offset of the amplifier.

![Figure 29: Output buffer DC simulation results.](image-url)

The slew rate detection circuit of Figure 25 was used in this amplifier, but not shown above for simplicity. The entire slew rate circuit is biased with one $I_B$, therefore it is responsible for less than 1/6 of the total bias current of the buffer. Since the total settling time specification
for the amplifier is 400 ns, 200 ns of large signal slewing time and 200 ns of small signal settling time have been allotted. To slew the amplifier from rail to rail in a time period of 200 ns requires a slew rate of 25 V/μs.

![Transient Response](image)

**Figure 30: SRE simulation results.**

As can be seen from Figure 30, a dramatic improvement in amplifier speed has been accomplished. The settling time to 1% has been improved by over a factor of two and the slew rate has been improved by a factor of 5. The slew rate circuit does cause some overshoot in the output of the amplifier, however, this is not necessarily a detriment when driving LCDs. The overshoot can help charge the LCD faster during large signal transients, because, when viewed as a large R-C network, the overshoot will be mostly filtered at the liquid crystal node.

### 2.6 Physical Implementation

LCD systems put many strict requirements on the display driver ICs and two of them are size and scalability. These two concerns were addressed by the architecture and the layout. The layout is shown in Figure 31.
Figure 31: DAC layout.

There are five main sections to the layout. The first section includes the three refresh amplifiers, a bias block for the refresh amplifiers and the sample and hold capacitors. The sample and hold capacitors are made from highly linear metal to metal capacitors. The second section comprises of the two output buffers and their bias block. The bias block is located in the center of section two to provide the best matching between the bias block and the amplifiers. In this test chip, separate bias blocks were used for the two groups of amplifiers. It is possible to use the same bias block for both groups of amplifiers to further save space and lower power. The third very thin section is located between sections one and four. This is where the polysilicon reference resistor is located. The resistor is laid out horizontally because the reference voltages are routed vertically down over the multiplexers in section four. The multiplexers are stacked vertically so they can easily share the reference voltages. The output voltages from the multiplexers are routed up through the center back to section two. Area five contains the digital decode logic for the multiplexers. Control signals are routed horizontally from the decode logic to the multiplexers. The small section just above the decode logic and
below the output amplifiers is the test multiplexer. The two vertical bars on the far right are power and ground bussing.

This arrangement makes it very easy to add or subtract channels. Multiplexers are simply appended to the bottom of section four and output buffers are appended to section two. This is a very compact layout with no wasted space.
Chapter 3: Experimental Results

The die photo of the converter is shown in Figure 32. The chip was tested on a manual wafer prober with a generic probe card.

Figure 32: Die photo.

Figure 33: Block diagram of test setup.
Figure 33 shows a block diagram of the complete test setup. The test setup was assembled from generic test components, which resulted in a less than optimal configuration for testing the DAC. Noise in the test setup was a constant issue when taking measurements. There were two main components of noise in the system. The first component was noise picked up from the environment by the long cables. The second component of noise was dominant and resulted from signals going through several cables and several connectors. Parasitic capacitances and inductances caused an excessive amount of ringing in the digital signals. Series resistors were inserted in all of the digital signals on the probe card adaptor board shown in Figure 33. The improvement in the digital signal integrity was significant (Figure 34), but it was still far from ideal.

![Figure 34: Digital signals before (left) and after (right) series resistors.](image)

Referring to Figure 34, the red trace at the top is the power supply voltage, the yellow trace is the output of the DAC, the green trace is the most significant bit (MSB) of the input code and the blue signal is $V_{drive}$. A major limitation of the design is the use of a single power supply. Since the refresh buffers, the reference resistor, the output buffers and the decoding logic all share the same power supply, noise will couple between them.
3.1 DAC Measurements and Results

The prototype device was loaded with a 200 Ω resistor in series with a 100 pF capacitor for each channel. This is more indicative of a real load; this converter has the ability to drive off-chip loads. Unless otherwise specified, the supply voltage was 5 V and the output buffer supply current was 42 μA. The DAC linearity is dependent on two factors. The first is the achievable matching in the reference resistor string and the second is the offset of the amplifier. Fortunately, the error in the reference resistor string is common to all 12 channels. Therefore, channel to channel matching is only dependent on amplifier offset. The total linearity of a measured converter in terms of LSBs, including both resistor and amplifier offsets is shown in Figure 35.
An integral non-linearity (INL) of \( \pm \frac{1}{2} \) LSB is required to guarantee 1 LSB of channel to channel matching. The results from this converter show that an INL of \( \pm 1 \) LSB was achieved. This is enough to guarantee linearity and functionality for a single converter, but channel to channel matching will be limited to 2 LSBs. The major source of the error comes from the offset in the output buffer. The measured INL of the reference portion of the DAC is shown in Figure 36.
Figure 36: INL of the reference resistor.

It can be seen that the INL of the reference resistor is $\pm 0.2$ LSB’s. The DNL will not be much different from the results in Figure 35 because the offset over a small range in the output buffer is constant as can be seen in Figure 39. Fortunately, this INL will only affect the absolute linearity of the individual DAC outputs.

The complete conversion cycle is shown in Figure 37. The two drive methods are superimposed to illustrate the superior settling time (and therefore conversion rate) of the self refresh method. $V_{drive}$ and $V_{sample}$ (from Figure 16) are also shown in the figure. For the self refresh method, $V_{drive}$ is high for the first 12.5% of the conversion cycle and $V_{sample}$ is active for the last 6.25% of the conversion cycle. For the conventional method, $V_{drive}$ and $V_{sample}$ are inactive, which results in the reference R-String’s intrinsic drive strength.

The voltage levels in Figure 37 are approximately 625 mV and 4.375 V which result from input codes 63 and 447. These codes were chosen to measure the maximum settling time because these are the nodes on the reference R-String that represent the maximum output impedances. Thus these nodes will be the slowest to charge the output buffer’s input.
capacitance. The conventional R-String DAC’s slowest response is with a code step of 0 to 256 or from 511 to 256, since the center of the R-String has the highest impedance. The positive step settling time was less than 500 ns for the folded converter, whereas the positive step settling time took over 1 μs for the conventional converter. The negative step settling times were similar with 450 ns for the folded case and over 1 μs for the conventional case.

![Figure 37: DAC performance with and without self refresh.](image)

The green trace in Figure 37 is the power supply voltage, the purple trace is the MSB of the input, the red signal is the $V_{\text{drive}}$ signal, the cyan signal is the conventional R-String DAC response and the blue trace shows the improvement of the buffered R-String DAC.

### 3.2 Operational Amplifier Buffer Measurements and Results

Figure 38 illustrates the benefit of the SRE circuit. The input signal’s color is green, the conventional opamp response is the yellow trace and the amplifier with SRE is the red trace. With an input voltage step of 0.2 V to 4.8 V, a two-fold decrease in settling time is achieved with
SRE and it has improved from over 1 µs to under 500 ns. This matches the simulation result of Figure 30.

![Figure 30](image)

**Figure 38: SRE amplifier (red) vs. non-SRE amplifier (yellow)**

The offset errors of 36 output amplifiers over the entire common mode range were also measured to gain an understanding of the statistical distribution. These data can be found in Table 4 and Figure 39.

<table>
<thead>
<tr>
<th>Vin (V)</th>
<th>Chip 1 AVG (mV)</th>
<th>Chip 1 STDEV (mV)</th>
<th>Chip 2 AVG (mV)</th>
<th>Chip 2 STDEV (mV)</th>
<th>Chip 3 AVG (mV)</th>
<th>Chip 3 STDEV (mV)</th>
<th>Totals AVG (mV)</th>
<th>Totals STDEV (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3</td>
<td>2.1</td>
<td>6.0</td>
<td>-0.2</td>
<td>8.1</td>
<td>3.4</td>
<td>7.4</td>
<td>1.8</td>
<td>7.2</td>
</tr>
<tr>
<td>2.5</td>
<td>0.5</td>
<td>2.3</td>
<td>-0.4</td>
<td>3.1</td>
<td>1.7</td>
<td>3.4</td>
<td>0.6</td>
<td>3.0</td>
</tr>
<tr>
<td>4.7</td>
<td>1.3</td>
<td>3.4</td>
<td>-0.7</td>
<td>5.0</td>
<td>2.4</td>
<td>5.4</td>
<td>1.0</td>
<td>4.7</td>
</tr>
</tbody>
</table>

**Table 4: Output buffer offset results.**
As can be seen from Table 4, matching between channels to within 1 LSB is not possible with good yield. Unfortunately, mismatch analysis was not performed before the test chip fabrication. The variation in offset over the common mode range is mainly due to the dual polarity front end of the amplifier (see Figure 21). The sources of the offset are analyzed in the appendix.

3.3 DAC Performance Summary and Comparisons

Table 5 contains the DAC performance characteristics as measured from the test silicon. The static power consumption was derived from the entire chip power, including bias blocks and refresh buffers, divided by the number of channels. The active area was derived from the area of
the core of the test chip divided by the number of channels. Therefore, the twelve converter 
channels including the bias blocks, refresh buffers and test circuitry occupied only 0.5 mm².

<table>
<thead>
<tr>
<th>Measurement Results</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Circuit Conditions:</strong> Process 0.5 μm CMOS, Power Supply 5 V</td>
</tr>
<tr>
<td><strong>Performance Metric</strong></td>
</tr>
<tr>
<td>Resolution</td>
</tr>
<tr>
<td>Conversion Rate</td>
</tr>
<tr>
<td>Static Power Consumption</td>
</tr>
<tr>
<td>Active Area</td>
</tr>
<tr>
<td>INL / DNL</td>
</tr>
</tbody>
</table>

**Table 5: DAC performance metrics.**

The figure of merit employed when comparing this DAC to previous efforts is called 
joules per bit areal density. This metric defines the power of a DAC with respect to its resolution 
per unit area.

\[
FoM = \frac{T_s \cdot P}{\left( \frac{B}{DAC} \right) \cdot \left( \frac{DACs}{mm^2} \right)} = \frac{pJ}{B/mm^2}
\]  

(25)

\(B\) is defined as the resolution, \(T_s\) is the settling time and \(P\) is the power. Figure 40 is a 
comparison of this work to previously reported work. Note that the vertical axis is logarithmic in 
scale and a lower value for figure of merit results in a more efficient converter.
Figure 40: DAC figure of merit comparison.

An alternate view is to consider a converter's energy consumption per DAC resolution and the number of DACs that can be fit into a unit area.
Chapter 4: Conclusions and Future Work

Key metrics for digital to analog converter circuits for portable display applications are low power, compactness, simplicity, and offset. A method for minimizing power while achieving the required conversion rate has been shown. Judicious use of buffer amplifiers and an optimized multiplexer enables this architecture to convert data at a moderate speed while maintaining high resolution. Other benefits of the architecture and the design methodology described in this work include the ability to easily scale the DAC to any number of channels in a power and space efficient manner.

The output buffer amplifier was also optimized in this paper. SRE greatly speeds up amplifiers with minimal bias current cost. Since internal slew rate limitations are mitigated, the class AB output stage can be sized to accommodate driving various loads. SRE is robust and does not change the small signal dynamics or offset of the amplifiers because it is inactive during quiescent operation. SRE is very compact, low power and the circuits can be scaled to use minimum power. An additional bonus of SRE is that larger compensation capacitors may be used to increase phase margin without detriment to internal slew rate.

Low power, area efficient methods for reducing the two dominant R-C time constants in the resistor string DAC architecture used for LCD column drivers have been presented. The resulting DAC architecture offers reduced settling time and power dissipation, a scalable circuit structure for multiple channels, and a compact physical layout. This architecture and accompanying design methods set a new benchmark in composite DAC performance of better than 0.60 pJ per bit per mm². Our converter was found to be over one order of magnitude more efficient than the second most efficient converter.
4.1 Improvements to this Work

The methods presented in this paper to minimize power in the DAC do not represent a unified model, since the R-String and the multiplexer in the DAC were optimized separately. This method may not result in the most efficient DAC for higher conversion rates or DACs with many more channels. A unified optimization methodology may need to be developed to best optimize the DAC.

The output buffer’s offset is too high to ensure channel to channel matching of 1 LSB. This offset may be minimized by modifying the design. It may not be practical to lower the one sigma offset to 1.5 mV, therefore a trim procedure or alternate amplifier architecture may need to be developed.

Noise was a limiting factor in the measurements. The test setup should be redesigned to utilize low capacitance and short-lead connections from the digital driver to the IC, or utilize an optimized evaluation board in conjunction with packaged parts. Also, the reference resistor string should have its own clean power domain so that the reference voltages are not affected by system noise.

4.2 Future Work

This work can be adapted to future display technology such as silicon-on-glass (SOG). SOG technology offers the potential to place all electronic modules directly on the glass substrate, thereby taking advantage of the large surface area required by LCD display panels. Placing the complete display system panel and electronics architecture on glass is referred to as system-on-panel (SOP). Display vendors have recognized that SOP offers the highest level of integration and the lowest system cost for LCD display products. A very large amount of power and space
reduction is possible by integrating 100% of the display electronics on the same surface. Work should be done to create an optimal display driver architecture for this future generation of LCD displays.
References

[1] LCD Technology Overview, Dick McCartney, National Semiconductor


Appendix

Output Buffer Offset Calculation

There are four main contributors to the offset of the amplifier as can be seen in Figure 41. These are the two input differential pairs, the PMOS current sources and the NMOS current mirror. The matching between each of these pairs of devices directly affects the operational amplifier’s offset. The differential pair directly affects the offset, whereas the current source and mirror’s offsets are reflected back to the input when the operational amplifier tries to correct the current mismatch.

![Figure 41: Output buffer offset contributors.](image)

As the input common mode voltage is swept, it is clear (from Figure 39 and Table 4) that there are three main regions of operation. The low range is defined as inputs less than 800 mV,
the upper range consists of input voltages within 800 mV of the upper rail, and the center range consists of all the voltages in between. The change in the offset is due to the fact that either the NMOS or the PMOS is operating near the rails and both differential input pairs are operating in the center range. Therefore, the effective $g_m$ of the input stage is cut in half near the rails.

Assuming statistical independence, the standard deviation of the offset is equal to the square root of the sums of the variances of the components:

$$\sigma_{os} = \sqrt{\sigma_{os-thn}^2 + \sigma_{os-thp}^2 + \sigma_{os-cs}^2 + \sigma_{os-cm}^2}$$  (26)

The standard deviations of threshold voltages are usually available for a given process. This is the main contributing factor to offset in this amplifier, therefore secondary effects such as $I_{D,SAT}$ and output impedance mismatches can be neglected.

Defining $\Delta I$ as $\Delta I = I_1 - I_2$, which is the difference in current from one leg of the current source (or mirror) to the other, $\Delta I$ is equal to:

$$\Delta I = g_m \cdot \Delta V_{th}$$  (27)

In a feedback configuration, the operational amplifier will try to offset this current source mismatch. This action will manifest itself as an input referred offset. The amplifier will have an offset voltage proportional to the current offset in the current source. The constant of proportionality is $g_m$. Therefore,

$$V_{os} = \frac{g_{m-cs}^2}{g_{m-1,2}} \cdot \Delta V_{th-cs} = \sigma_{os-cs}^2$$  (28)

It can be seen from (28) that the greater the $g_m$ of the input differential pair is, the easier it will be for the amplifier to correct the current offset in the current source. The variance of the current mirror’s input referred offset voltage is found in the same way.
Once the variances for the various contributors to offset are calculated, equation (26) is used to calculate the offset voltage. Figure 42 summarizes the Monte Carlo simulation results and Table 6 summarizes the one σ offset results.

![Graph showing Monte Carlo simulation results for Voff_high_25, Voff_mid_25, and Voff_low_25.]

<table>
<thead>
<tr>
<th>Input Range</th>
<th>σ_{os-thn}</th>
<th>σ_{os-tp}</th>
<th>σ_{os-cs}</th>
<th>σ_{os-cm}</th>
<th>Calculated σ_{os} Total (mV)</th>
<th>Simulated σ_{os} Total (mV)</th>
<th>Measured σ_{os} Total (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3 V</td>
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<td>3</td>
<td>2.8</td>
<td>10.4</td>
<td>11.2</td>
<td>7.6</td>
<td>7.2</td>
</tr>
<tr>
<td>2.5 V</td>
<td>3.5</td>
<td>3</td>
<td>1.3</td>
<td>3.9</td>
<td>6.2</td>
<td>3.1</td>
<td>3.0</td>
</tr>
<tr>
<td>4.7 V</td>
<td>3.5</td>
<td>0</td>
<td>2.4</td>
<td>4.7</td>
<td>6.3</td>
<td>4</td>
<td>4.7</td>
</tr>
</tbody>
</table>

Table 6: Output buffer offset summary.

While the hand calculations do not exactly match the simulation results, it can be seen that the general trend is the same. In both cases, the offset is highest when the input voltage is in the $V_{\text{LOW}}$ range. This is due to a combination of the offset contribution of the current mirror and the low $g_m$ of the input stage. The $g_m$ of the input stage is at its lowest in this range of operation because the NMOS input pair is off. Meanwhile, the $g_m$ of the current mirror is at its highest because it is receiving the maximum current. Both the PMOS input pair and the current mirror at the top of the folded cascode are feeding current into the mirror. Increasing the $g_m$ of the input...
stage is not an effective method to fix the problem. An increase in the PMOS input pair’s current will, in turn, increase the current consumption of the current mirror. The end result is an increase in $g_m$ proportional to the current in the input pair and an increase in the $g_m$ of the current mirror proportional to the square root of the added current. This relationship will continue until the input pair is biased in saturation where there will be no additional improvement in offset. The only effective methods to decrease offset in this range of operation is to increase the area of the PMOS input pair (to decrease $V_{th}$ variations), increase the area of the devices in the current mirror (to decrease $V_{th}$ variations), and decreasing the $g_m$ of the current mirror. Fortunately, increasing the length of the devices in the current mirror (while keeping the current constant), will also decrease the transconductance. Since the contribution of the PMOS input pair to the offset is already small, increasing the length of the current mirror devices will give the best results. For example, quadrupling the length of the device will cut the transconductance to one quarter of the original value and it will reduce the $V_{th}$ variation by one half which will result in a factor of eight improvement in the one sigma offset contribution of the current mirror.
A 250 Microwatt, 0.042 mm², 2 MSPS, 9-bit DAC for Liquid Crystal Display Drivers

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INTRODUCTION

Small format Liquid Crystal Display (LCD) technology imposes stringent design requirements on column driver DACs to be small in size, exhibit fast settling time, and dissipate low quiescent power. The DAC architecture should be easily expanded with multiple channels to support higher display resolutions. This paper introduces a low power, area efficient, scalable, DAC circuit architecture with fast settling switch matrix and buffer amplifier, optimized for use as an LCD column driver.

A quarter VGA (320 pixels by 240 pixels) display using an 80-to-1 multiplex ratio on the panel requires twelve DAC channels to drive the 960 source lines on the panel. A display with a 60 Hz frame rate, 240 lines, and no blanking, requires a maximum pixel refresh time of 860 ns. The conversion time for this DAC implementation was 500 ns, which allows for manufacturing margin and video blanking flexibility.

ARCHITECTURE

The N-bit DAC architecture is based on a simple resistor divider voltage reference [1] as shown in Figure 1. Reference voltages are digitally selected from the reference resistor string through a $2^{N-1}$ to 1 multiplexer. The internal load capacitance $C_{INT}$ is comprised of the parasitic capacitances of routing, multiplexer devices, and the input capacitance of the output buffer. The selected reference voltage is passed through an output buffer to drive a large panel capacitance. $M$ unique and independent DACs can be operated from the single voltage reference. The advantages of this architecture include its inherent low power, easy scalability to $M$ channels, built-in gamma correction using non-uniform value divider resistors, and channel matching to within the offset for two output buffers.

To minimize power dissipation of the reference, the composite string resistance $R$ is made relatively high. However, a large string resistance degrades settling time. The driving point resistance of the resistor string is reduced by buffering the resistor string at binary fold points, the points of maximum equivalent driving point resistance. As shown in the dashed line inset in Figure 1, inserting three reference refresh buffers (two binary points) reduces the driving source impedance from $R/4$ to $R/16$.

Figure 2 can be used to estimate the optimal number of folds to minimize the power and achieve the desired settling time (or conversion time) in a multi-channel DAC system where $M$ is a display panel variable. Addressing both the power and the settling time requirements for a given load capacitance ($C_{INT}$ is directly proportional to $M$) leads to a preferred number of binary folds in the reference resistor. Folding becomes increasingly important as $C_{INT}$ increases. For example, the power required to drive a 10 pF internal load capacitance is reduced by a factor of three after applying two binary folds (three refresh buffers) to the reference string.

The reference refresh buffer uses a switched capacitor circuit to sample the voltages on the resistor string during a quiescent period of the conversion cycle. During the active portion of the conversion cycle, the reference resistor string is quickly refreshed to the corresponding proportional reference voltage. The reference buffer is only required to drive the resistor string less than 25% of the total conversion time.

Full binary decode structures are often converted to a two dimensional array to reduce $C_{INT}[2]$. This 9-bit DAC architecture uses a three dimensional decode structure, requiring 3 sets of decoders, one for each dimension. Increasing the decode array dimensions comes with an increase in series switch resistance.

Junction capacitances will usually dominate the nodal capacitance. If the number of multiplexer array dimensions is low, the switch resistance is small compared to the Thevenin equivalent reference resistance so the junction capacitances can be added to the output buffer input capacitance to form $C_{INT}$.

A simplified schematic of a slew rate enhanced (SRE) output buffer is shown in Figure 3. A slew detect circuit [3] senses the polarity of the input transition. If $V_P$ encounters a fast high transition of magnitude greater then a few hundred millivolts, $V_n$ will lag behind. The slew rate detector senses that $V_P > V_n$, and boosts the current to charge compensation capacitor $C1$. Conversely, on a large negative going transition, the slew rate detector boosts the current to charge $C0$. Since internal slew rate limitations are mitigated, the class AB output
stage can be sized to the load. Compensation capacitors can be sized to improve phase margin without degrading internal slew rate. SRE is area efficient and improves on recent work [4] with better gain and offers rail-to-rail input common mode voltage range.

DAC channels can be added by attaching additional output buffers (at the upper right) and adding additional multiplexers (at the bottom) to the floor plan shown in Figure 4.

RESULTS
The improvement in settling time using the self refresh reference method is illustrated in the complete conversion reference cycle as shown in Figure 5. Input codes 63 and 447 correspond to the maximum equivalent Thevenin resistances to charge $C_{\text{INT}}$. The buffered reference resistor settled more than twice as fast (450 ns) as the conventional resistor string (1 µs). A summary of the measured DAC performance parameters is listed in Figure 6.

A figure of merit (FoM) for composite DAC performance can be expressed as quiescent power ($P$) multiplied by the conversion time ($T_s$) relative to the DAC bit resolution and number of DACs that can be placed into a unit area ($A$) of 1 mm2 or

$$\text{FoM} = \frac{T_s \cdot P}{\frac{N}{\text{DAC}}} \left(\frac{\text{DACs}}{\text{mm}^2}\right) = \frac{pJ}{\text{mm}^2}$$

Figure 7 illustrates the FoM for this DAC compared to previous work.

CONCLUSION
We have presented low power, area efficient methods for reducing the two dominant $R-C$ time constants in the resistor string DAC architecture used for LCD column drivers. The resulting DAC architecture offers reduced settling time and power dissipation, a scalable circuit structure for multiple channels, and a compact physical layout. This architecture and accompanying design methods set a new benchmark in composite DAC performance of better than 0.60 pJ per bit per mm².

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Figure 9.1.1: Multi-channel N-bit DAC Architecture.

Figure 9.1.2: Power versus internal parasitic capacitance versus number of folds.

Figure 9.1.3: Output Buffer with Slew Rate Enhancement.

Figure 9.1.4: Die Photo.

Figure 9.1.5: DAC Settling Time With and Without Self Refresh Buffers.

Figure 9.1.6: Measured DAC Performance Summary.
Figure 9.1.7: Comparative DAC Performance in pJ/b/mm².
To disconnect switches, set:
code = 001001001 and set nc_n = 0