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CMOS image sensor with bi-directional column sensor

Philip D. Thorpe II

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CMOS Image Sensor with Bi-Directional Column Sensor

by

Philip D. Thorpe II

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Computer Engineering

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Date
I would like to take this time to thank my advisor Dr. Ken Hsu and the other members of my committee Dr. Marcin Lukowiak and Dr. Dhireesha Kudithipudi for agreeing to oversee my work. I would like to thank my parents for supporting me through my college career. Finally, I would like to thank Dr. Zeljko (Jake) Ignjatovic. My consultations with him spurred me on to create this new architecture.
Abstract

CMOS image sensors have been around since the 1960's. However due to poor light sensitivity and poor signal-to-noise ratios (SNR) the architecture was not popular. Since then many improvements have been made to the architecture, making camera designs that use CMOS imagers more prevalent. Much of the improvement in SNR has been due to fixed-pattern noise reduction. Correlated double sampling (CDS) is a popular technique to reduce the effects of this source of noise. The circuitry required to implement CDS can be complex and hinders other areas of an image sensor performance in some schemes. This thesis proposes a new technique that attenuates noise due to DC offset without the use of CDS.

Beginning with a standard three transistor-per-pixel architecture, this thesis builds on previous CMOS image sensor designs and creates a new bi-directional amplifier architecture that eliminates DC offset due to transistor mismatch without the use of CDS. The architecture uses a single differential amplifier to both reset and readout the pixel. Simulations show that SNR range of the proposed column sensor is 48.71 - 44.63 dB, whereas an Active Column Sensor without CDS has an SNR of 31.88 – 28.78 dB under the same conditions.

Using the proposed column sensor, a layout (TSMC 0.35um) for a small 4X4 pixel image sensor was designed and prototyped which proves that the bi-directional amplifier can be used as a column sensor. The proposed prototype shows the viability of the architecture for a future production camera. The simulated result for the image sensor show that it can be reset in 200 ns read out in 3.4us and has an overall size of 107.9X118.1 um².
# Table of Contents

Acknowledgments iii  
Abstract iv  
List of Figures vii  
List of Tables ix  
Glossary x  

1 Introduction 1  
1.1 Motivation 1  
1.2 Organization of Thesis 2  

2 Background 3  
2.1 Image Sensors 3  
2.1.1 CCD 3  
2.1.2 CMOS 5  
2.1.3 CCD vs. CMOS 8  
2.2 CMOS Image Sensor Design Topologies 11  
2.2.1 Passive Pixel Sensor 12  
2.2.2 Active Pixel Sensor 13  
2.2.3 Digital Pixel Sensor 15  
2.2.4 Active Column Sensor 15  
2.2.5 Logarithmic Pixel 16  
2.3 Support Circuitry 17  
2.3.1 Analog to Digital Converters 18  
2.3.2 Correlated Double Sampling (CDS) 19  
2.3.3 Row Decoder 20  
2.3.4 Image Processing 21  

3 Proposed Architecture 22
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 Circuit Design</td>
<td>23</td>
</tr>
<tr>
<td>3.2 Modes of Operation</td>
<td>28</td>
</tr>
<tr>
<td>3.2.1 Soft Reset</td>
<td>28</td>
</tr>
<tr>
<td>3.2.2 Pixel Readout</td>
<td>29</td>
</tr>
<tr>
<td>3.2.3 Changing Between Modes</td>
<td>30</td>
</tr>
<tr>
<td>4 Prototype Design and Results</td>
<td>31</td>
</tr>
<tr>
<td>4.1 Simulation Results</td>
<td>31</td>
</tr>
<tr>
<td>4.1.1 Column Sensor</td>
<td>31</td>
</tr>
<tr>
<td>4.1.2 Pixel Array with Column Sensor</td>
<td>43</td>
</tr>
<tr>
<td>4.1.3 Row Decoder</td>
<td>46</td>
</tr>
<tr>
<td>4.1.4 A/D</td>
<td>47</td>
</tr>
<tr>
<td>4.1.5 Full Design</td>
<td>50</td>
</tr>
<tr>
<td>4.2 Design Layout</td>
<td>54</td>
</tr>
<tr>
<td>4.2.1 Pixel</td>
<td>54</td>
</tr>
<tr>
<td>4.2.2 Pixel Array</td>
<td>56</td>
</tr>
<tr>
<td>4.2.3 Pixel Array with column Sensor</td>
<td>58</td>
</tr>
<tr>
<td>4.2.4 Row Decoder</td>
<td>59</td>
</tr>
<tr>
<td>4.2.5 A/D Converters</td>
<td>60</td>
</tr>
<tr>
<td>4.2.6 Full Design</td>
<td>61</td>
</tr>
<tr>
<td>5 Conclusion</td>
<td>64</td>
</tr>
<tr>
<td>Bibliography</td>
<td>66</td>
</tr>
</tbody>
</table>
List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig 1</td>
<td>CCD Structure and Clocking Scheme</td>
<td>3</td>
</tr>
<tr>
<td>Fig 2</td>
<td>CCD Charge Flow Diagram</td>
<td>4</td>
</tr>
<tr>
<td>Fig 3</td>
<td>Structure of a CMOS Imager</td>
<td>5</td>
</tr>
<tr>
<td>Fig 4</td>
<td>N-Well Photo Diode</td>
<td>6</td>
</tr>
<tr>
<td>Fig 5</td>
<td>Pinned Photo Diode Structure</td>
<td>7</td>
</tr>
<tr>
<td>Fig 6</td>
<td>Photo-Gate Structure</td>
<td>8</td>
</tr>
<tr>
<td>Fig 7</td>
<td>Passive Pixel Sensor</td>
<td>12</td>
</tr>
<tr>
<td>Fig 8</td>
<td>Active Pixel Sensor</td>
<td>14</td>
</tr>
<tr>
<td>Fig 9</td>
<td>Example CDS Circuit</td>
<td>19</td>
</tr>
<tr>
<td>Fig 10</td>
<td>Proposed Amplifier Architecture</td>
<td>22</td>
</tr>
<tr>
<td>Fig 11</td>
<td>Delta Sigma A/D</td>
<td>27</td>
</tr>
<tr>
<td>Fig 12</td>
<td>Simplified Column Amp During Reset</td>
<td>29</td>
</tr>
<tr>
<td>Fig 13</td>
<td>Simplified Column Amp During Readout</td>
<td>30</td>
</tr>
<tr>
<td>Fig 14</td>
<td>Column Amplifier Control Waveform</td>
<td>30</td>
</tr>
<tr>
<td>Fig 15</td>
<td>DC Sweep of Readout</td>
<td>32</td>
</tr>
<tr>
<td>Fig 16</td>
<td>DC Sweep During the Reset Phase</td>
<td>33</td>
</tr>
<tr>
<td>Fig 17</td>
<td>AC Analysis of Pixel Reset</td>
<td>34</td>
</tr>
<tr>
<td>Fig 18</td>
<td>AC Analysis of Readout</td>
<td>35</td>
</tr>
<tr>
<td>Fig 19</td>
<td>Monte Carlo Simulation Example</td>
<td>36</td>
</tr>
<tr>
<td>Fig 20</td>
<td>ACS for Comparison [10]</td>
<td>38</td>
</tr>
</tbody>
</table>
Fig 21 : Voltage Transfer Curve for Proposed Design 39
Fig 22 : Voltage Transfer Curve for ACS [10] 40
Fig 23 : Offset Range Graph 41
Fig 24 : Offset Range Graph High Temperature 42
Fig 25 : Discharge Simulation 43
Fig 26 : Pixel Array Schematic 44
Fig 27 : Pixel Array Simulation 45
Fig 28 : Row Decoder Schematic 46
Fig 29 : Maximum Input Voltage Conversion 48
Fig 30 : Conversion Simulation for Effective Number of Bits 49
Fig 31 : Combined Design Schematic 51
Fig 32 : Overall Design Reset 52
Fig 33 : Overall Design Readout 53
Fig 34 : Pixel Layout 55
Fig 35 : Pixel Array Layout 57
Fig 36 : Pixel Array with Column Sensor Layout 58
Fig 37 : Row Decoder Layout 59
Fig 38 : Analog to Digital Converter Layout 60
Fig 39 : Overall Design Layout 62
Fig 40 : Overall Camera with Light Shield 63
List of Tables

Table 1: Sizings of Transistors for the Column Amplifier 23
Table 1a: Transistor Sizes for the A/D Converter 28
Table 2: Performance of the Prototype Architecture 35
Table 3: Monte Carlo Simulation Results of Prototype 37
Table 4: Simulation Results for the ACS Amplifier [10] 39
Table 5: Row Decoder Performance 47
Table 6: A/D Setup and Simulation Results 50
Table 7: Overall Simulation Results and Extrapolated Data 54
Table 8: Pixel Layout Data 56
Table 9: Pixel Size Chart 56
Table 10: Pixel Array Layout Data 57
Table 11: Pixel Array with Column Sensor Size 59
Table 12: Row Decoder Layout Data 60
Table 13: A/D Size 61
Table 14: Overall Imager Size 62
Glossary

Active Column Sensor (ACS) – An Architecture for CMOS Imagers where all of the pixels in a column share a portion of a buffer amplifier.

Active Pixel Sensor (APS) – A CMOS Image Sensor that has a buffer amplifier built into each pixel.

Bidirectional Amplifier – A differential amplifier in which the polarity of the input terminals can be switched.

Charge Coupled Device (CCD) – a device that has the ability to store charge (capacitor) and transfer that charge to a similar device.

Complementary Medal Oxide Semiconductor (CMOS) Image Sensor – Any group of photo-sensitive elements, that can capture an image, and was created by using a CMOS process.

Correlated Double Sampling (CDS) – A process where two samples of a signal are taken and subtracted which can be used to remove low frequency noise.

Dark Current – Discharge of a pixel when the pixel is not exposed to light, usually due to thermal effects.

Digital Pixel – A CMOS Image Sensor that has an A/D Converter built into each pixel of pixel giving the pixel a digital output.

Dynamic Range – “The difference between, or ratio, of the highest and lowest signal in an electronic circuit.” [27]

Fill Factor – The percentage of photo-sensitive area in a pixel.
Fixed-Pattern Noise – Noise that shows up on certain pixels in every image. It is usually caused by non-ideal conditions such as DC offset, that create offset between different pixels.

Passive Pixel Sensor (PPS) – A CMOS Image Sensor that uses only one transistor to address and reset the image sensor.

Quantum Efficiency (QE) - “The measure of the effectiveness of an imager to produce electronic charge from incident photons.” [9]

Thermal Noise – The noise in the circuit created by thermally generated charge carriers which it collected on a capacitive sensor such as a photo diode.
Chapter 1. Introduction

1.1 Motivation

The original CMOS image sensors were first produced in 1967. These CMOS sensors were found to be slow and very susceptible to noise. Due to poor performance they were quickly replaced by CCD imagers in 1970. While CCD had better performance than the original CMOS sensor, CCD required a specialized process that only a few fabrication plants had, making CCDs more expensive to produce. Throughout the decades research has been conducted on how to eliminate the drawbacks of CMOS imagers through changes to the CMOS imager architecture. Today for most applications, the performance gap between CCD and CMOS imagers has been closed [1].

CMOS image sensors are being placed into new applications every day. The proliferation of cameras embedded into mobile devices makes power consumption a very important factor in new image sensor designs. These sensors are created using smaller feature sizes and are placed in devices with decreasing rail-to-rail power supply voltages and lower maximum output. Many changes that can be made to consume less power have negative effects on image quality when using the standard pixel designs. Most of the current research is aimed at controlling power consumption by altering the imager architecture.

This thesis will create a new pixel architecture using a differential amplifier that has the ability to switch the polarity of the input terminals. This amplifier will be placed in a low resolution 4X4 pixel sensor to show the ability of this configuration to achieve a soft reset, reducing image noise by using a single differential
amplifier. The sensor will also be connected to a column level delta sigma A/D thus eliminating the need for a second chip to do the conversion.

1.2 Organization of Thesis

This thesis begins with a review of existing image sensor technology, design topologies and signal processing circuitry commonly found in camera on chip designs, in chapter 2. Chapter 3 presents the proposed architecture. Chapter 4 shows the simulation results and the circuit layout of the proposed circuitry. A conclusion of work is drawn in chapter 5.
Chapter 2. Background

2.1 Image Sensors

2.1.1 CCD

A charge coupled device (CCD) is formed by using multiple MOS capacitors in very close proximity. The devices have two functions: charge storage and charge transfer. The MOS capacitors are then biased into depletion forming potential wells. These wells can then be filled with charge, representing information. A multi-phase clock is then applied to the gates that form the MOS capacitors. The multi-phase clocking scheme attracts the charge from one device and pulls the charge to the neighboring device [2]. An example of this structure is shown in Fig 1.

![CCD Structure and Clocking Scheme](image)

*Fig 1: CCD Structure and Clocking Scheme*
A CCD image sensor is a two-dimensional array of capacitors, as shown in Fig 2. The array is connected so every column can be used as a shift register with circuitry to allow the charge from one device to be moved vertically to a neighboring device. A row of CCD on the edge of the imager is then set up as a shift register, so that the charge on the array can be moved across the array horizontally. At the end of the row, there is usually a single buffer that is used to read the CCD pixel values and sends the data off chip to support circuitry.

Fig 2: CCD Charge Flow Diagram

The CCD devices in an imager start out in a uniformly discharged state after the potential wells have been formed. The array is then exposed to light. As light hits each device, the photons excite the silicon generating electrons which then charge the capacitor that the photon struck. After the exposure period, the image is captured on the array. The image can then be read out using the shift register mode as described above. This process destroys the image on the CCD sensor as it is read out.
2.1.2 CMOS

CMOS image sensors are very similar to CCDs, in that there is a two-dimensional array of photo sensitive elements. However, in CMOS image sensors the photo-sensitive elements can be a range of different devices, each with a different set of performance constraints. To begin the imaging process, CMOS photosensitive elements are charged to a high voltage, creating the potential wells. As the pixels collect light, charge is dissipated from the photosensitive element lowering the pixel voltage. After the image has been captured, the pixels can be accessed by sending a signal to a control transistor which will then connect the pixel to an output transmission line. There is an output line for every column in the image sensor array.

Fig 3: Structure of a CMOS imager
The pixel array structure described in this section is standard for most CMOS imagers. However, the other circuitry depicted in Fig 3 is optional based on the choice of design.

The original photo elements of the CMOS imager were photo diodes formed by either a well/substrate junction or a substrate active junction. These diodes are very simple, and all of the area of the diode can be dedicated to collection of light. The drawback to this architecture is the diode's susceptibility to multiple noise sources. The structure of an N-well photo diode is shown in Fig. 4.

![Fig 4: N-well photo diode](image)

One of the sources of noise in a photo diode is dark current. Dark current is the discharge of a pixel when not exposed to light. To reduce dark current, the pinned photo diode was developed. A pinned photo diode is a structure with two asymmetrical CMOS transistors. Each transistor has a small area source terminal and both are connected by their larger drains as depicted in Fig 5. The drains of the two transistors are connected to form the photon collection area of the pixel. The sources of each transistor are used to read and reset the pixel and adjust for the dark current. These photosensitive elements
require extra signals to control the gates, which adds complexity to each pixel. As stated above, this design reduces the noise of the photo-sensitive element. However, to work properly the gates must be shielded from light reducing the photosensitive area in the pixel.

![Diagram of dark current and TX data](image)

**Fig 5: Pinned photo diode Structure**

A further improvement for noise reduction was to use a large transistor gate as the photosensitive element in the pixel. The structure of this device is shown in Fig 6. The design uses the gate capacitance to form the potential well, instead of the diode parasitic capacitances which are much smaller. This structure can be used to obtain higher fill factors than the pinned photo diode and has a better noise tolerance than regular photo diodes. However, in this design, the gate does not capture certain wavelengths of light as effectively per unit area as the photo diode architectures [4].
Some of the other design mechanisms for imagers are Bipolar Junction Transistors (BJT) as the photo sensor [7] and hybrid CMOS/CCD architectures [8]. While these designs are worth mentioning, it is hard to say from the literature how these photo sensors compare with standard CMOS and CCD designs.

2.1.3 CMOS vs CCD

The CMOS and CCD sensors are both formed from silicon with the same inherent material properties which should yield similar device performance. However, the fabrication and operation of each device creates image sensors with greatly differing performance characteristics. This section discusses some of the issues that arise when designing a new camera.

Cost

Cost is an important consideration for many consumer devices. When it comes to prices, CMOS was thought to be a better design route than CCD[28]. The CMOS
fabrication process uses larger wafers than CCD, making it possible to produce more imagers out of one wafer [30]. The CMOS fabrication process can be found in most semiconductor foundries giving a designer the ability to shop around for a fabrication and process that is the most cost effective for his or her design. Using CMOS design allows other peripheral circuits such as A/D and image processing circuits on the imager, while CCD image sensors must include these circuits off chip. This increases the cost of an overall camera design[1]. However, in reality many foundries have tweaked the CMOS processes for better imaging quality, resulting in increased development cost of CMOS process for high quality imagers. The added development cost has made many CCD imagers less expensive than CMOS to produce [1].

**Power**

Power consumption and power supply design are very important factor in mobile devices such as laptops, phones and PDA. These devices use batteries that can deliver a limited amount of current at a set voltage. A CCD array requires multiple power supply voltages and high power support circuitry to work properly which far out weights the reset power of the CMOS sensor. While improvements have been made to the CCD process, CMOS imagers still consume less power[1]. CMOS image arrays are used when embedding a camera into an already existing device.

**Noise**

There are many sources of noise in an image sensor, including thermal generation of electrons in silicon (thermal noise), current leakage (dark current), crosstalk (read noise). All of these different noise sources add up to incorrect values in the image array.
When comparing CCD and CMOS imagers, it is clear that CCD enjoys an inherent advantage over CMOS due to the higher rail to rail voltages, giving CCD a much higher signal to noise ratio than CMOS. Another issue for CMOS designs is the on chip support circuitry, which introduces a new source of crosstalk noise that can further decrease the signal to noise ratio [31].

**Quantum Efficiency**

“Quantum efficiency (Q.E.) is the measure of the effectiveness of an imager to produce electronic charge from incident photons” [9]. In other words, it is a measure of how effectively the sensor can collect light over the desired range of wavelengths. This factor is very important when it comes to imaging in low light conditions. The higher sensitivity to light will allow the camera to capture an image quickly, which reduces the chance of the camera moving during the image capture, causing a motion blur on the image. The faster image capture also reduces the effect of dark current noise in the image. Quantum efficiency (QE) is highly dependent on how much area is used to collect light by the imager. Since CMOS transistors must be shielded from light radiation to work correctly, making large parts of the imager insensitive to light. Furthermore, CCD manufactures can thin the silicon of a CCD and use the back of the circuit to collect light, allowing for fill factors of 100% [22]. These facts are the reason that the Q.E of CCD sensors is greater than their CMOS counterparts.

**Speed**

Speed of image capture can be separated into two different segments. The first segment is image acquisition time. For a well exposed picture, image acquisition speed is
governed by the image sensor QE. in which CCD has an edge. The second segment is the image read time or how fast an image can be taken off the imager and recorded to memory. CCD can only read out one pixel of an image at a time while CMOS imagers can read out one row of pixels at a time. Given a square N X N CMOS and CCD and k for one pixel read time it is clear that it takes k*N time to read out a CMOS imager, while it takes k*N² time read out the CCD. As image resolution increases, the read time gap increases in favor of CMOS imagers [29]. The integration of features such as A/D and memory buffers on CMOS imagers can further increase the speed at which an image can be captured.

**Dynamic Range**

Dynamic range is "The difference between, or ratio, of the highest and lowest signal in an electronic circuit" [27]. In image sensors, dynamic range more specifically refers to the ability of the sensor to capture detail in highlight and shadow [32]. The dynamic range of an image sensor is highly dependent on the sensor's signal to noise ratio (SNR) [28]. As discussed in the noise section, CCD has an advantage in SNR when compared to CMOS imagers.

**2.2 CMOS Image Sensor Design Topologies**

Although there have been advances in CCD technology over the years, the architecture of the pixel has remained relatively similar. However, research into CMOS pixels have yielded multiple changes to the architecture of the original pixel. These different topologies factor into the performance characteristics of the image sensor such as light sensitivity, image noise and capture speed. Much of the research addressed the
drawbacks that the original CMOS topology had when compared to CCD. These drawbacks led to CCD imagers becoming the de facto standard for digital image sensors from 1970 until the late 1990.

### 2.2.1 Passive Pixel Sensor

The original CMOS image sensor used an array of photo diodes with a single transistor as illustrated in Fig 7. The transistor is used as a switch to connect the pixel to a shared column bus for reset and readout. The pixel has a single control line used to connect the pixel to a column level bus. Today this topology is known as a passive pixel sensor (PPS), due to the architecture not having the buffer amplifier found in the active pixel sensor architecture.

![Passive Pixel Sensor Architecture](image)

*Fig 7: Passive Pixel Sensor Architecture*
This topology is the least complex of the CMOS architectures discussed in this thesis. The transistor in the pixel must be shielded from light. However, the rest of the pixel can be dedicated to light collection.

The PPS architecture was found to be very slow and had a very poor signal to noise ratio. Due to the large capacitance of CMOS photo-sensors on the column bus, these architectures are slow and require large buffer circuitry to reset the array. The large capacitance on the column lines is the source of most of the noise within the circuit.

### 2.2.2 Active Pixel Sensor

The Active Pixel Sensor (APS) replaces the PPS single transistor with three transistors. This allows reset and pixel select operations to be controlled by separate transistors that act as switches. Each operation now has its own data line, and the column bus is no longer needed to reset the pixel. The third transistor is used as a source follower with the gate connected to the pixel's photo sensor. Later designs of APS circuits replace the photo diode with a photo-gate pinned photo diode. Since these APS circuits have extra transistors, the designs are named by the number of transistors that reside in the pixel. As an example, the photo-gate in Fig. 6 would be a 4-T, where the original APS design is called 3-T APS.
This buffer removes the large capacitance of the photo sensor out of the column bus allowing for much faster and lower noise column bus performance than the passive pixel sensor. The separate reset transistor in each pixel splits the large reset buffer across the entire circuit and reduces the noise of transmitting a reset voltage across the entire circuit. This configuration eliminates most of the noise that made the CMOS imagers less attractive than CCD imagers[3].

The transistors in the pixels need to be shielded from light to work properly. The area occupied by the extra transistors cannot be used for light collection, thus the APS pixel is inherently less sensitive to light than a PPS pixel of the same size. Mismatches
between buffer transistors cause gain variations. These variations are a source of noise within the image sensor.

### 2.2.3 Digital Pixel

Building on the APS topology some designs have not only included a buffer amplifier, but also a full A/D converter[15, 23] with RAM to hold the digital value of the pixel [23]. After conversion these architectures transfer a digital value from the pixel over column bus. These architectures will only transmit one bit at a time to keep a single line for the column bus.

These architectures can acquire images very fast and have been shown to capture images at up to 10,000 frames/second [23]. The digital output of the pixel eliminates all of the noise transferring the data off of the pixel. Fixed pattern and temporal noise can be almost completely eliminated by simply taking multiple images and averaging the images in the pixel's memory.

The drawback is that the added transistors need to be shielded, reducing the fill factor of the pixel. This means that the photo sensor must be smaller, for each pixel which reduces light sensitivity of the pixel, or the pixel size must be made larger which reduces the overall resolution of the image sensor.

### 2.2.4 Active Column Sensors

As designs began adding complexity to each pixel to improve performance, the tradeoff of the lower fill factor and reduced light sensitivity was examined. For the Active Column Sensor (ACS), the decision between complexity and fill factor was that
the added pixel complexity was counterproductive for a good design. After the active pixel sensor (APS) was developed, it was thought that using an unity gain differential amplifier as a buffer would help further reduce fixed pattern noise. Rather than adding extra buffer transistors to each pixel, a design choice was made to use the APS pixel design as one side of the differential amplifier and have all of the pixels in the column share the rest of the transistors that make up the unity gain differential amplifier [10].

This design eliminates complexity in the pixel and allows for an overall higher fill factor for the pixels with a higher overall resolution imaging array. This topology eliminates the gain variation in the buffer, which was a major source of fixed pattern noise in the APS architecture. The ACS also enjoys a lower power consumption when compared to the digital pixel topology.

The drawback to this topology is that it is slower than other topologies such as the digital pixel design, because an entire column of pixels share an analog-to-digital converter. Since it is nearly impossible to match every transistor that makes up the differential amplifiers, there will always be some voltage offset which leads to a new source of fixed pattern noise in the circuit. This new source of fixed pattern noise can be fixed with correlated double sampling, which will be discussed later in section 2.3.1.

2.2.5 Logarithmic Pixel

The APS and ACS topologies dealt with the elimination of noise that was first encountered in the original CMOS imagery architectures. However, these designs did not approach the higher dynamic range found in CCD sensors. This issue can be dealt with by using a self-resting pixel found in [20] or by using multiple capture with the digital
pixel topology [23], but a different solution to this problem was found. The APS and ACS designs both have pixels that discharge linearly when exposed to light. By rearranging pixel elements, a new architecture was created with a pixel that discharges logarithmically [5].

The logarithmic pixel is much more sensitive than the linear pixel architecture, which usually has three or four decades of dynamic range. The logarithmic pixel, on the other hand, has six to seven decades of dynamic range [21]. This means that an image captured by an image sensor with this pixel architecture can show high contrast light changes within an image.

The drawback of the logarithmic pixel design is that the pixel is constantly being charged by at least one transistor. This can lead to a high amount of power being discharged by the pixel as compared with other CMOS architectures.

2.3 Support Circuitry

The CCD image sensor array has had many advantages over CMOS image sensors. The goal of CMOS image sensor research has been to have CMOS performance on par with CCD and then include A/D converters, image processing, or other useful circuitry on the same chip. This would make CMOS cameras less expensive to produce, because all of the functionality could be placed on the same chip. This would add to the expected CMOS price advantage because of the expense of the CCD process and the lack of specialized foundries [1]. This combination would further increase the power consumption edge that CMOS has on CCD which has allowed CMOS cameras to be
embedded in power sensitive electronics such as laptop computers, PDAs, and cell phones.

This section will cover parts of CMOS imagers that are not a part of the image sensor array. The correlated double sampling (CDS) process has an on-chip parallel in CCD, but the other circuitry cannot be implemented using the CCD process and requires secondary support chips. Additional functionality embedded on an imager and camera-on-chip architectures is an active area in the research community. This is a short list of features that are commonly seen in literature and does not encompass all support circuitry that can be found on a imaging chip.

### 2.3.1 Analog / Digital Converters

Analog-to-digital converters are used to convert the signal of a photo-sensor into a format that a computer can read. These converters must be made in a CMOS process, which means that they cannot be included on a chip with a CCD imager array. Placing the A/D converter on the same chip as the imager eliminates having to place an analog signal across a transmission line. By using the digital signal, the design gets a higher SNR over the transmission line off of the chip. The higher SNR allows the the imager to move data across the same transmission line faster. This is similar to the difference in speed between a modem and a DSL connection.

One drawback of putting an A/D on the same chip as the imaging array is that digital circuits can create noise that corrupts an analog signal. This noise can be reduced by design considerations such as separate analog and digital power connection and segregating the analog and digital circuitry to separate areas of the chip.
2.3.2 Correlated Double Sampling

Correlated double sampling (CDS) is an open loop way to remove low frequency noise from a circuit. There have been many different architectures proposed for this process in CMOS circuitry. Rather than talk about a specific architecture, this section will present the general concept of correlated double sampling. A simple CDS circuit is shown in Fig 9.

![CDS Circuit Diagram](image)

**Fig 9: Example CDS Circuit**

In CMOS circuitry, this process will usually involve two transistors used as switches and two capacitors used as analog memory. When the circuit is reset, one of the capacitors is allowed to sample the output signal of the pixel. Just after the reset has completed, the voltage on one of the capacitors is latched by closing the transistor. The other capacitor is then connected to the output of the circuit and allowed to sample the output of the pixel buffer. After the image has been acquired, the transistor switch is
closed and the voltage on the capacitor is held. At this point, the voltages are subtracted and the value is sent to an A/D as the final voltage of the circuit [18].

This circuitry eliminates nearly all reset and most fixed-pattern noise from an image which is its intended usage. This sampling also removes random image noise from the image, because the CDS process is similarly taking two images then averaging the images together. To further eliminate random noise, some designs have gone to a multi-sampling process taking more than two samples [16, 23].

CDS circuitry does a good job at reducing overall image noise. However, the capacitors required for CDS can be quite large, and it may be impossible to have a per-column CDS scheme. These CDS schemes cannot be implemented in high resolution or video image. To drive the capacitance of the CDS unit, circuits must be designed to consume more power.

2.3.3 Row Decoders

Due to the high resolution of some imager arrays, it is impossible to send a select signal directly to a row from an external pin. Instead, designs use a n-bit binary number to address each row. That number is then sent to a large array of n-input NAND or NOR gates which are set so only one will be active at a time. This decoder design is similar to row decoders for RAM arrays in most architectures.

Other architectures do not stop at a simple row decoder. Many designs include clock generators and counters on the chip. This allows the design to use fewer pins which provides extra pins for a higher resolution image sensor or as a control line for other support circuitry.
2.3.4 Image Processing

Higher resolution images are desired for many reasons. However, with a higher resolution image, there will be extra data that will need to be read out and stored into memory. For this reason, designs have begun to place compression circuit on an imager chip [11, 12]. Compression algorithms can be processor intensive and time consuming, so doing this compression on the imager can free up processor resources, which can be very important in real-time and embedded systems. There are also many imaging applications that require an analysis of an image rather than an image itself [13, 14]. A few designs have this processing built into the image sensor rather than doing the processing off chip.
Chapter 3. Proposed Architecture

The focus of this thesis will be on a novel column sensor design shown in Fig 10 and its performance when compared with other designs found in the literature. This thesis builds a small 4X4 pixel array to prove the performance of this circuit and shows the accommodations that are needed to support this architecture. The imager will have a row decoder, and each column will have its own A/D converter.

![Proposed Amplifier Architecture](image)

*Fig 10: Proposed Amplifier Architecture*

The three transistors in the APS circuit were examined, and it was decided to make the pixel as small as possible with the largest fill factor. Due to design rules, this
leads to transistor sizes, for the transistors labeled M1 and M2 in Fig 10, to have a width of 1.05 um and a length .35 um. Due to the mirroring, this leads to M3 and M4 having the same size. The switch transistors, M9, M14, M15 and M16, have minimum sizing to reduce the effects of switching noise. M5 needs to have a large w/l ratio because it is the current source for the differential amplifier and lower resistance allows for increased voltage swing. M6 and M7 were designed to create a .8 V bias for M5. The current mirror load transistors, M12 and M13, were chosen to be the same size as M1, because smaller transistors would reduce the overall voltage swing while the capacitance larger transistors would affect the performance of the circuit. All of the transistor sizes are shown in Table 1.

\textit{Table 1: Sizings of Transistors for the Column Amplifier}

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L um</th>
<th>Transistor</th>
<th>W/L um</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,M3</td>
<td>1.05/.35</td>
<td>M9,M14</td>
<td>.475/.35</td>
</tr>
<tr>
<td>M2,M4</td>
<td>1.05/.35</td>
<td>M15,M16</td>
<td>.475/.35</td>
</tr>
<tr>
<td>M5,M7</td>
<td>5.25/.35</td>
<td>M12,M13</td>
<td>1.05/.35</td>
</tr>
<tr>
<td>M6</td>
<td>.35/3.15</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Correlated double sampling, as discussed earlier, is a popular technique to eliminate noise from the output of an image sensor. Older CDS circuit designs are not as effective in the lower voltage range environments commonly found in current IC technologies. Current research has focused on how to implement CDS in the new low-swing environment [18] and the attenuation of the sources of fixed pattern noise before CDS [24]. This design continues in the research area by presenting a technique to cancel DC offset without the use of CDS.
3.1 Circuit Design

This design begins with the use of a N-well photo diode as the photo-sensor. This was chosen due to its high sensitivity and simplicity to manufacture. The drawback to this sensor is it has a lower signal to noise ratio than a photo-gate or a pinned photo diode. The pixel uses the standard 3-T photo diode pixel from Fig 8. Transistors M1, M2 and M14 make up the three transistors of the 3-T pixel. However, instead of being connected to a VDD, the reset transistor is now used as a switch for a feedback loop. The buffer and the select transistors are now a part of the differential column amplifier. Three transistors, M1, M2 and M14, are the only transistors that are located within the pixel. This allows the photo diode to be larger, giving each pixel a good fill factor.

The rest of the transistors are found outside of each pixel in the column level circuitry. As shown in Fig 10, transistors from a differential amplifier are used to both reset and read out the value of the photo diode. The amplifier is controlled by six transistors labeled M2, M4, M9, M14, M15 and M16, which act as switches. These transistors are controlled by four input signals labeled RST, RSTN, CS and CS2. CS is the row select line for the pixel that allows the user to select a pixel in the column that will be connected to the column-level circuitry. CS2 is the column select signal for the amplifier. If a design only needed to address one pixel at a time instead of an entire row, this transistor could be used to turn off the unwanted columns. During long integration time, this transistor can be used to turn off the amplifier and save power. For the proposed design, this transistor will always be in the on state and is only included to keep symmetry in the differential amplifier.
The RST and RSTN signals control the input terminal polarity and the feedback loops in the amplifier. If the RST signal is high and the RSTN signal is low, the feedback loop connected to VIN is enabled, while the current mirror load transistor M16 is enabled by the low voltage of RSTN. This setup makes the VOUT terminal positive input, while VIN is connected in a unity negative feedback configuration. This allows the circuit to accomplish a soft reset as described in [19].

When the RST line is low and the RSTN line is high, the VIN side of the amplifier is the positive input terminal, and the feedback loop connected to VOUT is enabled. In this configuration, the VIN terminal is now the positive input terminal and VOUT is connected in a unity negative feedback form. The pixel voltage can be read though the column amplifier and passed along for further processing.

The design of the proposed architecture began with the ACS design [10], and the hard/soft reset scheme found in [19] could be incorporated into one circuit. The new column sensor is not much more complex than the original ACS architecture, and should provide the benefits of both architectures. This design should provide some attenuation of reset noise due to its negative feedback scheme during reset [19, 26]. This circuit may not achieve the large reset noise reduction as was realized in the previous hard/soft reset architecture[19], because of the single stage amplifier. However, a slight reduction of reset noise, while only adding three transistors to the overall design should be a good tradeoff. During output, the proposed circuit unity feedback eliminates all gain variations due to transistor mismatch that was corrected with the ACS circuit. A final benefit of this design, in theory, is that by resetting and reading the pixel through the same amplifier, DC offset should be eliminated. The scheme can capture the amplifier's DC offset on the
pixel during reset. Since the 3T APS discharges the voltage linearly, when the pixel is read out by the amplifier, the voltage on the pixel has been adjusted for the DC offset. This is similar to correlated double sampling as described in [17].

This circuit will implement a two-to-four row decoder to address the pixels in the 4X4 pixel array. Due to the size of the array, the decoder was built with two input CMOS NOR gates. Most decoders are built using pseudo-NMOS design with buffers, which is done to save space in large arrays, but a pseudo-NMOS design does not make sense for an array this small. However, an adjustment to the regular decoder must be made for it to perform correctly. In Fig 10, the signal connected to M14 and M15 are the same. This is a correct configuration if each column amplifier only had one pixel in each column. For a column with more than one pixel, the control signals for M14 and M15 must be transmitted on separate lines.

The A/D chosen for this design was a single line output delta sigma A/D similar to the one found in [15]. An instance of this A/D will be connected to each of the column amplifiers through a transmission gate. The A/D has a sampling capacitor which initially captures the input signal on the capacitor while the RST going to M17 and M18 in Fig 11 is high. When RST is switched to low, the current voltage is locked and the A/D conversion begins. The A/D consists of two different amplifiers, and the A/D is controlled by a dual-phase clock. The first amplifier is a digital comparator or a single bit A/D converter. This amplifier compares the voltage of the capacitor to a reference VB2, which is a DC signal, and provides a digital 0 if the input is higher than the reference and a 1 otherwise. The output of the comparator is fed into the second amplifier, which is used to charge or discharge the capacitor for the next comparison by the A/D. By doing
this, the A/D circuit will generate a pulse with modulated (PWM) digital output signal which is different for every voltage placed in the comparator.

Fig 11: Delta Sigma A/D [15]

The size of the transistors in Fig 11 began with M7, M17, M18 being minimum size, because these transistors are used as switches. The minimum size reduces the non-ideal effects of switching on the overall circuit. Both of the capacitors, C1 and C2, were created by MOS capacitors. C1 is an integration capacitor, so the overall size of the transistor was large. C2 is used as analog memory on the gate of M13, so the transistor does not need to be as large as C1. The rest of the transistor sizes began with the W/L ratios of 3/1 for NMOS and 9/1 for PMOS transistors to adjust for the differences in
mobilities of the transistors. When the circuit was simulated with these transistor sizes, the voltage of the integrator changed at different rates depending on the value of the comparator. The size of the PMOS transistors was then adjusted to compensate for this nonlinearity, and the resulting component sizes are shown Table 1a.

Table 1a: Transistor Sizes for the A/D Converter

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L um</th>
<th>Transistor</th>
<th>W/L um</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 M2 M3 M4</td>
<td>2.1/.35</td>
<td>M7 M17</td>
<td>.475/.35</td>
</tr>
<tr>
<td>M5 M6 M8</td>
<td>1.05/.35</td>
<td>C1</td>
<td>1.65/1.65</td>
</tr>
<tr>
<td>M10 M11 M13 M14</td>
<td>2.1/.35</td>
<td>C2</td>
<td>.875/.875</td>
</tr>
<tr>
<td>M15 M16</td>
<td>1.05/.35</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.2 Modes Of Operation

3.2.1 Soft Reset

During soft reset, the positive terminal of the amplifier is connected to the signal labeled VOUT in Fig10 and Fig 12. While this is happening, a feedback path is opened to the photo diode. During this time, a reference voltage can be placed on this input to charge one of the photo diodes in the column. Once the pixel has been charged, the signal connected to M14 can be set low for the pixel disconnecting the feedback to the diode. A short period after the CS signal can be set low, fully disconnecting the pixel from the amplifier. At this time, the pixel can begin collecting light while the next pixel in the row is being reset. This functionality is similar to the functionality described in [19].
Fig 12: Simplified Column Amp During Reset

3.2.2 Pixel Readout

During pixel readout, the column amplifier will have to be switched, so that the positive terminal of the differential amplifier is connected to the pixel. VOUT is connected to the feedback as shown in Fig 13. In this mode, the value of the pixel can be read out and passed along to the ADC for conversion. At this time, this circuit's topology resembles the active column sensor found in [10].
3.2.3 Changing Between Modes

For any circuit, it is difficult to explain waveforms pertaining to operation. This section will provide Fig 14 to show how the amplifier is switched into its different modes of operation. This design has a rolling shutter, which means as one pixel is being reset, other pixels are collecting light for the next image or waiting to be reset.
Chapter 4. Prototype Design and Results

4.1 Simulation Results

4.1.1 Column Sensor

The column sensor is the main focus of this thesis and the novel idea presented in this paper. This section shows the collection the operational parameters for the design as proposed in chapter 3. The proposed reset/readout scheme was tested in simulation and compared with an ACS circuit to show the improvement of noise margin due to DC offset. Finally, the limitations of this circuit will be shown.

DC sweeps were done on the design to find the voltage transfer curves from input to output. This simulation show the region of the unity voltage gain at both input and output. The results of these simulations yield the operational voltage range of the image sensor. Fig 15 and Fig 16 show the unity gain range of the amplifier from 2.4 to approximately .5 volts. Since the offset is being stored on the pixel capacitor this range is further reduced by .2 volts of minimum and maximum bringing the final operation range of 2.2 to .7 volts.
Fig 15: DC Sweep of Readout
An AC sweep of the amplifier was done from both the input and the output of the circuit. AC analysis is usually done to obtain Bode plots, which show the stability of an operational amplifier. However, here the AC sweeps are useful in establishing the frequency range where amplifier maintains unity gain. Again, 50 fF was assumed as the capacitance of the diode, and a MOSCAP has been connected to the VOUT line as the load from the A/D. Figures 17 and 18 show the results from the AC analysis.

Fig 16: DC Sweep During the Reset Phase
Fig 17: AC Analysis of Pixel Reset
Fig 18: AC Analysis of Pixel Readout

At this point, the maximum voltage swing and the frequency of operation of the amplifier have been established by the previous simulations, and these numbers have been compiled into Table 2.

Table 2: Performance of the Prototype Architecture

<table>
<thead>
<tr>
<th>Column Sensor</th>
<th>Input Range(V)</th>
<th>Max Frequency of Reset(MHz)</th>
<th>Max Frequency of Readout (Mhz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.7 – 2.2</td>
<td>13.7</td>
<td>13.1</td>
</tr>
</tbody>
</table>
Once the basic operational conditions of the amplifier were established, the next step was to simulate the circuit to observe the performance of the reset/readout schemes for DC offset correction. To create the DC offset, the VTH0 parameter of each transistor was varied by a 5% tolerance and run through Monte Carlo as described in [24]. A transient simulation was then set up, so that initially the amplifier is in reset mode and is charging the pixel that is represented by a 50fF capacitor. After the pixel is charged, the amplifier is switched into readout mode, and at this time the voltage of the pixel can be read on the output terminal. The simulation was run with five different reset voltages. The simulations were run at 27 C and 125 C to show how temperature affects this design. The data collected in these simulations could then be used to create a voltage transfer curve from reset to readout. An example of a run of this simulation is shown in Fig 19.

![Monte Carlo Simulation example](image.png)
Each simulation consists of 50 curves in each Monte Carlo run. The maximum, mean and minimum voltage ranges were from the graph, and data in Table 3 was obtained by using the cursor at 100ns after reset. This data was used to create the voltage transfer curve of the amplifier from reset to readout. Voltage transfer is usually obtained though a DC sweep. However, since reset and readout use the same terminal, transient analysis must be used.

Table 3: Monte Carlo Simulation Results of Prototype

<table>
<thead>
<tr>
<th>T=27 C + -5% VTH0</th>
<th>Max</th>
<th>Mean</th>
<th>Min</th>
<th>Max-Min</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.200000</td>
<td>2.18890</td>
<td>2.18570</td>
<td>2.18170</td>
<td>0.007200</td>
</tr>
<tr>
<td>1.800000</td>
<td>1.77140</td>
<td>1.76790</td>
<td>1.76460</td>
<td>0.006800</td>
</tr>
<tr>
<td>1.400000</td>
<td>1.34220</td>
<td>1.33920</td>
<td>1.33440</td>
<td>0.007600</td>
</tr>
<tr>
<td>1.000000</td>
<td>0.91679</td>
<td>0.91203</td>
<td>0.90799</td>
<td>0.008800</td>
</tr>
<tr>
<td>0.700000</td>
<td>0.59700</td>
<td>0.59412</td>
<td>0.59155</td>
<td>0.005450</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>T=125 C + -5% VTH0</th>
<th>Max</th>
<th>Mean</th>
<th>Min</th>
<th>Max-Min</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.200000</td>
<td>2.20040</td>
<td>2.19070</td>
<td>2.16540</td>
<td>0.035000</td>
</tr>
<tr>
<td>1.800000</td>
<td>1.77590</td>
<td>1.76300</td>
<td>1.75930</td>
<td>0.016600</td>
</tr>
<tr>
<td>1.400000</td>
<td>1.34220</td>
<td>1.33710</td>
<td>1.33230</td>
<td>0.009900</td>
</tr>
<tr>
<td>1.000000</td>
<td>0.90888</td>
<td>0.90573</td>
<td>0.90128</td>
<td>0.007600</td>
</tr>
<tr>
<td>0.700000</td>
<td>0.59700</td>
<td>0.59573</td>
<td>0.57926</td>
<td>0.022450</td>
</tr>
</tbody>
</table>

For comparison of offset, a second amplifier was constructed based on the design in [10] and shown in Fig 20. This circuit was chosen because it was the initial basis for the new design presented in the thesis, and the two designs are fairly similar. Each of the transistors in Fig 20 has the same size as its counterpart with the same label in Fig 10. The values for the W/L ratios for these transistors can be found in Table 1.
Fig 20: ACS for comparison [10]

The simulation for comparison applies the same values of the reset signal directly to the VIN terminal. The same 5% tolerance on VTH0 was applied to all of the transistors in the circuit, and the results were collected and can be found in Table 4.

The results from Tables 3 and 4 show that the new switching amplifier design eliminates most of the offset caused by transistor mismatch. From the tables, the voltage transfer curves for both amplifiers were constructed. When plotting the voltage transfer curves, it was hard to see the difference that the bi-directional amplifier (BDA) makes in offset compensation.
Table 4: Simulation results For the ACS amplifier [10]

<table>
<thead>
<tr>
<th>T=27 C +5% VTH0</th>
<th>Max</th>
<th>Mean</th>
<th>Min</th>
<th>Max-Min</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.200000</td>
<td>2.235800</td>
<td>2.198900</td>
<td>2.155800</td>
<td>0.080000</td>
</tr>
<tr>
<td>1.800000</td>
<td>1.844200</td>
<td>1.804400</td>
<td>1.765100</td>
<td>0.079100</td>
</tr>
<tr>
<td>1.400000</td>
<td>1.432300</td>
<td>1.403300</td>
<td>1.376300</td>
<td>0.056000</td>
</tr>
<tr>
<td>1.000000</td>
<td>1.030000</td>
<td>1.009600</td>
<td>0.982270</td>
<td>0.047730</td>
</tr>
<tr>
<td>0.700000</td>
<td>0.734230</td>
<td>0.707180</td>
<td>0.661730</td>
<td>0.072500</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>T=125 C +5% VTH0</th>
<th>Max</th>
<th>Mean</th>
<th>Min</th>
<th>Max-Min</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.200000</td>
<td>2.254600</td>
<td>2.202900</td>
<td>2.160200</td>
<td>0.094400</td>
</tr>
<tr>
<td>1.800000</td>
<td>1.842900</td>
<td>1.802400</td>
<td>1.775700</td>
<td>0.067200</td>
</tr>
<tr>
<td>1.400000</td>
<td>1.437600</td>
<td>1.400600</td>
<td>1.362600</td>
<td>0.075000</td>
</tr>
<tr>
<td>1.000000</td>
<td>1.049500</td>
<td>1.008000</td>
<td>0.975490</td>
<td>0.074010</td>
</tr>
<tr>
<td>0.700000</td>
<td>0.756760</td>
<td>0.712570</td>
<td>0.665610</td>
<td>0.091150</td>
</tr>
</tbody>
</table>

This led to plotting the variation in the offset, which is shown in Figures 23 and 24. The data shows that the ACS architecture without CDS has an offset difference between 50mV- 0.1V, while the BDA has less than 10mV of variation in all simulations under nominal conditions.

Proposed Design Transfer Curve 5% Vth0 at 27 C

![Proposed Design Transfer Curve 5% Vth0 at 27 C](image)

Fig 21: Voltage Transfer Curve for the Proposed Design
The results from Figures 21 and 22 show the expected range of values that the BDA design and ACS without CDS can have at the simulated input voltages. The uncertainty in the graphs shows the expected fixed-pattern noise margin due to DC offset in each of these circuits. Therefore, the closer the line are together shows a reduction in the noise margin. The two graphs show that the BDA architecture can compensate for most DC offset variations that have been caused due to transistor mismatch.

![ACS Transfer Curve 5% Tolerance Vth0 at 27C](image)

*Fig 22: Voltage Transfer Curve for ACS [10]*

It can also be noted from Fig 21 that there is a loss of voltage shifting the transfer curve downward slightly. This is due to the added MOS switches inside the circuit. While this added noise source is accounted for in the simulation, further attempts to reduce this noise may improve the performance of the bi-directional amplifier.
It is shown that the BDA outperforms ACS in Figures 21 and 22. For a head to head comparison, the noise margins of both circuits were graphed in Fig 23. The graph shows that the BDA architecture reduces noise margin due to offset to under 10mV in all simulated cases, while the ACS best case noise margin is approximately 48mV. The results from ACS paper show that even after CDS the ACS circuitry has about a 4 mV noise margin [10]. Putting the improvement of the BDA architecture in terms of signal to noise ratio, the ACS design has a signal output range of 0.5-2.7 V with a noise margin of 0.0477-0.08 V. This translates into a simulated SNR between 31.88 - 28.78 dB. The BDA
has an output range of .7-2.2 V and a noise margin of .0054-.0088 V. Thus, the simulated SNR of the BDA is 48.71 - 44.63 dB

![Offset Range/Reset Voltage 5% tolerance at 125C](image)

**Fig 24: Noise Margin Comparison at High Temperature**

A second test was performed to show how well the BDA architecture performed under high temperatures. The noise margins of the BDA are still smaller than those of the ACS without CDS, but the BDA did not perform as well at the edges of the voltage range. This was due to the voltage on the pixel falling outside the maximum range of operation after reset. However, it is unclear whether this was caused by the higher Vt or increased switching error in the simulation. In terms of SNR, the ACS has a range of 30.32-27.38 dB, while the BDA shows a simulated noise ratio of 45.91-32.64 dB.
A third test was created by connecting a resistor to the input gate to simulate discharge during photon collection. A large resistor was connected to the VIN terminal along with the 50 fF capacitor. This simulation shows one weakness of this approach, which is that discharge of the diode must be linear for the bi-directional amplifier to work correctly. Any nonlinearity in pixel discharge adversely affects the ability of the architecture to compensate for DC offset. From Fig 25, as the voltage envelope on VIN drops from .1V to 60 mV, the envelope of VOUT increases from about 10 mV to 40 mV. This is an issue with correlated double sampling as well.

### 4.1.2 Pixel Array with Column Sensor

The performance characteristics for the bi-directional amplifier were established in the last section. However, the circuit pictured in Fig 26 was used to show that the
The proposed amplifier can work effectively as a column amplifier. The amplifier was split into the 3-T pixels, which are represented by the smaller square boxes, while the rest of the column amplifiers are in the rectangular boxes.

This circuit was simulated by applying a 2.2 volt signal to the VOUT terminal of the column amplifier while each of the pixels are strobed for reset, thus resetting the image sensor. After a reset, the voltage on a pixel should be the same as the voltage on the VOUT terminal with some slight attenuation as shown in Fig 27.
Fig 27: Pixel Array Simulation

Fig 27 shows the way that the pixel array should act when connected to the row decoder. The results of this simulation shows that the entire pixel array can be reset in about 200 ns. This simulation also shows that the BDA can be connected in a column sensor scheme and can be used to reset the pixels in the image sensor without the pixels discharging as the column amplifier is connected to the next row.
4.1.3 Row Decoder

The row decoder is a fairly common circuit and is standard in RAM design. This design uses all CMOS gates rather than their pseudo-NMOS counterparts, because of the pixel array size. As shown is Fig 28, the column decoder was built using two input NOR gates.

Fig 28: Row Decoder Schematic

The added AND gates are used to control the reset signal to each pixel. All of the transistors in the first set of inverters have a 1.05 um width and .35 um length. This setup does not yield optimum rise and fall times, but due to the layout design rules, it allows for the most transistors to be packed in the tightest amount of space. The circuit
was simulated with a 100 fF capacitive load on each of the outputs, and the rise and fall time results were collected in Table 5.

*Table 5: Row Decoder Performance*

<table>
<thead>
<tr>
<th>Row Decoder</th>
<th>Rise Time CS (ns)</th>
<th>3.06</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise Time CS (ns)</td>
<td>1.07</td>
<td></td>
</tr>
<tr>
<td>Rise time RST (ns)</td>
<td>0.39</td>
<td></td>
</tr>
<tr>
<td>Fall Time RST (ns)</td>
<td>0.26</td>
<td></td>
</tr>
<tr>
<td>Max Frequency (Mhz)</td>
<td>242</td>
<td></td>
</tr>
</tbody>
</table>

### 4.1.4 A/D

The Delta-Sigma A/D circuit shown in Fig 11 was used for this design with two modifications. The first modification was to replace the pass transistor used to disconnect the A/D from VIN with a full transmission gate. The second modification was MOSCAPs for C1 and C2. Using MOS capacitors was the only efficient way of making C1 and C2 using the TSMC 0.35um process. The capacitor change allows the IC layout tool to do a full Layout vs Schematic check on the circuit. The overall design was simulated to find the conversion speed for maximum and minimum voltages. The A/D circuit's bias and clocking scheme was then fine tuned to obtain the desired effective number of bits in A/D resolution. The simulation in Fig 29 begins with a 40 ns period to allow the MOSCAPs in the circuit to charge. Then the input path is closed, which allows the A/D to convert the input voltage to a digital output. The simulation is run until the signal is flipped from a logic value of 0 to a logic value of 1 for the maximum possible voltage at each end of the range.
Figs 29: Maximum Input Voltage Conversion

During one of the conversion simulations, a section was zoomed in on. The voltage on the MOSCAP was taken during two successive samples, and the effective number of bits was extrapolated from the data obtained.

Fig 29 shows the conversion of a 3.3 volt input into a digital signal. From this simulation it was shown that the A/D needs about 720ns after reset to do the full A/D conversion. Also, from this simulation the effective number of bits could be calculated using the difference in voltage on the integration capacitor between two consecutive samples. When this was done, the effective number of bits for the 0-3.3V range was found to be 8. After the A/D was shown to work properly, the biases and clocks were
adjusted to allow for an 8-bit A/D over the range of operation. The clocking scheme and bias data for the A/D can be found in Table 6.

![Analog Trace Chart]

**Fig 30: Conversion Simulation for Effective Number of Bits**

From Fig 30, the effective number of bits was calculated by taking the voltage of the integration capacitor after two successive comparisons. The number of bits was then calculated by dividing the full voltage range over the difference of the integrator. From this calculation, the effective number of bits was found to be 8. This number of bits was the same as the amount of bits found in paper [15]. Initially, the A/D was simulated for the full rail to rail range of TSMC0.35um 0-3.3 to establish that the design worked in simulation. When the effective number of bits was calculated over the operational range
of the bi-directional amplifier, the A/D only had a 6-bit resolution. The bias values and clock scheme were then changed to yield 8-bit resolution over the range of the BDA. The values for both A/D setups are shown in Table 6.

<table>
<thead>
<tr>
<th>Voltage range (V)</th>
<th>A/D full voltage range</th>
<th>A/D for image array</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vbias1</td>
<td>2.45</td>
<td>2.49</td>
</tr>
<tr>
<td>Vbias2</td>
<td>1.65</td>
<td>1.35</td>
</tr>
<tr>
<td>Phi1 Period (ns)</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Phi1 On (ns)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Phi2 Period (ns)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Phi2 On (ns)</td>
<td>2.2</td>
<td>1</td>
</tr>
<tr>
<td>Conversion time (ns)</td>
<td>720</td>
<td>720</td>
</tr>
<tr>
<td>Effective Number of Bits</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

### 4.1.5 Full Design

The overall image sensor design schematic is shown in Fig 31. This schematic includes all of the circuitry previously discussed in this chapter. The design consists of the row decoder to the far left of the image. The image sensor array is in the middle of Fig 31. There are also 4 A/D converters, one attached to each column and are on the left.
Using this schematic, both reset and readout simulation were performed, the results of which are in Figures 32 and 33. The performance test yielded the same results as the simulations depicted in Figures 26 and 28, which show that the array can be reset in 200 ns, and it takes about 720 ns to fully convert the output of one row from analog to digital. The difference between the simulations is the reset time of the A/D, which was increased to 100ns to allow for the column amplifier to charge the integration capacitor on the A/D instead of the simulated voltage source.
Fig 32: Overall Design Reset

Fig 32 and Fig 33 are a confirmation of the expected performance of the image sensor after all of the pieces of the sensor have been connected. Fig 32 shows the reset of a column in the sensor with a 2.2 volt reset signal. The row decoder is then allowed to reset each row of the image sensor. As expected from Fig 27, the rows are all reset to 2.2 volts. The switching noise of the overall circuit is more than what was expected from the previous simulation. The switching error shown in Fig 27 was less than 100 mV, while the simulation in Fig 32 shows a switching error of about 200 mV. Fig 33 shows the readout of the entire pixel array. Every row of the sensor array was set to 2.2 .7 2.2 .7 in the pixel and then was read out through the A/D converters.
Fig 33: Overall Design Readout

It is impossible to determine how many frames per second this image sensor can operate at without having a physical chip. It is possible from electrical simulation to show how fast the image sensor can be reset and how fast the imager can be read out in digital output and to use the data to extrapolate how fast a larger imager can operate. Simulation cannot yield a good integration time for photon collection. While integration time can be estimated, the quantum efficiency of the pixel may not be high enough to meet the estimate. Table 7 has the reset time and readout time data for the image sensor as well as some extrapolated numbers for the performance of a larger image sensor.
Rather than estimate integration time, the table gives the maximum amount of integration time that can be achieved for an image size while maintaining 60 frames per second.

Table 7: Overall Simulation Results and Extrapolated Data

<table>
<thead>
<tr>
<th>Sensor Size</th>
<th>Reset time</th>
<th>Readout time</th>
<th>Max Integration Time for 60 frames/sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>4X4</td>
<td>200ns</td>
<td>3.4us</td>
<td>16.64ms</td>
</tr>
<tr>
<td>1024X1024</td>
<td>51.2us</td>
<td>870.4us</td>
<td>15.72ms</td>
</tr>
<tr>
<td>2048X2048</td>
<td>102.4us</td>
<td>1.744ms</td>
<td>14.8652ms</td>
</tr>
</tbody>
</table>

4.2 Design Layout

The mask for this image sensor was designed using Mentor Graphics IC tool in the VLSI lab. The process used was the TSMC0.35um N-well CMOS process with digital design rules using the lambda measurement rule to create all cells. The process has one polysilicon layer and five metal layers. The single polysilicon layer means that all the capacitors needed for the A/D will have to be capacitor connected transistors. The lambda measurement rule is that each unit of lambda is one-half the length of the minimum feature size, or 2 lambda is .35 um for this process. This paper quotes the final sizes of measurements discussed in microns, but this may not be the case for design decisions made because of design rules. All of the physical layouts in this section have passed both a design rules check (DRC) and a Layout vs Schematic (LVS) check.

4.2.1 Pixel

The pixel's electrical simulation was incorporated in the simulation of the column amplifier, but it has a separate section for the pixel layout. The pixel shown in Fig 34 is the initial building block for an image sensor. It has three transistors, which are labeled
M1 M2 and M14 in Fig 10. The photosensitive element is the diode formed by the contact between N-well and Substrate.

Fig 34: Pixel Layout

This pixel is oddly shaped when compared to other pixel designs. The reason for the shape was a design rule that will be explained in the next section, but it is not an issue in research design for an electrical test. It is easy to see from Fig 34 that there is a large piece of metal covering the transistors in the pixel. This is the metal five layer, and it will be used exclusively as a light shield for the circuit. The pixel itself has a fill factor of 31%, which is good for a CMOS image sensor. The measurements of this design can be found in Table 8.
Table 8: Pixel Layout Data

<table>
<thead>
<tr>
<th>Pixel Cell</th>
<th>Size (lambda^2)</th>
<th>Size (um^2)</th>
<th>Fill Factor</th>
<th>Transistors per Pixel</th>
<th>Detector Type</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>44X66</td>
<td>7.7X11.5</td>
<td>31.12%</td>
<td>3</td>
<td>N-well Photo-diode</td>
</tr>
</tbody>
</table>

For comparison, Table 9 has been included with pixel sizes and fill factors where possible. These designs are from research cameras found in the literature. The table lists the size of the pixels and shows the feature size of the technology used to create each camera.

Table 9: Pixel Size Chart

<table>
<thead>
<tr>
<th>Pixel Design</th>
<th>Technology</th>
<th>Size (um^2)</th>
<th>Fill Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thesis Design</td>
<td>TSMC 0.35um</td>
<td>7.7X11.5</td>
<td>31.16%</td>
</tr>
<tr>
<td>Digial [15]</td>
<td>1.2(um)</td>
<td>60X60</td>
<td>2.91%</td>
</tr>
<tr>
<td>Photogate[4]</td>
<td>0.8(um)</td>
<td>16X16</td>
<td>35.00%</td>
</tr>
<tr>
<td>APS [19]</td>
<td>.5um</td>
<td>10X10</td>
<td></td>
</tr>
</tbody>
</table>

4.2.2 Pixel Array

The pixel array is closer to a 1:1 ratio than the singular pixel itself. This is due to the TSMC0.35um design rule that two wells of different potential must be at least 18 lambda (~3um) apart. This makes the array more square and cuts into the fill factor of the overall sensor array. The pixel could be redesigned using doped N-active material. However, the array would lose quantum efficiency to some wavelengths of light due to shallow junction depth. The layout of the array is shown in Fig 33.
The size and new fill factor measurements for the pixel array are in Table 10. The new fill factor is smaller than that of each pixel. Yet the design still has a better fill factor than the digital pixel, and the overall size of the 16 pixels is smaller than 1 digital pixel [15].

**Table 10: Pixel Array Layout Data**

<table>
<thead>
<tr>
<th>Pixel array w/o Column Sensors</th>
<th>Size(λa²)</th>
<th>228X294</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (μm²)</td>
<td>39.9X51.45</td>
<td></td>
</tr>
<tr>
<td>Fill Factor</td>
<td>22.06%</td>
<td></td>
</tr>
<tr>
<td>Transistors count</td>
<td>48</td>
<td></td>
</tr>
</tbody>
</table>
4.2.3 Pixel Array with Column Sensors

The column cell includes all of the transistors from Fig 10 except M1, M2 and M14, which are in each pixel. The M6 and M7 transistors are not in the column sensor cell, because these transistors make the bias voltage for the current mirrors and can be shared by all of the columns in the array. Fig 36 shows the combined pixel array with the column sensor. Each column sensor is slightly larger than the pitch of each pixel. This led to a small routing channel to be included between the two cells to allow for proper connection. This means that each pixel could have been wider to better accommodate column level design.

![Image](Fig 36: Pixel Array with Column Sensor Layout)

The addition of the column sensors completes the circuit that was simulated in Fig 25. This cell and the rest of the cells presented in this section will not have the metal five
light guard drawn over the cell, so the circuitry within the cell can be be easily seen. The light guard will be drawn over the final layout. The size of this cell is shown in Table 11.

Table 11: Pixel Array with Column Sensor Size

<table>
<thead>
<tr>
<th>Pixel array with Column Sensors</th>
<th>Size (lambda*2)</th>
<th>Size (um*2)</th>
<th>Transistors count</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>288X396</td>
<td>50.4X69.3</td>
<td>80</td>
</tr>
</tbody>
</table>

4.2.4 Row Decoder

This cell is the realization of the schematic shown in Fig 28. This circuit is used to address all of the pixels in the array. It allows the four CS and the four RST signals to be controlled by three external lines. The physical layout of this circuit is shown in Fig 37.

Fig 37: Row Decoder Layout
The row decoder is much larger than expected compared to the overall design. This is due to the small pixels and the extra AND gate that must accompany every row to properly address the pixels during reset. The design is larger than expected. However, it matches well with the pixel array making the connection of the two circuits much easier. The size of this decoder is shown in Table 12.

Table 12: Row Decoder Layout Data

<table>
<thead>
<tr>
<th>Row Decoder</th>
<th>Size(λ^2)</th>
<th>Size(μm^2)</th>
<th>Transistor Count</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>216X426</td>
<td>37.8X74.5</td>
<td>44</td>
</tr>
</tbody>
</table>

**4.2.5 A/D Converters**

The A/D is the most complex circuit in the design and is shown in Fig 38. The circuit only has 21 transistors, but there is no regular structure for the connections, making the circuit harder to route.

![Fig 38: Analog to Digital Converter Layout](image-url)
The sizing of the transistors varies greatly due to the 2 MOSCAPs in the circuit used for integration and to hold voltage for the D/A. These facts lead to the large open spaces within the cell. The size of the A/D is shown in Table 13.

<table>
<thead>
<tr>
<th>A/D Size</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (λ^2)</td>
<td>127X167</td>
</tr>
<tr>
<td>Size (μm^2)</td>
<td>22.2X29.225</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>21</td>
</tr>
</tbody>
</table>

**4.2.6 Full Design**

The overall design is shown in Fig 39 and Fig 40. Routing was an issue in this design due to the fact that the pixel was designed first and then the supporting circuitry was attached. The space between the A/D and the image sensor could have been better used for making the photo diode of each pixel larger. A better floor plan for this circuit would have been to start with the column amplifier and the decoder. From that point, the pixel and the A/D could have been designed to fit in tightly with the other circuitry. The large amount of space between the A/D and the pixel array has the benefit of isolating the analog and digital parts of the circuit, thereby reducing the amount of digital crosstalk that the pixel array would encounter.
Table 14 has the overall size of the design. The design is dominated by support circuitry. The pixel array only takes up 16% of the overall design space. Production image sensors have at least 50% of the physical space dedicated to the pixel array.

**Table 14: Overall Imager Size**

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size(λ^2)</td>
<td>617X675</td>
</tr>
<tr>
<td>Size (μm^2)</td>
<td>107.9X118.1</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>210</td>
</tr>
</tbody>
</table>
To finish the design, a layer of metal five was used to shield the transistors that were close to the pixel from light. The layout in Fig 40 is what would be used if this sensor were to be fabricated.

*Fig 40: Overall camera with Light Shield*
Chapter 5. Conclusion

This thesis investigated a novel way to reduce fixed pattern noise within a CMOS image sensor by resetting and reading pixels though the same amplifier. This process captures the amplifier's DC offset on the pixel and eliminates the offset when the pixel was read back though the amplifier. This design reduces the need for CDS by nearly eliminating the effects of a major noise source before reaching a sampling circuit, since the CDS unit will only have to compensate for reset noise.

The bi-directional amplifier has been shown to work as a column sensor from this thesis. The soft reset/readout system has been shown in Monte Carlo simulation to reduce DC offset that was caused by changes to Vth0 over a 5% tolerance. The simulated SNR of the bi-directional amplifier ranged from 44.63 dB to 48.71 dB. This is an improvement when compared to an ACS design with the same device sizing, which yields a SNR range between 28.78 dB and 31.88 dB under nominal temperature. This comes at the cost of reduced output swing, because now the pixel needs extra margin to store DC offset. Further development may yield an amplifier that does not use as much of its voltage swing to store the offset. The results of the simulations show that the bi-directional amplifier does not compensate for non-linear pixel discharge, which is also a problem with CDS. Finally, this thesis shows that the overhead of the bi-directional amplifier's soft reset / readout scheme is small and should allow a large portion of image acquisition time to be dedicated to light collection.
Future work on this topic would be to construct an actual image sensor using the bi-directional amplifier as a column sensor. With an actual imager, performance characteristics such as dynamic range and image quality can be measured and compared with other architectures. Improvements can be made to the architecture, making the amplifier more resilient under high temperature operation. The BDA uses a negative feedback loop during soft reset to charge the pixel. From the literature, this negative feedback loop can reduce reset noise of the pixel [19, 26]. This thesis demonstrated the BDA's ability to remove DC offset from the output signal. Future work could modify the architecture so that both reset noise and DC offset are removed, thus eliminating the need for CDS.
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