Temperature Evaluation of NoC Architectures and Dynamically Reconfigurable NoC

Aniket Dilip Mhatre

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Temperature Evaluation of NoC Architectures and Dynamically Reconfigurable NoC

By

Aniket Dilip Mhatre

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Computer Engineering

Supervised by

Dr. Amlan Ganguly
Department of Computer Engineering
Kate Gleason College of Engineering
Rochester Institute of Technology
Rochester, NY
February, 2014

Approved By:

Dr. Amlan Ganguly
Primary Advisor – R.I.T. Dept. of Computer Engineering

Dr. Sonia Lopez Alarcon
Secondary Advisor – R.I.T. Dept. of Computer Engineering

Dr. Gill Tsouri
Secondary Advisor – R.I.T. Dept. of Electrical Engineering
Dedicated to my parents, (Late) Mr. Dilip Mhatre

and Mrs. Ranjana Mhatre
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Abstract

Advancements in the field of chip fabrication led to the integration of a large number of transistors in a small area, giving rise to the multi-core processor era. Massive multicore processors facilitate innovation and research in the field of healthcare, defense, entertainment, meteorology and many others. Reduction in chip area and increase in the number of on-chip cores is accompanied by power and temperature issues. In high performance multi-core chips, power and heat are predominant constraints. High performance massive multicore systems suffer from thermal hotspots, exacerbating the problem of reliability in deep submicron technologies. High power consumption not only increases the chip temperature but also jeopardizes the integrity of the system. Hence, there is a need to explore holistic power and thermal optimization and management strategies for massive on-chip multi-core environments.

In multi-core environments, the communication fabric plays a major role in deciding the efficiency of the system. In multi-core processor chips this communication infrastructure is predominantly a Network-on-Chip (NoC). Tradition NoC designs incorporate planar interconnects as a result these NoCs have long, multi-hop wireline links for data exchange. Due to the presence of multi-hop planar links such NoC architectures fall prey to high latency, significant power dissipation and temperature hotspots. Networks inspired from nature are envisioned as an enabling technology to achieve highly efficient and low power NoC designs. Adopting wireless technology in such architectures enhance their performance. Placement of wireless interconnects (WIs) alters the behavior of the network and hence a random deployment of WIs may not result in a thermally optimal solution. In such scenarios, the WIs being highly efficient would attract high traffic densities resulting in thermal hotspots. Hence, the location and
utilization of the wireless links is a key factor in obtaining a thermal optimal highly efficient Network-on-chip.

Optimization of the NoC framework alone is incapable of addressing the effects due to the runtime dynamics of the system. Minimal paths solely optimized for performance in the network may lead to excessive utilization of certain NoC components leading to thermal hotspots. Hence, architectural innovation in conjunction with suitable power and thermal management strategies is the key for designing high performance and energy-efficient multicore systems. This work contributes at exploring various wired and wireless NoC architectures that achieve best trade-offs between temperature, performance and energy-efficiency. It further proposes an adaptive routing scheme which factors in the thermal profile of the chip. The proposed routing mechanism dynamically reacts to the thermal profile of the chip and takes measures to avoid thermal hotspots, achieving a thermally efficient dynamically reconfigurable network on chip architecture.
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Chapter 1  Introduction

The increase in computational complexities has led to an ever increasing demand of fast and powerful computers. Such powerful computers are often used in fields like astrophysics, weather forecasting, bioinformatics, oil and gas exploration as well as high-end consumer electronics. In accordance with the Moore’s law the number of transistors packed in a single chip is increasing at a massive scale. However, the clock speed technology cannot match the same growth rate as that of the transistor technology due to exponential increase in power dissipation directly proportional to frequency. In order to satiate the hunger for computational power, chip designers need to come up with new and innovative techniques to build powerful computers. This led to the advent of the multi-core chip era. As the number of cores on chip increase, interconnects start playing an important role in the performance of the system. A lot of research has been put into making on-chip interconnection architectures better and reliable. However, the potential of wireless interconnects to design reconfigurable NoCs to mitigate dynamic thermal issues is yet to be fully exploited.

1.1 Multicore Systems-on-Chip

Traditionally the performance of the system was increased by increasing the clock frequency. As technology advanced the number of transistors that could be fabricated on a single chip increased. Figure 1-1 shows the increase in transistor count versus time as per the Moore’s law. [1] Clock speed is directly related to power consumption. Higher the clock frequency, higher is the power consumption. This makes them unsuitable for low power devices. At higher levels of integration clock speed became a bottleneck in obtaining fast and powerful systems. As
technology advanced flip-flop delay became comparable to the combinational logic delay. With options running out to obtain fast and powerful computers, multicore chips proved to be a promising alternative in increase the system performance. Parallel processing capabilities of multi-core chips make them faster as compared to a uni-core system operating at the same clock frequency. Comparatively lower power consumption makes multi-core systems ideal for low power applications.

![Microprocessor Transistor Counts 1971-2011 & Moore's Law](image)

**Figure 1-1-1 Growth in transistor count with time [1]**

With technology scaling the wire delays increase significantly. Figure 1-2 shows the increase in wire delay as transistor technology scales down. [2] Long-distance interconnecting wires between multiple cores on the highly integrated system-on-chip show higher delays due to relatively longer lengths resulting in higher resistances and parasitic capacitances. Traditional
bus-based interconnect fabrics like the IBM CoreConnect [3] and the ARM AMBA [4] do not scale effectively as the system size increases.

Figure 1-2: Gate and Interconnect Delay versus Technology Generation [2]

The high levels of integration on multi-core architectures and the consequent increase in delays for global communication have lead chip designers to explore new global interconnection architectures, giving rise to the Network-on-Chip (NoC) paradigm.
1.2 The Network-on-Chip paradigm

With the advent of the multicore era more and more cores were integrated on a single chip to exploit core level parallelism. But, as the number of cores increased length of the wires connecting the cores increased resulting in larger inter-core communication delay. Global wires do not scale in length with scaling in technology; rather there is an exponential increase in global wire delay as the technology scales down [5]. Even with repeater insertion, the wire delay may exceed a single clock cycle. Ultra-deep submicron processes show that 80% of delays on the critical paths are due to interconnects [6] [7].

To mitigate the scalability issues of multi-core chips, a modular interconnect network is adopted. In these modular networks the cores no longer form a part of the communication fabric. Such a paradigm is known as Network-on-Chip (NoC) [8]. The NoC separates the computational cores form the communication fabric thus, providing a plug-and-play network independent of the cores. Data is routed as packets via a series of network elements typically switches and links. In NoC architectures the global wires are replaced by the network interconnects, improving the scalability and performance of the system. Figure 1-3 shows a typical NoC architecture.
In NoC architectures typically one of the three switching techniques namely; Circuit Switching, Packet Switching, and Wormhole Switching are used to deliver data from the source to the destination. In circuit switching, dedicated links are established between the source and the destination. In order to use a specific link other nodes must wait until the ongoing communication on that link has completed. Thus, this makes circuit switching unsuitable for networks with high traffic.
In packet switching the message is broken into smaller elements known as packets. These packets are then routed through the network independent of each other. At the receiver end the packets are reassembled to form the original message. With packet switching the entire network is utilized efficiently increasing the efficiency of the system; however it places a huge overhead on the switches. Switches in the network have to process the packets to form the entire message, In order to accomplish this switches need to have larger buffers to store the packets as they may be received out of order. This increases the buffer size of the switches and in turn increases the total area of the architecture making them unsuitable for NoCs.

In wormhole switching, the packet is divided into smaller units called flits. The size of the flit is determined such that, each flit is delivered in a single cycle. Only the header flit contains the routing information. The header flit establishes the path across the network. The body flits follow the path setup by the header flit to reach the destination. The tail flit is last flit of any packet which signals the end of packet and thus is responsible for the release of the reserved channel. Since there is a dedicated established by the header flit, communication by other nodes utilizing that path is blocked until the channel is released. To alleviate this issue virtual channels are introduced. Packets which are blocked be routed along any other available virtual channel. If a header flit does not find any free virtual channel it is dropped, in this case the source needs to retransmit the header flit. Switches have buffers to store flits until a path is available for transmission. Figure 1-4 shows the structure of a typical NoC switch. Due to the efficient utilization of the network and comparatively smaller network area, wormhole switching is popular among NoC architectures.
1.3 Emerging Interconnection Networks

Traditionally planar metallic interconnects are used to transfer data over NoC architectures. As technology is scaling down wires are getting thinner and thinner leading to an increase in its resistance. Increase in resistance leads to increase in latency and significant increase in power consumption. Increasing power consumption can lead to high on-chip temperatures which in turn compromises the performance and reliability of the chip [10]. According to the International Technology Roadmap for Semiconductors (ITRS) interconnects are the major bottlenecks to overcome the power-performance barrier in the future generations.

In order to improve the performance of traditional NoC interconnects new technologies like 3D integration, photonics and multi-band RF (wireless) interconnects are being explored [11] [12]. These alternative interconnect technologies are capable of improving the speed and energy dissipation of multi-core NoC designs. With 3D interconnect integration multiple active layers can be realized onto a single chip. The major advantage of 3-D ICs is the reduction in length and number of global interconnects, as a result it reduces the hop count and the length of each hop. This leads to increase in performance and decrease in power consumption [13]. However, due to the small foot print and high power density 3D ICs suffer from high
temperature dissipation. Also, fabricating 3D ICs has its own sets of challenges. Three-dimensional ICs face issues with inter-layer alignment, bonding, inter-layer contact patterning [13] and other manufacturing defects. Along with these issues, 3D IC design requires the development of new CAD tools as the traditional CAD tools can support 3D chip designs.

Another alternative to the metallic interconnects are the photonic interconnects which make use of optical interconnects to transmit data [14]. In photonic interconnects the data transmissions is carried at the speed of light hence, photonic interconnects have high bandwidth and low latency. Another advantage of the photonic interconnects is that optical waveguides exhibit extremely low data loss, making the data transmission reliable. The disadvantages of photonic interconnects is that it is difficult to manufacture photonic devices and integrate them with silicon-compatible devices.

Wireless interconnects i.e. multi-band RF interconnects transfer data in the form of electromagnetic (EM) waves. Data is modulated onto the carrier using amplitude or phase shift keying [15]. Wireless interconnects use wires as transmission lines to transmit data. Bandwidth of conventional interconnects can be increased using multiple access techniques. With EM waves the data is transferred at the speed of light resulting in overall low latency network. Wireless interconnects face an issue of manufacturing frequency oscillators and filters on-chip for the transceivers. In spite of the challenges wireless interconnects prove to be a promising alternative to the traditional interconnects as they accomplish long distance communication with low latency and high bandwidth without the need of laying out physical interconnects.
1.4 Wireless On-chip Interconnects

Emerging interconnect technologies face manufacturing and fabrication issues. However, it is important to overcome the limitations of the planar metal interconnects by adopting one of the emerging interconnect technologies. Among the different emerging interconnect technologies, wireless interconnects prove to be a promising alternative to the planar interconnects. In recent years a lot of research has been put into developing and fabricating wireless on-chip antennas [16] [17] [18]. These antennas are capable of operating in the range of tens of gigahertz to hundreds of terahertz. Research in the field of CMOS Ultra-Wide Band (UWB) technology [19] has shown the feasibility of on-chip wireless communication with antennas and transceivers operating in the sub-THz range of 100-500 GHz [20]. Recently it has been discovered that carbon nanotubes (CNTs) can absorb and emit radiation similar to that of antennas. They operate in the frequency range of terahertz and show dipole like behavior, this makes them suitable for on-chip antennas [17]. Failures with fabricating CNT antennas are much higher as compared to the CMOS process. Mm-wave CMOS transceivers operating in the sub-THz frequency ranges is a more near-term solution.

Wireless links provide a single-hop long distance shortcut making them susceptible to more traffic. As traffic increases power dissipation increases leading to temperature hotspots in regions around the wireless interconnects. Therefore, wireless links are the major cause of temperature hotspots in wireless NoC architectures and hence they gain prime importance while designing thermally optimal multi-core systems on chip.
1.5 Temperature-Aware Multicore System-on-Chip

With technology scaling down, power densities on chips have increased to such an extent that it has exacerbated the temperature issues with systems-on-chip [21]. Smaller chip area and smaller packaging has made affordable on chip cooling unfeasible thus, pushing the design focus towards reducing peak on-chip temperatures. With high temperature reliability of the chip along with its performance is compromised hence, extensive research has been directed towards reducing on-chip thermal hotspots. Dynamic Thermal Management (DTM) [22] is one of the effective techniques to reduce temperature hotspots. Recent works on DTM for multicore architectures focus on optimizing the performance and explore the design space in the presence of thermal constraints.

As the number of cores increase, the communication infrastructure also starts contributing considerably to temperature. Traditional multi-core NoC architecture with metal interconnects contribute a lot to the temperature hotspots as they use long, multi-hop metal wires. It is possible to achieve high-performance, robust and energy efficient multi-core chips buy adopting complex network architectures in conjunction with long distance wireless links. Novel networks like small-world exhibit properties favorable for NoC architectures. Small world networks have a very short average path length enabling them to achieve communication with minimal resources. NoC architectures can be designed with underlying small world networks and long wired links replaced with wireless can achieve phenomenally low on-chip temperatures. Recent work in [12] demonstrates temperature-aware small-world based wired NoC architecture with wireless links capable of eliminating temperature hotspots. Integrating DTM techniques in small world NoC architectures, high performance and low temperature multi-core systems can be achieved.
1.6 Thesis Contributions

This work explores different NoC architectures to find a thermally optimal NoC architecture and proposes an approach towards achieving thermal management in multicore chips. It aims at achieving a thermally optimal NoC architecture capable of reconfiguring itself based on some DTM techniques. It demonstrates the design of thermally aware small-world based NoC architectures. It further shows enhance in terms of temperature using DMT techniques. This thesis work also evaluates the temperatures of various wired as well as wireless NoC architectures. The following summarize the contributions made during this work.

- Temperature-Aware Architecture-Space Exploration
  - Evaluation of temperature for various wired and wireless NoC topologies.
  - Thermal-aware placement of wireless interconnects for lower temperature.

- Dynamic Thermal Management Scheme
  - Dynamic Thermal Management scheme for obtaining reconfigurable NoC architectures.
  - Evaluation of Thermal Management scheme on an optimized Network-on-Chip Architecture.

- Experimental Results
  - Setup of Simulation workflow involving Gem5, a full system simulator, and HotSpot, Temperature simulator, to evaluate System-on-Chip Temperatures and a cycle accurate Network-on-Chip simulator to implement wireless and wired NoC architectures in presence of different synthetic and real-time traffics.
  - Develop Dynamic Thermal Management scheme based on chip component temperatures to provide a reconfigurable architecture.
- Develop a cycle accurate simulator to implement and analyze the proposed DTM scheme.
- Obtain the experimental results for the different Network-on-Chip architectures
  - Peak achievable bandwidth
  - Packet energy dissipation
  - Peak and mean temperatures on NoC elements such as switches and links
- Obtain the experimental results for thermally optimal Network-on-Chip architectures integrated with the thermal management scheme.

➤ Publications

Chapter 2 Related Work

A substantial amount of work has been done in the NoC paradigm. Apart from the conventional Mesh, many NoC architectures have been proposed. Sophisticated interconnect architectures like torus, CLICHE (Chip-Level Integration on Communicating Heterogeneous Elements), folded torus, SPIN (Scalable, Programmable, Integrated Network), Butterfly Fat-Tree (BFT) and octagon [8]. These NoCs however use multi-hop, packet switched communication and hence face scalability issues. In [23] authors have demonstrated that by using the principles of small-world graphs to place the long distance links in the network the performance of the NoCs can be improved to a great extent. In [24] a comprehensive study on various WiNoC architectures and their design methodologies has been presented. The work in [20] highlights 2D mesh-based WCube architecture using wireless links in the sub-THz region. The design of wireless NoC (WiNoC) based on CMOS ultra wideband (UWB) is presented in [19]. The work in [25] is based on inter-router wireless scalable express channel for NoC (iWISE) architectures. The work in [12] and [10] focuses on novel NoC architectures with on-chip wireless interconnects. In these works hierarchical and hybrid WiNoC architectures are used to replace the traditional long distance wired interconnects with wireless links. The network is partitioned into smaller clusters known as subnets. The subnets are designed as a regular mesh or a ring like structure; this forms the first level of the network. These subnets are connected using wireless and wired links, which forms the upper level of the network. Along with scalability issues, reliability is another parameter which is explored in the non-conventional NoC architectures. WiNoCs with network architecture based on small-world connectivity has proven to be more reliable as compared to hierarchical NoC architectures [23][26].
All the work mentioned above emphasize on the performance and reliability of NoC architectures, very less attention has been given to the thermal profile of these architectures. The thermal profile of the chip can be improved by using dynamic voltage and frequency scaling (DVFS) [27]. Another technique to avoid thermal emergencies is Dynamic Thermal Management (DTM) [22]. In most DTM techniques the system is allowed to run as normal however, as soon as the temperature of the system reaches the thermal limit measures are taken to reduce the temperature. This may lead to suboptimal performance of the system. Such DTM techniques are known as reactive DTM techniques. The other type of DTM technique is the predictive DTM method [28]. In these techniques the future temperatures are predicted which allows a range of solution to get temperature of the chip down well before the thermal threshold has been reached. The technique proposed in [10], provides a distributed thermal scheme for thermal management at runtime. This scheme allows the routers to collaboratively regulate the network temperature profile to prevent thermal emergencies with minimal impact on performance. The aim of this work is to study complex network architectures and develop a thermally optimal wireless Network-on-Chip architecture, alongside propose a thermal aware dynamically reconfigurable NoC architecture.
Chapter 3  Temperature-Aware NoCs

In conventional wired NoCs the communication between the cores is facilitated by network components like switches and wired links resulting in multi-hop communication. This multi-hop communication results in high energy and high latency. Insertion of bypass paths or long-range shortcut has shown to improve the performance of conventional mesh based NoC architecture [29]. However, the traditional NoC architectures with long long-range metallic links are more susceptible to temperature issues. The long distance metallic links are responsible for high energy dissipation and latency and replacing them with high bandwidth wireless interconnects can alleviate the problem. Placement of wireless nodes (WIs) provide a single-hop, long distance alternative to the data packets. Thus, the WIs attract huge amount of data traffic leading to localized temperature hotspots around the WIs. This chapter aims at exploring different wireless NoC architectures that are capable of mitigating temperature hotspots without compromising the performance of the system.

3.1 Topologies

This section aims at explaining the different NoC architectures considered for this research. Mesh architecture is considered for this work, because it is a generic architecture commonly used in most NoC designs. Among the non-conventional architectures, hierarchical NoC is chosen. This work also explores nature inspired small-world based novel architecture. Along with these three wireline architectures, this work also studies the impact of incorporating wireless interconnects on the performance and temperature of the wireline architectures.
3.1.1 Generic Mesh

A generic Mesh architecture is a grid of interconnecting switches placed in a mesh pattern. In such a system each core has a switch associated with it, which is responsible for routing the data in and out of that core. Thus each switch has five duplex links; four links to its four neighboring switches and one link to the core. The switches on the edges however have only three links; two links to its neighboring two switches and one link to the core. Figure 3-1 shows a 64 core system with a regular Mesh NoC architecture.

![Figure 3-1: A 64 Core Mesh NoC Architecture](image)

3.1.2 Optimized Small-World NoC (OSNoC)

Generic Mesh based topologies have planar metallic interconnects and multi-hop links, which results in high energy dissipation and thus high on-chip temperatures. This problem
aggravates as the system size goes on increasing. As system size increases, the hop between two far apart block increases leading to high latency and high power consumption. This problem can be alleviated by taking inspiration form naturally occurring networks. Naturally occurring networks like microbial colonies, neural networks and social networks are neither completely regular nor completely random. They are characterized by many short range links and a few long range links. These networks appear to be cluster of nodes connected with each other. The links within a cluster are the short range links and hence they are large in number, whereas the clusters are connected by long range shortcuts resulting in fewer long range links [29]. Such networks are called Small-world Networks. Figure 3.2 shows a generic natural network small-world network.

![Figure 3-2: A generic naturally occurring small-world network](image-url)
Small-world networks have a special property, the relationship between the mean inter-node distance and the network is logarithmic in nature [30]. In [30] it is illustrated that, with increase randomness of the network the i.e. by incorporating shortcuts in a regular network the hop count of the network drops exponentially. This is depicted in figure 3.3. But on the other hand, as randomness of the network increases its clustering coefficient decreases. Drop in the clustering coefficient can hamper the fault tolerance of the network making it susceptible to segmentation due to link failures. Small-world networks lie in between regular networks and random networks, and possess high clustering coefficients as well as low average hop counts.

![Figure 3-3: Average Hop Count \( L(p)/L(0) \) and Clustering Coefficient \( C(p)/C(0) \) [30]](image)

A small-world network can be built by inserting long range shortcuts in regular networks like Mesh. The network thus formed is more efficient than the original network with respect to
latency and power dissipation if rewired with limited resources [23]. The average hop count of such a network is also low due to the presence of long range links.

The wired small-world network is established using an inverse power-law distribution as shown in (1) [23].

\[
P(i,j) = \frac{l_{ij}^{-\alpha}f_{ij}}{\sum_{i=1}^{n} \sum_{j=1}^{n} l_{ij}^{-\alpha}f_{ij}}
\]

Where, \( P(i,j) \) is the probability of establishing a link, between two switches \( i \) and \( j \), \( l_{ij} \) is the manhattan distance, \( f_{ij} \) is the frequency of communication between switch \( i \) and \( j \), and \( n \) is the total number of switches. It can be observed that the probability of link establishment between any two switches \( i \) and \( j \), which are at a manhattan distance of \( l_{ij} \) from each other is proportional to the distance raised to a finite negative power. The value \( \alpha \) is chosen such that the small-world topology has high performance gains and optimal wiring costs [26]. For the distance a tile-based floorplan is considered. This power-law based link distribution ensures the presence of both long and short links in the network. The factor \( f_{ij} \) i.e. the frequency of communication between the cores ensures that frequently communicating cores have higher probability of have direct links. The network is established by considering each pair of switches and establishing a link between them based on the probability given in (1). This setup is repeated to ensure no switch or group of switches are isolated. The number of links in this optimized small-world network (SNoC) is same as that of a regular Mesh network.
3.1.3 Optimized Small-world Wireless NoC (OSWiNoC)

A wireless small-world network is obtained by facilitating some of the switches with transceivers. Figure 3-4 shows a wireless small-world NoC architecture. A random instantiation of the topology following (1) and placing wireless links over it may not result in an optimal network in terms of performance, robustness and thermal profile. This is because the traffic densities through each switch and link could be different. Switches which provide shortcuts to distant cores i.e. long-range links and wireless interconnects attract a lot of traffic, as a result they are susceptible to failure. Moreover due to the traffic density they handle, they have high power dissipation and eventually lead to localized thermal hotspots. Also, random placement of WIs may change the dynamics of (1) leading to a suboptimal network in terms of performance. The performance of a small-world wireless NoC improves by deploying WIs to optimize the average hop-count between the switches [24]. However, deploying WIs solely based on hop-count can result in already well connected switches being equipped with wireless interconnects. Such switches are large with many ports and dissipate a huge amount of power as compared to the others leading to thermal hotspots. Also, the WIs would attract significant traffic leading to congestion and in turn limiting the peak performance of the system.
A technique of balancing the traffic throughout the NoC components is by optimizing the variation in utilization of the switches and links $u$, which is a product of its traffic density $t$ and size $d$.

$$ u = td $$

(2)

Here, traffic density is given by the number of paths between source-destination pairs passing through the component coupled along with the frequency of interaction between those pairs. The size of a switch depends on the number of port, while the size of a link depends on its length. The optimization of variance or standard deviation of utilization results in uniform distribution of power dissipation among the switches and thus reduces temperature hotspots.

OSWiNoC is obtained by optimizing the aggregate metric $\rho$, which take into account both, the average hop-count and the standard deviation in $u$.

$$ \rho = \phi h + (1 - \phi)\sigma_u $$

(3)
Where, \( h \) is the average hop-count and \( \sigma_u \) is the standard deviation of \( u \), both normalized to that of mesh network with same number of cores.

### 3.1.4 Wireless Mesh NoC (WiMesh)

The wireless mesh NoC is obtained by incorporating WIs in a regular 64 core mesh architecture discussed in section 3.1.1. The wireline mesh architecture is augmented with wireless interconnects based on the optimization outlined in section 3.1.3 to form the WiMesh network. The number of links in WiMesh is same as that of the regular mesh network with 64 cores.

### 3.1.5 Hierarchical Mesh NoC (HiMesh)

The hierarchical mesh is a two level hierarchical network. Its bottom layer consists of a 64 core planar mesh. These switches are grouped into regions called subnets, which are in turn connected with each other via hubs to form the upper layer of the hierarchy. All hubs are connected to all switches within their subnet. Also, all the hubs are connected with each other in a mesh like pattern. The entire architecture is a wireline architecture with all connections established through metallic links. In a typical hierarchical network, if a switch from one subnet wants to communicate with another switch from another subnet, the communication takes place via the hubs. However, this leads to excessive traffic to pass through the hubs, further congesting them. In HiMesh there are multiple paths for inter subnet communication, one route through the hubs and the rest through the underlying fully connected mesh network. The HiMesh has a threshold based routing policy, wherein if the distance between the source and the destination switch is greater than a certain threshold the data packet is routed via the upper level network of
hubs. The threshold is optimized for best performance. The HiMesh NoC consists of 64 switches and 8 hubs. The 64 core mesh architecture as depicted in section 3.1.1 forms the bottom layer of the WiMesh NoC architecture. This mesh architecture is divided into 8 subnets, each subnet consisting of 8 switches and a hub, which forms the upper layer of the network. Figure 3-5 shows a generic HiMesh architecture with 8 cores, for simplicity the links between the switches and the hubs are not shown.

Figure 3-5: Generic HiMesh architecture with 8 cores
3.1.6 Wireless Hierarchical Mesh NoC (HiWiMesh)

The wireless hierarchical mesh NoC is formed by augmenting the 64 core wireline hierarchical mesh (HiMesh) with wireless interconnects. WIs are placed on the top level hubs following the same optimization process as discussed in section 3.1.3.

3.2 Physical Layer Implementation: Antenna and Transceiver

Antennas and transceivers are the major components of the wireless interconnect. NoC antennas are designed such that they provide high power gains with least area overhead. In [16], it has been demonstrated that metal zigzag antenna possess the properties suitable for wireless NoC architectures. Figure 3-6 shows the layout of an on-chip antenna and transceiver circuitry reproduced from [16]. The architectures mentioned in section 3.1.3, 3.1.5 and 3.1.6 have the antenna design adopted form [8]. These antennas provide a 3dB bandwidth of 16 GHz and have a center frequency of around 60GHz, with a communication range of 20mm. These antennas are optimized for power efficiency with an axial length of 0.38mm in the silicon substrate.

The transceivers used in the wireless topologies under consideration are designed to achieve high throughput, high energy efficiency and high bandwidth. Transceiver design form [8] is used in the wireless NoC (WiNoC) architectures. Non-coherent on-off keying (OOK) modulation is used as its circuitry consumes very low power as it eliminates the necessity of power hungry components like PLLs.
3.3 Flow Control and Routing Policy

OSWiNoC has adopted wormhole routing in which data is transferred via flits using virtual channels (VCs) [31]. OSWiNoC is essentially an irregular architecture and in irregular architectures it is important to achieve distributed and deadlock-free routing of data flits. This is achieved through a layered shortest path routing policy (LASH) [32]. In LASH, shortest paths between different source-destination pairs are separated into multiple virtual layers with specific VCs dedicated for each layer. This avoids cyclic dependencies between paths in a particular layer. Computation of the path for each packet would result in a large overhead hence, the shortest path between any source and destination is pre-computed offline. Each switch has a routing table, which contains only the identity of the next switch corresponding to all possible final destinations. As a result, the memory required to store the routing table is linearly proportional to system size. When a header flit arrives at a particular switch the next switch is determined from the routing table based on the final destination of the packet. The header flit is
then routed to the appropriate port along the particular VC reserved for its source/destination pair. Only the next switch is determined at each intermediate switch making the routing decision fast and efficient. Since the routing paths are the shortest paths, high data rates can be achieved with moderate number of VCs to avoid deadlock [32]. In order to grant access to the wireless channel to multiple WIs in a distributed manner, token flow control is adopted. Only after all the flits belonging to a particular packet are transmitted, the token is forwarded to the next WI. Since WIs provide shorter paths to route packets, many messages would try to access them leading to congestion. To avoid congestion at the WIs, if no buffer space is available at the wireless port of a switch then the packet is routed through the shortest available wired path.
3.4 Experimental Results

In this section, the temperature profiles of the topologies highlighted in section 3.1 are evaluated and a comparative analysis is conducted based on their thermal profiles. The NoC architecture is characterized using a cycle accurate simulator. The NoC simulator models the progress of the data flits accurately per clock cycle for the flits, those flits that reach the destination as well as those flits that are dropped. The simulations were performed with ten thousand iterations, the first thousands of which were transient. For this work a moderate packet size of 64 bits is considered. Each flit is considered to be of 32 bits and the width of all wired links is same as the flit size. Wormhole routing is the routing policy adopted for both wired as well as wireless links. To match the current multicore technology trends [33] a system size of 64 is used. For a deadlock-free lash routing four layers are sufficient in a 64 core system [32]. Each layer has a single VC, with each VC having a buffer depth of two flits. WIs have an increased buffer size of 8 flits to avoid excessive number of packets from being dropped during the toke wait cycles [8]. The hubs in hierarchical wireless mesh (HiWiMesh) are increased to 16 to accommodate the heavy traffic flowing through them as they cater majority of the inter subnet communication. Synopsys tool is used to synthesize the network switches from a RTL level design using 65nm standard cell libraries from CMP [34]. Post-synthesis RTL models are used to obtain the delay and energy dissipation of the digital components. In order to obtain the delay and energy dissipation for the wired links Cadence tool is used. For the Cadence simulations lengths of every link are taken in to account and a die dimension of 20mm * 20mm is considered. The wireless transceiver adopted from [8] is designed and simulated using the TSMC 65-nm CMOS process. The transceivers dissipate 36.7mW of power and support a data rate of
16Gbps with a bit-error rate (BER) of less than $10^{15}$. The transceivers occupy around 0.3mm$^2$ area. For the experiments all the NoC switches are driven at a clock frequency of 2.5 GHz.

3.4.1 Performance Metrics

Maximum achievable bandwidth, average packet energy and temperature are the three metrics used to evaluate the performance of the NoCs discussed in section 3.1. Maximum achievable bandwidth is the peak sustainable data rate in number of bits successfully routed per second. The bandwidth, $B$ is defined as,

$$B = \tau N_{flit} f N_{cores}$$

Where, $\tau$ is the throughput, defined as the number of flits which are successfully routed to the destination per core per cycle at network saturation, $f$ is the operating frequency of the clock, $N_{flit}$ is the number of bits in the flit and $N_{cores}$ is the number of cores in the NoC. For evaluation of bandwidth system level cycle-accurate simulations are done using the NoC simulator.

Packet energy, $E_{packet}$ is defined as the average energy required to successfully route a packet from source to destination.

$$E_{packet} = \frac{1}{n_{pkt}} \sum_{i=1}^{n_{pkt}} \sum_{j=src}^{dest} (E_{link} + E_{switch})$$

Where, $n_{pkt}$ is the total number of packets successfully routed, $E_{switch}$ is the energy in the switches and $E_{link}$ is the energy in the link. The link energy is defined as the energy spent in sending a packet over a wired or wireless interconnect.

In order to evaluate the temperature and performance of the NoC architectures application specific traffic as well as synthetic traffic patterns are used. The peak link and switch
temperatures are obtained by system level simulations of real application based workloads. GEM5 [35], a full system simulator which can obtain detailed processor and network-level information was used to the application specific traffic patterns form SPLASH-2 and PARSEC benchmarks. For all GEM5 simulations a system of 64 alpha cores running linux is considered. The memory system is MOESI_CMP_directory, setup with private 64KB L1 instruction and data caches and a shared 64MB (1MB distributed per core) L2 cache. Three SPLASH-2 benchmarks i.e. FFT, RADIX and LU [36] and one PARSEC benchmark i.e. CANNEAL [37] are used as considered as they vary in characteristics from computational intensive to communication intensive in nature. Table 1 shows the behavior and problem size of the benchmarks.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Busy %</th>
<th>Idle %</th>
<th>Default Problem Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT</td>
<td>81.99</td>
<td>18.01</td>
<td>65,536 Data Points</td>
</tr>
<tr>
<td>RADIX</td>
<td>84.98</td>
<td>15.02</td>
<td>262,144 Integers, 1024 RADIX</td>
</tr>
<tr>
<td>LU</td>
<td>87.62</td>
<td>12.38</td>
<td>512x512 Matrix, 16x16 Blocks</td>
</tr>
<tr>
<td>CANNEAL</td>
<td>56.74</td>
<td>43.26</td>
<td>200,000 Elements</td>
</tr>
</tbody>
</table>

The processor-level statistics generated by GEM5 simulation are incorporated into McPAT (Multicore Power, Area, and Timing) [38] to determine the processor-level power statistics. The frequency of traffic interaction between the cores, $f_{ij}$, for the benchmarks is captured using GEM5. These $f_{ij}$s are used to generate traffic patterns for the benchmarks in the NoC simulator. NoC performance in terms of network bandwidth, average packet energy and
energy dissipation of the network elements is obtained through simulation done using the NoC cycle-accurate simulator. The network components are arranged over the 20mm*20mm die. These floorplan, along with power dissipation in presence of specific benchmarks are used in HotSopt [39] to obtain the steady state thermal profile of the entire system. The entire simulation flow is shown in figure 3-7.

Figure 3-7: Simulation Work Flow
3.4.2 Performance evaluation of different NoC architectures

In this section, a comparative study is conducted on the NoC architectures discussed in section 3-8. Maximum bandwidth and packet energy dissipation at network saturation are determined for the study. A uniform random traffic distribution is used for the simulations. The peak bandwidth at network saturation for a system size of 64 cores with uniform random traffic is shown in figure 1. Traditional mesh has the lowest bandwidth as compared to the other architectures. Regular mesh has on an average a larger hop-count as compared to the other NoC architectures under consideration hence the data packet crosses multiple switches before reaching the destination leading to a low bandwidth system. Addition of wireless interconnects in a tradition mesh i.e. WiMesh improves the bandwidth of system. The wireless interconnects provide shortcuts to the long distance paths, thus reducing the average hop-count of the system and in turn increasing its bandwidth. Hierarchical mesh shows a higher bandwidth as compared to mesh. It improves the performance over the traditional mesh due to reduced average hop-count. Reduction in hop-count facilitates a more efficient packet transmission from any source to destination, resulting in a high bandwidth system. However, in hierarchical topologies the hubs fall prey to congestion as they handle a lot of traffic. In HiMesh the traffic is distributed in such a way that it does not overload the hubs. Lower level mesh links are used for inter-subnet communication to avoid the hubs from getting overwhelmed. Threshold based selection is done between the two available inter-subnet alternatives. In HiMesh packets are routed through the hubs only if the number of hops between the source and destination is greater than six. This threshold based routing in HiMesh yields a higher bandwidth as compared to the other wireline networks. HiWiMesh is a modification of HiMesh with wireless interconnects in it. Thus, HiWiMesh had an average hop-count as compared to its wireline counterpart and hence it has
higher bandwidth as compared to HiMesh. OSNoC is based on small-world principles and hence the average number of hops between any source and destination pair is not too large. This results in a comparatively larger bandwidth as compared to the traditional mesh topology. However, OSNoC cannot match the bandwidth provided by HiMesh architecture. Also, OSNoC is structured such that it distributes traffic uniformly among the NoC components avoiding congestion. Due to the presence of wireless interconnects; OSWiNoc can achieve a higher bandwidth than that of OSNoC.

![Bandwidth (Tbps) Chart]

Figure 3-8: Peak bandwidth at network saturation.

The packet energy at network saturation for a 64 core system with uniform random traffic is shown in figure 3-9. Wireline mesh has the largest packet energy as on an average each packet crosses a large number of switches and links consuming energy as compared to the other topologies. Wireless mesh NoC, WiMesh shows a substantial improvement in packet energy as the WIs provide shortcut paths to the data packets and they cross fewer links and switches as
compared to the wireline mesh topology. Hierarchical mesh, HiMesh NoC has lower packet energy as compared to Mesh and WiMesh NoC architectures. The small-world based OSNoC has lower packet energy than that of HiMesh NoC architecture. In OSNoC the traffic is distributed uniformly, which results in lower packet energy. Also, HiMesh NoC architecture has incorporated the threshold based routing policy due to which longer paths in terms of hops from the lower lever of the hierarchy are used resulting in higher packet energy. The energy efficiency of the hierarchical and small-world topologies is improved by augmenting them with energy efficient wireless interconnects. OSWiNoC has a lower bandwidth than the OSNoC architecture, whereas HiWiMesh has the lowest packet energy than all the network topologies under consideration.

The HiWiMesh architecture has the highest bandwidth and the lowest packet energy among all the architectures discussed in section 3.1. This is because the HiWiMesh has the hierarchical architecture augmented with the energy-efficient wireless links. The hubs in the hierarchical network handle a high volume of traffic transferred between subnets making them the performance bottlenecks. Failure of these hubs can cause significant degradation in performance and energy efficiency. Small-world topologies are inherently resilient to failures and hence OSWiNoC has less effect due to failures. This makes OSWiNoC more suitable for NoC architectures as compared to HiWiMesh NoC architecture.
3.4.3 Thermal characteristics of different NoC architectures

In this section a comparative study is performed on the peak switch and peak link temperatures for the different NoC architectures discussed in section 3.1. For the temperature evaluation real application based traffic patterns are used as discussed in section 3.4.1. The benchmarks are mapped on to a 64 core system interconnected by the various NoC architectures under consideration. The selected benchmarks demonstrate a good variation in computation and communication intensity, which proves to be an effective environment to evaluate the network components such as NoC switches and links. The peak switch temperatures for the different architectures are shown in figure 3-10. Figure 3-11 depicts the peak link temperatures for the architectures. It can be observed that CANNEAL has higher peak link and peak switch temperatures as compared to the other benchmarks. This is because CANNEAL has a higher
intensity of communication and a hot-spot like traffic pattern. The temperatures for RADIX and LU on the other hand are lower than that of CANNEAL and FFT for all the architectures; this is because RADIX and LU have a lower traffic interaction than CANNEAL and FFT.

Figure 3-10: Peak switch temperatures for the different architectures evaluated with real benchmarks.
Figure 3-11: Peak link temperatures for the different architectures evaluated with real benchmarks.

It can be seen that the wireline mesh has the highest switch and link temperature. This is because no optimization has been performed on the wireline mesh, leading to a non-uniform distribution of traffic density. The non-uniform distribution of traffic leads to high packet energy.
dissipation resulting in heating of the network components. Consequently, temperature hotspots can be observed in the Mesh NoC architecture. For WiMesh, the optimized WI placement helps distribute the traffic reducing the peak link and switch temperatures as compared to the wireline mesh topology. However, the packet energy for WiMesh is much higher than that of OSWiNoC and HiWiMesh and hence we do not see a significant decrease in temperature for the former. For most of the benchmarks except LU, HiMesh and HiWiMesh have a lower peak temperature in comparison to Mesh and WiMesh. In the hierarchical topologies energy expenditure in data transfer is reduced due to the hierarchical structure, this low packet energy dissipation results in lower switch and link temperatures. However, for LU, the HiWiMesh have peak temperatures similar to that of HiMesh, at some instances even slightly higher than that of the latter. This is due to the threshold based routing, where the proportion of traffic utilizing the hubs do not change even after placing the WIs. In HiWiMesh, the WIs only change routing paths in the upper layer of the network which is used only when the hop-count between the source and the destination is greater than the threshold. Hence the temperature profile of the hierarchical topologies is tightly bound to the traffic pattern/application. The four architectures discussed above do not optimize the standard deviation of utilization and hence have higher peak temperatures as compared to the small-world networks. OSNoC is for both link utilization and hop-count due to which the traffic is more uniformly distributed among the network avoiding hotspot. As a result OSNoC has comparatively lower peak switch and peak link temperatures. The optimized placement of WIs in OSWiNoC helps distribute the traffic more evenly between the WIs. The energy-efficient wireless interconnects in the OSWiNoC further reduce the energy consumption in data transfer and consequently the least peak link and switch temperatures are obtained for the OSWiNoC architecture.
Based on a cumulative study of performance and temperature for all the NoC discussed in section 3.1, it can be inferred that OSWiNoC strikes a balance between performance and temperature and is more suitable for a multi-core system.
Chapter 4  
Dynamically reconfigurable network on chip

This chapter aims at proposing a dynamically reconfigurable network on chip architecture, which reacts to the varying temperature profiles of the die and reconfigures itself to achieve better thermal efficiency by avoiding thermal hotspots. In NoCs data is transferred in the form of flow control units called flits. A flit is the smallest amount of data that can be transferred between adjacent switches in one clock cycle [31]. Wormhole routing policy is the commonly adopted routing from most NoC architectures. In wormhole routing policy, whenever a packet is routed from the source to the destination the header flit reserves a path for the data transfer and the body flits follow the path reserved by the header flit. Most routing strategies strive to achieve shortest global paths between the nodes to reduce data latency. In irregular network architectures like small-world based NoCs the shortest paths with least number of hops between all source/destination pairs is determined offline using Dijkstra’s shortest path routing algorithm [40]. In such kind of NoC routing schemes when data is sent form one core to another, the path between them is reserved based on the fixed routing tree. Though this approach of pre-determined routing paths reduces latency, but it is rigid and does not account for the dynamic changes in the chip that could adversely affect its performance. For example, NoC components which provide high connectivity i.e. NoC elements which relay information between many core pairs tend to heat up faster than other NoC elements as they handle huge amount of traffic. If the NoC elements heat excessively it may endanger the integrity of the system. Hence, there is a need for a mechanism that can dynamically react to the thermal profile of the chip and take measures to avoid thermal hotspots.
4.1 Distance Vector Routing (DVR) to enable dynamic reconfiguration

A dynamic routing approach is needed which can respond to the on chip temperature increase and can distribute the heat dissipation avoiding hazardous thermal hotspots. This work aims at adopting the Distance Vector Routing (DVR) algorithm [41] based on the Bellman-Ford equation for the NoC environment. DVR takes into consideration the changing dynamics of any system and provides the best possible routing path for that situation. It is a standard for routing over the internet where varying traffic flow and congestion can adversely affect the network integrity. Unlike Dijkstra’s algorithm, DVR is a distributed algorithm where no single authority/core maintains the path cost to all other nodes in the network. In DVR, the neighboring nodes maintain cumulative path costs also known as distance vectors to all other nodes. The nodes periodically check the state of the links to its neighboring nodes and if there is any change in the link cost it recalculates the distance vector for that particular links and advertises this change to its neighbors. The neighbors, upon receiving the update recalculate their distance vector and in turn send the updated information to their neighbors. This process continues till eventually the entire network converges to a shortest path routing tree which is similar to that obtained through the Dijkstra’s routing algorithm.

In this work optimized small-world based NoC (OSNoC) is used as the framework in which distance vector routing technique is incorporated to achieve a thermally aware dynamically reconfigurable NoC architecture. In section 3.4.3 it has been established that among the wireline architectures, OSNoC is a better alternative to the regular Mesh NoC in terms of performance and temperature. Implementing DVR in OSNoC would further improve its thermal profile. In order to implement DVR a link cost function is designed, such that it reacts to the
changing thermal profile of the chip and avoids routing through the NoC elements experiencing dangerously high or rising temperatures.

A step cost function is used to incorporate the thermal characteristics of the NoC elements while evaluating the optimal path. The cost function is expressed as follows:

\[
C_{i,j} = \begin{cases} 
1, & T_{link_{i,j}} < T_{link}^{th} \text{ and } T_{switch_{j}} < T_{switch}^{th} \\
\infty, & T_{link_{i,j}} > T_{link}^{th} \text{ or } T_{switch_{j}} > T_{switch}^{th}
\end{cases}
\]  

(6)

Where \( i \) the source switch, \( j \) is the destination switch. \( T_{link_{i,j}} \) is the temperature of the link between the switches \( i \) and \( j \). \( T_{switch_{j}} \) is the temperature of the neighboring switch \( j \). \( T_{link}^{th} \) and \( T_{switch}^{th} \) are the link and switch thresholds temperatures respectively. Equation (6) ensures that a switch avoids relaying the data message over a link having temperature above the threshold and to a switch which has temperature above a specific threshold. Thus the DVR algorithm achieves a shortest path which has both link and switch temperatures below the threshold.

At network initialization, the distance vector for all the switches is set to 1, the routing tree thus obtained is a minimum distance, low latency routing tree similar to that obtained by Dijkstra’s routing algorithm. When a link or switch temperature crosses the threshold, its associated cost is set to \( \infty \). After a switch updates its DVR table, it advertises the new distance vectors to its neighbors. In accordance with the DVR protocol this process continues until network convergence has met. The DVR routing protocol facilitates the hotter NoC elements to cool without bringing the system to a halt by providing alternative relay paths. As soon as the NoC elements cool down and attain a temperature below the threshold the DVR algorithm sets their cost back to 1. This facilitates the network to utilize these elements again.
4.2 Experimental Results

In this section the temperature profiles of the NoC are studied to evaluate the effect of implementing DVR in the system. The simulation workflow as discussed in section 3.4 is modified to study the effect of DVR on the wireline small-world based OSNoC architecture. A NoC cycle accurate simulator is developed to model the flow of DVR packets in the NoC. DVR is modeled based on the cost function expressed in equation (6). The runtime system flow for the DVR algorithm is shown in figure 4-1.

Figure 4-1: Runtime System Flow for DVR

For the initial phase of the experimentations an evaluation of the steady state temperatures is performed with and without DVR is performed. A 64-core wired small-world based optimized
architecture (OSNoC) as discussed in section 3.1.2 is used as the framework on which DVR is implemented. High and low temperature of 100°C is considered for the DVR cost implementation. This makes the both the switches and links become active as soon as the temperature cools below the threshold. A synthetic uniform random traffic is used to evaluate the efficiency of the scheme with 30% offered load. The steady state temperatures are estimated using HotSpot tool. The steady state temperatures of the system without the DVR scheme is compared with the values obtained from system in which the NoC routing reconfigures once after the initialization stage. In order to avoid deadlocks in the routing paths, LASH routing policy is adopted as discussed in section 3.3. In the DVR mechanism, the routing table is updated every time a change in the link cost is encountered. Thus the routing table may change several times until the entire network converges. This may result in deadlocks. In order to avoid deadlocks, the proposed DVR scheme uses two DVR tables for every switch. The old DVR table is used to route all the data packets until the network converges. Only after network convergence the newly calculated DVR table is used to route all the newly generated data packets. Experimentally, it is found that a period of 500 cycles is sufficient for the entire network to converge in a 64 core system. The results are shown in figure 4-2 and figure 4-3. It can be observed that the number of switches and links falling in the higher temperature range is more for the system without DVR as compared to the system with DVR implemented in it. Due to the DVR scheme, there is 40% reduction in the number of switches above 140°C and approximately 71% reduction in the number of links above 150°C. This proves the efficiency of the system in reducing thermal hotspots.
Figure 4-2: Number of switches lying in different temperature regions

Figure 4-3: Number of links lying in different temperature regions
The steady state temperature analysis establishes that DVR reduces the number of NoC elements in the higher temperature range. The effect of DVR can be observed in detail with transient temperature analysis of the chip. In the second phase of the experimentations a transient temperature analysis is carried out on 64-core OSNoC architecture with the implementation of DVR as well as without DVR (with static shortest path routing). A link and switch threshold temperature of 60.15°C is used for the analysis. A simulation of 20000 cycles was carried out with an initial reset cycle of 1000. The system was monitored every 5000 cycles for temperature changes which in turn trigger the DVR scheme into action. Figure 4-4 and 4-5 show the distribution of the number of switches and links respectively over the temperature range for a system that has DVR implemented in it. Whereas, figure 4-6 and 4-7 show the distribution of the NoC elements over a temperature range for a system without DVR. It can be observed that in a system with DVR the number of NoC elements in the higher temperature range is lower than that compared to a system without DVR. The cost function of DVR prevents the switches and links having temperature the threshold from being utilized. As soon as they cross the threshold temperature cost associated with them is set to $\infty$. This prevents these NoC elements from being utilized and facilitates them to cool down. In contrast, for the system without DVR, we see that as time progresses the number of NoC elements lying in the higher temperature range increases. This is because the system lacks an adaptive routing policy and as a result the predetermined optimal paths get utilized over and over again, leading to an increase in their temperature. The DVR policy prevents the NoC elements whose temperature is above the threshold from being utilized, thus allowing them to cool down. However, we see some NoC elements above the threshold temperature because DVR is evaluated after specific intervals of time. During this time period the NoC components may get utilized and hence they may attain temperatures above the
threshold. This effect can be reduced by increasing the frequency of temperature evaluation and
DVR reconfiguration.

Figure 4-4: Number of switches over different temperature regions for a system with DVR
Figure 4-5: Number of links lying in different temperature regions for a system with DVR

Figure 4-6: Number of switches lying in different temperature regions for a system without DVR
Figure 4-7: Number of links lying in different temperature regions for a system without DVR

The temperature analysis shows that, the system with DVR implemented in it has a better thermal profile than a system without. However, the temperature analysis alone does not prove the efficiency of the system. It is important to study the impact on the performance of the system with the implementation of the thermal management scheme. Bandwidth and packet energy as discussed in section 3.4.1, are the two metrics used for the performance evaluation of the system. Table 2 shows the bandwidth and packet energy of both the systems, with DVR as well as without DVR. It can be observed that the system with DVR shows approximately 5% decrease in bandwidth as compared to a system without DVR. There is a reduction in bandwidth due to the flow of routing information (DVR packets) in the network, which utilize network resources. However, as compared to the data packets, DVR packets are short length and are destined to neighbors which are one hop away. As a result the DVR flits account for a fraction of the total
flits flowing in the network; hence they have a less impact on the bandwidth of the system. It can also be observed, that the packet energy of the system with DVR is approximately 18% higher that the system without DVR. The paths obtained from the DVR algorithm may result in suboptimal paths in terms of hop-count. As a result as compared to the system without DVR, the data packets may encounter more number of hops leading to an increase in the packet energy. Though with the implementation of DVR in NoCs the performance of the system degrades, however the impact is less achieving a good tradeoff in temperature and performance.

<table>
<thead>
<tr>
<th></th>
<th>Bandwidth (Tbps)</th>
<th>Packet Energy (nJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>System With DVR</td>
<td>1.097</td>
<td>26.4</td>
</tr>
<tr>
<td>System without DVR</td>
<td>1.153</td>
<td>21.7</td>
</tr>
</tbody>
</table>
Chapter 5 Conclusions and Future Work

In this work, various NoC architectures were explored to find the most suitable NoC architecture in terms of temperature, performance and energy for multiprocessor systems. Dynamically adaptive temperature-aware routing is incorporated into the system to achieve a reconfigurable network on chip architecture capable of avoiding localized hotspots. This chapter summarizes the results obtained during this thesis work.

The traditional NoC architectures implemented with planar interconnects suffer from high latency, significant power dissipation, and temperature hotspots due to long, multi-hop wired interconnects. This can be seen from the performance and temperature results of the Mesh architecture. Novel NoC architectures like HiMesh (hierarchical mesh) show better performance characteristics that the traditional mesh as the upper layer of the hierarchy provides shortcut paths, thus reducing the overall hop-count of the architecture. However, HiMesh has a temperature profile which is very application specific and does not show a consistently good temperature profile for all the benchmarks. Also, the hubs in HiMesh may become a bottle neck jeopardizing the integrity of the system. OSNoC is a small-world based NoC optimized for uniform distribution of traffic over the entire network. Results support that not only the performance characteristics of OSNoC are substantially better than of regular mesh architecture, but also the former has a temperature profile better than that of mesh for all the benchmarks. It can be also observed that placement of low power wireless interconnects optimized to distribute the traffic, improves the performance and temperature characteristics of the system. From the results it can be inferred that OSWiNoC is the most suitable architecture for multicore environments in terms of temperature, performance, energy and reliability.
OSNoC was further incorporated into a multicore system with Dynamic Thermal Management technique at the network layer to achieve a dynamically reconfigurable thermally aware network on chip architecture. Distance vector routing policy was adopted, which enabled the system to react to the changing thermal dynamics of the chip. A cost function was designed which enabled the system to utilize the relatively colder resources and thus prevent the relatively hotter resources from being over utilized, thus preventing thermal hotspots. Transient temperature results show that for a system with DVR there is approximately 50% reduction in total number of NoC elements above the threshold as compared to the system without DVR. Incorporating DVR thus facilitates the network to reconfigure itself such that the hotter NoC resources are utilized scarcely and thermal hotspots are avoided.

The future challenges to this work involves facilitating the architecture with wireless interconnects having beam steering capability, thus achieving a fully reconfigurable NoC architecture. Further incorporating core level DTM techniques like task reallocation and context switching would result in a fully thermal aware wireless NoC capable of reconfiguring itself at the physical layer, network layer as well as application layer.
Bibliography


