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DYNAMIC INPUT MATCH CORRECTION IN R.F. LOW NOISE AMPLIFIERS

by

TEJASVI DAS

A THESIS SUBMITTED

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PARTIAL FULFILLMENT

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IN

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TITLE OF THESIS:

DYNAMIC INPUT MATCH CORRECTION IN R.F. LOW NOISE AMPLIFIERS

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Date: 12 DEC '04

To my parents

-For giving me the freedom to make my mistakes
-For always believing in me

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I came to R.I.T in the fall of 2002, excited to learn circuit design, eager to experience life – and mildly put, these two years have been remarkable. In my advisor I have found an extraordinary person – a man who has become my ‘teacher’ in the true sense of the word. In my lab I have found a place which epitomizes honesty and integrity – and people who have enriched my life, professionally and personally.

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All who have accomplished great things have had a great aim, have fixed their gaze on a goal which was high, one which sometimes seemed impossible.

-Orison Swett Marden

ABSTRACT

An R.F. circuit that recognizes its faults, and then corrects its performance in real-time has been the holy-grail of RFIC design. This work presents, for the first time, a complete architecture and successful implementation of such a circuit. It is the first step towards the grand vision of fault-free, package independent, integrated R.F. Front End circuitry.

The performance of R.F. front-end circuitry can degrade significantly due to process faults and parasitic package inductances at its input. These inductances have wide tolerances and are difficult to co-design for. A novel methodology, which overcomes current obstacles plaguing such an objective, is proposed wherein the affected performance metric of the circuit is quantified, and the appropriate design parameter is modified in real-time, thus enabling self-correction. This proof of concept is demonstrated by designing a cascode LNA and the complete self-correction circuit in IBM 0.25 μm CMOS RF process.

The self-correction circuitry ascertains the input match frequency of the circuit by measuring its performance and determines the frequency interval by which it needs to be shifted to restore it to the desired value. It then feeds back a digital word to the LNA which adaptively corrects its input-match. It offers the additional flexibility of using different packages for the front-end since it renders the circuitry independent of package parasitics, by re-calibrating the input match on-the-fly. The circuitry presented in this work offers the advantages of low power, robustness, absence of DSP cores or processors, reduction in design cycle times, guaranteed optimal performance under varying conditions and fast correction times (less than 30 μs).

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Chapter 1. INTRODUCTION

1.1 RF Integrated Circuits

-1.1.1 The System-On-Chip (SoC) approach

-1.1.2 System-In-Package (SiP) implementation

1.2 Chip-package Co-design

1.3 Testing and Reliability

1.4 Necessity for this work

1.5 Preface to this work

-1.5.1 Package independence

-1.5.2 Fault Correction

-1.5.3 Organization

1.1 RF INTEGRATED CIRCUITS

The drive towards miniaturization within the CMOS semiconductor technology has led to an unprecedented reduction in transistor feature size with gate oxide thicknesses a few atoms wide. A significant factor in the success of the MOS transistor is the fact that it has been scaled to increasingly smaller dimensions, improving performance while decreasing power consumption. CMOS integrated circuits have become ubiquitous in today's electronics industry, offering the advantages of low cost, small size, high yield and reliability. This rapid shrinking of channel lengths has enabled MOS transistors to work at higher frequencies, breaking the GHz barrier. Along with the increasing demand for wireless and other forms of high-speed communication in the past few years, these factors have fuelled the development of a wide range of RF integrated circuit products [3].

1.1.1 The System-On-Chip approach

The persistent demands on miniaturization have resulted in escalating levels of integration. In the circuit board architecture, inter-connection and inter-communication between the different domains are responsible for majority of the real-estate overheads. The next logical step, enabled by rapid strides in technology, was the amalgamation of analog, digital, RF, and mixed-signal circuitry onto a single chip, using the same fabrication process. This has resulted in the advent of several highly integrated Radio Frequency System-On-Chip implementations [1, 2, 3], depicted in Figure 1.1.

Figure 1.1 The System-On-Chip (SoC) approach

1.1.2 System-In-Package (SiP) implementations

Each of these domains – digital, analog, and RF circuitry pose different, and sometimes conflicting demands on the fabrication process. RF circuitry, for example, requires high-quality on-chip passives [4]. This in turn necessitates a thick, low resistance top metal layer specialized for inductors, and a high-resistivity substrate. Analog circuits require transistors with high output impedance and high linearity, while size is the

dominant factor for digital circuits. These incompatible demands among the circuitry of a single system has led to the development of an alternate means of integration: while the circuits are fabricated on different dies, which enables the use of different fabrication processes, they are integrated onto the same package, leading to System-In-Package (SiP) implementations [5,6,7] (3-D stacking, Multi-chip modules, etc., Figure 1.2).

Figure 1.2 The integrated System-In-Package (SiP) approach

In either approach, the complex interaction of signals across the analog, digital and RF domains and the chip-package interactions place a huge burden on the packaging technology. The package exerts significant influence on the system performance, and consequently, its accurate characterization is a necessity for the success of such RFIC implementations.

1.2 CHIP-PACKAGE CO-DESIGN

The rapid increase in circuit operating speeds, I/O pin count and functionality, coupled with the complex behavior of deep sub-micron devices, have placed unique

challenges on the encompassing package. Furthermore, at radio frequencies, package parasitics are no longer negligible [8]:

Figure 1.3 (a) Interconnection of chip and package through bond-wires. (b) parasitics associated with the chip-package interface.

- Inductances of the order of a tenth of a nano-henry and capacitances of the order of a tenth of a pico-farad can have a huge influence on chip-performance.
- Package bond-wires or solder bumps (Figure 1.3 (a)) are generally of the order of a few nano-henry.
- Other package associated parasitics that influence chip performance include mutual inductances and pad resistances (Figure 1.3 (b)).

- In addition, Electro-Static Discharge devices (ESD) present non-negligible parasitic inductances and capacitances, and they must be accounted for during the design process [17].

Traditionally, circuit design and its packaging have been conducted by different groups, leading to sub-optimal results from an overall system performance perspective. In addition, due to the high frequency complex inter-module interactions, ‘Package aware’ design for RF transceivers has become a necessity. Consequently, the RFIC industry has accepted a paradigm shift to chip-package co-design, which involves concurrent design of both chip and package [9, 10], where all the packaging effects are accounted for during the circuit design process. It must be noted, however, that most of these parasitics have very high tolerance limits, and this makes it almost impossible to accurately model or predict them. Therefore, the performance of RF circuits cannot be accurately predicted during design or simulation.

1.3 TESTING AND RELIABILITY

RF circuits are prone to unique reliability issues, such as on-chip inductor faults, ground inductance loops, etc. In today’s era of integration, the RF core exists as a sub-system among many heterogeneous modules, and complex inter-module interactions (for example, the digital circuitry can inject switching noise, which can be severely detrimental to the RF core performance) make testing an even more critical issue. In addition, process faults and variations are only part of the list of probable causes of system failure. Package parasitics, as mentioned in the earlier section, can have large

variations and result in severe performance degradation. The quality factor of on-chip passives is abysmally low and unpredictable (30%): this can lead to soft-faults in the circuits. To compound this issue, access to the RF core in such a complex system may almost prove impossible to achieve. Hence there was a pressing need to develop non-intrusive testing methods for RF circuits [11], and thus was born the Built-in-Self Test (BiST) approach.

The most important requirement of such testing is **minimal intrusion**. Any probing device used should not alter the performance of the circuit being tested. This requirement is a particularly challenging issue in RF circuits, since even small inductances and capacitances can have a significant impact on the circuit. The other requirements are low power, real estate and processing overheads, and reliability of the testing circuitry itself.

Several attempts have been made in recent literature to address the problem of RF front-end reliability with the view of quantifying the effect of the various above mentioned factors on circuit performance through self-test, thereby attempting to improve the robustness of the RF part shipped to the end customer. Many approaches such as the loop back technique proposed in [12] and the end-to-end approach proposed in [13] involve significant processing and real estate overheads since they require the presence of additional DSP processing to achieve self test. Approaches such as the signature test method proposed in [14] are very computationally intensive, requiring a large amount of off line computation to estimate circuit performance. Current commercial approaches require the use of costly ATE (Automated Test Equipment) testers, which results in high

test cost in addition to very large test times to test RF parts. Power-supply current based testing [15, 16] has been one of the more promising techniques, where the supply current is analyzed, and signature patterns quantify the performance degradation. None of the above approaches have led to a fully integrated testing solution for RF circuits, as yet.

1.4 NECESSITY FOR THIS WORK

Having laid-out the background in the previous sections, we now discuss certain outstanding issues, critical to RFIC performance, which current approaches fail to address. This work, as will be shown, accounts for these problems successfully.

While the chip-package co-design methodology and BiST approaches address many issues by accounting for parasitics during the design process [17], development of early design techniques, etc., they fail to account for the following problems:

- **Wide tolerance ranges of package parasitics:** In current approaches, accounting for package parasitics during the design process does not alleviate the problem of tolerances. Since these parasitics are subject to wide variations that cannot be predicted during the design cycle [18], the performance of the circuitry may degrade to sub-optimal levels once fabricated and packaged. More importantly, it leads to unpredictability of RFIC performance since these tolerances cannot be accounted for during simulation, and raises serious reliability issues.
- **Dependence of ESD protection on environmental conditions:** ESD parasitics can possess large tolerances, and this leads to the same problem mentioned above. Further, the choice of ESD protection is dependent on the external conditions of

the RFIC's expected application, and any change in ESD devices necessitates a complete re-design of the circuitry.

- **Availability of different packaging techniques:** In any of the current approaches, a change in package alters the parasitic impedances and package thermal characteristics; this necessitates modification of the existing design, or, in the worst-case, repetition of the entire circuit design cycle. In either case, it requires a new fabrication cycle, escalating costs.
- **Correction of faults:** It has been already mentioned that no complete integrated testing solution exists for RFICs yet. Testing, however, merely quantifies the performance of the circuit, and does nothing to *increase* reliability. It has value in identifying chips that degrade beyond acceptable levels, and ensures that the defective product does not reach the end-user. In addition to process faults, other factors such as switching noise coupled from the digital module, power supply coupling, etc. can degrade performance drastically. Quite evidently, a circuit topology that not just quantifies its performance, but also corrects itself in real time will be a highly desirable quality; it can significantly improve reliability.

Hence, a circuit topology that dynamically self-corrects its performance to changing packages and/or package parasitics, process faults and variations, other soft faults, and ESD events, can help cut down design cycle time, reduce cost and ensure optimal performance under varying conditions. Such an approach is a major step towards immunizing the circuit performance from package characteristics, and significantly improving reliability.

1.5 PREFACE TO THIS WORK

This work presents the first-ever successful attempt at self-corrective RF circuits. It presents a unique architecture that enables on the fly modification in the performance of RF circuits, and proves the concept by demonstrating a complete implementation. This architecture sidesteps the many obstacles that have prevented the success of such a system so far.

1.5.1 Package Independence

The proposed architecture takes a significant step towards addressing a critical bottleneck in today's RFIC technology – packaging effects. It progresses a step further than merely modeling and characterizing package effects on the chip; it is an attempt to render the chip independent of these effects, redefining the co-design paradigm. It proposes a chip-level solution to package issues, and drastically reduces chip-dependence on accurate modeling and characterization of packages. By ensuring that a single front-end design will adapt itself dynamically to package parasitic variations, it cuts down on design cycle times appreciably; it also facilitates seamless package portability.

1.5.2 Fault Correction

As mentioned earlier, a low cost solution for RF self test, with a view towards improving reliability of the integrated circuit part has not yet been observed in published literature. We propose a technique to drastically increase RF integrated circuit reliability not only by quantifying the performance of the RF circuit on-chip but by also correcting for the change in performance. This work demonstrates this concept towards correcting

the input match of an LNA: it is the first step towards the grand vision of self-corrective circuits.

The end-result is a methodology that will quantify and correct the performance of the RF circuit to account for process variations and faults as well as package and passive parasitic tolerances. This will not only make the RF circuit insensitive to package parasitics but will also allow it to be portable between various packages while dynamically adjusting the performance to account for the parasitics in the new package.

1.5.3 Organization

A system for the self-correction of the input match for any RF front-end circuit such as a Low Noise Amplifier (LNA) or mixer is described in Chapter 2. A novel two-tonal approach is presented wherein the testing process depends solely on the difference between two signals that pass through the same sensing circuitry, thus rendering the entire technique insensitive to process, temperature, power supply and the precision of the test signal itself.

We demonstrate the application of this methodology to correct for shift in input match frequency due to variations in parasitic inductances at the input of the LNA and process faults such as variations in gate-source capacitances. The choice of this particular circuit is deliberate: the LNA is the most critical circuit in any RF front end, because the noise and the gain of this block most influences the noise figure of the entire front end. Therefore, the testability and reliability of this sub-circuit is of prime importance, to ensure reliability of the entire RF product. The circuit implementation of all components is discussed in Chapter 3, while the results and layout are presented in Chapter 4. The

proposed technique is in itself very robust and will not be affected by variations in process or temperature. In addition to this, the method also involves low computational and power overheads since it does not require the presence of a DSP core. The technique uses input signals of moderate precision to test and correct the front-end circuit with correction times lower than 30 microseconds. Chapter 5 lists the summary and directions for future work.

This work is the first step towards the ultimate goal of package independent, fault tolerant RF Integrated Circuits.

Chapter 2. ARCHITECTURE

- 2.1 Why feedback will not work
 - 2.2 The 'Locked loop' concept
 - 2.3 Sensing the Input match
 - 2.4 The novel 'two-tonal' approach
 - 2.4 Signal processing
 - 2.6 The 'Tapped coil'
 - 2.7 Self-correction algorithm
 - 2.8 Merits of this architecture
-

2.1 WHY FEEDBACK WILL NOT WORK

Traditionally, self-correction in analog circuits has been achieved by using voltage or current feedback, where a part of the output voltage or current is sampled and fed back to the input to achieve increased robustness with respect to process variations. However, this technique has several pitfalls when applied to the RF domain. In integrated RF front ends, it is not always possible to have access to the output port of the individual circuit to sample the output signal without influencing the performance of the circuit. As mentioned in the previous chapter, the entire scheme *must* be minimally intrusive. In addition to this, feedback components such as transformers, multipliers, etc., have wide tolerances making the entire feedback system unreliable. This approach creates significantly complex stability issues. In comparison to low frequency circuits, RF circuits are highly sensitive to layout parasitics and mutual coupling effects. Metal trace parasitics, in the order of a tenth of a nano-henry and tens of femto-farads are no longer negligible due to operations in the GHz domain. While stability is inherently difficult to achieve at these frequencies, such fine sensitivity to parasitics and coupling further

complicates the issue, degrading both reliability and predictability. RF circuits with no feedback are finely balanced. Introducing feedback will essentially re-define the entire design paradigm, and destroys our objective of rendering current RF circuits fault-tolerant with *minimal intrusion*. It is thus seen that traditional feedback techniques introduce significant design complexity, creating a need for the redesign of the RF circuit in question as a complete feedback system, with all its associated complexity.

Figure 2.1 The self-correction methodology.

2.2 THE 'LOCKED LOOP' CONCEPT

The current work proposes an alternative technique that senses the performance of the RF circuit with minimal intrusion while simultaneously removing the constraints on

the feedback circuitry. It is analogous to the locking¹ achieved in Phase Locked Loops (P.L.L.), and hence the terminology ‘locked loop’. The technique consists of an RF forward path where RF information (in the case of this work, the transient H.F. current) corresponding to the circuit performance is sensed with minimal intrusion and amplified to required levels. As will be described in greater detail in subsequent sections, since this methodology does not pose any noise requirements, simple amplifiers with resistive loads can be used to achieve this gain. Also due to the robustness of the two-tonal technique, (described in Section 2.4) the actual numerical value of the gain does not influence the self-calibration. This amplified information is then down converted to base-band or DC for further processing. The resultant baseband/digital signal quantifies the performance metric under question and can be used as a BiST readout. This signal is then used to modify the requisite design parameters in the RF circuit to correct for the variation in performance without requiring any redesign of the original circuit. This idea is summarized in Figure 2.1.

Since the sensed RF information is not necessarily at the output node, the proposed method lays much greater emphasis on avoiding intrusion into the circuit performance. In addition to this, the entire feedback path functions in the low frequency or DC domain thereby alleviating the stringent noise and aforementioned design complexity requirements that plague traditional high frequency feedback schemes. As will also be seen, this methodology differs from the traditional feedback concept in one

¹ As in P.L.L.’s, the algorithm used in this work iterates through a series of possibilities, and at the end of each cycle computes if it has moved closer to the desired performance. Once a ‘lock’ is achieved, the process is complete.

more principal aspect: the output is neither sampled, nor fed-back to the input. Instead, the performance metric is measured, and a decision is made, dynamically, to modify (if required) a design parameter in the circuit. This ‘self-correction’ signal is in the form of a digital word, eliminating the potential problems of noise and precision. Both the input and output ports of the circuit under consideration remain untouched. Since most of the processing circuitry acts on low frequency signals, these circuits will also present relatively low overheads in the RF front-end. The following chapters of this work will describe the application of this methodology towards the self-correction of the input-match of a LNA.

The objective of input match self-correction was addressed by a four fold approach: firstly, to sense a signal which is indicative of the input match of the circuit; secondly, to process this signal appropriately into a form which quantitatively describes the input match of the circuit; thirdly, to use this information to send a signal back to the circuit where the match can be re-calibrated towards the desired value, and finally to provide for a mechanism in the circuit which can adaptively change S_{11} in real time based on the aforementioned feedback signal.

2.3 SENSING THE INPUT MATCH

The first step in this process is to establish a means of sensing some signal from the circuit that, with further processing if required, will ultimately provide information about its input match. RF circuits draw current from the power supply, which provides definite signatures that can be analyzed (with minimal intrusion) to determine circuit

attributes. Some potential placements of the sensing element for a single-ended Cascode LNA are shown in Figure 2.2 [19]:

- Placing it in series with the drain inductor (Figure 2.2 (a)) degrades gain, S_{22} and noise figure.
- It can be placed in series with the bypass capacitor (Figure 2.2(b)), which is necessarily present in almost every RF circuit². This placement however, degrades gain and S_{22} significantly.
- Placing it in series with the source inductor (Figure 2.2(c)), and re-designing the input match along with the sensing resistor results in minimal impact on S_{11} and noise figure.

Fig 2.2 Potential placements for the sensing resistor

² RF circuits have bypass capacitors to provide the H.F. current, since the power supply path from the outside path will present non-negligible parasitic impedances.

Further, it is advantageous for this element to be a resistor, as opposed to an inductor or capacitor³. From the above discussion it is evident that, in terms of minimal intrusion, placing a small resistor in series with the source inductor results in the optimal solution.

This approach creates a voltage indicative of the input match frequency with minimal intrusion on the circuit's behavior. It is possible to distinguish changes in the current due to faults on the output side of the circuit by using a similar mechanism at the input side of the next circuit in the RF front-end chain (for example, the LNA is followed by a Mixer). By co-designing the circuit with the sensing resistor, its impact on input match can be rendered negligible, and on noise figure and dynamic range, minimal⁴.

The current variations in the LNA due to a shift in the input match are of small magnitude (tens of μA). Further, since the resistor value is quite small (7 ohms, in this work), this voltage needs to be sufficiently amplified before further processing. The voltage from the resistor is fed to a source follower stage, which provides isolation to the LNA from the rest of the sensing circuitry.

2.4 THE NOVEL 'TWO-TONAL' APPROACH

As will be described later in this chapter, it is the peak-to-peak amplitude of the voltage across the sensing resistor that contains input match information and hence we need to convert this RF voltage into DC, which quantifies S_{11} . The sensed RF voltage is

³ The quantification of any performance metric in a RF circuit generally involves sensing certain signals at multiple frequencies. The frequency dependent characteristics of capacitors & inductors complicate this process.

⁴ [19] discusses the impact of the sensing resistor on LNA design and its performance in greater detail.

peak-detected and used for further processing. The circuitry that performs this operation is called the ‘sensor chain’, and is explained in Section 2.5.

One of the most important requirements of this process is to ensure that the self-correction circuitry itself is extremely robust; process variations and faults in the self-correction circuitry *should not* be mistaken for that of the circuit under consideration. Towards this objective, a novel ‘two-tonal’ approach is presented, which, due to the fact that its output is the difference of two signals that pass through the same overhead circuitry, is extremely resilient. This approach further altogether removes the dependency on absolute parameters like accuracy of gain, linearity, etc.

Figure 2.3 The ‘two-tonal’ approach

For a given input match, the spectral output of this sensor chain is a steadily decreasing monotonic (almost linear) curve as frequency increases. Further, the current in the LNA and hence the sensed voltage varies monotonically as the S_{11} match is varied. To ascertain the exact offset through which the input tuning frequency needs to be shifted and to render this technique independent of process, temperature and power supply variations in the sensing circuitry itself, we use the two-tonal approach. The success of this methodology depends, among many other things, on the careful selection of tones. They must lie on either side of the desired input match frequency (shown in Figure 2.3 as Tone 1 and Tone 2) such that the S_{11} variation lies within their bounds. For example, suppose the LNA is designed for a nominal match at 3 GHz and the expected input match variation is between 2.8 GHz and 3.2 GHz. Tone 1 must be chosen such that it is less than 2.8 GHz and tone 2, greater than 3.2 GHz. This selection procedure ensures that the monotonicity of the sensed voltage versus input match is consistent across the frequency spread (2.8 GHz to 3.2 GHz, in this case).

Two test signals corresponding to the above frequencies are applied to the LNA one after the other. Each signal passes through the same sensing circuitry and these outputs (V_{tone1} and V_{tone2}) are peak detected and stored on two capacitors. Decreasing the input matched frequency increases the amplitude of the first tone (V_{tone1} , as depicted in Figure 2.3 (b)) and decreases the amplitude of the second signal (V_{tone2} , as depicted in Figure 2.3 (b)). The difference between V_{tone1} and V_{tone2} provides a measure of the shift in S_{11} , and hence the frequency offset by which input match needs to be moved to correct it to the designed value.

The fact that both tones pass through the same sensor and peak detector, and it is their difference that is processed, renders this process robust. Any unexpected variation, for example, high ambient temperature, will affect both the tonal-signals equally, and the subtracted signal will retain its faithfulness. It is shown in Chapter 4 that this method is insensitive to process variations, temperature and power supply variations. Furthermore, this differential method of ascertaining input match frequency renders the technique immune, for example, even to a 50% variation in the gain of the sensor, tolerances in the sensing resistor value or the precision of the input test signal itself. It must be mentioned at this point that the use of a third tone at the desired input match frequency (3 GHz, in the above example) can also provide quantification of the magnitude of the input match. This information can be used to correct the magnitude of the match if it falls below acceptable levels.

2.5 SIGNAL PROCESSING

As mentioned in the earlier sections, the sensed voltage from the LNA is quite small in magnitude and needs to be amplified. It is then converted to DC by peak-detecting the signal. Consequently, any amplification of the voltage signal mentioned above need not be noise-free or low-noise⁵. This allows one to use resistors, and simple single-stage gain configurations (the push-pull amplifier, or the Common Source amplifier used in this work) can amplify the signal up to a few hundreds of millivolts.

⁵ We would otherwise be faced with the amusing conundrum of requiring LNAs to quantify LNA performance. It should also be mentioned that using other variants of RF amplifiers (with inductors) in the self-correction process will greatly increase chances of faults and variations in the testing circuitry itself, thus opening the door for mistakenly identifying non-existent faults.

Robustness can be accomplished with feedback in the amplifier (source degeneration, for example), but after extensive simulations, it was deemed unnecessary due to the resilience of the ‘two-tonal’ approach. Further, the amplitude of the test signal can be considerably higher than the typical input signal amplitudes to the LNA, within the limits of its linearity and dynamic range. This in turn brings down the amplification needs of the sensing amplifier. This signal is then input to a peak detector which outputs a DC signal in proportion to the input match of the LNA.

The processing circuitry required for this work consists of:

- PMOS Source-follower
- RF Sense Amplifier
- RF Peak detector (PD)
- Storage elements (capacitors)
- DC Buffers
- DC Subtractors
- Comparators
- Digital logic and clocking

The self-correction algorithm, explained in detail in Section 2.7, will elaborate on the functionality of each circuit. The output (for each tone) from the peak detector is stored on different capacitors, and the subtraction is performed by op-amps. The op-amps draw their inputs through buffers to minimize charge loss in the capacitors and isolate the peak detection circuitry. The rest of the processing circuitry is comprised of comparators, again derived from op-amps, and digital circuitry and clocking. As will be seen later, a number of timing pulses are required for this process, and in this work, they are all derived from a global clock signal. The final output of the processing circuitry will be an n-bit digital word, which will be fed to the LNA. It will also be seen that although the output is a digital word, we avoid the need for A-D converters in our

technique. It must once again be emphasized that none of the aforementioned processing circuitry has high-precision / accuracy requirements.

2.6 THE ‘TAPPED COIL’

With the above setup, the last piece required to complete the ‘puzzle’ is a mechanism in the LNA which, while not requiring any major design modifications, must allow for dynamic input match changes. The input match of the inductively-degenerated cascode LNA is given by [20]:

$$Z_{in} = \frac{g_m L_s}{C_{GS}} + j(\omega(L_s + L_g) - \frac{1}{\omega C_{GS}})$$

Figure 2.4 Sensing the input match using resistor R_s

- g_m is the transconductance of M_1 (Figure 2.4). It is controlled by the size (W/L) and the DC current through M_1 . However, varying g_m to vary the input match will also result in other undesirable changes, like power consumption, gain, dynamic range, etc.
- L_s is the source coil of the LNA. It is responsible for the magnitude of the match. In other words, if correctly balanced, at the resonant frequency, the effective input impedance will be a pure resistive value of:

$$Z_{in} = \frac{g_m L_s}{C_{GS}}$$

Hence varying L_s will *not* vary the input match frequency.

- C_{GS} is the gate-source capacitance of M_1 . Adding additional capacitance in series with L_g will enable us to control S_{11} frequency. In order to be dynamically adjustable, a varactor is needed, but unfortunately, MOS varactors in most RFIC processes (IBM, TSMC, both 0.25 μm and 0.18 μm processes) *must* have one end grounded. Hence the capacitor has to be used in parallel (from gate of M_1 to ground), rather than in series. Using the capacitor in series has the undesirable effect of changing the real part of the input impedance too⁶, and after numerous simulations it was concluded that a varactor can be used only if a transformer is used to couple the input source to the input port of the LNA.

⁶ This leads to a complex impedance network, which when transformed into its series RLC equivalent (after a fair amount of math), changes the real part of the impedance when the varactor is varied. This implies that the varactor varies both the frequency and magnitude of the input match.

- L_g is the gate coil of the LNA, and varying this element changed *only* the S_{11} match frequency. In this work, it is the gate coil that acts as the vehicle that completes the self-calibration ‘locked-loop’.

In order to adaptively move the input match of the LNA, the gate inductor value is made variable by tapping it at several points. Package parasitics introduce additional inductance (with very large tolerances) at the input pad of the LNA (for example, bond wires). In this work, we show that process faults and these parasitics can be accounted for in real-time by re-calibrating the input coil of the LNA. This technique also facilitates the use of the LNA in different packages with different parasitic inductances; the circuit can re-align itself to the original input match on the fly.

The gate coil (L_g) is designed for a nominal value and then tapped off at different intervals in its outer-most turn, with each tap leading to a switch. By including the interconnects and switch capacitance in the design process, this coil can be characterized to give accurate inductance values. Based on which switch is turned on, one and only one tap of the coil will be shorted to the input pad of the LNA (Figure 2.5), and this tap determines the input match of the LNA.

2.7 SELF-CORRECTION ALGORITHM

In this section, we describe the mapping of the above methodology to the specific purpose of correcting the input match of a LNA. The circuit architecture is depicted in Figure 2.5 and the algorithm for calibration is outlined below:

Figure 2.5 Circuit Architecture for correction of LNA input match frequency

Step1: Having chosen the two tones (tone1 and tone2) to be used for the input signals, the switch connecting the first tap of L_g is closed, and a test signal with a frequency of tone1 is applied to the input of the LNA.

Step 2: The resultant output of the PD is stored in capacitor C_1 through switch S_1 . S_1 is now turned off.

Step 3: Repeat step 1 for tone2, and store the resultant output in capacitor C_2 . The switch connecting the first tap of the inductor is now turned off. Since the capacitors have no

discharge path, their leakage is minimal and can be reduced to negligible values by choosing appropriate capacitances.

Step 4: The second tap of L_g is now closed (changing the value of L_g and hence moving the input match) and the above process is repeated, storing the P.D outputs in different capacitors (C_3 and C_4). At this stage of the process, we have stored the output of the sensor chain for two taps of L_g .

Step 5: Switches S_5 through S_8 are turned on simultaneously, connecting the capacitors to the buffers. For both taps of L_g , the tonal difference amplitudes are calculated by means of two subtractors (V_{T1} and V_{T2}).

Step 6: Now V_{T1} and V_{T2} are compared individually with V_{IDEAL} , where V_{IDEAL} is the voltage difference of the two tones for the desired input match. Although in this work V_{IDEAL} is a finite value for ease of implementation, it can be ensured that V_{IDEAL} is 0 V by slope-correcting the gain of the sense amplifier with respect to frequency, thereby making the calibration independent of a fixed reference voltage.

Step 7: If V_{T1} is closer to V_{IDEAL} than V_{T2} , the first tap of L_g is connected to the input pad, and self-calibration process is complete. If V_{T2} is closer to V_{IDEAL} , then steps 1 to 6 are repeated, this time for the second and third taps of L_g instead of the first and second taps.

Step 8: The self-calibration will be complete when $V_{T(i)}$ will be closer to V_{IDEAL} than $V_{T(i+1)}$ (this is true since the amplitude of the sensed voltage is monotonic as the input match frequency is varied). If this condition never occurs, then the last tap of L_g is chosen since it will provide an input match closest to the desired frequency.

All the switches need to be turned on for specific intervals periodically, and these pulses are derived from a global 2 MHz clock, using decoding circuitry. The algorithm described above follows the linear-search model. Although not maximally efficient in terms of the time taken, this methodology provides adequate recompense in return, in the form of simpler circuitry and ease of implementation.

2.8 MERITS OF THIS ARCHITECTURE

- Perhaps the most important criterion of any test-and-correct circuitry is to ensure that any faults and variations of the test circuitry itself will not mistakenly identify non-existent faults. The two-tonal approach, coupled with simple processing circuitry that does not use any feedback or inductors greatly minimizes the probability of that occurrence.
- The ‘locked-loop’ methodology eliminates all the associated complexity of a traditional feedback scheme, while retaining its usability.
- It requires minimal overhead circuitry.
- It requires no DSP cores or processor requirements, which is typical of many RF test methods.
- It does not require A-D conversion or analog memory cells, and consumes little power. The entire processing circuitry, with the exception of a few latches, can be turned off completely once the process is complete.
- The entire time taken for the self-calibration depends on the number of taps in L_g ; we show in this work that each tap requires about 3 μ s

processing time. This compares very favorably to times taken by current commercial test schemes [8], wherein the testing period itself is in the order of hundreds of milliseconds.

- The only *intrusion* in this methodology is the small sensing resistor (7 ohms in this work). The value of the resistor is flexible, and can be reduced further at the cost of increasing the gain of the sense amplifier. This should not pose major problems since cascading an extra stage of the amplifier is straightforward and increases gain significantly.
- By dynamically adapting a single design to various package variations and facilitating package portability, it cuts down on design cycle time, and reduces the dependence of circuit performance on accurate package characterization and modeling.

The architecture described above carefully side-steps many potential roadblocks in sensing and correcting the performance of RF circuits. The simplicity and ease of implementation, which is the subject of the next chapter, is testimony to the strength of this methodology.

Chapter 3. CIRCUIT IMPLEMENTATION

3.1 Single-ended 1.9 GHz LNA with Sensing resistor

-3.1.1 LNA Design

-3.1.2 Tapped Gate coil

3.2 The Sensor chain

-3.2.1 Source Follower

-3.2.2 Amplifier

-3.2.3 Peak Detector

3.3. Low frequency & Digital processing

3.4. Timing

3.5. Limitations

3.6. Implementation Summary

The previous chapter has described the general methodology that can be adapted to specific RF circuits. Typically, RF front-end circuitry is interfaced to the outside world (antenna) through a Low Noise Amplifier (LNA). Consequently, it is the LNA that forms the physical connection between the package and the integrated circuit, and package parasitics have a direct impact on its performance. Further, the LNA is the most critical block of any front end since its noise and gain affects the performance of the entire system. Thus it becomes an ideal choice for this work – self-correction can be demonstrated for both process faults and package tolerances/flexibility.

The Single-ended Cascode LNA is perhaps one the most widely used LNA topologies [17]. Although the balanced (differential) topology⁷ offers more advantages, the single-ended LNA enjoys popularity for its ease of implementation, and the fact that it possesses lesser real-estate and power consumption requirements.

⁷ Although the specific implementation details may differ, the methodology, in general, can be implemented for other topologies and other classes of circuits as well.

The self-correction methodology described in preceding chapter has been applied to a 1.9 GHz CMOS Single-ended source degenerated narrow-band cascode LNA. This chapter discusses, in detail, the implementation of the LNA and all of the associated processing circuitry. All circuitry has been designed and laid out in the IBM 6 Metal layer 0.25 μm RF process (CMOS6RF) with a 2.5 V power supply.

3.1 SINGLE-ENDED 1.9 GHz LNA WITH SENSING RESISTOR

The first stage of a receiver is typically a low noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages. Aside from providing this gain, while adding as little noise as possible, an LNA should accommodate large signals without distortion, and frequently present a specified impedance, usually 50 ohms, to the input source.

The RF circuit in question, in this case the LNA, needs to be co-designed to accommodate for two factors. It must accommodate a minimally intrusive sense mechanism that will allow the extraction of its match information, and should also provide for a mechanism to recalibrate the match if deemed necessary, to obtain optimal performance.

3.1.1 LNA Design

The sensing mechanism in the LNA is provided for by a 7 ohm resistor (R_s) that has been placed in series with the source inductor, in the return current path of the LNA. As explained in Chapter 2, this is the point of least intrusion for the resistor, and the sensed current can be mapped to changes in the input match of the LNA. The resistor

value is the optimal solution for the trade-off between reducing the degradation of noise figure and dynamic range of the LNA on one side and achieving sufficient sensitivity to be able to adequately detect variations in the input match. Although S_{11} is also degraded, the LNA can be designed with the resistor in the equation for input match to get back most of the input match. Due to the differential nature of the methodology described in previous sections, the success of the calibration approach is unaffected by the tolerances in the actual value of the resistance.

Figure 3.1 Schematic of Cascode LNA with tapped gate inductor

The schematic of the LNA is shown in Figure 3.1. The addition of the sensing resistance changes the input match equation, adding two extra terms:

$$Z_{in} = \frac{g_m L_s}{C_{GS}} + j(\omega(L_s + L_g) - \frac{1}{\omega C_{GS}}) + R_s - j \frac{g_m R_s}{\omega C_{GS}}$$

Co-design with R_s involves designing S_{11} using this modified equation. At resonance, the imaginary part of the impedance cancels out since:

$$\omega(L_s + L_g) = \frac{1}{\omega C_{GS}} + \frac{g_m R_s}{\omega C_{GS}}$$

resulting in an input resistance of:

$$Z_{in} = \frac{g_m L_s}{C_{GS}} + R_s$$

The value of L_s required to achieve a 50 ohm match is 0.75 nH. The input transistor of the LNA forms a current mirror with the transistor ($M3$) of the bias circuit. The width of the bias circuit transistor is chosen to be one-tenth of the input transistor to minimize power overhead of the bias circuit. The supply voltage and a reference resistance (R_{BIAS}) set the current through the left-hand side of the current mirror in conjunction with the V_{gs} of the input transistor. Resistance R_2 must be made large enough so that its noise contribution can be ignored [20]. Since the input resistance is 50 ohms, R_2 is chosen to be 5 K ohms. An external gate-source capacitance (C_{GSX} , Figure 3.1) with a value of 0.6 pF has been included; this results in a nominal L_g value of 9 nH. The output load (L_d and C_L) values were chosen to resonate at 1.9 GHz.

$$f = \frac{1}{2\pi\sqrt{L_d C_L}}$$

The DC blocking capacitor is chosen to be 30 pF so that its impedance at 1.9 GHz is negligible. A power supply bypass capacitor, as discussed earlier, of 30 pF was connected between V_{DD} and ground. Since in this work, we are interested in the input-

side of the LNA only, no impedance-transformation is needed at the output node of the LNA. It is directly connected, through a DC blocking capacitor, to the output pad.

3.1.2 Tapped Gate Coil

The self-correction of the LNA in the present case has been achieved by using a digitally tapped gate inductor at the input of the LNA. The digitally tapped inductor as shown in Figure 3.1 consists of NMOS switches that are connected to the gate inductor at various points in its outermost turn and can be used to tap into various sections of the gate inductor. Therefore, by turning the switches on or off, the value of the gate inductor can be varied, thereby varying the frequency of match.

It is of significance that the inductor and its associated parasitics be characterized accurately. The gate inductor was laid out and simulated using ASITIC [21] to determine

Figure 3.2 Layout of gate coil. The dimensions are: radius = 220 μm , width of metal = 5 μm , spacing = 5 μm . It was created on the topmost (Analog metal) layer.

the parasitic inductances and capacitances associated with the structure (Figure 3.2). This structure includes all the metal strips used for various interconnections up to the input pad. The NMOS switches are chosen to have a W/L of $68\mu\text{m}/0.25\mu\text{m}$, providing an ideal balance between on-resistance and device capacitance⁸. The five ‘taps’ of the coil are connected to the NMOS switches, and are referred in subsequent sections as tap1, tap2, and so on, up to tap5.

Tap no.	Inductance value	Corresponding S_{11} freq.
1	7.4 nH	1.7 GHz
2	8.1 nH	1.8 GHz
3 (nominal value)	9 nH	1.9 GHz
4	10 nH	2.0 GHz
5	11 nH	2.1 GHz

Table 3.1 The tapped coil values and corresponding S_{11} frequency

Figure 3.3 Pi-model for the gate coil when tap 3 is turned on (nominal value)

⁸ Bigger widths reduces the on resistance (in direct proportion), while increasing gate-source, gate-drain and bulk capacitances.

The LNA is then co-designed to account for these parasitics (the Pi-model from ASITIC is used for the gate coil, Figure 3.3) as well as the parasitic capacitances and finite on-resistance associated with the MOS switches. The tapped gate inductor designed in this work has five taps, providing inductance values between 7.4 nH and 11 nH (Table 3.1). These taps were chosen such that the input match of the LNA can be varied from 1.7 GHz to 2.1 GHz in steps of 0.1 GHz. Since all the taps have to be connected to a single input pad, care has been taken to:

- Ensure that the interconnects are placed at least three turn widths away from the coil.
- All the taps have been drawn out with perpendicular metal strips that are wider than the width of the inductor to minimize additional inductance.

In addition to the above precautions, the whole structure was simulated in ASITIC to account for any mutual and additional inductances.

The input to the NMOS switch array is a digital word that dictates which one of the 5 taps is to be turned on, thereby fixing the value of the gate inductance of the LNA. For example, if the parasitic inductance of the package increases, the tap can therefore be shifted, reducing the amount of on-chip gate inductance, thus restoring the frequency of input match for the LNA. The resolution or range of correction can be improved by increasing the spacing and number of taps respectively.

3.2 THE SENSOR CHAIN

3.2.1 Source Follower

The voltage across the sensing resistor R_s is then fed to a PMOS source follower with a resistive load. The source follower serves to isolate the LNA from any processing circuitry that will follow and also provides a relatively broadband interface to transfer the sensed signal across the sensing resistor to the processing circuitry. The size of the source follower transistor is kept small so that it presents a negligible capacitance at the source node of the LNA. This capacitance is equivalent to adding additional interconnect related parasitics at the source node of the LNA, and it does not affect the LNA performance. Its output is AC-coupled to the amplifier stage through a DC blocking capacitor.

Figure 3.4 The source follower and amplifier

3.2.2 Amplifier

The magnitudes of voltage variations across R_s corresponding to changes in the input match are relatively small. However, as described in the previous section, since the

amplitude of the test signal can be considerably higher than typical LNA inputs, the resultant gain requirements of the amplifier are very moderate. In addition to this, due to the absence of any restrictions on noise figure of the sensed signal simple common source amplifiers with resistive loads can be used to achieve the required amplification. Push-pull amplifiers can provide very high gain, but need extensive bias stabilization for a stable operation. Two cascaded common source stages have been used to construct the amplifier because it is possible to AC-couple the sensed signal from one stage to another, while providing independent DC biases to each stage. The minimum required gain from this amplifier was eight. Simple resistive bias was found to be adequately stable, since it depends on the ratio of two resistors⁹. 1 K ohm resistive loads have been used because they provide the required gain, while also presenting optimal source impedance to the peak detector that follows. No feedback has been incorporated into the amplifier due to the inherent robustness of the two-tonal approach¹⁰. As will be shown in Chapter 4, as long as the amplifier can provide a minimal gain at all process, supply and temperature corners, variations in the numerical value of the gain will not affect the successful calibration of the RF circuit. The amplifier and the source follower form the sense amplifier (SA, Figure 2.5, Figure 3.4). Since more common source amplifiers can be cascaded as described above (making it possible to achieve higher gains), it may even be

⁹ The resistive pair mismatch data in the IBM PDK lists the percentage mismatch for various resistance pairs. By choosing appropriate widths for the polysilicon resistors, mismatch can be minimized to less than 2-3%.

¹⁰ The amplifier was designed with source-degeneration feedback & drain-gate resistor feedback, and simulation results indicated that the final success of the process would not be compromised even in the case of no feedback.

possible to reduce the value of the sensing resistor by a few ohms to take advantage of the available gain, further minimizing intrusion on the LNA.

3.2.3 Peak Detector

A standard half-wave diode (inverting) voltage doubler (Figure 3.5) has been designed to peak detect the sense amplifier's output. The diodes are current-biased in the linear region for the range of its input signals. Since the P.D output has to be stored on four different capacitors, the output capacitor is duplicated four times ($C_1 - C_4$) and they are connected to node N_1 (Figure 3.5) through transmission gates ($S_1 - S_4$). This eliminates the need for external memory capacitors. The transmission gates are driven by digital pulses generated in the digital circuitry. The ratio of input and output capacitance values was chosen to be 5:3 to ensure optimum charge transfer.

Figure 3.5 Half-wave inverting diode Peak Detector

This peak detector was robust across process, supply and temperature variations. The drift in diode characteristics will be canceled out since the difference of two signals that have passed through the same PD is considered. The diode area is a trade-off

between on-resistance and capacitive parasitics. For this application, the on-resistance is not a critical issue since we can always allocate extra time for the capacitors to charge.

The entire sensor chain is also provided with a robust high frequency return path by connecting a 30 pF capacitor between power supply and ground.

3.3 LOW-FREQUENCY & DIGITAL PROCESSING

The outputs of the peak detector are fed to the two subtractors (S_{B1} and S_{B2} , Figure 2.5) through unity gain buffers. Due to the presence of the buffers, the peak detector capacitors have no discharge path (to discharge the capacitors when required, a switch is connected across each capacitor and ground. It is only turned on at the end of a correction cycle) thereby retaining all their charge except leakage. Since the signals handled by the unity gain buffer and the two subtractors are DC voltages, a standard folded cascode op-amp (Figure 3.6) is adequate for both these functions. The folded cascode configuration is chosen because of its high output impedance, high gain and inherently high output swing for the given process.

The op-amp is biased using a wide swing cascode current mirror with an external bias reference of 1 V. Accuracy requirements are fairly relaxed since the op-amps are used in a feedback system at DC levels only. The op-amp was designed to have a gain > 1000, a power consumption < 1mW, and was compensated with a 7 pF capacitor. The subtractors were designed to have a gain of 3, with the corresponding feedback resistor values being 100K ohms and 300K ohms. Since the gain is dependent on the ratio of

these resistors¹¹, it is not subject to huge variations. The two comparators C_{P1} and C_{P2} are also obtained by using the folded cascode configuration. The outputs of the comparators are used to drive standard digital logic.

Figure 3.6 Folded-cascode op-amp connected as a unity-gain amplifier with current mirror bias.

The self-correction process begins by discharging the storage capacitors and resetting the digital circuitry.

Figure 3.7 Generation of “Continue” signal. When “Continue” goes low the calibration clock is held to zero by A3 and the process halts.

¹¹ For an unsalicyded polysilicon resistor, the absolute tolerance is in the order of 25-30%, while as the mismatch tolerance between a resistor pair is less than 5% when appropriately sized and laid-out.

- The '*continue*' signal (see Figure 3.7) essentially controls the calibration exercise. It is clocked by the '*discharge*' pulse, which ensures that any transient glitches in the '*continue*' signal will not halt the calibration process prematurely (latch L_1 in Figure 3.7).
- At the end of each comparison cycle, '*discharge*' goes high to reset the capacitor charges to zero before the next cycle begins. The state of the '*continue*' signal when '*discharge*' is high will determine if the cycle of calibration stops.
- As we proceed through the taps sequentially, (tap1 and tap2 are compared in the first cycle, tap2 and tap3 in the second, and so on), the '*continue*' signal remains high until we reach the tap that shifts the S_{11} match closest to the desired value.
- At the end of this cycle, '*continue*' goes low (AND gate A_2) and the cycle stops.
- This indicates that the best input match lies in-between these two taps, and the tap closest to the desired match will be chosen using another set of subtractors, after which the calibration process will stop.
- Once calibration is complete all the digital circuitry can be powered off with the exception of the latches holding the final tap values. Therefore the calibration circuitry poses very low power overheads.
- The calibration process can correct any input match that lies within a frequency window that is determined by the number and resolution of the taps. It is possible that the input match degrades beyond the 'window'. If S_{11} match frequency has reduced drastically, for example, then tap1 of the inductor will provide the closest match.

- This potential occurrence is also accounted for by the AND gate (A_2 in fig 3.7) that creates the ‘*continue*’ signal. When the condition occurs wherein outputs of both comparators are low in the first cycle itself, A_2 will pull ‘*continue*’ low, ensuring that tap 1 is turned on and the calibration process is not continued any further.

3.4 TIMING

The timing for the entire correction process including the timing for the switches is carried out in integral multiples of a time unit provided by a single low frequency (2 MHz) clock, which is generated off-chip. This eliminates any dependence on absolute delays and makes the timing scheme process independent. The timing for various switches is derived by decoding the appropriate states of a 5-bit synchronous counter (Figure 3.8) and latching the resultant signal to eliminate glitches. The remainder of this section discusses the decode circuitry¹². Karnaugh maps were used for some decode logic circuits. The process described below is summarized in Table 3.3, at the end of this section.

The 5-bit J-K flip-flop counter forms the heart of this decode setup. It begins to countdown when the process is started. Its five outputs (Q_0 - Q_4 , Figure 3.8) are then used to generate digital pulses appropriately. When the proper gate coil tap is identified, the clock to the counter is frozen, and as shown later, that tap is permanently turned on, until

¹² All digital circuitry used in this work was constructed using the standard cell library for the IBM 0.25 μ m process.

the next correction cycle. It is driven by a global RESET signal that resets its states when a new correction cycle begins.

Figure 3.8 The 5-bit synchronous counter using J-K flip flops. CLK is the global clock signal. The SET pins of all flip-flops are connected to ground. RESET is a global signal that resets all the flip-flops whenever the self-correction process begins. Q0-Q4 are the counter outputs.

Figure 3.9 shows the logic that uses the outputs of the 5-bit counter to generate the pulses that drive the output of the peak detector (switches S_1 - S_4 , Figure 3.4). The logic for switch S_1 (C1L in Figure 3.9), for example, is given by:

$$C1L = \overline{Q_4} \cdot \overline{Q_3} \cdot \overline{Q_2} \cdot Q_1 \cdot Q_0$$

All the four tracks pass through three stages of gates to ensure that the time-delay from the clock transition to output transition remains constant. The output is then latched to ensure that any transitional glitches are suppressed. The four capacitors are discharged

Figure 3.9 The pulses for the four capacitor outputs of the peak detector. C1L-C4L drives switches S1-S4 respectively (Figure 3.5).

Figure 3.10 The capacitors of the peak detector are discharged before each cycle.

before any self-correction process begins (by the global RESET, a switch shorts the capacitors to ground), and also after each cycle. For example, referring to the algorithm discussed in section 2.6, in the first cycle tap1 and tap2 are compared. Before the second cycle begins, the capacitors are discharged. This circuitry is depicted in Figure 3.10.

Figure 3.11 The 2-bit counter used to control the taps.

During each such cycle, two taps have to be turned on – these taps are decided by another 2-bit counter. In other words, this counter (Figure 3.11) will turn on taps 1 and 2 in the first cycle, taps 2 and 3 in the second cycle and so on. This is accomplished as follows:

- The global RESET clears the counter. When the counter output (S_1S_0) is 00, taps 1 and 2 are turned on (the circuitry for this operation is depicted in Figure 3.13).
- When the first cycle ends, the counter increments its count to 01. Now, in this cycle, taps 2 and 3 are turned on, and this process continues.

During each cycle, the two appropriate taps have to be turned on sequentially *i.e.*, during the first half of the cycle ‘tap i ’ is on and during the second half, tap ‘ $i+1$ ’ is turned on. The pulses for these taps are generated by the circuit in Figure 3.12. The output of Figure 3.12 is two pulses within each self-correction cycle. In each cycle, these pulses

have to be routed to the appropriate taps. This action is accomplished by decoding the 2-bit counter outputs (S_1S_0) with TAP1L and TAP2L (Figure 3.12). The logic is shown in Figure 3.13.

Figure 3.12 The decode logic used to turn on tap 'i' (TAP1L) and tap 'i+1' (TAP2L) in each self-correction cycle.

The last piece of circuitry needed is shown in Figure 3.14. We have already explained that the self-correction process is complete when the 'continue' signal goes

Figure 3.13 The decode logic used to turn on the appropriate taps in each cycle. In other words, the logic used to determine the 'i' and 'i+1' in Figure 3.12

Figure 3.14 When 'continue' goes low, the clock freezes, and the appropriate tap is turned on permanently.

Clock Pulse count	Output of 5-bit Counter (Fig 3.8)	Action taken
0	0 0 0 0 0	All digital circuitry is reset.
1	0 0 0 0 1	Tap 1 is turned on – TAP1L in Figure 3.12 and T1 in Figure 3.13
3	0 0 0 1 1	Switch S ₁ is turned on (the 1 st capacitor) – C1L in Figure 3.9
4	0 0 1 0 0	Switch S ₁ is turned off (the 1 st capacitor) - C1L in Figure 3.9
7	0 0 1 1 1	Switch S ₂ is turned on (the 2 st capacitor) – C2L in Figure 3.9
8	0 1 0 0 0	Switch S ₂ is turned off (the 2 st capacitor) – C2L in Figure 3.9
9	0 1 0 0 1	Tap 1 is turned off - TAP1L in Figure 3.12 and T1 in Figure 3.13
11	0 1 0 1 1	Tap 2 is turned on – TAP2L in Figure 3.12 and T2 in Figure 3.13
13	0 1 1 0 1	Switch S ₃ is turned on (the third capacitor) – C3L in Figure 3.9
14	0 1 1 1 0	Switch S ₃ is turned off (the third capacitor) – C3L in Figure 3.9
17	1 0 0 0 1	Switch S ₄ is turned on (the third capacitor) – C4L in Figure 3.9
18	1 0 0 1 0	Switch S ₄ is turned off (the third capacitor) – C4L in Figure 3.9
19	1 0 0 1 1	Tap 2 is turned off – TAP2L in Figure 3.12 and T2 in Figure 3.13
20 – 25		Time for processing circuitry to compute 'continue' signal
If 'continue' is low, the clock freezes, and the appropriate tap (tap1 or tap2, in this case) is turned on. If, on the other hand, it remains high, we continue.		
26	1 1 0 1 0	Discharge goes high – CAPDISCH in Figure 3.10
27	1 1 0 1 1	Discharge goes low – CAPDISCH in Figure 3.10
28	0 0 0 0 0	The 5-bit counter is reset. Simultaneously, the 2-bit counter in Figure 3.11 increments, and S ₁ S ₀ = 01
29	0 0 0 0 1	Tap2 is turned on now – TAP1L in Figure 3.12 and T2 in Figure 3.13
The process continues until 'continue' goes low. When continue goes low, the logic in Figure 3.14 will turn on the appropriate tap permanently.		

Table 3.2 The timing logic process summarized

low. At that instant, the clock to the timing circuitry is frozen¹³. The information as to which tap needs to be turned on permanently is present in the output bits of the 2-bit counter. These states are used in the logic shown in Figure 3.14 to latch the appropriate tap to 'on' position, and the self-correction process is complete.

The entire process described above is summarized in Table 3.2.

3.5 LIMITATIONS

The switches used in the tapped coil possess a finite on-resistance and capacitance, leading to two undesirable effects. The capacitance hangs at one end of the coil, thus reducing its self-resonant frequency. The typical self-resonant frequency of these coils is greater than 5 GHz¹⁴, and hence any minor (5-10%) degradation will not impact a circuit working at 1.9 GHz – no measurable change in the circuit performance can be detected. The on-resistance, however, degrades the quality factor of the inductor, increasing the noise figure. After optimizing the transistor's size for minimum noise figure, a degradation of 12-16% was observed. While this trade-off may not be acceptable for certain extremely low-noise applications, it can be tolerated in majority of RF front-end solutions. Future work includes exploring alternatives that impact noise figure to a lesser extent (there exists in literature [22] Q-sensing and enhancing circuits).

¹³ The clock of the timing counter is gated by the 'continue' signal. Therefore the entire calibration process is halted when the 'continue' signal goes low.

¹⁴ This is the absolute minimum. The Gate inductors (7nH-10nH) in most RF processes will have a self-resonant frequency of 8 GHz and above.

3.6 IMPLEMENTATION SUMMARY

As mentioned earlier, the single-ended Cascode LNA was chosen to verify the proof-of-concept due to its popularity and ease of implementation. Initially, the choice of a 7 ohm sense-resistor did seem to pose high-gain requirements in the following sense-amplifier. However, since the test signals are completely in the user's control, the LNA's input can be driven by signal levels that are higher than normal, bringing down the gain requirement considerably. There exists the classical design trade-off: higher resistor values will ease the burden on the processing circuitry, while intruding more on the LNA performance. More sophisticated amplifiers can be designed, and the value of the sense resistor can be reduced further. In the final analysis, 7 ohms does not degrade the LNA performance beyond acceptable levels and is a fair choice for this work.

As elucidated in Chapter 4, the use of a slope-corrected amplifier can eliminate the need for an external, accurate reference voltage source. With reference to varying the input-match, two solutions held potential – shunting a varactor across the gate of the input transistor, and tapping the gate coil. The latter approach was preferred since the varactor varies both input match frequency and magnitude, taking away a degree of freedom.

Another potential design decision was with respect to the various digital pulses that were needed. The use of state-machines was sacrificed in favor of the easier option of using a counter and decoding its output-states. Using a counter to decode all the pulses across five self-correction cycles requires a 8-bit counter. This work, however, circumvents this issue by using a single 5-bit counter (this counter is reused by re-setting

it after every self-correction cycle) and a 2-bit counter (this counter keeps a count of the self-correction cycles executed).

In essence, this work has adopted the simplest, yet workable, approach possible, embracing a safety-first approach and avoiding potential complications. By conclusively validating the self-correction proof-of-concept for the first time in RFICs, the door has now been opened for better and more sophisticated implementations.

Chapter 4. SIMULATION RESULTS

- 4.1 Circuit response
 - 4.2 The Self-correction process
 - 4.2.1 Addition of parasitic inductance*
 - 4.2.2 Reduction of C_{GS}*
 - 4.3. Robustness
 - 4.4. Layout
-

This chapter presents simulation results for the circuits presented in the preceding chapters and demonstrates the success of the self-correction methodology. Simulation under normal conditions is carried out at room temperature (28°C), nominal process parameters and a perfect power supply voltage (2.5 V). I.Cs, however, will be subject to a range of temperatures (based on their application), power supply fluctuations and process variations. It is common practice, and indeed necessary, to design circuitry such that it meets specifications at the two extreme conditions that it will possibly be subject to:

- Strong Corner: Lowest possible threshold voltage¹⁵, lowest possible temperature¹⁶, and highest possible power supply voltage. Since circuit performance will be better at this corner than normal conditions, care must be taken to ensure that specifications such as power consumption, dynamic range, headroom, etc., are acceptable.
- Weak corner is the opposite of the strong corner. Typically, circuitry is designed to meet minimum requirements at the weak corner.

¹⁵ The IBM Process Design Kit includes 3-sigma process variations and a corners simulation setup based on extensive test data.

¹⁶ MOS devices have negative temperature coefficients, and hence are 'stronger' at lower temperatures.

We present simulation results of the circuitry at all three conditions (strong, weak and nominal), and confirm the robustness of the two-tonal approach. The chapter concludes with the layout of the entire circuitry¹⁷.

4.1 CIRCUIT RESPONSE

For the cascode LNA designed above, it was ascertained that the input test signal could be as high as 160 mV before reaching headroom and linearity limits. To provide a safe margin, 130 mV was chosen as the amplitude for the test signals (since this is in the user's control, it can be changed during the process of calibration).

Figure 4.1 shows the spectral output of the sense amplifier when connected to the LNA. The response, as desired, is linear and monotonic over the frequency range of interest (the output increases with respect to frequency as the Peak Detector is inverting in nature).

Figure 4.1 Spectral response of sensor chain

¹⁷ All Simulation was carried out in Cadence ® Spectre RF suite, and layout in Virtuoso ®.

Tap no.	sensor chain o/p for tone1(1.6GHZ)	sensor chain o/p for tone2(2.2GHZ)
1	1098.54 mV	1391.57 mV
2	1112.85 mV	1375.63 mV
3	1128.67 mV	1365.23 mV
4	1150.61 mV	1356.95 mV
5	1166.88 mV	1355.01 mV

Table 4.1 Output of Sensor Chain for all taps of L_g

Figure 4.2 The transient response of the sensor chain. It is seen that the output settles to its final value at $t = 300$ ns.

Table 4.1 lists the output of the sensor chain (input to LNA, output from P.D) for both tones (1.6 GHz and 2.2 GHz) over all the five taps of L_g . As explained in Chapter 3, the output of tone 1 increases monotonically with respect to frequency as the input match frequency is reduced (since the peak detector is inverting in nature, the output of the sensor chain itself will actually decrease) and vice versa.

Figure 4.2 depicts the transient response of the sensor chain. It is seen that the output settles to its final value within 300 ns, and hence the choice of a 2 MHz clock is appropriate. The shortest possible pulse generated by the decode logic will be one clock

cycle, which, in this case, is 500 ns. It has been ensured that this time period is sufficient for the sensor chain to settle to its final value. Further, the use of buffers minimized charge leakage - the capacitors lost less than 1% of their charge in 2 μ s (Figure 4.3).

Figure 4.3 Charge leakage is negligible due to the presence of buffers

The sensor chain delivered a gain of 9.4 at room temperature and nominal process parameters¹⁸. Figure 4.4 illustrates the excellent linearity achieved by the sensor chain.

Figure 4.4 Transfer characteristic of the sensor chain. It exhibited excellent linearity.

¹⁸ The required voltage gain was 8.5, and it was ensured that this number was achievable even at the weakest corner.

4.2 THE SELF-CORRECTION PROCESS

The self-correction methodology is verified by simulating two potential scenarios:

- Either due to package parasitic tolerances, or due to the usage of a different package for a RF chip, the package lead inductance can vary over 1 nH. In this section, we simulate the self-correction process by the addition of 1nH inductance at the input pad of the LNA.
- Either due to a process fault, or mere process variations, the gate-source capacitance of the input transistor can vary by 10%-15%. We demonstrate the self-correction process by deliberately reducing the capacitance by 15%, and letting the process circuitry correct the input match.

4.2.1 Addition of parasitic inductance

Figure 4.5 illustrates the self-calibration process for the first case. Table 4.2 lists the values of the various signals through the entire procedure. ‘*Discharge*’ goes high periodically, after each cycle and at the beginning of the process, to reset the capacitor charges to zero; this pulse also latches the ‘*continue*’ signal to the digital circuitry. In other words, there is a possibility that the ‘*continue*’ signal may rapidly switch states during a self-correction cycle¹⁹. To avoid this occurrence, the ‘*continue*’ signal is propagated to the digital circuitry only when ‘*discharge*’ goes high *i.e.*, at the end of each cycle.

¹⁹ When the storage capacitors are charging/discharging, the comparator outputs may switch states. This fluctuation is transitory – it is not valid. Consequently, it *must* not be acted upon by the decision-making circuitry.

Figure 4.5 Output voltages of various stages over entire correction process. The entire process halts at the end of three cycles when 'continue' goes low - (a) Voltage across sense resistor at source of LNA. A gap of $3\ \mu\text{s}$ is provided after each cycle to allow the analog processing circuitry to settle to its final value. (b)(c)(d) & (e) Capacitors discharge to 0 V after every cycle when discharge pulse goes high. (f) & (g) V_{T1} and V_{T2} are the differences between voltages across C_1 - C_1 and C_3 - C_4 respectively. (h) 'Discharge' also acts as clock for latch L_1 . (i) 'Continue' goes low after 3 cycles indicating that the closest input match is between Tap3 and Tap4.

The digital circuits are reset and ‘*continue*’ is gated high at the beginning of the process. Figure 4.5(a) shows the output voltage of the sense resistor. During the first cycle, tap1 is turned on and the P.D. charges C_1 and C_2 with 1343 mV and 1098 mV, corresponding to tone1 and tone2 respectively. Tap2 is then turned on and the corresponding voltages are stored in capacitors C_3 and C_4 . Subtractor output V_{T1} is the difference between C_1 and C_2 (with a gain of 3), and this is compared with 600mV (for this LNA, an ideal match of 1.9 GHz corresponds to a V_{IDEAL} of 600 mV) by comparator C_{P1} . Similarly, C_{P2} compares the corresponding voltages for tap2. As Table 4.2 indicates, both C_{P1} and C_{P2} outputs remain high, thus keeping the ‘*continue*’ signal high through the next cycle. Similarly, C_{P1} and C_{P2} outputs remain high for cycle two, and the process continues into the third cycle. At the end of this cycle, output of C_{P2} goes low (tap4, since V_{T2} drops below 600 mV), and this turns ‘*continue*’ low (as mentioned in earlier sections, the response is monotonic: the ideal tap is reached only when one subtractor output falls below 600 mV). The sequential cycling process now stops. Two additional subtractors determine which of the two taps (tap3 and tap4) lie closer to the desired input match frequency (they choose the tap whose subtractor output is closest to 600mV). This tap is now turned on, and the self-calibration process is complete.

The time taken per tap was 1.75 μ s, time per cycle (two taps, settling time and discharge time) was 6.2 μ s, and time for the entire calibration process was 18.7 μ s²⁰. In the worst-case scenario where all five cycles are required for calibration, the time

²⁰ For these simulations, a clock faster than 2 MHz was used to demonstrate the speed of the methodology. Using a 2 MHz clock will slow down the process, but it still remains less than 100 μ s, and compares very favorably with the milli-second range required in current testing schemes.

required is 21.75 μ s. It is seen that even if the number of taps are increased to 20, the calibration time will not exceed 250 μ s.

Cycle 1				
	Tap1, Tone1	Tap1, Tone2	Tap2, Tone1	Tap2, Tone2
P.D (mV)	1343.15	1098.22	1335.32	1105.63
Subtractor	729.93 mV (V_{T1})		684.561 mV (V_{T2})	
Comparator	HIGH		HIGH	
Continue	HIGH			
Cycle 2				
	Tap2, Tone1	Tap2, Tone2	Tap3, Tone1	Tap3, Tone2
P.D (mV)	1335.34	1105.58	1328.24	1113.68
Subtractor	684.762 mV (V_{T1})		640.013 mV (V_{T2})	
Comparator	HIGH		HIGH	
Continue	HIGH			
Cycle 3				
	Tap3, Tone1	Tap3, Tone2	Tap4, Tone1	Tap4, Tone2
P.D (mV)	1328.38	1113.8	1321.62	1127.65
Subtractor	640.06 mV (V_{T1})		579.4 mV (V_{T2})	
Comparator	HIGH		LOW	
Continue	LOW			

Table 4.2 Voltages of various stages for each calibration cycle. $V_{IDEAL} = 600$ mV.

Figure 4.6 S_{11} curves before and after correction. The correction re-aligns input match from 1.82 GHz to 1.894 GHz.

Figure 4.6 shows the input match conditions at all three stages:

- The designed and desired input match frequency is 1.9 GHz.
- The addition of 1 nH inductance moves the S_{11} frequency to 1.82 GHz
- The self-correction circuitry re-aligns the frequency to 1.894 GHz.

4.2.2 Reduction of C_{GS}

Figure 4.7 illustrates the waveforms for the case where the gate-source capacitance is reduced by 15%. The waveform behavior follows the same pattern as in the previous section. Since in this case the reduction of C_{GS} shifted S_{11} to a higher frequency, the ideal tap lies between tap2 and tap3, ('Continue' goes low after the end of the second cycle, signaling the end of the correction process) and the correction process was completed in 12.2 μ s. Figure 4.8 depicts the S_{11} curves. The input match frequency changes to 2.04 GHz from 1.9 GHz due to the reduction in gate-source capacitance. At the end of the self-correction process, it is re-aligned at 1.92 GHz.

These two scenarios discussed above (the current section and the previous section) move the S_{11} frequency in opposite directions, and the results conclusively prove that the correction process can successfully handle both situations.

Figure 4.7 Output voltages of various stages when C_{GS} is reduced by 15%. The pattern is similar to that of Figure 4.5. In this case, the process took only 12.2 μ s since the ideal tap was between tap 2 and tap 3.

Figure 4.8 S_{11} before and after correction when C_{GS} of the input transistor is reduced by 15%.

4.3 ROBUSTNESS

The circuit was simulated for process variations using Monte-Carlo and Corners (3-sigma variation of process parameters) analysis. For this work, the two extreme temperature values were chosen to be 10°C and 50°C and power supply variation was assumed to be 8%. These numbers are reasonable: this is an experimental chip, and will not be subject to external weather conditions. Further, since the chip will be probed directly (without any packaging), the power supply voltage will not be subject to much variation.

The gain of the sense amplifier varied between 12.3 and 8.6 (at 1.9 GHz) over the weakest and strongest corners, but due to the two tonal approach, this variation will not

affect the outcome as long as sufficient gain is ensured at the weakest corner and headroom is ensured at the strongest corner.

Figure 4.9 Spectral Response of Sensor Chain over process, temperature and power supply corners. Strongest corner is simulated at temp=10 C and Vdd+4%. Weakest corner is simulated at temp=50 C and Vdd-4%.

Figure 4.9 shows the spectral response of the sensor chain for both the weakest (weak process, 50°C, 2.46 V power supply) and strongest corners (strong process, 10°C, 2.54 V power supply). The curves remain linear and monotonic.

Figure 4.10 plots the gain of the sensor chain at both the corners – it remains linear and stable.

(a) Strongest corner

(b) Weakest corner

Figure 4.10 Transfer function Sensor Chain over process, temperature and power supply corners. Strongest corner is simulated at temp=10 C and Vdd+4%. Weakest corner is simulated at temp=50 C and Vdd-4%.

The entire self-correction circuitry presented in Chapter 3 was re-simulated at the weakest corner. Contrasting the results to Table 4.2²¹, which indicates the results for nominal process and ideal temperature and power supply values, it was observed that

²¹ The absolute values for the corners have not been included, for they have nothing new to convey.

although the absolute values have changed, the output of the comparators still continue to remain high until the end of the third cycle, demonstrating the robustness of this process. As shown in Figure 4.11, self-correction was successful even at the weakest corner, confirming the robustness of the methodology used in this work.

Figure 4.11 S_{11} curves before and after correction for the weakest corner. Nominal S_{11} at this corner was 1.844 GHz, addition of a parasitic inductance shifted it to 1.738 GHz, and after calibration the input match aligned itself at 1.839 GHz.

4.4 LAYOUT

Figure 4.12 depicts the entire layout, and the sub-sections have been highlighted. The power and ground buses, as highlighted in Figure 4.12, are at least 60 μm wide (they are 100 μm wide in some segments) – this is necessary to ensure that they do not generate any significant inductance. This factor is crucial since these buses run across the width and breadth of the layout, and the turns might create inductance loops if they are not wide enough. Further, the power and ground buses are laid right on top of each other, on

Figure 4.12 Layout²² of complete circuitry

²² The layout depicted is before dummy metal patterns were placed to fulfill local and global metal density requirements

consecutive metal layers, such that they generate additional power-ground bypass capacitance. All power and ground connections are made to these buses, and these buses in turn connect to the central ground-return bypass capacitor. All metal connections have been made adequately wide to ensure that they can safely carry the DC and AC current through them.

There exists six power and six ground pads, laid out in an alternating fashion to suit the power probes²³. The input and output pads to the LNA are Ground-Signal-Ground (G-S-G) pads, to suit the G-S-G probes to be used to test the chip. All pads are 100 μm X 100 μm in size, with a pitch of 150 μm for the input/output pads and a pitch of 125 μm for the power pads.

All high frequency circuits have a ground-return bypass capacitor connected from V_{DD} to ground. The metal traces connecting each inductor have been modeled in ASITIC, and their effect has been accounted for in the design process. Finally, all pads have been protected by double-diode Electro-Static Discharge (ESD) structures and RC power clamps.

²³ The particular power probe to be used for testing this chip has a similar structure.

Chapter 5. CONCLUSIONS

5.1 Summary
5.2 Future work

The continuing trend towards higher levels of on-chip integration will render external probing mechanisms more and more difficult. Further, the constant and relentless drive towards smaller transistors, especially in the sub 90 nm regime, has given rise to complex behavioral, modeling and fabrication problems, and inevitably, it has brought with it serious questions and concerns about yield and reliability. With the direction that the CMOS industry is evolving towards, what is really needed is not just on-chip testing systems, but on-chip, non-intrusive methods of detecting *and* correcting, if possible, process faults.

RF chips are subject to heavy influence from package parasitics – inductances and capacitances that can be comfortably ignored in the MHz domain are dominant in the GHz area. This issue, in recent years, has resulted in the chip-package co-design paradigm, where the chip is essentially designed accounting for the parasitics involved in its intended package. We run into problems here due to large tolerances in the package parasitics, which makes it difficult to predict their accurate values. Further, a change in package will mean a complete re-design of the front-end.

The work presented in this thesis demonstrates successfully an extremely robust, low-overhead methodology and circuitry that is the first step towards self-corrective,

package-independent RF circuits. To the author's knowledge, it is the first-ever attempt made towards this objective.

5.1 SUMMARY

Traditional feedback and Automatic Gain Control (AGC) approaches pose significant problems²⁴ with RF circuits. The 'locked-loop' technique presented in Chapter 2 side-steps these issues, yet provides a mechanism for dynamic modification of design parameters. Further, a very important concern with any such test-and-correct circuitry is the robustness of the processing circuitry itself: errors in the processing circuitry can easily be mistakenly attributed to the circuit under consideration. The two-tonal approach described in Chapter 2 is highly resilient, as demonstrated in Chapter 4. These two architectural creations form the cornerstone of this work – they eliminate the roadblocks that have prevented such an idea from being successful thus far. The self-correction signal fed to the LNA is a digital word. This not only renders noise issues inconsequential, but also ensures an accurate, error-free mechanism.

LNAs are ideal circuits to evaluate this methodology since they are generally the first and most influential circuit in the front-end transceiver chain – they form the interface between the IC and the package, and their performance directly depends on package parasitics. Due to its popularity and ease of implementation, this work has utilized the single-ended Cascode narrow-band topology to demonstrate the proof-of-concept. The small-valued sensing resistor provides a minimally intrusive sensing mechanism, and a tapped gate coil is used to vary the input match. The gate coil, along

²⁴ Intrusion and stability are the two main concerns.

with the NMOS switches and interconnects was carefully simulated in ASITIC to accurately model the inductance and its associated parasitics. Further, the size of the switches presents a trade-off between on-resistance and capacitance to substrate.

The sense amplifier and peak detector were straightforward implementations of cascaded common-source amplifiers and a half-wave doubler. No feedback was required due to the inherent nature of the two-tonal approach. The digital and clocking circuitry was comprised of basic decode logic designed from the standard cell library. The only major design decision was to use a 5-bit (by re-using it after every cycle) and a 2-bit counter instead of using an 8-bit counter.

Chapter 4 has presented extensive simulation results. All components used the design were non-ideal models that included all associated parasitics. We have shown the results for two potential anomalies: a parasitic inductance on the input pad of the LNA and a decrease in gate-source capacitance due to process variations. Further, the robustness of the methodology has been conclusively demonstrated by simulating the circuitry across strong and weak corners (including temperature and power supply variations) – the input match is corrected dynamically in every case.

This work enjoys the advantages of low-overhead circuitry, minimal intrusion, low power consumption (the circuitry can be switched off after the self-correction process), no requirements of DSP cores, processors or A-D converters, baseband/DC signal processing, test signals of moderate precision and possesses very fast correction times – in the order of tens of μs . It compares very favorably with existing techniques, which perform RF test with test times in the order of hundreds of milliseconds. By

adapting a single design to various packaging scenarios and variations, it cuts down on design cycle times, and is a significant step towards first-time silicon success.

5.1 FUTURE WORK

This section outlines the shortcomings of this work, and presents potential directions for future work. As already mentioned, this is merely the first step on the long road towards achieving self-corrective, package independent RF CMOS circuitry.

- **S_{11} magnitude correction:** The tapped gate-coil used in this work allows for dynamic modification in the input match frequency. However, some process faults or packaging effects may affect the magnitude of S_{11} , degrading it beyond acceptable levels. The use of a third-tone at the exact input-match frequency (1.9 GHz in this work) can quantify S_{11} magnitude at that frequency. Further work is also required to identify the design parameter that will be modified to improve this magnitude: an obvious choice would be a tapped source-coil.
- **Tapped coil:** The tapped coil does contribute additional parasitics, in the form of the on-resistance and capacitance of the NMOS switches. Although these effects can be co-designed for during the design cycle, further research in this area might result in better mechanisms.
- **Timing:** This work utilizes the output states of a counter and decodes them to generate all the timing pulses. Since the speed of the clock used was 2 MHz, the minimum resolution of time was 500 ns, and hence all timing pulses/delays were

in multiples of 500 ns. Other approaches can possibly offer better resolution, which will translate to faster self-correction times.

- **Intrusion:** The sense resistor of 7 ohms is not totally non-intrusive, although it has been shown [11] that the degradation of the LNA's performance is acceptable when the LNA is co-designed with the resistor. An obvious step forward is to reduce the value of this resistor. This requires an increase in amplification (from the current value of 8.5) of the sense amplifier, which can be achieved by cascading more stages, or using a different topology. In the limit, there exists the possibility of making the jump from minimal intrusion to non-intrusion. In other words, to eliminate the resistor and use the source coil as the sensing element. Initial work in this direction has shown that it is indeed possible, although it does require a re-work of the architecture.
- **Slope Corrected amplifier:** This work requires an external, accurate reference voltage (V_{IDEAL} , Section 4.2.1). This voltage is the expected output of the sense amplifier if S_{11} frequency is ideal. During self-correction, the output of the sense amplifier is compared to V_{IDEAL} , and its relative value is indicative of the actual S_{11} frequency: based on this value, steps are taken to correct the match. By carefully re-designing the sensor chain such that its frequency response will have a slope of our choice (slope-correction), we can ensure that V_{IDEAL} is 0 V. Obviously, this requires a more sophisticated sensor chain, but will remove the need for the external reference altogether: The sensor chain's output can be compared with 'Ground'.

- **LNA Topology:** This work uses the single-ended Cascode LNA to verify the proof-of-concept of self-correction. It can be implemented for other LNA topologies as well, for example, the differential balanced topology. One or more of the following circuitry may differ: the sensing mechanism, the algorithm, the sense amplifier, the peak detector, timing, clocking, but the architecture and the concept remain the same.
- **The RF Front end:** A logical extension is to extend this work for all circuitry in a typical RF front end, which is necessary for the vision of self-corrective and package-independent RF front ends. Further, the self-correction circuitry in each of the RF circuits can complement each other: the sensing mechanism in the mixer can isolate faults that have occurred on the output-side of the LNA, while the sensing mechanism in the LNA can concentrate only on faults that have occurred on the input-side.
- **Comprehensive fault correction:** This work has addressed the issue of S_{11} frequency correction. There exists the vast area that covers identification and correction of other types of faults. Further exploration is required to:
 - To identify the possible faults that might occur in RF circuits.
 - To recognize the manner in which all of these faults affect the performance of the specific circuit.
 - To design an algorithm that quantifies, with high accuracy, all these faults.
 - To clearly classify the faults into two categories: ones that can be dynamically corrected, and ones that are not correctable.

- To build circuits than can correct for any of the faults that fall in the first category.
- **Other processes:** The circuitry described in this thesis was designed in the IBM 6RF 0.25 μm CMOS process. *SiGe* is popular alternative for high speed RF design; the same architecture can be used to develop similar mechanisms. Since the process utilizes Bipolar transistors, the design process will be considerably different.

The chip is currently being fabricated at the IBM foundry, and will be characterized in the near future.

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