Design and Simulation of Dual channel MOSFET’s

A performance evaluation for Strained Si/Strained SiGe channel

Master’s Thesis Defense
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Key Messages

- Process induced strain is the most significant innovation in submicron MOS transistor technology, but scalability is a major bottleneck in driving performance for sub 65 nm technologies.

- Compound semiconductor material such as SiGe a promising solution for foreseeable future of MOS transistor technology.

- Dual channel CMOS transistor technology with a biaxial tensile strained Si and biaxial compressive strained SiGe channel is a promising solution to sustain the scaling challenges.

- Challenges with SiGe devices: leakage issues, surface roughness and cross hatching, higher cost and process complexity with substrate development.
Outline

• Introduction
  • Background
  • Motivation
  • Objective

• Physical Theory
  • Basic Mechanical Stress
  • Physics behind Biaxial and Uniaxial Strain.

• SiGe as a Channel Material
  • Dual channel MOS Architecture
  • Design specifications.

• Modeling and Simulation.
  • Process Simulation.
  • Device Simulation.

• Electrical Results

• Conclusion and Future Work
Objective

- To design, optimize and evaluate the performance of strain Si/Strain SiGe dual channel heterostructure MOS transistor for sub 65 nm technology.

- Formulation of unified modeling scheme based on different physics-based model in order to design, simulate and predict device behavior.
Scaling Trends and Challenges

- Scaling enables more transistor and increased performance.
- Challenges with Scaling
  - SCE becomes more and more dominant coupled with increase scattering, and leakage.
  - Approaching fundamental, scientific and engineering limits with conventional CMOS
Strain as a Solution

- Strain in Si as a performance booster.
- High electron and hole mobility, more performance per watt.
- Next generation strain: SMT, SPT, strain with hybrid orientation technique, SSOI, e-SiC

Ref: Jan et al. IEDM Tech, Oct 2005, Courtesy (Intel Corp)
Performance Vs Scalability of Strain Silicon

- Density hurts strain, resulting in low and saturated performance.
- Source/Drain proximity issues, higher defect densities, process integration challenges and higher manufacturing cost with scaling.

Courtesy: Semiconductor International : Ref Aaron Thean Freescale, Strain Si Update, March 07
Innovation Enable Technology Pipeline as a solution to Scaling

- New channel material such as SiGe and heterostructure devices as potential candidate for sub-65 nm technology.
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Mechanics of Strain

Material A (tens/comp) (eg. Nitride)

Material B (eg. Si)

Due to material mismatch of A & B, arising from material composition, lattice size, different thermal expansion rate. A will introduce mechanical stress on B

Strain in Silicon

\[
\text{Strain } (\varepsilon) = \frac{a_{\text{silicon}^*} - a_{\text{silicon}}}{a_{\text{silicon}}}
\]

- If \(a_{\text{silicon}^*} > a_{\text{silicon}}\), Tensile Strain.
- If \(a_{\text{silicon}^*} < a_{\text{silicon}}\), Compressive Strain

Ref: Victor Chan IBM SRDC, Hope well Junction, Jan 2007
Stress Induction

![Graph and diagram showing stress induction and strain]

- **Substrate Induced Strain – strain in x-y plane.**
  - Biaxial Tensile Stress – Tensile component in x-y plane and compressive stress in z plane
  - Biaxial Compressive Stress – Compressive Stress in x-y plane and tensile stress in z plane.

- **Uniaxial Process Induced Strain – Strain in x plane.**
  - Common stress configuration – e-SiGe, Stress Liners and SMT

- $a_{\text{SiGe}(y)} < a_{\text{Si/Ge}(x)}$

- Biaxial Compressive Stress

- $a_{\text{SiGe}(<)} < a_{\text{SiGe}(>)}$

- Biaxial Tensile Stress

\[
a_{\text{silicon}} < a_{\text{SiGe}}
\]

Biaxial Tensile Stress
Strain splits the conduction valley into four in-plane conduction $\Delta_4$ valleys and two out-of-plane conduction $\Delta_2$ valleys (lower energy).

- Preferential population of electron in $\Delta_2$ valleys. Lower effective mass, high mobility

$\mu = e\tau/m^*$
Hole Mobility

- Strain causes mixing of bands thus making HH and LH degenerate.
- Degeneracy cause band wrapping and repopulation of holes in top-most layer, thus increasing hole mobility.
- $\mu_H$ unstrained $< \mu_H$ biaxial tensile $< \mu_H$ uniaxial compressive $< \mu_H$ biaxial compressive
## Strain Comparison

<table>
<thead>
<tr>
<th>Strain</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Scalability and Performance</th>
</tr>
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<tbody>
<tr>
<td>Biaxial Tensile</td>
<td>🌻</td>
<td>🙃</td>
<td>Scalable, high performance for NMOS High process cost, process challenges – defect free epi layers</td>
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Dual channel MOS comprises of tensile strained Si/compressively strained SiGe *pseudomorphically* grown on virtual substrate.

- For PMOS, both Si and SiGe (strained) acts as channel layers.
- For NMOS, channel remains confined to Strain Silicon layer.
Critical Thickness & Strain Relaxation

Strain Relaxation and critical thickness based on Matthew & Blakslee\(^1\)

\[
h_c = \frac{b(1 - \nu \cos^2 \alpha)}{8\pi(1 + \nu)f \cos \theta \left[1 + \ln \left( \frac{h_c}{b} \right) \right]}
\]

Critical thickness as variance of Ge mole fraction for growth at 550°C \(^2\)

- Critical Thickness defined as minimum value of the film thickness, above which the strain in the film relaxes due to misfit dislocation, elastic and plastic deformation and half loop nucleation.
- Approaches to reduce defect:
  - LPCVD
  - Graded Buffer
  - Wafer Bonding

\(^1\)Yasuhiro Shiraki et al., Surface Science Report, 2006
**CMOS Integration of DCH MOS**

- Different strained silicon cap layer for NMOS and PMOS.
- Size of NMOS strain Si cap layer $\geq 5$ nm.
- Size of PMOS strain Si cap layer $< 3$ nm.
- The virtual substrate thickness is optimized to 90 nm (20 nm + 70 nm).
Device Theory – Band Diagram, NMOS

Comparison of single channel (left) and double channel (right) band structure under positive bias.

- The band offset between strained Si and compressive strained SiGe leads to a sufficient discontinuity in conduction band.
- Electrons remain confined to strained Si layer in $\Delta_2$ conduction valley.
At $V_g = V_{TSN}$

- The depletion regions is formed in strained Si cap layer.
- At $V_g = V_{TSN}$ the inversion occurs in strained Si Layer.
- Due to band alignment, inversion charge due to electron remains in strained Si, even at strong inversion).
Device Theory – Band Diagram PMOS

\[ \Delta E_V = 0.238x - 0.03x^2 \]

For \( x = 0.3 \), \( \Delta E_V = 0.0687 \)

\[ \Delta E_V \sim 0.74x \]

For \( x = 0.3 \), \( \Delta E_V = 0.222 \)

- Valence band offset of compressively stressed layer lower in energy than both underlying strained Si and relaxed SiGe.
- High valence band discontinuity for strained Si/strained SiGe compared to strained Si/SiGe.

Comparison of single channel (left) and double channel (right) band structure negative bias.
PMOS Operation

Conduction current density as a function of sheet hole concentration in PMOS

- Accumulation region \( (V_G \geq V_{FBS}) \).
- Depletion region \( (V_{THS} > |V_G| > V_{FBH}) \), the strained SiGe channel starts getting depleted first.
- Inversion \( (V_{THS} \geq V_G) \) layer is formed in strained SiGe; \( (V_{TS} \geq V_G) \) a small parasitic channel forms in strained Si cap layer.
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Modeling and Simulation Flowchart

Process Steps & Conditions
- Etch
- Implant
- Diffusion
- Epitaxy
- CVD

ATHENA
S-SUPREM 4

Doping Profile
Device Description

C - Functions
- Model SiGe
- conv SiGe

Bias Set up, I/P conditions

ATLAS
S-PICES (Si)
BLAZE (SiGe)

Process - Variability Analysis.
DC, AC and voltages for device structure
I-V log files, SPICE Parameters
AC Analysis, CV curves
Epitaxial deposition of all layer @ 500 C, *in-situ* doped.
- Low temperature growth → low surface roughness, better film conformality.
- Graded SiGe (step growth of 0.1).
- Relaxed SiGe, 15% Ge.
- Strained SiGe, 30% Ge, compressive stress.
Substrate Doping Profile

PMOS Substrate

- Germanium out diffusion at Si/SiGe interface.

NMOS Substrate
Process Flow

Nitride Deposition and Oxide Growth. Controlled removal of Si from PMOS

STI Development, 0.312 μ Trench

Deposit Sacrificial Oxide. PMOS and NMOS VT adjustment

1.7 nm LPCVD, Oxynitride Deposition

1300 Å of Polysilicon deposition

Gate stack Pattern, define CD ~ 65 nm

LPCVD Spacer I (Oxide),

S/D Implant I.

Pattern Spacer I Gate Oxide

LPCVD Nitride (SPACER II)

S/D Implant II.

Spacer II Pattern

RTA, 900 C, 15 sec

Silicidation 450 C @ 10 Sec
Thermal Effects on Dopant Diffusion

- Phosphorous tends to diffuse more in SiGe as compared to As.
- Compared to As, P shows more sensitivity to anneal time and temperature.
- High anneal time/temperature and low anneal temperature/high anneal time are worst cases and shows degraded device performance.
# Device Modeling

## ATLAS

<table>
<thead>
<tr>
<th>S-PICES (Si)</th>
<th>ATLAS</th>
<th>BLAZE (Si/SiGe)</th>
</tr>
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<tbody>
<tr>
<td>Energy Balance Transport Model</td>
<td>Drift –Diffusion, Boltzmann transport, velocity overshoot and velocity saturation</td>
<td></td>
</tr>
<tr>
<td>Band Gap Narrowing Model</td>
<td>Band Gap Narrowing due to SiGe and Si, Density of states and effective mass.</td>
<td></td>
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<tr>
<td>Carrier –Carrier Scattering Model</td>
<td>Carrier Scattering, lattice scattering, dopant fluctuation, ionized impurity scattering</td>
<td></td>
</tr>
<tr>
<td>Conc. SRH Model</td>
<td>Phonon transition, auger transition, surface recombination, impact ionization and tunneling</td>
<td></td>
</tr>
<tr>
<td>Density Gradient Quantum Model</td>
<td>Quantum correction to carrier temperature, conduction and potential profile based on Wigner function and Schrodinger-Poisson Equation</td>
<td></td>
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<tr>
<td>Field Based Mobility</td>
<td>Field Based Mobility dependence, velocity saturation.</td>
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Drain Current Model

Ref B. Bindu et al. IEEE TED, 06, 2006

**PMOS**

\[
I_{D_{\text{sub}}}^H = \frac{-W \mu_p^{\text{SiGe}} V_t^2 C_D}{\alpha_p V_D} \left[ \exp \left( \frac{|V_G - V_{\text{THP}}|}{m_p V_t} \right) \right] \left[ 1 - \exp \left( \frac{|V_D|}{V_t} \right) \right] |V_G| \leq |V_{\text{THP}}| \\
I_D = \left\{ \begin{array}{ll}
I_{D_{\text{sat}}}^H \{1 + V_D - V_{\text{THP}}^H \} & |V_{\text{THP}}| \geq |V_G| \leq |V_{\text{THP}}| \\
I_{D_{\text{sub}}}^H + I_{D_{\text{sat}}}^H \{1 + \lambda_p |V_D - V_{\text{THP}}^s| \} & |V_G| \geq |V_{\text{THP}}| 
\end{array} \right.
\]

**NMOS**

\[
I_{D_{\text{sub}}}^l = \frac{-W \mu_n^{\text{Si}} V_t^2 C_n}{\alpha_n V_D} \left[ \exp \left( \frac{|V_G - V_{\text{Thn}}|}{m_n V_t} \right) \right] \left[ 1 - \exp \left( \frac{|V_D|}{V_t} \right) \right] |V_G| \leq |V_{\text{Thn}}| \\
I_D = \left\{ \begin{array}{ll}
I_{D_{\text{lin}}}^l \frac{V_D}{2V_{\text{Thn}}} \left[ 1 + \theta_n^s (V_G - V_{\text{Thn}}) \right] & |V_D| \leq |V_{\text{Dain}}^s| \\
I_{D_{\text{lin}}}^l + I_{D_{\text{sat}}}^l \{1 + \lambda_p |V_D - V_{\text{Dain}}^s| \} & |V_D| \geq |V_{\text{Dain}}^s| 
\end{array} \right.
\]
$I_D-V_{DS}$ Curves

- High drive current for NMOS and PMOS
- NMOS - 0.94 mA/µm and PMOS - 0.45 mA/µm at $V_{GS} = 1.2$ V.
$I_D - V_{DS}$ Comparison with Intel’s 65 nm ULP MOS

- Well matched I-V curves
- Simulated results show improved performance of $\sim 16\%$ at $V_{GS} = 1\, V$

Compared with Jan et al., *IEDM*, 08, 2005

Intel Work ($L_g = 54\, \text{nm}, T_{ox} = 1.7\, \text{nm}$)

This work ($L_g = 55\, \text{nm}, T_{ox} = 1.7\, \text{nm}$)
$I_D-V_{DS}$ DCH Vs. Biaxial Tensile MOS

**SPECS** | **This Work** | **Comparison Work**
---|---|---
$T_{ox}$ | 1.7 nm | 1.3 nm
$L_{eff}$ | 55 nm | 50 nm
**Technology** | Biaxial Tensile & Compressive | Biaxial Tensile


- Improved PMOS and NMOS drive currents by ~ 20%.
- At higher $V_g$ the PMOS drive current is comparable to comparison work.
Threshold Voltage

Threshold voltage of 0.22 and -0.22 for NMOS and PMOS at Vds = 0.1 V.

Dual channel exhibits lower threshold value than single channel device.
Subthreshold & DIBL

PMOS

- Subthreshold swing of 88 mV/decade and 78 mV/decade for PMOS and NMOS.

- DIBL of 26mV/V and 12 mV/V for PMOS and NMOS.
Leakage

- Off state leakage current of ~ 10 nA/μm and 80 nA/μm for NMOS and PMOS ( @ |V_{DS}| = 1V).
- Ion/Ioff exceeds 10 orders of magnitude.
PMOS Leakage Vs Gate Length

- Off-state leakage increases with decrease in gate length.
- Performance degrades almost by 100 x.
Mobility in Strained Si/Strained SiGe Channel

- PMOS mobility improves by 12% over uniaxial stressed e-SiGe PMOS.
- Peak NMOS mobility of 278 cm²/V.s, no available published data for NMOS mobility at 65 nm.
Overlap Capacitance

\[ C_{GS} = C_{gsd} + C_f \]

- Overlap capacitance of 9.73E-09 and 1.63E-09 F/m² for NMOS and PMOS, respectively.
Capacitance Model

\[ C_A = \frac{dQ_s}{d\psi_s} = C_{LD} \left[ 1 + \frac{\psi_s}{2\nu_t} \right] \]
\[ C_{LD} = \varepsilon / \sqrt{\varepsilon \nu_t / qN_D / A} \]
\[ C_g = C_{ox} \text{ in series with } C_A \]

\[ V_{THS} < V_G < V_{FBS} \text{ Depletion} \]
\[ C_D = \frac{1}{C_{ox}} \left[ \sqrt{1 + \frac{2C_{ox}^2(V_G - V_{FBS})}{q\varepsilon_{sl}N_a / d}} - 1 \right] \]
\[ C_g = C_D \text{ series with } C_{ox} \]

For highly doped case, \( C_g = C_{LD} \text{ in series with } C_{ox} \)

\[ V_G > V_{TH} \text{ Inversion} \]
\[ C_{TH} = -q(d\rho^H_s / d\psi_s) \]
\[ C_g = C_{ox} \text{ in series } C_{TH} \]

\[ V_{TS} \geq V_G \text{ Strong Inversion} \]
\[ C_{TS} = -q(d\rho^S_s / d\psi_s) = -q(d\rho^S_s / dV_G)(dV_G / d\psi_s) \]
\[ C_g = C_{ox} \]
Total Gate Capacitance

PMOS Total Gate Cap

NMOS Total Gate Cap

\[ C_G = \frac{1}{C_{ox}} + \frac{1}{C_D + C_I} \]
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Challenges

- Surface roughness and cross hatching.
- Germanium out diffusion and strain relaxation.
- High Leakage
- Process challenges in CMOS integration and high cost

Cross hatching in Strained Si/SiGe wafer
Ref S. H. Olsen et al., IEEE TED, 2003

Surface Roughness in Strained Si/SiGe wafer
Ref S. H. Olsen et al., IEEE TED, 2003
Future Work

- **Modeling**
  - Models for effectively calculating strain in layers.
  - Strain dependence of mobility and effective density of state calculation.
  - More robust diffusion profiles and models for SiGe.
  - Compact Models development for Strained Si technology.

- **Device Optimization**
  - Using Strained SiGe without Si cap for PMOS, for improved device behavior.
  - High -k dielectric for integrating gate dielectric with SiGe layer.
  - Metal Gate Integration.
  - Developing a low cost process method with lower defect and dislocations by optimizing LPCVD method.
Key Messages

- Process induced strain is the most significant innovation in submicron MOS transistor technology, but scalability a major bottleneck in driving performance for sub 65 nm technologies.

- Compound semiconductor material such as SiGe, III-V’s, a promising solution for foreseeable future of MOS transistor technology.

- Dual channel CMOS transistor technology with biaxial tensile strained Si and biaxial compressive strained SiGe channel a promising solution to sustain scaling challenges

- Higher drive currents and comparable performance with process induced strain.

- Challenges with SiGe channel: leakage issues, surface roughness and cross hatching, higher cost and process complexity with substrate development
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RIT Library

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QUESTIONS
BACKUP SLIDES
Substrate Induced: Biaxial Tensile Strain

- Pseudomorphic growth of epi layer either by MBE or LPCVD.
- Silicon under Biaxial tensile stress ($a_{\text{silicon}} < a_{\text{SiGe}} (x)$).
- Stress induction in $xy$ plane.

Ref: Victor Chan IBM SRDC, Hope well Junction, Jan 2007
- $Si_{1-y}Ge_y$ film deposited over $Si_{1-x}Ge_x$ ( $y > x$)
- $Si_{1-y}Ge_y$ film under biaxial longitudinal and transverse compressive stress, with an out of plane tensile component.
Process Induced stress: Uniaxial Strain

- Process induced strain, strain in x (110) direction.
- Common stress techniques, plasma enhanced nitride layer deposition, stress memorization technique, and e-SiGe in S/D region.
- Present in current 90 nm and 65 nm technology.
MISFIT DISLOCATION

- Above critical thickness, film relaxes due to
  - elastic deformation,
  - plastic deformation
  - Dislocation or half loop nucleation
- Approaches to reduce defect
  - LPCVD or Epitaxy between 500 ~ 800 C followed by CMP.
  - Graded Buffer
  - SiGe Free Strained Si/ SOI integration

Ref: Matthew Erdmann, 204th Meeting ECS, October 2003. (courtesy: Amber wave)
RSCE in N-MOS

- NMOS devices show reverse short channel effect, initial increase in threshold voltage with increase in VDS.
- Boron pile up due to transient enhanced diffusion seems to be the cause.
Doping Profile after Silicidation

- Junction Depth calculated from SIMS profile $\sim 78$ nm for PMOS and 35 nm.
- S/D doping of order $\sim 1E21$ cm$^{-3}$. 