Switched-Capacitor Voltage Doubler Design Using 0.5 μm Technology

Hanfeng Wang
Switched-Capacitor Voltage Doubler Design Using 0.5 µm Technology

by

Hanfeng Wang

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering

Approved by:

_________________________________________________
Advisor: Dr. Robert J. Bowman

_________________________________________________
Member: Dr. Daniel B. Phillips

_________________________________________________
Member: Dr. James E. Moon

_________________________________________________
Department Head: Dr. Sohail A. Dianat

Department of Electrical and Microelectronic Engineering
Kate Gleason College of Engineering
Rochester Institute of Technology
Rochester, New York
January 2014
Abstract

Switched-Capacitor Voltage Doubler Design Using 0.5 μm Technology

by

Hanfeng Wang

Master of Science in Electrical Engineering

Rochester Institute of Technology, Rochester, New York

While integrated circuit (IC) power management has been an eternal topic for chip designers, inductor based DC-DC converters have been dominant in the field for years. However, because of the natures of inductors: large electro-magnetic interference, high coupling noise, and difficult silicon fabrication process, they are not favorable to on-chip solutions. Switched-capacitor (SC) DC-DC converters, which adopt capacitors for their energy storage components, have become increasingly popular among both the academia and the industry, because, apparently, they avoid the drawbacks of the inductor counterparts, and can be directly implemented on-chip without additional fabrication process.

In this paper, we will investigate one of the most famous SC voltage doubler topologies, which is known as “Favrat Cell”. By designing a chip, which converts 1.5 V voltage input to 2.5 V voltage output at 1 mA current load, we will walk through the details of a SC DC-DC converter design, including the switch cell, timing system, regulation loop and efficiency analysis. The design uses two 200 pF pumping capacitors and a 400 pF output capacitor in On-Semi half-micron technology. Four-way interleaved phase structure is adopted to reduce the output voltage
ripple. The gate-drive strategy of the switches has been improved to further reduce the reverse current injections during transitions. A new high-ratio voltage booster topology based on the cross-coupled topology has been introduced and will be discussed in comparison with the Dickson charge pump topology.
Contents

Abstract .............................................................................................................................................. i
Contents ........................................................................................................................................ iii
List of Figures ................................................................................................................................... v
List of Tables .................................................................................................................................... viii
Acknowledgments ........................................................................................................................ ix

Chapter 1 Introduction .................................................................................................................. 1
  1.1 Motivation ................................................................................................................................ 1
  1.2 History ..................................................................................................................................... 3
  1.3 This Work ............................................................................................................................... 8

Chapter 2 Switch Core Design ...................................................................................................... 10
  2.1 Original Topology .................................................................................................................... 10
  2.2 Switch Resistance Reduction ................................................................................................. 11
    2.2.1 Output Path Resistance Reduction .................................................................................... 12
    2.2.2 Charging Path Resistance Reduction ................................................................................. 22
  2.3 Bulk Current Prevention .......................................................................................................... 29
  2.4 Reverse Injection Prevention .................................................................................................... 31
    2.4.1 Ancillary Charging Paths Reverse Current Leakage ............................................................... 33
    2.4.2 Charging Paths of Ancillary Capacitors Reverse Current Leakage .................................... 36
    2.4.3 Output Switches Reverse Current Injection ....................................................................... 39
  2.5 Operational Analysis ............................................................................................................... 45
    2.5.1 Charging Behavior .............................................................................................................. 45
    2.5.2 Discharging Behavior .......................................................................................................... 47
List of Figures

Figure 1.1. (a) An inductor-based voltage converter and (b) physical implementation of an inductor ................................................................. 1
Figure 1.2. Topology of (a) a 2/1 step-up converter and (b) a 1/2 step-down converter .......... 2
Figure 1.3. 3/1 step-up ladder topology ............................................................................ 4
Figure 1.4. (a) Phase 1 and (b) phase 2 of the 3/1 step-up ladder topology ....................... 5
Figure 1.5. Dickson charge pump .................................................................................. 6
Figure 1.6. Cross-coupled topology ............................................................................. 7
Figure 2.1. Cross-coupled charge pump topology .......................................................... 10
Figure 2.2. Low-level to full-scale level shifter with inverting logic ............................... 13
Figure 2.3. Overdrive enhancement for PMOS switches ................................................ 15
Figure 2.4. Alternative wiring methods (a) and (b) for the level shifter ......................... 17
Figure 2.5. (a) non-inverting low-level to full-swing signal generator with (b) simulation result ..................................................................................................... 18
Figure 2.6 (a) Inverting and (c) non-inverting low-level to full-swing signal generator and (b) (d) their simulation results ........................................................................................................ 21
Figure 2.7. (a) Circuit without charging path resistance reduction and (b) simulation result .... 23
Figure 2.8. Solution to enhance the conductance of charging path .................................. 25
Figure 2.9. Possible topology for 4/1 charge pump .......................................................... 27
Figure 2.10. Intersection view of a PMOS switch showing the parasitic bipolar transistors ..... 29
Figure 2.11. PMOS body connection not preventing the body current ............................ 30
Figure 2.12. PMOS body connection preventing body current ........................................ 31
Figure 2.13. Presentation of reverse current existing in the topology ............................. 32
Figure 2.14. Logic components generating reverse injection 1 ...................................... 34
Figure 2.15. Correction made to prevent reverse injection 1 ........................................ 35
Figure 2.16. Logic components generating reverse injection 2 ...................................... 37
Figure 2.17. Correction made to prevent reverse injection 2 ........................................ 38
Figure 2.18. Logic components generating reverse injection 3 ...................................... 40
Figure 2.19. Attempt 1 to prevent reverse injection 3 .................................................... 42
Figure 2.20. Attempt 2 to prevent reverse injection 3 ................................................................. 44
Figure 2.21. Helper circuit to enhance the conductance of the charging paths ................................. 46
Figure 2.22. Zoom-in view of the output switch and capacitors ....................................................... 47
Figure 2.23. Plotted results at the output with the size of the PMOS switch changing as a parameter.................................................................................................................................. 49
Figure 2.24. Plotted current behaviors at the pumping capacitor and output capacitor with the size of the PMOS changing as a parameter .......................................................................................................................... 50
Figure 2.25. Initial pump-up voltage levels at both nodes with the size of PMOS changing as a parameter.................................................................................................................................. 51
Figure 2.26. Plotted results for different initial conditions............................................................... 52
Figure 2.27. Plotted result showing the output voltage level in a transient period ....................... 53
Figure 2.28. Analytical output levels with the size of the PMOS switch changing as a parameter .................................................................................................................................. 54
Figure 3.1. Clock system block diagram ......................................................................................... 56
Figure 3.2. Schematic of the voltage-controlled oscillator ............................................................... 57
Figure 3.3. Simulation result at the output of the VCO with and without output buffer .............. 58
Figure 3.4. Plotted current density flowing into the capacitor in one cycle ...................................... 60
Figure 3.5. (a) Topology and (b) signal sequence of a clock divider ............................................. 62
Figure 3.6. (a) Topology and (b) transient signals of a non-overlapping clock generator ....... 64
Figure 3.7. Alternative topology using NOR gates ........................................................................... 65
Figure 3.8. Topology of a four-stage tapered buffer ........................................................................ 66
Figure 4.1. Block diagram showing the feedback loop ................................................................. 67
Figure 4.2. Bandgap voltage reference topology ............................................................................. 69
Figure 4.3. Schematic of the proposed voltage reference ............................................................... 72
Figure 4.4. Schematic of the proposed OTA .................................................................................. 73
Figure 4.5. Schematic of the bias circuit for the OTA ................................................................. 74
Figure 5.1. Diagram showing the loss terms .................................................................................... 76
Figure 5.2. Capacitor charged by constant voltage source ............................................................. 78
Figure 6.1. Block diagram of the proposed design ......................................................................... 84
Figure 6.2. Simulated transient output voltage at 1 mA load ...................................................... 85
Figure 6.3. Transient output voltage with load changing from 500 µA to 1 mA at 2.5 µs .......... 85
Figure 6.4 Output voltage ripples with (a) 500 μA and (b) 1 mA load........................................... 86
Figure B.1. Schematic of the delay cell in the non-overlapping clock generator ...................... 114
Figure B.2. Sketch showing the transient nodal voltage levels in the delay cell......................... 115
List of Tables

Table 3.1 Truth table of node A-D with CLK ................................................................. 62
Table 6.1 Performance and parameter comparison......................................................... 87
Acknowledgments

I would like to acknowledge those who helped me or made a great impact on me during my Master’s education.

I would like to give thanks to my advisor, Dr. Robert Bowman, who welcomed me to the career as an analog IC designer and guided me technically. Sometimes being mean, though, he shaped my tough personality, both academically and mentally.

I would like to express my appreciation to Dr. Daniel Phillips, who helped me and had faith in me when I encountered obstacles. He also influenced me greatly with his rigor and integrity.

I would love to give my sincere worship to Dr. James Moon, who gave me my first English lecture that was fully understandable to me, who has always been patient with students and ready to help. He made me realize what kind of person I wish to be.

I would like to acknowledge my dear friends at RIT, Qinglong Li, Dongfang Xu and Wei Fan. They are the persons who back me up during my Master’s studies while my parents are far away. I would also like to thank my girl, Zejia Wei, whose understanding and generosity allowed me to concentrate on my studies.

Finally, I wish to thank RIT, who brought me here and gave me a colorful and unforgettable experience at such a white, quiet and lovely place, Rochester, New York.
In memory of my grandmother, Shenmin Guan
Chapter 1

Introduction

1.1 Motivation

Traditional DC-DC power converters adopt inductors for default energy storage components, which, however, exhibit two major drawbacks, namely, large electro-magnetic interference and coupling noise, and a difficult fabrication process. Figure 1.1 sketches the diagram of an inductor-based voltage converter and an inductor’s physical implantation in a normal process.

![Diagram of inductor-based voltage converter](image)

Figure 1.1. (a) An inductor-based voltage converter and (b) physical implementation of an inductor

$R_{out}$ represents the series loss of the converter.

$$V_{out} = \frac{n}{m} V_{in} - I_{load} R_{out} \quad (1.1)$$
During the last decade, switched-capacitor (SC) DC-DC converters, using capacitors for their energy storage components, drew more and more attention by scholars and the industry, because they perfectly solve the major drawbacks encountered by their inductor-based counterparts and provide even higher efficiency and power density.

Figure 1.2 shows conceptual architectures of a 1:2 step-up SC converter (a) and a 2:1 step-down SC converter (b).

In Figure 1.2, $\Phi 1$ and $\Phi 2$ are non-overlapping clock signals normally occupying half of the clock cycle. In both cases, during $\Phi 1$, $C_{fly}$ charges up to $V_{in}$, which makes it contain a total charge of $Q = C_{fly} \times V_{in}$. The charge stored in the flying capacitors remains unchanged during the transition from phase 1 to phase 2, which makes $V_{out} = 2V_{in}$ for (a) and $V_{out} = 1/2V_{in}$ for (b).

Switched-capacitor DC-DC converters have been applied in commercial products for many years. The motivation is to provide fully integrated on-die power management with low noise, and they need no additional steps during fabrication. They were historically applied to generate a
voltage higher than supply voltage to erase the memory stored in FLASH. The efficiency and voltage stability are not that important in this application. As research has progressed, people have pushed SC converters into the domain that inductor-based converters occupied, since they exhibit lots of characteristics superior to the inductor-based ones, especially in low-power applications. The unavoidable ripple voltage caused by the charging and discharging period can be greatly relieved by interleaved-phase arrangement.

1.2 History

Charge pump was originally developed by Cockcroft and Walton to generate a very high voltage for electron acceleration, which was not for circuits’ power supply. Therefore, the structure of the first charge pump was called the Cockcroft-Walton voltage multiplier or ladder topology [2].
As shown in Figure 1.3, again $\Phi_1$ and $\Phi_2$ are non-overlapping complementary clock signals. Charge are pumped from bottom to top based on the charge sharing that happens when two capacitors are connected in parallel. $C_A$ is always supplied by $V_{in}$. Capacitors $C_1$ and $C_2$ are responsible for transferring the charge from $C_A$ to $C_B$ and from $C_B$ to $C_C$, respectively. Suppose no charge is stored in any of the capacitors initially and the capacitors are of the same size. At the end of $\Phi_1$, both $C_A$ and $C_1$ contain a total charge of $Q = C_A \cdot V_{in}$. At the end of $\Phi_2$, both $C_B$ and
A total charge of $Q/2$. At the end of next $\Phi_1$, both $C_B$ and $C_2$ contain a total charge of $Q/4$. After a few cycles, both $C_C$ and $C_B$ would contain a total charge of $Q$ and maintain a voltage level of $V_{in}$ at steady state, and thus $V_{out} = 3V_{in}$. Once we swap the entry of input and output, it turns out to be a 3:1 step-down converter. Figure 1.4 shows its two non-overlapping phases.

![Figure 1.4](image)

Figure 1.4. (a) Phase 1 and (b) phase 2 of the 3/1 step-up ladder topology

Dickson changed the original design to use the clock voltage level to buck the capacitors, the result of which is named Dickson charge pump [8], as shown in Figure 1.5.
In normal operation, $C_1$, $C_2$ and $C_3$ maintain different levels of voltage; they contain different amounts of charge if they are of the same size. Every capacitor is charged by the previous stage and supplies the next stage. The conversion ratio can be increased by simply cascading more stages. If the stray capacitance is taken into account, the output voltage could be expressed as:

$$V_{out} = V_{in} - V_d + N \left( \frac{C}{C+C_s} * V_{clk} - V_d \right)$$  \hspace{1cm} (1.2)$$

where $V_d$ represents the forward biased diode voltage drop, $V_{clk}$ represents the voltage swing of the clock signal, $N$ represents the number of stages in cascade and $C_s$ represents the value of the stray capacitance.

Some problems exist in this structure. Because of charge sharing with the stray capacitors, the voltage across the pumping capacitors can only be bucked by $\frac{C}{C+C_s} * V_{clk}$ for every stage. The fatal disadvantage of it is the intrinsic threshold voltage drop upon every stage, adding that if the
diodes are realized by CMOS devices, the large source-to-bulk voltage would raise the threshold voltage as well\(^1\). Although many corrections had been made for improvement, Dickson’s structure was still not applicable for low-voltage applications [3].

The state-of-the-art voltage doubler design was developed by Favrat [4], which was a cross-coupled 2-capacitors 4-switches structure, as shown in Figure 1.6. A lot of high performance step-up converters [5], [7], [9] are designed based on this structure. In this paper, we will investigate this structure in detail.

![Cross-coupled topology](image)

**Figure 1.6. Cross-coupled topology**

\(^1\) Threshold voltage of transistor will change according to source to bulk voltage due to body effect:

\[ V_{th} = V_{T0} + \phi_F (\sqrt{|V_{SB}| + 2|\phi_F|} - \sqrt{2|\phi_F|}) \]

where \( \phi_F \) represents the voltage difference between the Fermi level and the Fermi level of the bulk material and \( V_{T0} \) represents the extrapolated gate-to-source voltage that forms the strong inversion layer without body effect.
One defect that limits the application of the switched-capacitor converter is the output ripple due to the charging and discharging of the capacitors [9]. This problem can be alleviated by increasing the output capacitance or applying faster switching frequency at the cost of die area or switching loss [3]. The multiple-phase design was widely used on inductor-based converters, and was applied to switched-capacitor converters [5]. By using this method, charges are distributed more gently [1], avoiding abrupt current steering. High capacitance density and low parasitic capacitance ratio can be directly translated into high power density and high efficiency [2], respectively. Some designs achieved very high efficiency while delivering a high power per area, especially using SOI process [1], [11]. Some ideas for switchable multi-topology [1], [12], [13] design have appeared recently. They provide high efficiency in a wider range. Output regulations are generally based on hysteretic feedback methods [2] on timing circuits [5], [6].

1.3 This Work

In this work, we will focus on every detail of design techniques for a voltage doubler based on the cross-coupled topology.

The chip is designed to convert a 1.5 V voltage input to approximately 2.5 V voltage output which can drive a 1 mA current load with voltage ripple less than 0.5%. The target efficiency is 70% with 1 mW/mm² power density. The rail voltage 1.5 V is chosen because it is barely the sum of PMOS and NMOS threshold voltages in this half micron process, which makes the design more challenging. This work can be applied under 1.8 V rail voltage with little modifications.
The design uses two 200 pF flying capacitors and a 400 pF output capacitor in 0.5 micron technology. Four-way interleaved phase structure is adopted to reduce the ripple.

Some arrangements come from the literature and have been directly adopted in this work. Some adjustments have been made from the original papers.

In Chapter 2, the switch cell topology based on [4], [5], [7] will be studied in detail, which includes the structure working mechanism, latch-up prevention, level shifter design, switch resistance reduction, interleaved-phase arrangement, test results and analysis.

In Chapter 3, the timing system design techniques will be discussed, including the current-starved VCO design, the cascaded clock divider, the non-overlapping clock generator, the tapered buffer and attempts to eliminate the reverse injection current.

In Chapter 4, the regulation loop will be studied, which includes the error amplifier design and the band-gap reference design.

In Chapter 5, efficiency optimization techniques and analysis will be discussed.

Simulation results and future works will be included in Chapter 6 and the paper will be concluded in this chapter, too.
Chapter 2

Switch Core Design

2.1 Original Topology

The switching cell of this work adopts the famous cross-coupled topology which was first proposed by Y. Nakagome et al. [14].

![Cross-coupled charge pump topology](image)

Figure 2.1. Cross-coupled charge pump topology
As shown in Figure 2.1, the clock system generates two non-overlapping clocks and feeds them to the bottom plate of the capacitors. At steady state, during phase one, the clock signal boosts $C_1$ up. If we assume $C_1$ has already been charged to $V_{DD}$ during the previous phase and the clock signal swing is $V_{DD}$, the voltage level at the top plate of $C_1$ goes to $2V_{DD}$ and meanwhile PMOS M3 turns on, and $C_1$ discharges to the load. At the same time, the bottom plate of $C_2$ is grounded and NMOS M2 turns on and PMOS M4 turns off since the gate of M2 which is also the gate of M4 goes to $2V_{DD}$. This makes $C_2$ charge up to $V_{DD}$ and be ready to be discharged. During phase two, the flying capacitors $C_1$ and $C_2$ swap their roles: the gate of NMOS M1 (which is also the gate of PMOS M3) going high turns M1 on and M3 off, so $C_1$ gets charged; the gate of NMOS M2 and PMOS M4 reduces to approximately $V_{DD}$, turning M2 off and M4 on, and $C_2$ gets discharged to the load.

We choose NMOS devices for the charging path because they provide automatic junction bias. We use PMOS devices for the output switch to avoid the threshold voltage drop from the pumping capacitors to the output capacitor because there is no higher voltage beyond $2V_{DD}$.

Interestingly, as we can see in this topology, all the four switches are driven internally. To make the circuit work in low-voltage design as proposed, some modifications should be made.

### 2.2 Switch Resistance Reduction

The topology is originally proposed in application of DRAM design [14]. Scholars discovered the potential of it and made adjustments. Since the driving signals of the switches for both the charging path NMOS transistors and the discharging path PMOS transistors are generated from the top plates of the pumping capacitors, they are unstable and subject to overdrive shrinking.
The treatment for these is building ancillary circuits to generate stable large-overdrive signals to reduce the paths for both charging and discharging.

### 2.2.1 Output Path Resistance Reduction

As shown in Figure 2.1, the output switches M3 and M4 are driven simply by the top plates of the pumping capacitors, which provide voltage swings of $V_{DD}$ to $2V_{DD}$, at steady state. That is, the output switches’ gate voltage levels are around $V_{DD}$, which is 1.5 V, during their ‘on’ states, which means about 0.5 V voltage-overdrive for the PMOS switches. We should use large devices to reduce undesired $V_{DS}$ drop when the output current is large.

Additionally, if we examine the operation in phase 1, at the beginning $C_1$ is fully charged and $C_2$ is discharged after the previous phase. As time goes on, the voltage across $C_1$ decreases and $C_2$ increases. The overdrive voltage is clamped even tighter because of the discharging process of $C_1$ and charging process of $C_2$.

To adjust this without using a prohibitively large device, a 0 to $2V_{DD}$ swing clock signal that can drive the PMOS devices M3 and M4 is desirable. This voltage can be generated from the clock signal and the DC output but not internally.
As shown in Figure 2.2, a level shifter is designed to spread the clock swing from 0-$V_{DD}$ to 0-$2V_{DD}$. The idea is to generate a voltage level high enough to turn off the PMOS device MP3 of the output inverter whenever necessary. Ideally, when the clock signal goes high, MN2 pulls the voltage level of node $B$ to ground, thus MP1 is turned on and pulls the voltage level of node $A$ to $2V_{DD}$. During the next phase, MN1 turns on, and therefore pulls node $A$ to ground and turns on MP2. At this moment, node $B$ is at $2V_{DD}$. That is how we generate the $2V_{DD}$ clock swing using the 4-transistor latch system.

In practice, some details should be mentioned to make the latch work functionally.

First, the driving capability of the bottom NMOS devices must be much stronger than the upper PMOS devices. Let’s examine the transition period between phase 1 and phase 2. At the end of phase 1, node $B$ should be grounded and node $A$ linked to the power supply. When the transition happens, MN1 turns on and MN2 turns off. These cause the voltage at node $A$ to begin to drop,
and node $B$ floats. The voltage at node $A$ can be pulled down to zero only if the latch is started that turns off MP1. MP1 can be turned off by turning on MP2 so as to pull the floating node $B$ to the upper supply voltage. MP2 turns on when voltage at node $A$ drops below the power supply voltage by $V_{TP}$. In a word, the latch can be activated only if the voltage at node $A$ drops by $V_{TP}$ during the transition. If the driving capabilities of the PMOS devices are stronger or even comparable to that of the NMOS devices, the voltage level of node $A$ would stay somewhere between $2V_{DD}$ and $2V_{DD}-V_{TP}$ and the left string of the latch, which is composed of MP1 and MN1, would maintain a constant current during the phase period, which is not desirable.

How should we size the transistors to limit the cost as well as prevent driving issues arising from both the previous and the next stage? A minimum allowable ratio of the width of the NMOS versus the PMOS devices is desirable to provide guidance on specific sizing. Intuitively, the NMOS transistor has better intrinsic current driving capability than PMOS transistor because of the higher mobility. However, notice that the gate drive voltages of the PMOS transistors are about twice of those of the NMOS transistors. The minimum ratio still has to be over 1. This can be calculated by letting

$$\frac{1}{2} \mu_n C_{ox} \frac{W_n}{L} (V_{GSn} - V_{Th})^2 (1 + \lambda(V_{DSn} - V_{DSn, sat})) = \frac{1}{2} \mu_p C_{ox} \frac{W_p}{L} (V_{SGp} + V_{Th})^2 (1 + \lambda(V_{SDp} - V_{SDp, sat})) \quad (2.1)$$

The subscript $n$ and $p$ represent the NMOS transistor and PMOS transistor, respectively. Using half micron technology, we can assume the threshold voltages, the carrier mobility and $\lambda$ of the NMOS and PMOS devices are known values. Let the gate-to-source voltage of the NMOS
transistor equal 1.5 V and that of PMOS transistor equal 2.6 V\(^2\) and by inspection we can conclude that \(V_{DSn} = 2.6 - V_{DSP}\). We can calculate the ratio \(\frac{W_n}{W_p}=1.21\). That is the ratio for NMOS and PMOS devices to barely maintain a constant current, thus also the minimum ratio to start the latch.

Second, the driving capability of the inverters should be considered.

Second, the driving capability of the inverters should be considered.

Figure 2.3. Overdrive enhancement for PMOS switches

---

\(^2\) The output voltage cannot reach \(2V_{DD}\) in real operation due to the ripple. It is practically between 2.5 V to 2.6 V. Using 2.6 V here would make the result overestimate the minimum value of the ratio a little bit.
As shown in Figure 2.3, the output of the level shifter is connected to the gate of the output PMOS switch, which is meant to conduct the 1 mA load current during its phase. Since the PMOS switches are big transistors, the output inverters of the level shifter cannot be set small, or slow transition behavior will arise. Nevertheless, these transistors should not be set too large, because they may be driven by the PMOS latch transistors which set the size of the NMOS devices below them. From an efficiency point of view, these devices should be sized as small as possible.

An alternative wiring is shown below in Figure 2.4(b).
By inspection, we find that the two circuits are doing the same job. After careful investigation, we conclude that the advantage of (a) is that MN3 is driven directly by the clock, which has a large driving capability provided by the buffer, so the load of MP1 is eased. However, since the gates of the transistors of the output inverter are not connected together, the switch signal cannot be synchronized to these gates due to the delay of the latch: when the inverter tries to pull the output signal to the upper rail, the output node keeps floating for the delay of the latch. The result shows that the output signal experiences a slow rising time as expected. Another advantage of (b) is that the output inverter is driven by a full swing signal, which provides a better current driving capability at the falling edge compared to (a).

In our case, circuit (b) is preferable.
It is obvious that the above circuit outputs a $0-2V_{DD}$-swing negative-logic signal from the $0-V_{DD}$-swing input signal. Likewise, we can deduce the structure to generate positive-logic full-swing output as shown in Figure 2.5.

Figure 2.5. (a) non-inverting low-level to full-swing signal generator with (b) simulation result
If we are about to generate full-swing negative and positive signals from a $V_{DD}$-2$V_{DD}$-swing signal using the same idea, we can deduce the circuits as shown in Figure 2.6, where the green lines are input signals and the red lines are the output full-swing signals.
Figure 2.6 (a) Inverting and (c) non-inverting low-level to full-swing signal generator and (b) (d) their simulation results
2.2.2 Charging Path Resistance Reduction

![Diagram of charging path resistance reduction with labels VDD, M1, M2, C1, C2, CLK, Φ1, Φ2, A, B, (a)]
Now we investigate the problems that the original circuit may encounter during the charging period. As we can see in Figure 2.7(a), the pumping capacitors are simply charged by the NMOS devices above them. One problem arises when the load current is large and the switching frequency is slow\(^3\): the ripple voltage is so large that the gate-to-source voltage of the charging NMOS devices clamp to \(V_{TN}\), the threshold voltage of the NMOS devices, leading to undesired shutting down of the charging path. Specifically, as shown in Figure 2.7(a), in the half cycle that \(C_2\) is to be charged, if we assume that the voltage level at the top plate of \(C_2\), which is node \(B\), raises from some point to 1.5 V and node \(A\) discharges from 3 V to some point below 1.5+\(V_{TN}\), M2 will have been shut down before node \(B\) is charged to 1.5 V, and in this case, node \(B\) would

\[^3\text{The ripple voltage can be roughly predicted by } \Delta V = \frac{I_{load}}{2C\Delta V}, \text{ where } I_{load} \text{ is the load current and } C \text{ is the value of the pumping capacitor.}\]
never be boosted to 3 V by the clock signal during the next half cycle, so the assumption collapses. As we can see in Figure 2.7(b), the pink line represents the voltage level of node A, which is also the source of M1, and the blue line represents the voltage level of node B, which is also the source of M2.

\[
\Delta V = \frac{Q}{C} \Rightarrow \frac{d\Delta V}{dt} = \frac{dQ/dt}{c} = \frac{1}{c}
\]  

(2.2)

According to (2.2), the slope of the figure is proportional to the current through the device. If the load current is large, the slope of node A would be steep and the voltage level at node A would drop rapidly. This would increase the resistance of the charging path as we can see in Figure 2.7(b): the slope of the blue line decreases to zero and the charging path closes. This problem is inevitable in low-voltage light-load slow-switching operation because the switches are driven internally, just like the overdrive problem for PMOS output switches addressed in previous section. The body effect, which increases the threshold voltage of the NMOS devices, worsens the situation by limiting the voltage drop of the output.

Likewise, the solution is to generate a stable external signal to drive the charging path switches. Also, to ensure low charging path resistance, large swing signal is desired.
Figure 2.8. Solution to enhance the conductance of charging path

Figure 2.8 illustrates the schematic of one possible solution proposed in [4]. Capacitors $C_3$ and $C_4$ mean to boost the signal coming out of the level shifters even one $V_{DD}$ higher. Their responsibility is to provide a voltage level high enough to drive the gates of M3 and M4, which are very small capacitive load, around 100 fF. Therefore, they do not need to be large. In Figure 2.8, NMOS transistors M3 and M4 act as the low-resistance switches. By inspection, we observe that their gates are driven by stable voltage signals with a swing of $0-3V_{DD}$. Both M3 and M4 enjoy overdrives around $2V_{DD} - V_{TN}$, which lead to about 16 times bigger charging current than the $VDD - V_{TN}$ overdrive ones according to the square law equation. Capacitors $C_3$ and $C_4$ are
charged by the rail through NMOS transistors M5 and M6, respectively. With the additional paths provided by M3 and M4, the pumping capacitors can be charged much faster during their cycle.

According to the literature, NMOS transistors M1 and M2, the original charging switches with gate drive generated internally, are indispensable in order to start up the charge pump. However, this argument deviates from the author’s judgment and experimental results.

Now we take a closer look at the circuit in Figure 2.8 to figure out how the pump starts up. Ignore the ancillary charging path of transistors M3 and M4 for the time being. Suppose there is no charge stored in capacitors $C_1$ and $C_2$ initially, so the voltages across the capacitors are zero. As soon as the clock signal on the left of the symmetric schematic steps up to $V_{DD}$, the gate level of M2 goes to at least $V_{DD}$. This can make capacitor $C_2$ up to $V_{DD} - V_{TN}$ at most. Nevertheless, as long as $C_2$ is charged, M1 can enjoy a better overdrive in the next half cycle than that of M2 during the current phase, and that translates to a larger amount of charge that $C_1$ can receive during its charging period, and therefore a higher overdrive for M2 in the next cycle. The positive feed-through of the two capacitors maintains the voltage step-up of the voltage levels at their top plates until one of them charge up to $V_{DD}$. Otherwise, the threshold voltage clamp-down happens as addressed above in this section. We are not concerned about that at this moment since we are discussing the start-up issue. Now we consider the ancillary charging path transistors M3 and M4 and compare them with the original charging path M1 and M2. Notice that if the upper rail of the level shifter is $V_{DD}$, the level shifter basically behaves as an inverter. Therefore, the bottom plates of the capacitors $C_3$ and $C_4$ are fed with the same logic signal as those of $C_2$ and $C_1$, respectively. If we omit the original charging switches M1 and M2, it is interesting to discover that NMOS transistors M5 and M3 and capacitors $C_3$ and $C_1$, though not of the same size,
compose another cross-coupled structure on the left hand side, same on the right hand side.

These two sub-pumps’ operation follow the same pattern as the central pump and they should be able to start up themselves as we discussed earlier. The simulation result proves this argument: either structure with or without the existence of transistor M1 and M2 can reach the same output voltage level, though the structure with M1 and M2 settles a little bit faster due to the parallel combination of the charging switches.

Since the pump is able to generate a voltage level up to $3V_{DD}$ by the level shifter buck signal, we are led to consider whether this structure could generate higher voltage that can drive a current.

![Possible topology for 4/1 charge pump](image)

Figure 2.9. Possible topology for 4/1 charge pump

The structure shown in Figure 2.9 may be a candidate for higher conversion ratio, $4V_{DD}$ in this case. The voltage level bucked by capacitors $C_3$ and $C_4$, which is $3V_{DD}$, is extracted by another pair of PMOS transistors and fed to another level shifter to generate clock signal with a swing of $0-3V_{DD}$, which would boost the pumping capacitors $C_5$ and $C_6$. We notice here that capacitors $C_5$ and $C_6$ need to be large since they mean to provide the output current, while capacitors $C_1, C_2, C_3$ and $C_4$ need not be large since they only need to feed a level shifter in the following stage.
Consequently, buffers should be added between the output pumping capacitors and the level shifters. Again, the charging switch on-state resistance should be considered. Here, the charging paths of \( C_1 \) and \( C_2 \) are less important, so are \( C_3 \) and \( C_4 \), since they are not designed to be exhausted during each cycle. Transistors M5 and M6 need large overdrives to fully charge capacitors \( C_5 \) and \( C_6 \), so we connect the gate of M5 to node \( A \) and gate of M6 to node \( B \). Finally, the output would be boosted to \( 4V_{DD} \) by 3 combinations of capacitor and level shifter. We can cascade more stages to generate even higher multiples of \( V_{DD} \).

This topology reminds us the Cockcroft-Walton and Dickson structures illustrated in Figure 1.3 and Figure 1.5, respectively. As we may conclude, the mechanism of Cockcroft-Walton voltage multiplier is based on charge sharing: the voltage is boosted by purely parallel and series connection of capacitors; Dickson’s structure uses clock signals to buck the capacitor which are charged by the capacitor in previous stage; this structure uses capacitors to buck the clock signal to further buck the capacitors. More precisely and concisely, the Cockcroft-Walton voltage multiplier is a pure series-parallel capacitor structure; the Dickson charge pump is a hybrid of series-parallel capacitor and clock boosting structure; the proposed structure by the author is a pure clock boosting structure. The advantage of a charge-sharing structure is that it can provide very high efficiency if the stray capacitance is low, but it occupies large die area by the equal sized capacitors. The advantage of the proposed structure is that the capacitors do not need to be equally sized, which means that the area does not need to be a linear accumulation of the conversion ratio. Thus die area could be saved, but efficiency may not be guaranteed due to the buffers for the large swing clock signals. We also need to pay special attention that the converted voltage should not exceed the specified maximum voltage of the process to prevent undesired
breakdown. In this point of view, this structure cannot provide conversion ratio as high as that which the Cockcroft-Walton structure can achieve.

Further investigation of the proposed structure falls beyond the discussion of this paper and will be studied in the author’s future research.

### 2.3 Bulk Current Prevention

Another problem for this charge pump circuit is the voltage bias for the output series PMOS transistors.

Figure 2.10. Intersection view of a PMOS switch showing the parasitic bipolar transistors

As shown in Figure 2.10, there are three parasitic PNP bipolar devices existing in the N-well process while forming a PMOS transistor: one lateral device formed by the source and drain of
the PMOS transistor and the N-well and two vertical devices formed by the source/drain of the PMOS transistor, the N-well and the substrate. It is obvious that if we fail to bias the N-well with the highest voltage of the system, the parasitic bipolar transistors may be undesirably turned on. The effect of the vertical bipolar devices could be especially undesirable since their on state causes quasi-permanent charge loss. The connection as shown in Figure 2.11 will turn on the parasitic bipolar transistors if the output voltage drops by a junction voltage below the top plate of the pumping capacitor.

![Diagram](image)

**Figure 2.11.** PMOS body connection not preventing the body current

The idea to solve this is to use the clock signal to always switch the higher voltage between the two pumping capacitors to bias the body of the PMOS transistor [4]. As illustrated in Figure
2.12, PMOS transistors M5 and M6 are added to the circuit. They can be minimum sized since they only need to bias the bodies of M3 and M4 and they share the same large-swing gate drive with M3 and M4. The capacitor $C_b$ is added to maintain the voltage level during the dead time of the signal and does not need to be large. In this arrangement, the parasitic bipolar devices will not be turned on even if the output voltage drops by a junction voltage during the operation.

![Figure 2.12. PMOS body connection preventing body current](image)

2.4 Reverse Injection Prevention

Almost all switched-capacitor circuits require their charging and discharging clock signals to be non-overlapping. That is because if both them are switched on, the charging and discharging
switches together will create a path that connects the voltage source to the load directly. That is not efficient because this path makes reverse injection current from the load to the voltage source possible for the step-up charge pump case. Similarly, any switch that connects a high voltage level to the voltage source with lower voltage level may generate reverse injection current and degrade the efficiency. So, the gate drive signals of the switches should be given extra attention. However, if the circuit is built according to the structure proposed in [4], the pumping cell would suffer from strings of reverse current as shown in Figure 2.13. Reverse injection 1, 2 and 3 refers to the malfunction caused by switches M3 (M4), M5 (M6) and M7 (M8), respectively. We will address the problems and solutions in the following subsections in numerical sequence.

![Figure 2.13. Presentation of reverse current existing in the topology](image-url)
After rearranging the clock drive strategy, based on simulation, an average loss current of 146μA is prevented, which is over 4% increase on efficiency.

2.4.1 Ancillary Charging Paths Reverse Current Leakage

If the logic blocks are ideal (no rise or fall time or intrinsic delay), there would not be reverse injection problem in the proposed circuit [4] in Figure 2.13. However, in reality, several nanoseconds’ delay may cause considerably large amount of loss.
Reverse injection 1 refers to the current leakage caused by transistors M3 and M4 during the transition of clock signals from low to high. Let us zoom in the related parts and temporarily ignore the rest of the circuit of Figure 2.13 for simplicity. As illustrated in Figure 2.14, the clock signal boosts capacitor $C_1$ up and turns transistor M3 off through the level shifter. As we take the delay caused by the level shifter into account, there will be an overlapping period at the rising
edge of the clock signal when both signal at the bottom plate of capacitor $C_1$ and signal at the gate of transistor M3 are high. This will turn on transistor M3 and make some amount of the charge stored in $C_1$ flow to the voltage source and degrade the efficiency.

![Diagram of clock signal and circuit components](image)

Figure 2.15. Correction made to prevent reverse injection 1
Since the intrinsic delay of the level shifter is unavoidable, we cannot eliminate the overlapping period driving the transistor M3 with the signal generated from the same clock signal. The solution is to generate the driving signal of transistor M3 from the complementary clock signal. As illustrated in Figure 2.15, M3 is driven by the signal generated from $\overline{CLK}$, which is a full swing voltage with thin high-state window. This can successfully avoid the overlapping period by isolating edges of the driving signal of capacitor $C_1$ and transistor M3.

2.4.2 Charging Paths of Ancillary Capacitors Reverse Current Leakage

Very similar to reverse injection 1, reverse injection 2 refers to the current leakage caused by transistors M5 and M6 during the transition of clock signals from low to high. Let us also zoom in these related parts and ignore the rest of the circuit in Figure 2.13 for simplicity. As illustrated in Figure 2.16, if the level shifter delayed the rising edge of the clock signal, there will be a period that both the driving signal of capacitor $C_3$ and transistor M5 are high. This will cause the undesired charge flow from $C_3$ to the voltage source through M5.
As we indicated in Section 2.2.2, the combination of transistors M5 and M3 and capacitors $C_1$ and $C_3$ is basically another cross-coupled charge pump structure. Consequently, any overlap of the clock signals will lead to undesired waste of power. That is why capacitor $C_3$ should not be driven directly by the inverted driving signal of $C_1$. 

Figure 2.16. Logic components generating reverse injection 2
Actually, after we adjust the circuit as illustrated in Figure 2.15, we have already fixed the reverse injection 2. However, although the capacitors $C_3$ and $C_4$ may be small, the author prefers to drive the gates of transistor M5 and M6 with the inverted full swing clock signals, which can provide larger overdrive, as shown in Figure 2.17.

![Circuit Diagram with Level Shifter]

Figure 2.17. Correction made to prevent reverse injection 2
2.4.3 Output Switches Reverse Current Injection

Reverse injection 3 refers to the current leakage through output PMOS transistors M7 and M8 during the transition of clock signal from high to low. Noticing that, in Figure 2.18, the clock signal and the driving signal of PMOS device M7 cannot be switched down simultaneously due to the intrinsic delay of the level shifter, there exists a period that both signals stay low, during which the pumping capacitor ‘steals’ some charge from the output capacitor. That is undesirable. The nature of reverse injection 3 is different from that of reverse injection 1 and 2 in that 3 is caused by overlap of low signal while 1 and 2 are caused by overlap of high signal. Therefore, we cannot apply the same treatment to reverse injection 3 as we did to reverse injection 1 and 2, since there is no thinner low-voltage window available. We need to generate a separate PMOS driving signal with earlier rising edge.
Attempt 1 is to generate two pairs of non-overlapping signals for the pumping capacitors and the PMOS transistors with different dead time and delay as shown in Figure 2.19. We ignore the helper circuits here for simplicity. Let the dead time and delay of the pumping capacitors’ non-overlapping signal pair be $\tau_1$ and $D_1$, respectively, and those of the PMOS transistors’ non-
overlapping signal pair be $\tau_2$ and $D_2$, respectively. Theoretically, if we let $\tau_1 > \tau_2$, $D_1 > D_2$ and $D_1 - D_2 = 1.5(\tau_2 - \tau_1)$, the overlapping period of the low signal will be eliminated with a dead time of $0.5(\tau_2 - \tau_1)$. However, in reality, the intrinsic delays of the logic gate are hard to control. We can never assign an exact value for the intrinsic delay. Therefore, attempt 1 would not be the first choice.
Figure 2.19. Attempt 1 to prevent reverse injection 3
Attempt 2, on the other hand, avoids the calculation and generates the driving signal of the PMOS output transistors with the original clock signal as shown in Figure 2.20. As described in the timing diagram, the driving signal of the PMOS output transistors will turn them off ahead of the clock signal, settling the pumping capacitor down by $\tau$, where $\tau$ refers to the dead time of the non-overlapping signals. This way, the output switch will never be on when the pumping capacitor of their side is in its charging state. This efficiently avoids the reverse injection.
Figure 2.20. Attempt 2 to prevent reverse injection 3
2.5 Operational Analysis

In this section, we will discuss the charge-pump operation in details in a pattern of data analysis from a design perspective. We divide it into two subsections: charging and discharging behaviors.

2.5.1 Charging Behavior

As illustrated in Figure 2.7, during-steady state operation, the voltage levels at node $A$ and $B$ tend to clamp together, and therefore shrink the overdrive voltage of the charging transistor and reduce the current capability of the device. The body effects of the charging transistors worsen this circumstance. Consequently, we adopted charging transistors with gate drive generated outside the charge pump to eliminate this problem, as illustrated in Figure 2.8. To achieve both functionality and efficiency, we should set the ancillary capacitors $C_3$ and $C_4$ properly. Specifically, as shown in Figure 2.21, capacitor $C_4$ should be big enough to allow the top plate of $C_4$ to maintain a certain voltage after the charge sharing with the gate capacitance of MN4 during the transition, so that the overdrive of transistor MN4 can be large enough to maintain a low resistance charging path during the steady state.
The gate capacitance of MN4 can be calculated as:

\[ C_{gate} = \frac{2}{3} \times C_{oxn} = \frac{2}{3} \times 100 \mu m \times 0.6 \mu m \times 2.5 fF/\mu m^2 = 100 fF \quad (2.3) \]

which is a rough estimation since the gate capacitance is a function of overdrive voltage. Then, we estimate the value of capacitor \( C_4 \) to maintain \( \frac{3}{4} \) of its voltage capacity after the charge sharing:

\[ C_{gate} \times (V_{gate,after} - V_{gate,before}) = \frac{1}{4} \times C_4 \times (V_{4,before} - V_{4,after}) \quad (2.4) \]

\[ V_{gate,after} - V_{gate,before} = (3 - 1) - (1.5 - 2.5) = 3 V \quad (2.5) \]

\[ V_{4,before} - V_{4,after} = (4 - 2.5) - (3 - 2.5) = 1 V \quad (2.6) \]
where $V_{\text{gate, before}}$ represents the voltage capacity of the gate capacitance of MN4 before the charge sharing procedure and $V_{\text{gate, after}}$ represents that of MN4 after the charge sharing procedure, and the same representations of $V_{4, \text{before}}$ and $V_{4, \text{after}}$ for capacitor $C_4$. We conclude that so long as we set the value of $C_4$ larger than $1.2 \, \text{pF}$ that we can ensure a voltage level higher than $3 \, \text{V}$ at the top plate of capacitor $C_4$, that is, an overdrive voltage of $2 \, \text{V}$ for transistor MN4, at steady state.

2.5.2 Discharging Behavior

In this section, it is time to examine the output part at the time window when the output switch is on. For a better understanding of the charge pump circuit and a design guidance, the author finds it beneficial as well as interesting to translate the circuit at a mathematical basis: to imitate the behavior of a circuit simulator using Matlab coding.
As shown in Figure 2.22, after the optimization, the output path can be simplified to two capacitors and an independent current source connected by a PMOS transistor. Since the gate of the PMOS transistor is connected to ground when the switch signal is on, the overdrive of the PMOS device should be $V_1$ at this time. How does the size of the device influence the output behavior? What drives the circuit to start to pump up? When does the pump reach its steady state? The answers to these questions will be unveiled after we perform the following data analysis based on the device constraints.

Let us first set the nodal voltages at $V_1$ and $V_2$ to be some arbitrary values near the steady state, say 2.6 V and 2.1 V, respectively. At this time, we can conclude that the transistor is operating in triode region since the source to drain voltage is less than the source to gate voltage by more than a threshold voltage of the PMOS transistor. We can write as follow:

$$
\begin{align*}
\left\{ \begin{array}{l}
\mu_p C_{ox} \frac{W}{L} \left[ (V_1 - |V_{TP}|)(V_1 - V_2) - \frac{(V_1 - V_2)^2}{2} \right] = I_{load} + C_{out} \frac{dV_2}{dt} \quad (a) \\
I_{load} + C_{out} \frac{dV_2}{dt} = -C_{pump} \frac{dV_1}{dt} \quad (b)
\end{array} \right.
\end{align*}
$$

The careful reader may discover that equation (2.8b) can be deduced to:

$$t \times I_{load} + C_{out} (V_2(t) - V_2(0)) = C_{pump} (V_1(0) - V_1(t)) \quad (2.9)$$

where $V_1(0)$ and $V_2(0)$ represent the voltage level of $V_1$ and $V_2$ at time 0, also known as the initial conditions. Equation (2.8a) can be deduced to a first-order ordinary differential equation in respect of $V_1$ and $t$ by plugging equations (2.8b) and 2.9 into it. We can plot the family curves of $V_1$ and $V_2$ vs. time on the same axis with $\frac{W}{L}$ changing as a variable.
Figure 2.23. Plotted results at the output with the size of the PMOS switch changing as a parameter.

In Figure 2.23, the family curves at the top and bottom represent the voltage levels of $V_1$ and $V_2$, respectively. $I_{load}$ is set to 1 mA. The innermost light blue curves are plotted when the PMOS device is sized to 400/1 and the outermost purple curves are plotted when the PMOS device is sized to 20/1.

Figure 2.23 provides a lot of insight into the behavior of the output part of the circuit. First, we notice that $V_1$ drops drastically at the beginning and $V_2$ rises at the same time. This is when large current flows out of the pumping capacitor and supplies both the load and the charging output capacitor. However, this cannot last long, since as $V_1$ and $V_2$ clamp together, the resistance of the PMOS switch goes high and decreases the current, which decelerates the process of the $V_1$ and $V_2$ clamping together interactively. And finally, as we can see in Figure 2.23, at some time between 10 and 20 nanoseconds, $V_2$ starts to drop, which means that the load is supplied by both pumping
capacitor and the output capacitor. This can be proved by plotting the current flowing out of the pumping capacitor and the current flowing into the output capacitor.

Figure 2.24. Plotted current behaviors at the pumping capacitor and output capacitor with the size of the PMOS changing as a parameter

As we can see in Figure 2.24, the upper family curves represent the current flowing out of the pumping capacitor while the lower one represent the current flowing into the output capacitor with changing variable $\frac{w}{L}$. As predicted, the current flowing into the output capacitor falls below zero, which can be interpreted to mean that the current starts to flow out of the output capacitor. The sizing of the PMOS output switch determines how fast the charge is delivered from the pumping capacitor to the output capacitor and how large the output ripple could be: the bigger the PMOS switch is, the faster the charge is delivered and the larger the ripple will be.
Second, according to Figure 2.23, we can conclude that if the switching frequency is sufficiently fast, in other words, the period is small, the output capacitor is charged up and the output voltage is increased. At the very beginning of the transient period, we assume that there is no charge stored in the capacitors. Therefore, during the first cycle, the voltage level of $V_1$ and $V_2$ should be 1.5 and 0. Notice that at this moment, the PMOS switch is operating in saturation. This means that the nodal voltages are governed by:

$$\frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_1 - V_{TP})^2 [1 + \lambda (V_1 - V_2 - V_{DSat})] = I_{load} + C_{out} \frac{dV_2}{dt} \quad (a)$$

$$I_{load} + C_{out} \frac{dV_2}{t} = -C_{pump} \frac{dV_1}{dt} \quad (b)$$

We can also plot this as follows:

Figure 2.25. Initial pump-up voltage levels at both nodes with the size of PMOS changing as a parameter
In Figure 2.25, we can see that, for large switches, although the changes are gentle because of the weak dependence on $V_{ds}$ and high load current, the output voltages are climbing. After a few cycles, the PMOS switch reaches its triode region, and the current grows bigger and the voltage climbs faster.

Third, if we assume that the charging process is ideal, that is, the pumping capacitor is charged to 1.5 V without exception before the PMOS is turned on, we can plot the voltage at the output with different initial conditions. In this case, we adopt only the 400/1 for PMOS size for clarity.

![Graph showing voltage vs time for different initial conditions](image)

**Figure 2.26.** Plotted results for different initial conditions

As shown in Figure 2.26, the red lines at the bottom to the blue lines at the top represent the voltage levels at the top of the pumping capacitor and the output capacitor with changing initial
condition of output voltage from 2.3V to 2.9V as a variable. We can find that the higher the initial output voltage level is, the less it is going to increase, and the faster it starts to decrease. So, for a given switching period, there should be a moment that end point equals to the start point. Thus, we can always perform a simulator’s transient analysis by plotting (2.8) along a continuous period of time.

![Graph showing output voltage level](image)

**Figure 2.27.** Plotted result showing the output voltage level in a transient period

Figure 2.27 proves the prediction and suggests that the output settles around 350 ns. We can compare this Matlab figure with Figure 6.4 generated by Cadence.

Also, we can discover the influence of sizing on the output behavior:
Figure 2.28. Analytical output levels with the size of the PMOS switch changing as a parameter

Figure 2.28 shows the maximum voltages the output can reach and the settling times influenced by differently sized PMOS switch. It indicates that if the $\frac{W}{L}$ of the PMOS device is over 160, there won’t be much influence of sizing on the performance.

Matlab codes for the discussion of this section can be seen in Appendix A.
Chapter 3

Timing Circuits

Like we mentioned in Chapter 1, the switch core discussed in the previous chapter will be four-way phase-interleaved. First of all, we need a voltage-controlled oscillator (VCO) so that the charge pump can be regulated via frequency control. Secondly, the clock will be distributed by cascaded clock dividers. Thirdly, each equally phase-shifted clock signal will be distributed into two non-overlapping signals. Since every pair of signals is driving two 50 pF capacitors, finally, a tapered buffer is necessary before the non-overlapping signals are fed into the capacitors. The block diagram of the timing system is depicted in Figure 3.1.
We divide this chapter into four parts to illustrate the design of the four functional blocks of the timing system in this charge pump circuit.

3.1 Voltage-Controlled Oscillator

Inverter-based ring oscillators generate pulses because of the delay produced by every stage of it. There is a $\frac{N-1}{N} \times 180$ degree phase shift from the previous stage, where $N$ is an odd number.
representing the number of stages. The delay of each stage is determined by the value of gate capacitance of the inverter and slewing current. Therefore, with a fixed number of stages, the frequency of the output pulse depends on both the size of the inverter and the sinking current. Below is the topology we adopted in this design.

Figure 3.2. Schematic of the voltage-controlled oscillator

Figure 3.2 represents a five-stage current-starved voltage-controlled ring oscillator. The delay of each stage is governed by the current supplied by the current mirrors on both top and bottom of the inverter when the inverters are properly sized by design. The current fed to the inverters is tuned by the gate voltage of MN1. The resistor under MN1 is placed to make the current gain more linear, so that the frequency gain can be more linear. Also, it can prevent the current from growing too high to maintain normal operation especially when the output of the charge pump is low at start up. The output buffer can be an inverter, which is necessary to refine the output from the ring oscillator to a square wave as shown in Figure 3.3.
Figure 3.3. Simulation result at the output of the VCO with and without output buffer

Arbitrarily, we want the oscillator to operate at its center frequency of 5 MHz when $V_{ctr}$ is pinned at 1.1 V to provide a starved current of 5 $\mu$A. Then, the value of the resistor can be reached by:

$$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{ctr} - R * I - V_{TN})^2 = I$$  \hspace{1cm} (3.1)$$

where $I$ is the starved current. The resistance can be solved to approximately 50 $\Omega$.

The inverters are sized so that the output pulse frequency is 5 MHz when the current is 5 $\mu$A. If we assume the rising and falling time of each stage in the ring oscillator are the same, we can reach the rising or falling edge by:

$$f_{center} = \frac{1}{N \times 2 \times t_{rise}}$$  \hspace{1cm} (3.2)$$
where \( N \) represents the number of stages, in our case 5. Then we can solve for the input capacitance of each stage according to:

\[
t_{\text{rise}} = \frac{V_{DD} \times C_{\text{in}}}{I}
\]  

(3.3)

At this time, we can solve for the widths of the NMOS devices by:

\[
C_{\text{in}} = \frac{3}{2} \times C_{\text{ox}} \times W \times L \times (K + 1)
\]

(3.4)

where \( W \) is the width and \( L \) is the length, which can be set to 0.6 arbitrarily. \( K \) represents the ratio of PMOS to NMOS device in an inverter, which is normally set to 2.

To keep MN1 in saturation region, we can write:

\[
V_{DD} - V_{GSP} - I_{DR} > V_G - I_{DR} - V_{TN}
\]

(3.5)

\[
V_{ctr} < V_{DD} - V_{GSP} + V_{TN}
\]

(3.6)

Notice here that the gate-to-source voltage of the PMOS device is somewhat comparable with the threshold voltage of the NMOS device knowing that the body effect exists and the current is relatively small. Thus, we should keep the control voltage generated from the regulation circuit small to prevent the degradation of linearity.

Another issue worth mentioning is that we need to check if the current we set at the beginning is smaller than the intrinsic current of the inverter after the size is determined. We won’t be able to control the delay if the current is not starved.
Finally, we need to set an initial condition anywhere around the loop of the ring during simulation since the ring oscillator has no input and the simulator operates on the basis of Kirchhoff nodal analysis.

### 3.2 Cascaded Clock Dividers

Figure 2.24 gives us some intuition about how the output capacitor is charged. Here, in Figure 3.4, we plot the current flows into the output capacitor when the PMOS switch is on for convenience.

![Figure 3.4. Plotted current density flowing into the capacitor in one cycle](image)

Since the integration of current with respect to time is the total charge flow, we realize that most of the charge is delivered to the output capacitor during only the first 1/10 of the period. During
this period, the current drops from 4 mA to minus 400 μA, which means that the output capacitor experienced a short drastic charging period followed with a long mild discharging period.

Accepting that the pattern of the current cannot be changed, why can’t we redistribute the first 1/10 current behavior along the whole period by phase shifting the divided capacitors? This way, the output capacitor avoids abrupt current flow in a short period and the negative current somewhat alleviates the large charging current. The charge is transferred more finely along the period and the output voltage ripple is efficiently reduced.

The phase shifted clocks can be realized by cascading clock dividers. A clock divider can be realized as illustrated in Figure 3.5.

(a)
At the first glance, we notice that the circuit is composed of two duplicated subunits fed to each other. Each unit is composed of a decision circuit and a NAND latch. The decision circuit decides whether the subunit operates as master or slave circuit depending on the input clock: 0 for master and 1 for slave. To understand the operation of this, we may monitor the signal patterns at nodes $A-D$ in Table 3.1.

<table>
<thead>
<tr>
<th>CLK</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 3.1 Truth table of node $A-D$ with $CLK$
The outputs of latch1 change states only when nodes $A, B$ convert from 1, 1 to 1, 0 or 1, 1 to 0, 1. Thus, the output pulse frequency is half of the original clock. And, $output1$ to $output4$ are one-by-one phase-shifted by 90 degrees, which is also half a period of the input clock. Notice that if we want the four-way interleaved pump cell to operate at a center frequency of 5 MHz, we need a 20 MHz clock from the oscillator.

We only need $output1$ and $output2$ here since $output3$ and $output4$ are simply the inversion of $output1$ and $output2$, which will be converted to non-overlapping signals anyway.

### 3.3 Non-overlapping Clock Generator

To feed both sides of a converter cell, a pair of non-overlapping clock signal is needed. This can be generated by the topology shown in Figure 3.6(a).
As illustrated in Figure 3.6, the circuit is just a NAND gate latch added with delay units before the signals are taken. The transition starts only when either of the NAND gate is fed by a ‘low’. The ‘high’ always appears at one string of the outputs after a period of \( d \) when the other output string has a ‘low’. Thus, as long as \( d \) is sufficiently large, ‘high’ signals will not appear at both of the output strings at the same time. The delay time \( d \) can be approximately predicted by properly sizing the delay units according to equations below.

\[
d_1 = \frac{C_{in} \times V_{TN}}{2I_n} + \frac{C_{in} \times V_{TP}}{2I_n} = \frac{5W+L(K+1)+V_{TN}}{2\mu_{n}^{*}(V_{DD}-V_{TP})^2} + \frac{5L^2(K+1)+V_{TP}}{\mu_{n}^{*}(V_{DD}-V_{TN})^2} \quad (3.7)
\]

\[
d_2 = \frac{C_{in} \times V_{TN}}{2I_p} + \frac{C_{in} \times V_{TP}}{2I_n} = \frac{5W+L(K+1)+V_{TN}}{\mu_{n}^{*}(V_{DD}-V_{TN})^2} + \frac{5L^2(K+1)+V_{TN}}{\mu_{p}^{*}(V_{DD}-V_{TP})^2} \quad (3.8)
\]

\[
d = \frac{d_1 + d_2}{2} \quad (3.9)
\]
where \( d_1 \) represents the delay of master string while \( d_2 \) represents the slave string (the master string is the string the NAND gate of which has ‘low’ inputs while the slave string is the string the NAND gate of which has ‘high’ inputs), and \( d \) is the average of \( d_1 \) and \( d_2 \). \( C_{in} \) represents the input capacitance of the delay cell and can be calculated by (3.4). \( K \) is the ratio of sizes for PMOS device to NMOS device of the delay cell. The derivation of (3.7) and (3.8) is performed in Appendix B.

The careful reader may wonder if the non-overlapping clock generator circuit can also be implemented with NOR gates like Figure 3.7 shows. The answer is yes. However, people do not use it because of low conductance of the series-connected PMOS transistors.

![Figure 3.7. Alternative topology using NOR gates](image)

### 3.4 Tapered Buffer

To reach a minimum delay while driving the large pumping capacitors, tapered buffers are needed. By sizing the inverter around \( e \) times larger than the previous stage, so that the propagation delays of each stage are equal, the minimum total propagation delay is reached:

\[
(t_{rise} + t_{fall})_{total} = 0.7 \times N \times (R_{n1} + R_{p1}) \times (C_{out1} + e \times C_{in1}) \quad (3.10)
\]
where, $R_{n1}$ and $R_{p1}$ represent the effective resistances of the NMOS and PMOS transistors, respectively, of the first stage; $C_{out1}$ and $C_{in1}$ represent the output and input capacitances of the first stage, respectively; $N$ represents the number of stages and can be calculated as:

$$N = \ln \frac{C_{pump}}{C_{in1}} \quad \text{(3.11)}$$

The topology is illustrated in Figure 3.8:

![Figure 3.8. Topology of a four-stage tapered buffer](image)

Figure 3.8. Topology of a four-stage tapered buffer
Chapter 4

Regulation Circuits

Since the output of the DC-DC converter can be loaded with a current source that varies from 200 µA to 1 mA, to provide a relatively stable output voltage, the converter needs to be regulated. In this converter, we adopt the traditional regulation system [9] as shown in Figure 4.1:

![Block diagram showing the feedback loop](image)

Figure 4.1. Block diagram showing the feedback loop

The upper rails are not depicted in Figure 4.1. The output voltage level is divided by the resistors and compared to a temperature and rail-independent voltage level generated by the bandgap voltage reference circuit. The ratio of the resistors is assigned so that the divided desired output voltage is equal to the output of the bandgap reference circuit. The difference between these two voltages will be amplified by the operational transconductance amplifier (OTA) and fed to the
control node of the VCO that we discussed in Section 3.1. Therefore, the output voltage level is regulated by adjusting the switching frequency.

The ratio of the resistors is set according to the desired output voltage level, while their total resistance is designed according to the tradeoff between efficiency and die area (or power density). Suppose we are using a divider of total resistance 100 kΩ. Should the desired output voltage be 2.5 V and the load current be 1 mA, there would be a DC current of 25 µA consumed by the resistors and considered as thermal waste, which degrades the efficiency by at least 2.5%. If a better efficiency is desired, the total resistance should be enlarged, which is already a large die area.

The capacitor $C_{dv}$ is added for the input of the OTA to maintain a relatively constant voltage level against the frequently changing voltage ripple.

This chapter will be divided into two sections to introduce the two blocks, namely, bandgap reference and operational transconductance amplifier, making up the regulation loop of this converter.

### 4.1 Bandgap Voltage Reference

This section will introduce the bandgap voltage reference that sets the output voltage of the voltage converter to a desired value through the regulation loop. With proper design, the voltage reference will generate a voltage level that varies little with changing temperature. The challenge comes from the relatively low rail voltage with high threshold voltages of the devices.
Because the available $V_{dd}$ of the circuit is 1.5 V and the threshold voltages for NMOS and PMOS devices are roughly 0.7 V and 0.9 V, respectively, the traditional self-biased structures are not applicable in this design (stacking the transistors would further increase the threshold voltages of the devices due to body effect).

The proposed topology [15] is shown in Figure 4.2:

![Figure 4.2. Bandgap voltage reference topology](image)

The current mirrors MP1 and MP2 and the amplifier enforce that the voltage level at node $A$ equals at node $B$ so that the current flows in each branch are the same. Connecting node $A$ to the inverting input and node $B$ to the non-inverting input of the amplifier ensures that the loop converges since the common-source PMOS transistor is an inverting amplifier. This is based on
the assumption that the small-signal output resistance at node \( B \) is bigger than that at node \( A \). The current flow in a diode can be expressed as:

\[
I_D = I_S \cdot e^{V_D/nV_T}
\]  \hspace{1cm} (4.1)

where \( I_S \) is the diode’s scale current, \( V_D \) is the voltage across the diode and \( V_T \) is the thermal voltage, which is 26 mV at room temperature (we use \( I_S = 10^{-18} \) A and \( n=1 \) in this paper). Since \( D_2 \) is \( K \) times bigger than \( D_1 \), we can write:

\[
V_{D1} = nV_T \cdot \ln \frac{I}{I_S}
\]  \hspace{1cm} (4.2)

\[
V_{D2} = nV_T \cdot \ln \frac{I}{KI_S}
\]  \hspace{1cm} (4.3)

\[
V_{D1} = V_{D2} + I_{D2} \cdot R_1
\]  \hspace{1cm} (4.4)

\[
R_1 = \frac{nV_T \cdot \ln K}{I}
\]  \hspace{1cm} (4.5)

where \( I \) is the desired current set in both branches. We then check the validity of the assumption:

\[
\frac{\partial V_{D2}}{\partial I} + R_1 > \frac{\partial V_{D1}}{\partial I}
\]  \hspace{1cm} (4.6)

Now we have a PTAT (proportional to absolute temperature) current:

\[
I = \frac{n \cdot k \cdot \ln K \cdot T}{q \cdot R_1}
\]  \hspace{1cm} (4.7)

The voltage across resistor \( R_2 \) is:
\[ V_{R2} = \frac{L \cdot n \cdot k \cdot \ln K \cdot T}{q} \]  \hspace{1cm} (4.8)

Assuming that the temperature coefficient of the voltage across a diode is \(-1.6 \text{ mV/°C}\), to generate a zero temperature coefficient voltage level at \(V_{ref}\), we let

\[ \frac{\partial V_{R2}}{\partial T} = 1.6 \text{ mV/°C} \]  \hspace{1cm} (4.9)

\[ L = \frac{1.6 \times 10^{-3} \cdot q}{n \cdot k \cdot \ln K} \]  \hspace{1cm} (4.10)

\[ R_2 = L \times R_1 \]  \hspace{1cm} (4.11)

The schematic is illustrated in Figure 4.3.
Since the circuit is self-biased, a start-up circuit is needed to prevent zero current flows in each branch. Transistors MP6, MP7 and MN3 form the start-up circuit. If no current flows in MP1, the gate of MP1 should be biased with $V_{DD}$, and so is that of MP6: both MP1 and MP6 are turned off. The voltage level at node $C$ should be a little higher than ground. The voltage level at node $A$ should be ground. Therefore, transistor MP7 is turned on and steers current from the gate of MP1 to node $A$ until they reach the designed voltage level. In normal operation, transistor MP7 should be turned off since the voltage level at node $C$ is near $V_{DD}$.

Since the rail voltage is relatively low compared to the threshold voltages, the operational amplifier is realized with four transistors (MN1, MN2, MP4 and MP5). The ratios $(W/L)$ of the
mirror PMOS transistors are set small to reduce the current. The channel lengths of the transistors of the amplifier are made large to increase the small-signal output resistance. Both actions are aimed at enlarging the gain of the amplifier. Transistor MP8 is connected to operate as a capacitor, which compensates the amplifier at its highest impedance node.

4.2 Operational Transconductance Amplifier

In this section, we are designing an OTA to tune the output clock frequency of the VCO. An OTA is an operational amplifier with high impedance nodes only at its input and output nodes. Still, due to the relatively low rail voltage, we are using the simple structure shown in Figure 4.4:

![Schematic of the proposed OTA](image-url)

Figure 4.4. Schematic of the proposed OTA
Since the $V_{SG}$ drop from the common mode point to the input node is unavoidable and the non-inverting input node will be fixed at about 1.1 V, PMOS input devices are not applicable for this 1.5 V design.

The ratios (W/L) and the lengths of the output transistors can be made large to increase the gain and enhance stability.

The bias circuit is illustrated in Figure 4.5:

![Bias Circuit Schematic](image)

Figure 4.5. Schematic of the bias circuit for the OTA

It is a constant-$g_m$ bias circuit with start-up circuit preventing a zero current circumstance. The reference current is set by properly sizing the resistor and the ratio of transistors MP1 to MP2:

$$V_{SG1} + IR = V_{SG2} \quad (4.12)$$
\[ R = \frac{2}{\sqrt{2\mu_p c_{ox} \left( \frac{W}{L} \right)^2}} \left( 1 - \sqrt{\frac{(W/L)^2}{(W/L)^2_1}} \right) \]  

(4.13)

Notice that the transconductance of MP2 depends only on \( R \) and geometric ratios.

\[ g_{m2} = \frac{2\left[ 1 - \sqrt{\frac{(W/L)_2}{(W/L)_1}} \right]}{R} \]  

(4.14)

Any other transistor biased by this reference has the same attribute:

\[ g_{m_i} = \sqrt{\frac{(W/L)_{iD_i}}{(W/L)^2_{D2}}} \times g_{m2} \]  

(4.15)

for PMOS transistors or

\[ g_{m_i} = \sqrt{\frac{\mu_n(W/L)_{iD_i}}{\mu_p(W/L)^2_{D2}}} \times g_{m2} \]  

(4.16)

for NMOS transistors.

The channel lengths are made large to enlarge the output resistances of the transistors for better stability of the transconductances and uniformity of the reference currents.
Chapter 5

Efficiency Analysis

In this chapter, we will talk about the theoretical efficiency calculations of the charge pump based on the conclusions of previous work and the author’s own understanding.

The efficiency of a voltage converter can be calculated by:

\[ \eta = \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{loss}}} \] (5.1)

where \(P_{\text{load}}\) represents the power delivered to the load while all other power consumptions are concluded as \(P_{\text{loss}}\). Since the power delivers to the load is part of the design specification, optimizing the power efficiency is minimizing the power loss.

As will be explained later, any switched-capacitor DC-DC converter can be simplified into a circuit shown in Figure 5.1:

![Diagram showing the loss terms](image-url)

Figure 5.1. Diagram showing the loss terms
The voltage transformer in the circuit is ideal. The four resistors other than the load resistor models the four loss components that may be discovered in a switched capacitor DC-DC converter circuit, which include two series terms and two parallel terms. As expected, the series terms can cause output voltage reduction from the ideal ratio that the topology provides. We illustrate the loss mechanisms of either series or parallel terms in the following two sections.

5.1 Series Loss

Due to the nature of capacitors, transmitting power through switched-capacitor circuits causes voltage ripples and therefore current ripples at the output. Any ripple voltage or current beyond the minimum value at the output can be regarded as loss. While the voltage drop is inevitable, the ripple current can be minimized by interleaving the topology as much as possible [1]. For simplicity, we assume that the current-ripple loss is negligible in the following analysis.

In this section, the loss resistors that are in series with the load will be discussed. Namely, the first resistor $R_{s1}$ models the intrinsic loss that caused by the nature of the topology, which may be defined as slow-switching limit (SSL) in some literature; the second term $R_{s2}$ models the conduction loss that caused by the non-ideality of the switches, which may be defined as fast-switching limit (FSL) [2] [3]. However, the total series loss-resistor cannot be accurately expressed by simply connecting the two resistors in series. We connect them in series in Figure 5.1 for clarity. Detailed discussion about how they are connected can be found in [2]. We discuss these two terms accordingly in the following subsections.
5.1.1 Intrinsic Loss

First of all, a fact should be clear that charging a capacitor with a DC voltage source will cause intrinsic power loss.

![Capacitor charged by constant voltage source](image.png)

Figure 5.2. Capacitor charged by constant voltage source

As shown in Figure 5.2, the switch turns on at time zero when the capacitor starts to be charged by the voltage source. The voltage level at the top plate of the capacitor reaches the voltage source voltage value $V$ when the time approaches infinity. Here, the energy stored in the capacitor is:

$$E_C = \int_0^Q V_C(q) \, dq = \int_0^Q \frac{q}{C} \, dq = \frac{1}{2} \frac{Q^2}{C} = \frac{1}{2} CV^2$$

(5.2)

where $Q$ is the total charge stored in the capacitor when the capacitor is charged to $V$, $V_C$ represents the voltage across the capacitor with charge $q$ in it.

The total energy consumed by the voltage source can be calculated as:

$$E_V = \int_0^\infty V \cdot i(t) \, dt = V \cdot Q = C \cdot V^2$$

(5.3)

An amount of $\frac{1}{2}CV^2$ energy is lost during this process. Similarly, an amount of $\frac{1}{2} \Delta V \cdot I_L$ power is lost in our charge pump due to this fact, where $\Delta V$ is the ripple voltage, which is also the voltage that the pumping capacitor is charged by $V_{DD}$ in each cycle.
Secondly, although all power excluding the term discussed above is transmitted from the voltage source to the load (assuming all components are ideal), the ripple voltage power at the output should still be counted as loss since it is useless to the load. Assuming \( R_L \cdot C_{pump} \gg T/2 \), where \( T \) is the switching cycle, the slope of the ripple should be relatively fixed. The ripple power loss can be calculated as

\[
P_{LS1b} = \frac{2}{T} \int_t^{t+T/2} V(t)I_L dt = \frac{1}{2} \Delta V \cdot I_L
\]  

(5.5)

Finally, the intrinsic power loss can be summed as:

\[
P_{LS1} = P_{LS1a} + P_{LS1b} = \Delta V \cdot I_L = \frac{I_L^2}{2 \cdot f \cdot C_{pump}}
\]  

(5.6)

It is reasonable to model this loss as a resistor with resistance value:

\[
R_{S1} = \frac{1}{2 \cdot f \cdot C_{pump}}
\]  

(5.7)

The intrinsic capacitor loss is also known as SSL [2] [3], which is characterized by impulsive charge transferring and ideal switches when the RC constant of the switch-on resistance and the pumping capacitor is negligible compared to the switching period. This loss dominates at low frequencies.
5.1.2 Conduction Loss

The second-term series loss is switch conduction loss, which is caused by the on resistances of the switches and the equivalent series resistor of the capacitors. The nature of this loss can also be normalized as a FSL [2] [3]. The circuit reaches this limit when the switching period is far less than the RC constant of the switch resistance and pumping capacitor. The charge is transferred by constant currents between the components and the capacitors can be modeled as constant current sources.

This part of loss can be calculated as:

\[ P_{LS2} = I_L^2 \cdot (\sum_i R_{ON} + ESR) = I_L^2 \cdot [(R_{ON,PMOS} + R_{ON,NMOS}) + ESR] \]  

(5.8)

where, the sum term is the total switch resistance for conducting currents in each half cycle (in our case one PMOS and one NMOS switch are on), ESR represents the equivalent series resistance of the pumping capacitors.

It is hard to accurately calculate the resistance when a switch is on, since its overdrive voltage changes along the period as the capacitor is charging or discharging. Nevertheless, we can roughly model it in its triode region as below:

\[ R_{ON,PMOS} = \frac{L}{\mu p C_{ox} W_P V_O} \]  

(5.9)

\[ R_{ON,NMOS} = \frac{L}{\mu n C_{ox} W_N V_O} \]  

(5.10)
where $V_o$ represents the overdrive of the switches, which is also somewhere around the output voltage due to the ancillary circuits. This can be better shown in Figure 2.13 and related discussion.

### 5.2 Shunt Loss

In this section, we discuss the two shunt resistors $R_{P1}$ and $R_{P2}$ that are shown in Figure 5.1. We model the loss caused by the stray capacitance of the pumping capacitors as $R_{P1}$ since these capacitors are charged by $V_{tn}$ during each period; the loss caused by gate parasitic capacitors as $R_{P2}$ since these capacitors are charged by the overdrives of the switches, which are about the output voltage level as discussed in Section 2.2.

The stray capacitance includes top plate parasitic and bottom plate parasitic capacitors. We absorb them into bottom plate parasitic capacitor since they experience the same voltage swing. This part of the loss can be calculated as:

$$P_{LP1} = 2 \cdot f \cdot C_{bott} \cdot V_{tn}^2$$  \hspace{1cm} (5.11)

The gate parasitic capacitance loss is caused by frequently charging and discharging the gate-to-source capacitance. It is also hard to accurately model since it varies with gate-to-source voltage. We roughly calculate the gate-switching loss as:

$$P_{LP2} = 2 \cdot f \cdot C_{ox} \cdot L \cdot \sum_l W_l \cdot V_O^2 = 2 \cdot f \cdot C_{ox} \cdot L \cdot (W_{PMOS} + W_{NMOS}) \cdot V_O^2$$  \hspace{1cm} (5.12)

where the sum term represents the total width of switches that are turned on during each transition, $L$ stands for the minimum length.
5.3 Optimization

As concluded above, the total loss can be expressed as follow:

\[ P_{\text{Ltotal}} = P_{\text{LS1}} + P_{\text{LS2}} + P_{\text{LP1}} + P_{\text{LP2}} \]  \hfill (5.13)

If we size the width of PMOS transistors three times the width of NMOS transistors for simplicity and ignore the ESR loss, the expression above can be reduced to:

\[ P_{\text{Ltotal}} = I_L^2 \left( \frac{1}{2fC_{\text{pump}}} + \frac{2L}{\mu nC_{\text{ox}}W_{\text{NMOS}}V_o} \right) + 2f \left( C_{\text{bott}}V_{\text{in}}^2 + 4C_{\text{ox}}L \cdot W_{\text{NMOS}}V_o^2 \right) \]  \hfill (5.14)

By making

\[ \frac{\partial P_{\text{Ltotal}}}{\partial f} = 0 \]  \hfill (5.15)

the optimized frequency is determined:

\[ f_{\text{opt}} = \frac{I_L}{2 \sqrt{C_{\text{pump}}(C_{\text{bott}}V_{\text{in}}^2 + 4C_{\text{ox}}L \cdot W_{\text{NMOS}}V_o^2)}} \]  \hfill (5.16)

By inspection of (5.14), it can be concluded that, at high power density, meaning that the load current is high at relatively low pumping capacitance, the series resistance terms become dominant. We may trade some shunt loss for an optimized intrinsic series loss by using a faster clock rate. On the contrary, when the power density is low and the shunt loss terms become more significant, we may slow down the clock rate to alleviate the shunt loss at the cost of higher intrinsic loss.

By making

\[ \frac{\partial P_{\text{Ltotal}}}{\partial W_N} = 0 \]  \hfill (5.17)
the optimized width of NMOS switch is deduced:

\[ W_{N,\text{opt}} = \frac{I_L}{\sqrt{4\mu_n f C_{ox}^2 V_O^3}} \]  \hspace{1cm} (5.18)
Chapter 6

Conclusion

The simulated results of the proposed circuit will be shown and the paper will be concluded in this chapter. We put the full block diagram here for convenience as Figure 6.1.

Figure 6.1. Block diagram of the proposed design

6.1 Results

Figure 6.2 shows the behavior of the circuit ramping to 2.5 V at 1 mA load.
Figure 6.2. Simulated transient output voltage at 1 mA load

Figure 6.3 shows the settling behavior when the load switches from 500 µA to 1 mA.

Figure 6.4 shows the ripple of the output voltage at 500 µA and 1 mA.
Figure 6.4 Output voltage ripples with (a) 500 μA and (b) 1 mA load
The performance of the proposed circuit is listed in Table 6.1 with comparison to some previous work.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>32 nm</td>
<td>32 nm</td>
<td>32 nm</td>
<td>130 nm</td>
<td>32 nm</td>
<td>45 nm</td>
<td>0.35 µm</td>
<td>0.5 µm</td>
<td></td>
</tr>
<tr>
<td>Topology</td>
<td>2/3,1/2,1/3</td>
<td>1/3</td>
<td>1/2</td>
<td>1/2</td>
<td>1/2</td>
<td>1/2</td>
<td>1/2</td>
<td>2/1</td>
</tr>
<tr>
<td>Interleaved phase</td>
<td>32</td>
<td>4</td>
<td>1</td>
<td>16</td>
<td>32</td>
<td>1</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>C&lt;sub&gt;out&lt;/sub&gt;</td>
<td>0</td>
<td>2.2 µF</td>
<td>2 µF</td>
<td>400 pF</td>
<td>0</td>
<td>N/A</td>
<td>400 pF</td>
<td>400 pF</td>
</tr>
<tr>
<td>Area</td>
<td>0.378 mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>N/A</td>
<td>0.25 mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>2.25 mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>6678 µm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>1200 µm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>79.76%</td>
<td>77%</td>
<td>70%</td>
<td>82%</td>
<td>60%</td>
<td>90%</td>
<td>70%</td>
<td>71%</td>
</tr>
<tr>
<td>Power density</td>
<td>860 mW/mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>N/A</td>
<td>540 mW/mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>0.67 mW/mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>1123 mW/mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>2185 mW/mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table 6.1 Performance and parameter comparison

### 6.2 Conclusion and Future work

The design considerations of a switched-capacitor voltage doubler are addressed in detail through the paper. Gate-drive strategies have been improved from the former work to suppress reverse injections; a new topology for a voltage tripler has been proposed; a new way using Matlab to simulate the circuit for a better understanding of the switched-capacitor voltage converter has been introduced.
The author’s future work may include laying out the chip if a fabrication opportunity is possible; simulating the proposed topology in Section 2.2.2; extending the analysis discussed in Section 2.5.2 to interleaved-phase topologies.
Appendix A

This analysis is aimed for a visual grasp of the voltage ripples and interaction between pumping capacitor and the output capacitor of the charge pump and design guidance. The data is constrained by the differential equation sets (2.8) and (2.10) according to KCL and KVL and will be simulated transiently. Variables are listed below that appear in the functions.

- \( v1 \): vector that stores the voltage levels at the top of the pumping capacitor during a discrete time period of one cycle
- \( v2 \): vector that stores the voltage levels at the top of the output capacitor during a discrete time period of one cycle
- \( t \): vector that stores a discrete time span
- \( v10 \): the initial condition of \( v1 \) at \( t=0 \)
- \( v20 \): the initial condition of \( v2 \) at \( t=0 \)
- \( s1 \): the ratio \( W/L \) of the PMOS output switch
- \( v3 \): the symbolic expression of \( dv1/dt \) generated by plugging equation (2.8b) into (2.8a) or (2.10b) into (2.10a)
- \( dv \): \( dv1/dt \)
- \( ipump \): vector that stores the currents flow out of the pumping capacitor
- \( ic \): vector that stores the currents flow into the output capacitor
vector that stores multi-cycle voltage levels at the top of the pumping capacitor during a discrete time span

vector that stores multi-cycle voltage levels at the top of the output capacitor during a discrete time span

plot voltage in one cycle

plot current in one cycle

legends

plot voltage in multi cycles

A.1 CalculateV3.m and CalculateV3saturate.m

The following calculates the symbolic expressions of $\frac{dv_t}{dt}$, so that the solver needs to solve only one ordinary differential equation instead of an equation set.

CalculateV3.m

```matlab
1 v1=sym('v1');
2 t=sym('t');
3 v10=sym('v10');
4 v20=sym('v20');
5 s=sym('s');
```
6 \ v2=0.5*(v10-v1)-(2.5e6)*t+v20; \ \ %v10 \ is \ the \ voltage \ level \ of \ v1 \ at \ t=0; \ v20 \ is \ the \ voltage \ level \ of \ v2 \ at \ t=0.

7 \ v3=(-1)*(37*s*(1e-6))*[(v1-0.9)*(v1-v2)-0.5*(v1-v2)^2]/(2e-10); \ \ %s \ represents \ the \ size \ of \ the \ PMOS \ device \ W/L

CalculateV3saturate.m

1 \ v1=sym('v1');

2 \ t=sym('t');

3 \ v10=sym('v10');

4 \ v20=sym('v20');

5 \ s=sym('s');

6 \ v2=0.5*(v10-v1)-(2.5e6)*t+v20; \ \ %v10 \ is \ the \ voltage \ level \ of \ v1 \ at \ t=0; \ v20 \ is \ the \ voltage \ level \ of \ v2 \ at \ t=0.

7 \ %v3=(-1)*(37*s*(1e-6))*[(v1-0.9)*(v1-v2)-0.5*(v1-v2)^2]/(2e-10); \ \ %s \ represents \ the \ size \ of \ the \ PMOS \ device \ W/L

8 \ v3=(-1)*(37*s*(1e-6))*(v1-0.9)^2*[1+0.05*(0.9-v2)]/(2e-10);
A.2 Triode.m and Saturate.m

Triode.m and Saturate.m are the voltage constraints at the tops of the output and pumping capacitors set by the PMOS output transistor that operates in triode and saturation regions, respectively, which are also an ordinary differential equations.

Triode.m

1     function dv = triode(t,v1)
2       global s1
3       global v10
4       global v20
5
6     dv = (22365127662870639732064256*s1*((2500000*t + (3*v1)/2 - v10/2 - v20)^2/2 - (v1 - 9/10)*(2500000*t + (3*v1)/2 - v10/2 - v20))/120892581961462921875;
7     end

Saturate.m

1     function dv = saturate( t, v1 )
2     %ODE function when PMOS in saturation region
3     % generated from 'calculateV3saturate' changing the s to s1
4     global s1
5  global v10
6  global v20
7  dv = -(22365127662870639732064256*s1*(v1 - 9/10)^2*(125000*t + v1/40 - v10/40 - v20/20 + 209/200))/120892581961462921875;
8  end

A.3 Sizinginfluenceonvoltagelevel.m and Currentbehavior.m

Sizinginfluenceonvoltagelevel.m and Currentbehavior.m plot the voltage behavior at the top of the two capacitors and the current behavior through the PMOS switch, respectively, in one arbitrary cycle with the PMOS size changing as a parameter.

Sizinginfluenceonvoltagelevel.m

1  global v10
2  global v20
3  global s1
4
5  v10 = 2.6;
6  v20 = 2.4;
7  s1 = 20;
for i=1:1:20
s1=s1+20;
[t,v1]= ode45(@triode, [0:1e-9:1e-7], v10);

v2=0.5*(v10-v1)-(2.5e6)*t+v20;
p=plot(t, v1, t, v2);
set(p, 'Color', [1-(i*0.05), i*0.05, 1]);
%l=zeros(20,1);
%l(i)=legend('V1&V2@W/L=20');
%set(l, 'Interpreter', 'none');

ipump = zeros(size(v1));
ic = zeros(size(v2));

for j=1:1:101
ipump(j) = -(37*s1*((2500000*t(j) + (3*v1(j))/2 - v10/2 - v20)^2/2 - (v1(j) - 9/10)*(2500000*t(j) + (3*v1(j))/2 - v10/2 - v20))/1000000;
ic(j) = ipump(j)-(1e-3);
end
%q = plot(t, ic, t, ipump);
%set(q, 'Color', [1-(i*0.05), i*0.05, 1]);

hold all;

%ylabel('Current flows out of pumping capacitor and current flows into output capacitor')
xlabel('t/s');

ylabel('voltage at the top of pumping capacitor and output capacitor/V')
end

%title('current behavior');
title('Sizing Analysis of the Output Switch');

h=legend('V1@W/L=20','V2@W/L=20','V1@W/L=40','V2@W/L=40','V1@W/L=60','V2@W/L=60','V1@W/L=80','V2@W/L=80','V1@W/L=100','V2@W/L=100','V1@W/L=120','V2@W/L=120','V1@W/L=140','V2@W/L=140',...}

'V1@W/L=160','V2@W/L=160','V1@W/L=180','V2@W/L=180','V1@W/L=200','V2@W/L=200','V1@W/L=220','V2@W/L=220','V1@W/L=240','V2@W/L=240','V1@W/L=260','V2@W/L=260',...}

'V1@W/L=280','V2@W/L=280','V1@W/L=300','V2@W/L=300','V1@W/L=320','V2@W/L=320',...}
0', 'V1@W/L=340', 'V2@W/L=340', 'V1@W/L=360', 'V2@W/L=360', 'V1@W/L=380', 'V2@W/L=380', 'V1@W/L=400', 'V2@W/L=400');

37    legend('ResizeLegend');

38    set(h, 'Orientation', 'horizontal');

39    set(h, 'FontSize', 7);

40    set(h, 'Location', 'EastOutside');

41    h = legend(v1(1), 'V1@W/L=20', v2(1), 'V2@W/L=20', v1(19), 'V1@W/L=400', v2(19), 'V2@W/L=400');

Currentbehavior.m

1     global v10

2     global v20

3     global s1

4

5     v10 = 2.6;

6     v20 = 2.4;

7     s1 = 20;
for i=1:1:20
    s1=s1+20;
end
[t,v1]= ode45(@triode, [0:1e-9:1e-7] , v10);
v2=0.5*(v10-v1)-(2.5e6)*t+v20;
%p=plot(t, v1, t, v2);
%set(p, 'Color', [1-(i*0.05), i*0.05, 1]);
[l]=zeros(20,1);
%l(i)=legend('V1&V2@W/L=20');
%set(l, 'Interpreter', 'none');

ipump = zeros(size(v1));
ic = zeros(size(v2));

for j=1:1:101
    ipump(j) = -(37*s1*((2500000*t(j) + (3*v1(j))/2 - v10/2 - v20)^2/2 - (v1(j) - 9/10)*(2500000*t(j) + (3*v1(j))/2 - v10/2 - v20))/1000000;
ic(j) = ipump(j)-(1e-3);
end
q = plot(t, ic, t, ipump);
set(q, 'Color', [1-(i*0.05), i*0.05, 1]);
hold all;

ylabel('Current flows out of pumping capacitor and current flows into output capacitor')

xlabel('t/s');

%ylabel('voltage at the top of pumping capacitor and output capacitor/V')

data

title('current behavior');

%title('Sizing Analysis of the Output Switch');

h=legend('Ipump@W/L=20','Ic@W/L=20','Ipump@W/L=40','Ic@W/L=40','Ipump@W/L=60','Ic@W/L=60','Ipump@W/L=80','Ic@W/L=80','Ipump@W/L=100','Ic@W/L=100','Ipump@W/L=120','Ic@W/L=120','Ipump@W/L=140','Ic@W/L=140',...'

'Ipump@W/L=160','Ic@W/L=160','Ipump@W/L=180','Ic@W/L=180','Ipump@W/L=200','Ic@W/L=200','Ipump@W/L=220','Ic@W/L=220','Ipump@W/L=240','Ic@W/L=240','Ipump@W/L=260','Ic@W/L=260',...'

'Ipump@W/L=280','Ic@W/L=280','Ipump@W/L=300','Ic@W/L=300','Ipump@W/L=320','Ic@W/L=320','Ipump@W/L=340','Ic@W/L=340','Ipump@W/L=360','Ic@W/L=360','Ipump@W/L=380','Ic@W/L=380','Ipump@W/L=400','Ic@W/L=400');
A.4 Initialpumpingup.m and Changeofinitialcondition.m

*Initialpumpingup.m* shows the voltage behavior at the tops of the two capacitors during the first cycle when the capacitor’s voltage storage is low with PMOS size changing as a parameter.

*Changeofinitialcondition.m* plots the voltage behavior at the tops of the two capacitors charging from different storage levels.

Initialpumpingup.m

1 global v10
2 global v20
3 global s1
4
5  v10 = 1.5;
6  v20 = 0;
7  s1 = 20;
8
9  for i=1:1:20
10    s1=s1+20;
11  [t,v1]= ode45(@saturate, [0:1e-9:1e-7] , v10);
12  v2=0.5*(v10-v1)-(2.5e6)*t+v20;
13  p=plot(t, v1, t, v2);
14  set(p, 'Color', [1-(i*0.05), i*0.05, 1]);
15  %l=zeros(20,1);
16  %l(i)=legend('V1&V2@W/L=20');
17  %set(l, 'Interpreter', 'none');
18  ipump = zeros(size(v1));
19  ic = zeros(size(v2));
20  for j=1:1:101
21    ipump(j) = -(37*s1*((2500000*t(j) + (3*v1(j))/2 - v10/2 - v20)^2/2 - (v1(j) - 9/10)*(2500000*t(j) + (3*v1(j))/2 - v10/2 - v20))/1000000;
101

22 \text{ic}(j) = \text{ipump}(j)-(1e-3);

23 \text{end}

24 \%q = \text{plot}(t, \text{ic}, t, \text{ipump});

25 \%\text{set}(q, 'Color', [1-(i*0.05), i*0.05, 1]);

26 \text{hold all;}

27

28 \%\text{ylabel}'(\text{Current flows out of pumping capacitor and current flows into output capacitor}')

29 \text{xlabel}'(t/s)';

30 \%\text{ylabel}'(\text{voltage at the top of pumping capacitor and output capacitor/V}')

31 \%\text{end}

32 \%\text{title}'(\text{current behavior}')';

33 \%\text{title}'(\text{Sizing Analysis of the Output Switch}')';

34

h=\text{legend}'V1@W/L=20',V2@W/L=20',V1@W/L=40',V2@W/L=40',V1@W/L=60',V2@W/L=60',V1@W/L=80',V2@W/L=80',V1@W/L=100',V2@W/L=100',V1@W/L=120',V2@W/L=120',V1@W/L=140',V2@W/L=140',...'

35

'V1@W/L=160',V2@W/L=160',V1@W/L=180',V2@W/L=180',V1@W/L=200',V2@W/L=20
0', 'V1@W/L=220', 'V2@W/L=220', 'V1@W/L=240', 'V2@W/L=240', 'V1@W/L=260', 'V2@W/L=260', ...

'V1@W/L=280', 'V2@W/L=280', 'V1@W/L=300', 'V2@W/L=300', 'V1@W/L=320', 'V2@W/L=320', 'V1@W/L=340', 'V2@W/L=340', 'V1@W/L=360', 'V2@W/L=360', 'V1@W/L=380', 'V2@W/L=380', 'V1@W/L=400', 'V2@W/L=400');

37    %legend('ResizeLegend');

38    %set(h, 'Orientation', 'horizontal');

39    set(h, 'FontSize', 7);

40    set(h, 'Location', 'EastOutside');

41    %h=legend(v1(1), 'V1@W/L=20', v2(1), 'V2@W/L=20', v1(19), 'V1@W/L=400', v2(19), 'V2@W/L=400');

42

Changeofinitialcondition.m

1     global v10

2     global v20

3     global s1

4

5     v10 = 3.0;
6 \quad v20 = 2.2;

7 \quad s1 = 400;

8

9

10 \quad \text{for } i=1:1:7

11 \quad v20=v20+0.1;

12 \quad [t,v1]= \text{ode45}(@triode, [0:1e-9:1e-7] , v10);

13 \quad v2=0.5*(v10-v1)-(2.5e6)*t+v20;

14 \quad p=\text{plot}(t, v1, t, v2);

15 \quad \text{set}(p, 'Color', [1-(i*0.12), 0, i*0.1]);

16 \quad %l=zeros(20,1);

17 \quad %l(i)=\text{legend}'V1\&V2@W/L=20';

18 \quad %set(l, 'Interpreter', 'none');

19 \quad \text{ipump = zeros(size(v1));}

20 \quad \text{ic = zeros(size(v2));}

21 \quad \text{for } j=1:1:101

22 \quad \text{ipump}(j) = -(37*s1*((2500000*t(j) + (3*v1(j))/2 - v10/2 - v20)^2/2 - (v1(j) - 9/10)*(2500000*t(j) + (3*v1(j))/2 - v10/2 - v20))/1000000;
ic(j) = ipump(j)-(1e-3);

end

%q = plot(t, ic, t, ipump);

%set(q, 'Color', [1-(i*0.05), i*0.05, 1]);

hold all;

%ylabel('Current flows out of pumping capacitor and current flows into output capacitor')

xlabel('t/s');

ylabel('voltage at the top of pumping capacitor and output capacitor/V')

end

title('one cycle operation with changing initial condition');

%title('current behavior');

%title('Sizing Analysis of the Output Switch');

%h=legend('V1@W/L=20','V2@W/L=20','V1@W/L=40','V2@W/L=40','V1@W/L=60','V2@W/L=60','V1@W/L=80','V2@W/L=80','V1@W/L=100','V2@W/L=100','V1@W/L=120','V2@W/L=120','V1@W/L=140','V2@W/L=140','V1@W/L=160','V2@W/L=160','V1@W/L=180','V2@W/L=180','V1@W/L=200','V2@W/L=200',...
A.5 ContinuousAnalysis.m and Settlingtimecomparison.m

ContinuousAnalysis.m is the transient voltage prediction at the output of the voltage converter with arbitrary initial conditions and switching frequency.

Settlingtimecomparison.m is the continuous analysis with changing PMOS switch sizing as a parameter.
ContinuousAnalysis.m

1  global v10

2  global v20

3  global s1

4

5  v10 = 3.0;

6  v20 = 2.2;

7  s1 = 400;

8  t1=[0:1:399];

9  v11=zeros(400);

10  v22=zeros(400);

11

12

13  for i=0:1:7

14

15  [t,v1]= ode45(@triode, [0:1e-9:(49e-9)] , v10);

16  v2=0.5*(v10-v1)-(2.5e6)*t+v20;
17 \%p=plot(t, v1, t, v2);
18 \%set(p, 'Color', [1-(i*0.16), 0, i*0.1]);
19 for j=1:1:50
20 \% t1(i*50+j)=t(j);
21 v11(i*50+j)=v1(j);
22 v22(i*50+j)=v2(j);
23 end
24
25 v20=v2(50);
26
27 \%l=zeros(20,1);
28 \%l(i)=legend('V1\&V2@W/L=20');
29 \%set(l, 'Interpreter', 'none');
30 \%ipump = zeros(size(v1));
31 \%ic = zeros(size(v2));
32 \%for j=1:1:101
33 \%ipump(j) = -(37*s1*((2500000*t(j) + (3*v1(j))/2 - v10/2 - v20)^2/2 - (v1(j) - 9/10)*(2500000*t(j) + (3*v1(j))/2 - v10/2 - v20))/1000000;
\begin{verbatim}
34   %ic(j) = ipump(j) - (1e-3);
35   %end
36   %q = plot(t, ic, t, ipump);
37   %set(q, 'Color', [1-(i*0.05), i*0.05, 1]);
38   hold all;
39
40   ylabel('Current flows out of pumping capacitor and current flows into output capacitor')
41   xlabel('t/s');
42   ylabel('voltage at the top of pumping capacitor and output capacitor/V');
43   end
44   p1=plot(t1,v22);
45   xlabel('t/ns');
46   ylabel('Output Voltage/V');
47   title('Output Ripple');
48   title('current behavior');
49   title('Sizing Analysis of the Output Switch');
\end{verbatim}
global v10
global v20

v10 = 3.0;

v20 = 2.2;

s1 = 20;

t1 = [0:1:399];

v11 = zeros(400);

v22 = zeros(400);

for k = 2:1:19
    s1 = 20 + k * 20;
    for i = 0:1:7
        [t, v1] = ode45(@triode, [0:1e-9:(49e-9)], v10);
        v2 = 0.5 * (v10 - v1) - (2.5e6) * t + v20;
        %plot(t, v1, t, v2);
    end
end
19    %set(p, 'Color', [1-(i*0.16), 0, i*0.1]);
20    for j=1:1:50
21       % t1(i*50+j)=t(j);
22       v11(i*50+j)=v1(j);
23       v22(i*50+j)=v2(j);
24    end
25
26    v20=v2(50);
27
28    %l=zeros(20,1);
29    %l(i)=legend('V1&V2@W/L=20');
30    %set(l, 'Interpreter', 'none');
31    %ipump = zeros(size(v1));
32    %ic = zeros(size(v2));
33    %for j=1:1:101
34    %ipump(j) = -(37*s1*((2500000*t(j) + (3*v1(j))/2 - v10/2 - v20)^2/2 - (v1(j) - 9/10)*(2500000*t(j) + (3*v1(j))/2 - v10/2 - v20))/1000000;
35    %ic(j) = ipump(j)-(1e-3);
36 \%end

37 \%q = plot(t, ic, t, ipump);

38 \%set(q, 'Color', [1-(i*0.05), i*0.05, 1]);

39 hold all;

40

41 \%ylabel('Current flows out of pumping capacitor and current flows into output capacitor')

42 \%xlabel('t/s');

43 \%ylabel('voltage at the top of pumping capacitor and output capacitor/V');

44 end

45 p1=plot(t1,v22);

46 xlabel('t/ns');

47 ylabel('Output Voltage/V');

48 title('Output Ripple');

49 hold all;

50 end

51 \%title('current behavior');

52 \%title('Sizing Analysis of the Output Switch');
h=legend('Vout@W/L=60','Vout@W/L=80','Vout@W/L=100','Vout@W/L=120','Vout@W/L=140',... 'Vout@W/L=160','Vout@W/L=180','Vout@W/L=200','Vout@W/L=220','Vout@W/L=240','Vout@W/L=260',... 'Vout@W/L=280','Vout@W/L=300','Vout@W/L=320','Vout@W/L=340','Vout@W/L=360','Vout@W/L=380','Vout@W/L=400');

%legend('ResizeLegend');

%set(h, 'Orientation', 'horizontal');

set(h, 'FontSize',7);

set(h, 'Location', 'EastOutside');

%h=legend(v1(1), 'V1@W/L=20', v2(1), 'V2@W/L=20', v1(19), 'V1@W/L=400', v2(19), 'V2@W/L=400');
Appendix B

Consider the circuit shown in Figure B.1.

![Circuit Diagram]

Figure B.1. Schematic of the delay cell in the non-overlapping clock generator

We define the time period between when node $IN$ falls to low and node $C$ starts to rise as $d_1$, and time period between when node $IN$ rises to high and node $C$ starts to fall as $d_2$.

Since the rail voltage is 1.5 V and the threshold voltages for NMOS and PMOS are 0.7 V and 0.9 V, respectively, the switching point happens when one transistor is off while the other starts to turn on.
We assume that currents flowing in the logic gates during transitions are constant for simplicity and the previous stage of this circuit has strong current driving capability. The voltage behaviors of node \( IN, A, B \) and \( C \) could be depicted in Figure B.2.

![Figure B.2. Sketch showing the transient nodal voltage levels in the delay cell](image)

We model the capacitive load of each gate as:

\[
C_{load} = \frac{5}{2} C_{ox}
\]  

(B.0.1)

the current steering into the node as:

\[
\frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{DD} + V_{Tp})^2
\]  

(B.0.2)

the current steering out of the node as:

\[
\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{Tn})^2
\]  

(B.0.3)
Since node $IN$ is fed by a large current, we approximate $d_1$ and $d_2$ with the periods between the outer dashed lines. If all of the NMOS devices in the logic gates are sized as $W/L$ and PMOS devices as $K*W/L$, the delays can be predicted by:

$$d_1 = \frac{C_{load} \times V_{Tn}}{I_p} + \frac{C_{load} \times V_{Tp}}{I_n} = \frac{5L^2 \times (K+1) \times V_{Tn}}{\mu_p \times (V_{DD} - V_{Tn})^2} + \frac{5L^2 \times (K+1) \times V_{Tp}}{\mu_n \times (V_{DD} - V_{Tn})^2} \quad (B.0.4)$$

$$d_2 = \frac{C_{load} \times V_{Tn}}{I_p} + \frac{C_{load} \times V_{Tp}}{I_n} = \frac{5L^2 \times (K+1) \times V_{Tn}}{\mu_n \times (V_{DD} - V_{Tn})^2} + \frac{5L^2 \times (K+1) \times V_{Tp}}{\mu_p \times (V_{DD} - V_{Tn})^2} \quad (B.0.5)$$
Bibliography


