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Abstract

Power supply noise coupling represents a challenge in the design of current and future analog and mixed-signal circuits and systems. In this thesis, power supply noise coupling is analyzed at the circuit level. As a representative study, power supply noise coupling in a voltage reference is studied. The precision of a voltage reference circuit is critical to the performance of other analog and RF circuits. Therefore, there is much value in developing a deeper understanding of the mechanisms through which power supply noise coupling occurs in this fundamental analog and RF system building block. A model representing the amount of noise coupling in the frequency domain is developed and verified through circuit simulations. A practical design solution for increasing high frequency power supply noise rejection is identified and evaluated. Finally, the effect of technology scaling on power supply noise is studied in two successive CMOS processes.

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Chapter 1

Introduction

1.1 Voltage Reference

A voltage or a current reference is used in almost every chip design. It serves as the reference from which bias voltages and currents for other circuits are derived. The precision of this reference therefore, is critical to the overall performance of all analog and mixed-signal circuits. References must maintain a dc value that lies in an acceptable range in the presence of temperature variations, process variations, and other electromagnetic interference from noise sources.

The precision of a voltage reference with respect to temperature, process, and power supply variations is very critical to the performance of RF circuits and systems, too. Voltage references that deviate from their expected dc values can produce undesirable effects such as bit errors in analog-to-digital converters, non-linearity in RF mixers and low-noise amplifiers (LNA). As more circuits are integrated onto a single chip, controlling the precision of the designed reference becomes a more difficult, yet increasingly important task for chip and package designers.

1.2 Noise

Fig 1.1: *Example floorplan of chip with RF, analog and digital circuits.*

Integrating digital, mixed-signal, and radio-frequency (RF) circuits in a single chip and package as shown in Figure 1.1 creates many problems for circuit and system designers. Fast switching digital circuits create noise in both the power supply and the substrate (GND plane). Substrate noise couples through the substrate and onto the bulk terminal of transistors in analog circuits. Through the body effect, a small variation in the threshold voltage of transistors is produced, which can cause non-linearities in the victim circuit. Guard rings around sensitive analog circuits and substrates with higher resistivities help reduce the amount of substrate noise coupling.

Switching noise from digital circuits is another noise source analog circuits must contend with. As shown in Equation (1.1), the transient current created by fast switching

$$V_{REAL} = V_{DD} + L \left(\frac{dI}{dt} \right) - IR \quad (1.1)$$

digital circuits results in voltage fluctuations of the power supply. Analog circuits with poor power supply noise (PSN) rejection figures can be seriously affected by the presence of this noise. To reduce the effects of switching noise on the analog power supply, separate power supply planes are used for analog and digital circuits. This reduces the effect of digital switching noise on mixed-signal and analog circuits to an almost negligible level.

High frequency power supply noise in RF systems is created by noise injection from RF circuits. Mixed-signal and other analog circuits may share a common supply with RF circuits, making analog circuits susceptible to noise components from RF circuits. This interaction stresses the importance of high frequency noise rejection in mixed-signal and analog circuits and particularly in voltage references.

1.3 Organization of Thesis

In Chapter 2, power supply noise is further described. Previous work showing methods to reduce the amount of power supply noise coupling is presented. Further, a general overview of voltage references is provided in this section. Also, previous work on power supply noise attenuation in voltage references is presented. In addition, a system perspective driving the motivation for analyzing power supply noise in voltage references is presented.

In Chapter 3, a standard voltage reference circuit is analyzed in detail. A model representing the amount of power supply noise coupling has been developed. It is expected that development of the model will result in a better understanding of the mechanisms through which power supply noise coupling occurs for the chosen voltage reference. A method to reduce the power supply noise coupling is also presented.

The effect of technology scaling on power supply noise coupling will be analyzed in Chapter 4.

In Chapter 5, the findings of this research are summarized along with a look at future work in the area of power supply noise.

Chapter 2

Background

With continued scaling of supply voltages and increased integration, power supply noise becomes a major design concern for reference circuits. Power supply noise concepts and previous research relating to power supply noise are presented in this chapter. Also presented in this chapter are design parameters and circuit concepts relating to voltage reference design. A review of both power supply noise concepts and voltage reference design creates a more coherent development of the reason for studying power supply noise in voltage references.

2.1 Power Supply Noise

In early mixed-signal and analog designs, the major source of power supply noise was due to switching noise from digital circuits only. Further integration resulted in the addition of RF circuits onto the same chip, which contributed to an increase in power supply noise, particularly at higher frequencies. Device scaling and higher levels of integration are the main reasons for an increase in power supply noise. As devices are continually scaled, power supplies are reduced to maintain gate reliability and reduce power consumption. However, a lower supply voltage results in reduced noise margins in both digital and analog circuits. As more devices are integrated in a single chip or

package, more sources and sinks for power supply noise are packed closer together, all with varying degrees of sensitivity to power supply noise. This creates an environment which requires tighter control of power supply noise to ensure signal integrity of the most sensitive circuits.

There are many different solutions to controlling power supply noise. One of the most commonly employed solutions is to add decoupling capacitors both on and off chip; however, the use of this method in highly integrated designs has resulted in the uncovering of inefficiencies in cost and performance. Off-chip decoupling capacitors provide a reduction in power supply noise up to 100 MHz. Noise beyond 100 MHz must be decoupled on-chip or by other methods. In [1], a power supply noise aware floorplanning methodology is developed. Using the noise aware floorplanning approach compared to the current method of post-floorplan decoupling, a 21% reduction in the number of decoupling capacitors and a 40% reduction in the peak power supply noise has been demonstrated. In [2], early decoupling optimization is achieved through architecture level prediction. An equivalent RLC network, as shown in Fig. 2.1, models the power plane and the switching activity is simulated by current sources. Early power supply decoupling optimization therefore, is achieved by abstracting switching activity. This allows for quick optimization of the necessary on and off-chip decoupling solution.

Fig. 2.1: *RLC equivalent of power supply plane. Reprinted from [2].*

In [1], a power supply noise aware floorplanning algorithm is developed and in [2], an architectural level abstraction is used to optimize on-chip decoupling capacitor placement. Both papers imply that power supply noise must be considered in early design stages and show that early consideration of power supply noise can result in an improved decoupling solution. These papers however, do not extend the circuit models to include power supply noise effects in analog and RF circuits. For these algorithms to be applicable to mixed-signal and RF circuits, a method by which to model the effect of power supply noise on these circuits is required. The analysis of a voltage reference in Chapter 3 provides a detailed look on how to model power supply noise in a voltage reference. The developed model can be used as a quick method for determining the need of power supply noise rejection in highly integrated designs. Also, the analysis will

provide another example of how consideration of power supply noise in the early phases of circuit design can provide improved attenuation of power supply noise.

2.2 Voltage References

Voltage references can be designed in numerous topologies using many different process technologies. Almost all references are designed such that across process, temperature, and supply variations, the dc reference is kept within a specified range. This section will provide a description of methods used to design references with controlled dc variations.

2.2.1 Temperature Independence

The variation of a component value with respect to temperature is called its temperature coefficient (TC). For example a p+ poly resistor with silicide block has a TC between 160 to 200 ppm/°C [3]. The base to emitter voltage of a bipolar transistor has a negative TC and the thermal voltage ($V_T = kT/q$) has a positive TC [4]. By combining the two, an ideal reference with a near zero temperature coefficient can be designed. This circuit is called a bandgap reference. A simplified bandgap voltage reference is shown in Figure 2.2. The problem with a bandgap reference is that supply voltages continue to scale below the bandgap potential of silicon. 0.18 μm processes already use 1.8 V and

Fig. 2.2: *Bandgap reference circuit. Reprinted from [9].*

0.13 μm processes use 1.2 V. It is projected that the next technology node will reduce the supply even further to 0.9 V [5]. New design techniques are needed to extend the usefulness of bandgap references below 1 V operation. Nonetheless, the bandgap reference is still widely used and will continue to be used with more innovative circuit design techniques to overcome the reduction in power supply.

To digress a little, an example of how bandgap references are actually extended below 1 V is briefly presented. In order to reduce the produced voltage output below 1 V, resistive subdivision is used. The resulting circuit from [6] is shown in Figure 2.3. The amplifier in Figure 2.3 is biased through a self-biasing approach. The resistive

Fig. 2.3: *Sub 1 V bandgap reference circuit. Reprinted from [6].*

subdivision is achieved by resistors R_{2A1} and R_{2A2} and symmetrically by R_{2B1} and R_{2B2} .

The current, I , is defined by Equation (2.1). Where R_2 is the sum of R_{2A1} and R_{2A2} .

$$I = \frac{V_{BE2}}{R_2} + \frac{V_T \ln(N)}{R_1} \quad (2.1)$$

When mirrored to M3, the voltage reference is produced. The final equation is shown in equation (2.2).

$$V_{REF} = \frac{R_3}{R_2} \left[V_{BE2} + \left(\frac{R_2}{R_1} \ln N \right) \cdot V_T \right] \quad (2.2)$$

To determine the minimum supply voltage of the circuit in Figure 2.3, the voltage at N4 (or N3) is observed. The sum of the voltages across the two resistors R_{2B1} and R_{2B2} is

equivalent to the base-to-emitter voltage of Q2. At N2, the voltage can be written as a voltage division of the base-to-emitter voltage. Another factor to consider is that transistors M2 and M1 must be kept in saturation. Therefore, there must also be sufficient voltage to turn those transistors on. The final equation determining the minimum supply voltage is shown in Equation (2.3). It can be seen from Equation (2.3)

$$V_s(\text{min}) = \left(\frac{R_{2B2}}{R_{2B1} + R_{2B2}} \right) \cdot V_{EB2} + |V_{thp}| + 2|V_{DS(sat)}| \quad (2.3)$$

that the minimum supply voltage is highly dependent on the sizes of the resistors R_{2B1} and R_{2B2} (and R_{2A1} and R_{2A2}) [6]. Thus, the designer can minimize this by decreasing R_{2B2} .

2.2.2 Process Independence

Circuit designers have the least control over process variations. That is because mismatches occur as a result of “microscopic fluctuations in dimensions, dopings, oxide thickness, and other parameters that influence component values [7].” It is not uncommon to see 20% variations for on-chip passives and 10% variations on threshold voltages of MOS transistors across different process runs. On a single chip however, two resistors match to a tighter tolerance than what can be matched across different wafers. Therefore, it is common practice to use a ratio of passives for better matching of capacitors and resistors. According to a classic study by Pelgrom, the variance of the

threshold voltage of a MOS transistor is inversely proportional to the transistor area [8]. Therefore, better transistor matching can be realized at the cost of area.

Process variations are an inherent part of integrated circuit design and cannot be avoided. Often, however, variations are due to systematic statistical variations that can be accounted for through various layout techniques. A thorough discussion of layout matching techniques will not be discussed here, but a few important points will be emphasized as they pertain directly to the discussed voltage reference design and layout. For better matching of any component a single material should be used, widths should be kept constant, geometries should be kept identical, and orientation should be consistent for all components where matching is desired. For transistors in general, matched devices should be kept compact as possible to reduce vulnerability to gradients and where possible, common-centroid layouts should be used.

The final and most expensive way to reduce the effects of process variations, is to add post processing steps. Resistors and capacitors can be laser trimmed to achieve smaller tolerances. On-chip fuses can be programmed to allow for variability of passives by removing or adding components to change the net value. Redundant components on-chip however, require addition silicon area. Post processing steps therefore, are not preferred methods for component matching, but for some applications it may be the only way to obtain the desired precision.

2.2.3 Power Supply Independence

Supply independence is achieved by designing circuits that bias themselves. Self-biasing results in dc conditions that are independent of V_{DD} . In other words, V_{DD} will fall out from the resulting design equations. For example, the output voltage equation for the bandgap reference from Figure 2.2 shows no dependence on V_{DD} . This equation is shown in (2.4). Results similar to that in Equation (2.4) are highly desirable and achieved in various topologies, yet these first order results are somewhat misleading. For example,

$$V_{REF} = V_{BE1} + V_T \left(\ln \frac{A_{E1}}{A_{E2}} \frac{R_1}{R_2} \right) \left(1 + \frac{R_1}{R_3} \right) \quad (2.4)$$

Equation (2.4) does not include the effects of channel length modulation. In the bandgap reference, channel length modulation of the transistors in the op amp results in current variations; hence, producing voltage variations at the output reference.

So far V_{DD} was considered only as a dc source. However, today one has to start accounting for ac coupled noise. Noise on the power supply can couple onto the reference voltage, producing frequency dependent variations of the output. Power supply noise is a very critical factor when characterizing supply independence. The following section will consider noise on the power supply of a bandgap reference and will serve as an introduction to the analysis of power supply noise in voltage references in Chapter 3.

2.3 Power Supply Noise in Voltage Reference Circuits

In [9], the authors develop a thorough frequency domain analysis of the attenuation of power supply noise of various voltage reference topologies. Three of the four topologies however, require bipolar or BiCMOS based technologies. The fourth is a bandgap reference, which uses a *pnp* transistor, but can be fabricated in CMOS processes using an *n*-well as the base, a *p*+ region in the *n*-well as the emitter, and a *p*+ region over the *p*-type substrate as the collector. Since the analysis presented later focuses on CMOS processes, a summary of the analysis provided for a bandgap reference will be the only topology considered here.

The authors develop a small-signal model of the circuit from Figure 2.2. Because a bandgap reference makes use of an op amp, the small-signal model increases in complexity. Rather than creating a complex transistor-based small-signal model of the op amp, the authors chose to model the op amp with its output resistance and two voltage controlled current sources. The small-signal model used is shown in Figure 2.4. I_{dd} represents the gain from the supply line and I_D represents the differential gain. A further abstraction of the model is made by treating the system “as a feedback amplifier with an input noise [9].”

Fig. 2.4: *Small-signal model of bandgap reference. Reprinted from [9].*

The authors conclude with a frequency dependent expression that models the noise coupling for the bandgap reference. The final expression in [9] suggests that the supply rejection of the voltage reference depends heavily on the performance of the op amp. This makes it difficult to truly predict the expected noise attenuation without the use of a more complete model for the op amp. A full model of the op amp however, is difficult to obtain since the op amp architecture will vary for different applications. Nonetheless, within the limits of their assumptions, the analysis presented in [9] is valuable and provides a methodology with which to develop frequency-based power supply noise attenuation models for other voltage reference topologies.

2.4 Effect of Power Supply Noise Coupling In Pipelined Analog-to-Digital Converters

The primary motivation for analyzing the effects of power supply noise in voltage references is due to previous work in the design of a pipelined analog-to-digital converter

(ADC). As mentioned earlier, the precision of a voltage reference is critical to many different circuits, but greatly emphasized in the design of a pipelined ADC. In this section, a system perspective of power supply noise in a representative pipelined ADC design is described. This is achieved by demonstrating the effect of power supply noise in ADC's.

The first point of designing a pipelined ADC is to determine the number of bits of resolution and decide on the optimal number of pipelined stages. Many designs make use of the 1.5 bits per stage architecture. Therefore, a typical stage of this architecture is

Fig. 2.5: Typical stage of a pipelined ADC. Reprinted from [10]

analyzed. Figure 2.5 shows what a typical pipelined stage looks like. The important element of design to observe from Figure 2.5 is that a large number of dc voltages are necessary for a single stage of a pipelined ADC. The digital-to-analog converter,

depending on design, may require one or up to three different dc voltages. The focus however, will be on the comparator threshold voltages necessary to resolve the two bits per stage. A comparator with a fixed dc reference is found in almost all ADC architectures. Therefore, the following analysis can also be extended to other ADC architectures.

It is expected that a voltage reference with poor power supply noise rejection will result in a reference voltage with noise superimposed onto the dc output. A comparator with a noisy voltage reference can result in bit errors. The resulting bit errors are a function of the noise amplitude. To demonstrate that bit errors can result, a discrete time comparator is designed with a resolution of 8-bits. The input voltage is considered ideal, whereas the reference voltage, suffers from power supply noise coupling effects. To simulate a voltage reference with poor power supply rejection, a sinusoidal source with a dc offset is used. Figure 2.6 shows the schematic representing the test system. The input

Fig. 2.6: *Test system of comparator with a noisy voltage reference.*

voltage is 1.355 V and the voltage reference is 1.35 V with a 20 MHz noise coupled to it. Therefore, it is expected that the output bit should be a logic '1'. However, the noise amplitude on the voltage reference is purposely made large enough to go beyond the 1.355 V test input to demonstrate where errors may occur. In Figure 2.7 the bottom waveform shows the input reference under the influence of high amounts of power supply noise with poor rejection from a simulated voltage reference. The top waveform

Fig. 2.7: Output waveforms from test system.

shows the clock waveform and the middle waveform shows the resulting output bit. Observing the output bit waveform shows that an error occurs in one of the periods. It is important to note that the input voltage is sampled when the clock is low. The bit error

occurs in the third clock period. The other three periods however, result in valid outputs. Looking at the sampling times, it can be clearly observed that an error results based on the amplitude of the noise at the sampling instant. Therefore, bit errors are shown to be independent of noise frequency. This demonstrates that power supply noise at all frequencies can have an effect on the resulting output bit.

Bit errors in ADC's are much more complex than presented above. It is a non-linear function of input voltage, resolution, and full-scale voltage. Therefore, no attempt is made to model this effect. In general, however, power supply noise in a pipelined ADC can cause degradation in differential and integral non-linearity, which may result in missing codes in extreme cases. The reason for presenting the previous analysis is to demonstrate the importance of a robust voltage reference design. In particular, a voltage reference with high power supply noise rejection capability. Even in a complex ADC design, much of the burden of precision falls on the voltage reference alone. Therefore, understanding the effect of power supply noise in ADC's begins with understanding of power supply noise in voltage references.

2.5 Scope of Research

The main goal of this research is to gain a deeper understanding of power supply noise in analog circuits. A general voltage reference core is designed and analyzed to achieve this result. The other desired outcomes of this research are summarized below.

- To develop a frequency-based model to aid in locating critical transistor parameters when considering power supply noise coupling in analog circuits. An accurate model may serve as a method to quickly approximate the amount of noise coupling when developing a chip-level power supply noise decoupling solution.
- To determine the key transistor parameters and quantify their effects by relating them to power supply noise attenuation. This is done through circuit simulations.
- To develop a solution for improving power supply noise attenuation in the design of a voltage reference circuit.
- To quantify the effect of technology scaling on power supply noise coupling by designing the voltage reference in two successive CMOS processes. Also, to evaluate the effectiveness of the demonstrated solution in both technologies.

Chapter 3

Analysis of Power Supply Noise in a Threshold Voltage Referenced Voltage Reference Circuit

This chapter presents a thorough study of a threshold voltage referenced self-biasing voltage reference circuit. The design of and the effects of power supply noise on the described circuit will be studied in detail. A model describing power supply noise coupling in the frequency domain is also developed in this chapter.

3.1 Description of Circuit

Figure 3.1 shows the full schematic description of the voltage reference [11]. Transistors M_9 - M_{12} are used for startup only and will be discussed later in the design section. Transistors M_1 - M_8 and resistors R_1 and R_2 create the core of the voltage reference. The current produced by M_1 , in branch 1, is mirrored to both branch 2 and branch 3. Branch 2 is the branch containing resistor R_1 and branch 3 is the right most branch. Transistors M_4 , M_6 , and M_8 are identical in size, producing equal currents in all three branches. Resistor R_1 produces V_{GS1} , which sets the current in branch 1 and branch 2. Equation 3.1 shows how V_{GS1} is established. Since the voltage across R_1 is equivalent

Fig 3.1: Threshold voltage referenced self-biasing voltage reference circuit.

$$V_{GS1} = V_{TN} + \sqrt{\frac{2I_1}{\mu_n C_{OX} \left(\frac{W}{L}\right)}} \quad (3.1)$$

to V_{GS1} , Equation (3.2) can be written as follows.

$$I_2 R_1 = V_{GS1} \quad (3.2)$$

V_{REF} is created by mirroring the same current to branch 3, and dropping it across resistor R_2 . The resulting voltage reference equation is shown in (3.3). Combining equations

$$V_{REF} = I_3 R_2 \quad (3.3)$$

(3.2) and (3.3) however, results in equation (3.4). Equation (3.4) shows that the resulting

$$V_{REF} = V_{GS1} \left(\frac{R_2}{R_1} \right) \quad (3.4)$$

reference is a function of a ratio of resistors. As mentioned in section 2.2.2, a ratio of components provides better accuracy with respect to process variations. Further discussion regarding the layout and circuit design techniques used to minimize the effects of process variations will be discussed in the design and layout sections. Another desirable characteristic of the result given in (3.4) is that the produced voltage reference is independent of V_{DD} . At dc, this result is accurate. A reference designed for 1.25 V in a 2.5 V technology exhibits only a 0.7 mV increase and a 1.1 mV decrease when the supply voltage changes ten percent up and down, respectively. This is shown in Figure 3.2.

Fig. 3.2: Effect of changes in V_{DD} on output voltage.

Although at low frequencies robustness is exhibited by the voltage reference, high frequency noise components behave much differently and couple due to different

mechanisms. The effect of power supply noise on the output voltage will be modeled in section 3.3.1.

In Chapter 2, it was emphasized how it is important for a voltage reference to provide a stable dc reference in the presence of temperature variations also. Because a proprietary process is being used, the exact temperature coefficients for the threshold voltage and resistors are not available. Therefore, an estimate is necessary. If the size of M_1 is made large, the second term in (3.1) becomes small enough where the approximation in (3.5) would be almost true [11]. Using the assumption in (3.5) and

$$V_{GS1} \cong V_{TN} \quad (3.5)$$

substituting it into (3.4), results in (3.6). Equation (3.6) provides an easier estimate to

$$V_{REF} = V_{TN} \left(\frac{R_2}{R_1} \right) \quad (3.6)$$

obtain an equation representing the overall TC of the output voltage. Taking the partial derivative of (3.6) with respect to temperature results in (3.7a). Further simplifying

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{TN}}{\partial T} \left(\frac{R_2}{R_1} \right) + V_{TN} \frac{\partial}{\partial T} \left(\frac{R_2}{R_1} \right) \quad (3.7a)$$

(3.7a) results in (3.7b). Since both R_1 and R_2 are made of the same material, their TC's

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{TN}}{\partial T} \left(\frac{R_2}{R_1} \right) + \left(\frac{V_{TN}}{R_1^2} \right) \left[R_1 \left(\frac{\partial R_2}{\partial T} \right) - R_2 \left(\frac{\partial R_1}{\partial T} \right) \right] \quad (3.7b)$$

will be equal, resulting in equation (3.7c). The second term results in a relatively small

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{TN}}{\partial T} \left(\frac{R_2}{R_1} \right) + \frac{\partial R}{\partial T} \left(\frac{V_{TN}}{R_1^2} \right) [R_1 - R_2] \quad (3.7c)$$

value, therefore the overall TC can be estimated by (3.7d). Equation (3.7d) shows that

$$\frac{\partial V_{REF}}{\partial T} \cong \frac{\partial V_{TN}}{\partial T} \left(\frac{R_2}{R_1} \right) \quad (3.7d)$$

the overall TC of the voltage reference is dominated by the TC of V_{TN} , which is a negative value. This estimation is validated by Figure 3.3, which shows that an increasing temperature results in a reduction in the output voltage; hence, as equation (3.7d) predicts, the circuit has a negative TC.

Fig. 3.3: *Effect of temperature on output voltage.*

3.2 Design of the Voltage Reference

In order to properly size resistors and transistors, the desired output voltage must be known first. For this particular design, an output voltage of 1.25 V is targeted. Transistor M_1 and resistor R_1 are first sized to produce a given current. A current that is too low would require a large resistor at R_2 to produce 1.25 V, and a large current would

consume more power. Therefore, there exists a tradeoff between area and power consumption. A current of 100 μA is chosen which results in a moderately sized resistor at R_2 . The resistor size that results can be constructed using a $p+$ poly resistor with silicide block. M_4 , M_6 , and M_8 are sized to provide matching branch currents. They are made relatively large to provide better matching and to minimize the necessary overdrive voltage. Transistors M_3 , M_5 , and M_7 are sized to keep the transistors above them in saturation. M_5 is made slightly smaller than M_3 and M_7 , which are equal in size, to account for the difference in the V_{DS} of transistors M_4 , M_6 , and M_8 . Hence, providing better matching of the branch currents. The final sizes of all transistors and resistors are shown in Table 3.1. Although the channel lengths seem arbitrarily chosen at this time, a clearer understanding of why a channel length of 0.48 μm is chosen will be explained after providing the complete model for the power supply noise coupling for this reference circuit.

Component	Size
M1	25.2/0.48
M2	25.2/0.48
M3	131.04/0.48
M4	100.8/0.48
M5	120.96/0.48
M6	100.8/0.48
M7	131.04/0.48
M8	100.8/0.48
M9	5.1/0.3
M10	10.2/0.3
M11	4.8/0.3
M12	4.8/0.3
R1	6.233k Ω
R2	12.5k Ω

Table 3.1: *Table of component sizes and values.*

Transistors M_9 - M_{12} serve as a startup circuit and have no purpose during normal operation. The reason a startup circuit is needed is because the designed circuit has two stable operating points. This is explained by Figure 3.4. The non-linear current produced by M_1 intersects the linear current from branch 2 at two locations. If the gate of M_5 is at V_{DD} and the gate of M_2 is at ground at startup, then the operating current that

Fig. 3.4: Stable operating points of voltage reference. Reprinted from [11].

results can potentially be 0 A. In other words, the circuit is operating at point B. To correct this problem, M_9 “turns on and pulls the node upward toward point A [11].” Transistors M_9 - M_{12} are sized such that the gate to source voltage of M_9 is made small enough to sufficiently turn off during normal operation of the voltage reference.

3.2.1 Layout of the Voltage Reference

The layout of the voltage reference was done using Cadence's Virtuoso layout tool. Resistors are made using $p+$ poly with silicide block and can be seen on the bottom portion of Figure 3.5. The resistors are surrounded by substrate ties to reduce the effect of substrate coupling. To provide better matching, both resistors are laid out in a single direction and in the same area. The startup circuit transistors, M_9 - M_{12} , are located in the middle portion of the layout directly above the resistors. The final area of the voltage reference was $40\text{ }\mu\text{m}$ by $106\text{ }\mu\text{m}$.

Fig. 3.5: *Layout of voltage reference.*

3.3 Power Supply Noise Coupling Model

Developing a deeper understanding of the mechanisms through which power supply noise coupling occurs has many advantages. In particular, the circuit parameters that produce the greatest amount of coupling can be identified and minimized in early circuit design stages. An accurate model may serve as a method to quickly approximate the amount of noise coupling when developing a chip-level power supply noise decoupling solution. For these main reasons, a frequency domain mathematical model is sought and derived for this particular voltage reference circuit. The derivation and analysis of the model is presented in this section.

3.3.1 Derivation of Power Supply Noise Coupling Model

In order to develop a model for the noise coupled from the power supply to V_{REF} , small-signal equivalent circuits are used along with a few approximations. A small-signal equivalent circuit containing every small-signal parameter of all transistors would create a complex circuit, which would likely yield a complicated result. The latter would probably not be very helpful in getting insight into the key parameters that affect power supply noise coupling. Therefore, a few approximations are made and validated.

The first approximation relates to the noise coupled onto nodes V_1 and V_2 , shown in Figure 3.1. In order to determine the amount of noise coupled from the supply to both V_1 and V_2 , branch 2 is analyzed with branch 1 and 3 removed. The low-frequency small-

signal equivalent circuit of branch 2 is shown in Figure 3.6. Notice that body-effect is neglected, but channel-length modulation is not. M_5 and M_6 are diode-connected transistors; therefore, their small-signal equivalent reduces to a resistor with a value of $1/g_m$. Since Figure 3.6 is a low frequency equivalent model, the gate of M_2 can be approximated as being at ac ground.

Fig. 3.5: Low-frequency small-signal equivalent circuit of Branch 2.

Nodal analysis of the equivalent circuit is completed to obtain an expression representing the gain of the noise from the supply (V_N) to both V_1 and V_2 . Equations (3.8) through (3.10) show the resulting nodal equations at nodes V_1 , V_2 , and above R_1 , respectively.

$$V_1(g_{m5} + g_{m6}) - V_2(g_{m5}) - V_N(g_{m6}) = 0 \quad (3.8)$$

$$-V_1(g_{m5}) + V_2\left(g_{m5} + \frac{1}{r_{o2}}\right) - V_{R_1}\left(g_{m2} + \frac{1}{r_{o2}}\right) = 0 \quad (3.9)$$

$$-V_2\left(\frac{1}{r_{o2}}\right) + V_{R_1}\left(\frac{1}{R_1} + g_{m2} + \frac{1}{r_{o2}}\right) = 0 \quad (3.10)$$

Combining (3.10) and (3.9):

$$\frac{V_2}{V_1} = \left[\frac{x(g_{m5})}{x\left(g_{m5} + \frac{1}{r_{o2}}\right) - R_1\left(g_{m2} + \frac{1}{r_{o2}}\right)} \right] \quad (3.11)$$

$$\text{where } x = r_{o2} + g_{m2}r_{o2}R_1 + R_1$$

Substituting (3.11) into (3.8):

$$\frac{V_1}{V_N} = \frac{g_{m6} \left[x\left(g_{m5} + \frac{1}{r_{o2}}\right) - R_1\left(g_{m2} + \frac{1}{r_{o2}}\right) \right]}{\left[x\left(g_{m5} + \frac{1}{r_{o2}}\right) - R_1\left(g_{m2} + \frac{1}{r_{o2}}\right) \right] (g_{m5} + g_{m6}) - x(g_{m5})^2} \quad (3.12)$$

Substituting (3.11) into (3.12):

$$\begin{aligned} \frac{V_2}{V_N} &= \left(\frac{V_1}{V_N} \right) \left(\frac{V_2}{V_1} \right) \\ \frac{V_2}{V_N} &= \left[\frac{V_1}{V_N} \right] \left[\frac{x(g_{m5})}{x\left(g_{m5} + \frac{1}{r_{o2}}\right) - R_1\left(g_{m2} + \frac{1}{r_{o2}}\right)} \right] \end{aligned} \quad (3.13)$$

Equation (3.12) represents the gain from the supply to V_1 and (3.13) shows the gain from the supply to V_2 . When real-values for the small-signal parameters are substituted, both expressions reduce to approximately 1. Equation (3.12) reduces to 1.00128 and (3.13) reduces to 0.9986424. This shows that the noise on the power supply couples onto both nodes V_1 and V_2 in its entirety. This result was obtained for low frequencies, but simulations indicate that this approximation is also valid for high frequencies. Figure 3.7 shows the gain between the power supply and V_1 and V_2 from 10 Hz to 10 GHz. Since there is such a small amount of noise attenuation between the supply and both V_1 and V_2 , both nodes can be approximated by V_N for most of the shown frequency range. In order to simplify the small-signal equivalent of branch 3, this approximation will be used.

Fig. 3.7: Gain from V_N to V_1 and V_2 .

The result in (3.12) and (3.13) allow for branch 3 to be isolated from the rest of the circuit. This permits a simpler and more intuitive model to focus the investigation on. The full small-signal model for branch 3 is shown in Figure 3.8. Figure 3.8 again ignores body-effect. C_1 and C_2 in Figure 3.8 represent the sum of the drain to bulk and source to bulk junctions at the associated nodes. The model, as shown in Figure 3.8, is still not

Fig. 3.8: Full small-signal model of Branch 3.

simplified to the point where the resulting gain equation provides any insight into the power supply noise coupling mechanisms. Through simulations in SPICE and calculations in Matlab, it was determined that the most significant contribution of

coupling comes from the drain to bulk and source to bulk junction capacitances only. This result is obtained by iterating through the small-signal model and removing the parameters that have the least effect. Each time a parameter is removed, the resulting change is recorded. If the effect of removing the parameter results in a small change in the attenuation curve, then that parameter can be removed without compromising the accuracy of the model. Therefore, an even further simplified model can be obtained. The final small-signal model is shown in Figure 3.9.

Fig. 3.9: *Final simplified small-signal model of branch 3.*

Using Figure 3.9 and the approximations for V_1 and V_2 , an expression representing the gain of power supply noise from the supply to V_{REF} can be found. Nodal analysis of branch 3 will then result in a closed form expression modeling the noise attenuation between the supply and V_{REF} for the full reference circuit. Equation (3.14) and (3.15) show the resulting nodal equations for nodes V_X and V_{REF} respectively.

$$V_X \left(sC_1 + \frac{1}{r_{o8}} + \frac{1}{r_{o7}} + g_{m7} \right) - V_{REF} \left(\frac{1}{r_{o7}} \right) - V_N \left(\frac{1}{r_{o8}} + g_{m7} \right) = 0 \quad (3.14)$$

$$-V_X \left(g_{m7} + \frac{1}{r_{o7}} \right) + V_{REF} \left(sC_2 + \frac{1}{r_{o7}} \frac{1}{R_2} \right) + V_N (g_{m7}) = 0 \quad (3.15)$$

Solving (3.15) for V_X with respect to V_{REF} and V_N :

$$V_X = V_{REF} \left[\frac{sC_2 + \frac{1}{R_2} + \frac{1}{r_{o7}}}{g_{m7} + \frac{1}{r_{o7}}} \right] + V_N \left[\frac{g_{m7}}{g_{m7} + \frac{1}{r_{o7}}} \right] \quad (3.15)$$

Substituting (3.15) into (3.13) and solving for V_{REF} over V_N :

$$Num = s(C_1 g_{m7}) + g_{m7} \left(\frac{1}{r_{o8}} + \frac{1}{r_{o7}} + g_{m7} \right) - \left(\frac{1}{r_{o8}} + g_{m7} \right) \left(g_{m7} - \frac{1}{r_{o7}} \right)$$

$$Den = s^2 C_1 C_2 + s \left[C_1 \left(\frac{1}{R_2} + \frac{1}{r_{o7}} \right) + C_2 \left(\frac{1}{r_{o8}} + \frac{1}{r_{o7}} + g_{m7} \right) \right] + \left[\left(\frac{1}{R_2} + \frac{1}{r_{o7}} \right) \left(\frac{1}{r_{o8}} + \frac{1}{r_{o7}} + g_{m7} \right) - \left(\frac{1}{r_{o7}} \right) \left(\frac{1}{r_{o7}} + g_{m7} \right) \right] \quad (3.16)$$

$$\frac{V_{REF}}{V_N}(s) = \frac{Num}{Den}$$

Simplifying (3.16):

$$\frac{V_{REF}}{V_N}(s) = \frac{s(C_1 g_{m7}) - \frac{1}{r_o^2}}{s^2 C_1 C_2 + s \left[C_1 \left(\frac{1}{R_2} + \frac{1}{r_o} \right) + C_2 \left(\frac{2}{r_o} + g_{m7} \right) \right] + \left[\frac{2}{R_2 r_o} + \frac{1}{r_o^2} + g_{m7} / R \right]} \quad (3.17)$$

The result obtained in (3.17) is an important result that demonstrates that noise coupling for this circuit can be modeled with a closed form expression. Also, it shows that power supply noise coupling is independent of the transconductance of M_8 , but highly dependent on the transconductance of M_7 and the small-signal resistance of both transistors M_7 and M_8 . More importantly, (3.17) demonstrates that the transfer function contains one zero and two poles dependent on the capacitances C_1 and C_2 . This result suggests that the transfer function can be altered through various design “handles.” A change in channel length, transconductance, area of the drain and source junctions, or R_2 will result in a change in the gain of power supply noise between the supply and the output, V_{REF} . To aid in understanding the effect of the different parameters, a low-frequency expression is derived from (3.17). Equation (3.18) is obtained by assuming $s = 0$ in (3.17). From Equation (3.18), it can be concluded that the low frequency gain can be

$$\frac{V_{REF}}{V_N} = \frac{R_2}{g_{m7} r_o^2 + 2r_o - R_2} \quad (3.18)$$

adjusted by changing the transconductance or the channel-length. To simplify the discussion, it will be assumed that R_2 is fixed. This is because a change in R_2 would

require changes to the transistor sizes resulting in changes in the transconductance and the small-signal resistance values. From (3.18) it can be seen that an increase in channel length, with aspect ratios kept constant, results in an increase in the attenuation. In other words, a reduction in the noise coupling gain would result. Similarly, if channel length is kept constant and the aspect ratio of M_7 is increased, an increase in the attenuation can be seen; however, the increase in noise attenuation by changing the transconductance has a much smaller weight than when changing the channel length. Therefore, it is preferred that the circuit designer adjusts channel length to increase noise attenuation at lower frequencies.

Equation (3.18) shows a clear direction a circuit designer can follow to increase low-frequency noise attenuation, but a closer look at (3.17) shows that low-frequency noise attenuation is not gained without a cost. The equation for estimating the source to bulk and drain to bulk capacitances is given by (3.19) [4], where A is the terminal area and P is

$$C_{DB} = C_{SB} = AC_j + PC_{jsw} \quad (3.19)$$

the terminal perimeter. Increasing the transconductance and the channel length results in an increase in both the source/drain terminal area and perimeter. Therefore, C_1 and C_2 from (3.17) will be modified, resulting in a shift in the associated poles and zeros of the noise transfer function; hence, producing a change in noise attenuation at higher frequencies. The effect of changing the channel length on the full transfer function cannot be estimated by inspection. Therefore, it is necessary to use either a circuit simulator or Matlab to predict any changes that will result.

Because simulations provide quicker and more accurate results, investigating changes in channel length and its effect on noise attenuation has been done in SPICE rather than in Matlab. Before continuing with this analysis however, the noise attenuation predicted by the model and results from simulation will be compared. This is just to show that had a simulation engine not been available, the same analysis could be conducted in Matlab with accurate results. Figure 3.10 shows a plot of the noise attenuation from the model and from simulation. The transistor sizes and component values used are from Table 3.1. It can be seen that the model provides a more optimistic estimate of the noise attenuation in the frequency range 10 kHz to 100 MHz and a pessimistic estimate at lower frequencies. To account for this error, a small scaling factor, β , can be added to the

Fig. 3.10: Comparison of model to actual circuit simulation.

transconductance (g_{m7}) and another scaling factor, α , can be added in front of the capacitance, C_1 . Inserting the scaling factors results in the plot in Figure 3.11, which more accurately predicts the noise attenuation. The scaling factor α is between the range 2 and 3 and β is in the range 3 and 4. The accuracy of the model suggests that equation (3.18) can accurately serve as a quick method to predict the amount of power supply noise coupling in the designed voltage reference circuit.

Fig. 3.11: Comparison of model with scaling factors and actual circuit simulation.

3.3.2 Analysis of Power Supply Noise Coupling Model

The purpose of deriving the model in (3.17) and (3.18) was to provide a mathematical expression to aid in the identification of those transistor parameters which have the biggest impact on power supply noise rejection. Clearly from (3.18) it is seen that channel length has a direct impact on low-frequency attenuation. Changes to channel length also have an indirect impact on the high-frequency noise attenuation since the associated source and drain capacitances vary as transistor dimensions are changed. This is linked into equation (3.18). Viewing (3.18) from a control systems perspective suggests that varying the capacitance will modify the poles and zeros of the transfer function. Therefore, there exists a tradeoff between transistor channel length and power supply noise rejection. In order to better understand the effect of varying channel length on power supply noise rejection, circuit simulations are done where the channel length is varied while aspect ratios are held constant. Aspect ratios are kept constant so that the change in power supply noise rejection can be attributed to varying channel lengths only. A change in the aspect ratio would result in a change in the transconductance also. Using TSMC's 0.25 μm CMOS process, the designed voltage reference is redesigned with channel lengths from 0.24 μm to 2.4 μm , in 0.24 μm increments. All transistors, excluding the startup transistors, have the same channel length. The resulting plots of power supply noise coupling gain versus frequency for all designed channel lengths are shown in Figure 3.12.

Fig. 3.12: *Power supply noise gain vs. frequency for varying channel lengths for the voltage reference design in TSMC 0.25 μm CMOS process.*

There are a number of different conclusions that can be extracted from these plots. First, there is an obvious change in the power supply noise attenuation behavior as channel length is changed. Equation (3.18) predicts that low-frequency power supply noise will be further attenuated as channel length is increased. This prediction is verified in Figure 3.12. A nearly 20 dB increase in attenuation is achieved just by doubling the channel length from the minimum size of 0.24 μm to 0.48 μm . Another conclusion that can be made from Figure 3.12 is that, regardless of channel length, there is almost no noise attenuation beyond 100 MHz. After low frequencies, channel length has the greatest effect on noise rejection in the range 1 kHz to 100 MHz. This is a very important result since typically off-chip decoupling capacitors are used to provide noise

attenuation up to 100 MHz. A circuit designer then has the flexibility of trading off low frequency noise attenuation for greater attenuation in the range 1 kHz to 100 MHz. In this frequency range, increasing channel length degrades noise attenuation. This can be attributed to the fact that as channel length is increased, the first zero is shifted further to the left. This can easily be related back to (3.17). If the numerator in (3.17) is solved for s , the result is (3.19). As stated earlier, an increase in channel length will increase both C_1 and r_o ; therefore, quickly making the zero smaller.

$$s = \frac{1}{C_1 g_{m7} r_o^2} \quad (3.19)$$

In Chapter 2, it was stated that power supply noise could result from fast digital switching or RF circuits. Noise beyond 100 MHz therefore, is a major concern. From Figure 3.12 it can be seen that there is no noise rejection beyond 100 MHz. This is a major problem in making this voltage reference circuit a practical circuit in designs with high levels of integration and hence, high amounts of power supply noise. Therefore, a solution to reduce high frequency noise was sought.

3.3.3 Increasing Noise Attenuation

In order to increase the amount of noise rejection beyond 100 MHz, one of the poles from (3.17) must be shifted further to the left. Ideally, a full canceling of the zero would result. To understand how this may be done, the denominator of (3.17) is studied. The denominator is influenced by C_1 , C_2 , g_{m7} , R_2 , and r_o . R_2 will not be changed due to

reasons mentioned earlier. Changing channel length also causes r_o to change, but from 3.11 it is seen that this causes no improvement beyond 100 MHz. The only remaining parameters are C_1 and C_2 . Adding capacitance at either node will cause a shift in the pole; however, one node may require less capacitance than the other.

In order to understand the effect of adding capacitance at either node, an approximation to (3.17) is made. The squared term in the denominator of (3.17) can be assumed negligibly small, since it is simply C_1 and C_2 multiplied. Adding capacitance at one node would make the capacitance on the order of picofarads and the other capacitance is on the order of femtofarads. This results in a term that is on the order of 10^{-21} . Therefore, the assumption that the squared term can be neglected is justified.

Equation (3.20) shows the denominator of (3.17) after removing the squared term.

$$s \left[C_1 \left(\frac{1}{R_2} + \frac{1}{r_o} \right) + C_2 \left(\frac{2}{r_o} + g_{m7} \right) \right] + \left[\frac{2}{r_o} + \frac{1}{r_o^2} + \frac{g_{m7}}{R_2} \right] \quad (3.20)$$

Solving (3.20) for s shows clearly how C_1 and C_2 effect the resulting pole. This is shown in (3.21). In order to shift the pole further to the left, the denominator of (3.21) must be

$$s = \frac{\frac{2}{R_2 r_o} + \frac{1}{r_o^2} + \frac{g_{m7}}{R_2}}{C_1 \left(\frac{1}{R_2} + \frac{1}{r_o} \right) + C_2 \left(\frac{2}{r_o} + g_{m7} \right)} \quad (3.21)$$

increased. C_1 is multiplied by a smaller value than C_2 , therefore, increasing C_2 will have a greater effect than increasing C_1 . For the design with component values and transistor sizes listed in Table 3.1, C_1 is multiplied by 1.0863×10^{-4} , whereas C_2 is multiplied by

0.0018845. In order to have an equal pole shifting effect, the change in capacitance at C_1 would need to be an order of ten greater than the change in capacitance at C_2 .

According to (3.21) and the discussion above, a capacitance at C_2 will result in a pole shift and increased high frequency noise attenuation. The effectiveness of this solution however, can only be judged by the size of the capacitance needed. If a small capacitance can be placed on chip with a only small area tradeoff, then this solution would be satisfactory. In order to better quantify the effect of adding a capacitor at C_2 with different values, simulations have been conducted. The capacitance at C_2 is varied from 0 pF to 2.5 pF in increments of 0.5 pF. Figure 3.13 shows the resulting effect on the power supply noise attenuation with a fixed channel length of $0.48\text{ }\mu\text{m}$.

Fig. 3.13: *Power supply noise attenuation vs. frequency for voltage reference with varying capacitance values added at output node.*

From 3.13 it can be seen that the predicted effect that the pole will shift to the left does occur. Adding capacitance at C_2 has no effect on the power supply noise attenuation levels until approximately 10 MHz. By simply adding a 0.5 pF capacitor, a -10 dB change at 10 GHz occurs. A 2.5 pF capacitor, which provides -25 dB of noise attenuation at 10 GHz, is a very practical capacitance size that can be placed on-chip. Using a metal-insulator-metal (MiM) capacitor with an average unit capacitance of $1 \text{ fF}/\mu\text{m}^2$ would only require 0.0025 mm^2 of chip area. Compared to the layout of the circuit, this capacitance value would add approximately a 60% increase in the final layout area. The significant gain in power supply noise attenuation as well as its reasonable area requirement qualifies the capacitor solution as practical.

Chapter 4

Effect of Technology Scaling on Power Supply Noise Coupling

4.1 Power Supply Noise Coupling and Technology Scaling

As the semiconductor roadmap indicates, supply voltages will continue to reduce while transistors dimensions are scaled [5]. Power supply noise will become an increased problem for circuit and package designers as noise margins shrink and more circuits are integrated onto a single chip. In order for a circuit to be reused in a future technology node, it must maintain an acceptable amount of noise rejection. Degradation of the noise rejection figure would result in expensive redesigns or require additional methods with which to increase power supply noise attenuation. In this section, the effect of technology scaling on power supply noise coupling is analyzed. This is accomplished by comparing the voltage reference design in both TSMC's 0.25 μm and 0.18 μm CMOS processes.

4.1.1 Results from 0.18 μm Design

In order to compare the resulting performance with respect to power supply noise, the voltage reference from Figure 3.1 is redesigned using TSMC's 0.18 μm CMOS process. To maintain consistency between the two designs, aspect ratios used in the 0.25 μm design are approximately preserved in the 0.18 μm design. Table 4.1 shows the resulting transistor sizes and component values used for the redesigned voltage reference. The design is again made using a branch current of 100 μA and an output voltage of 1.25 V.

Component	Size
M1	40.32/0.36
M2	40.32/0.36
M3	70.56/0.36
M4	80.64/0.36
M5	60.48/0.36
M6	80.64/0.36
M7	70.56/0.36
M8	80.64/0.36
M9	5.1/0.3
M10	10.2/0.3
M11	4.8/0.3
M12	4.8/0.3
R1	5.046k Ω
R2	12.5k Ω

Table 4.1: *Table of component sizes and values for the 0.18 μm voltage reference design.*

Before presenting the simulated power supply noise coupling for the 0.18 μm design, a brief discussion predicting the behavior of the scaled voltage reference is provided. As transistor dimensions decrease, the associated parasitic capacitances decrease. The

drain/source to bulk capacitances in the 0.18 μm process scale down by nearly 55% when compared to the 0.25 μm process. The channel length modulation coefficients however, remain relatively constant. This means that the small-signal resistance (r_o) across both technologies stays relatively constant. There is a 50% increase in the value of the term $\mu_p C_{ox}$ when scaling down to the 0.18 μm process. This affects the transconductance (g_m) value, but as was described earlier, the transconductance has a very small influence on the overall noise attenuation both at low and high frequencies. Taking a look back at (3.18), the low frequency power supply noise gain equation, it can be concluded that there will be a minimal change between the two technologies at low frequencies. R_2 does not change, the small-signal resistance is held relatively constant, and the transconductance change has only a small effect on the denominator of (3.18); therefore, low-frequency power supply noise attenuation should remain relatively consistent between the two technologies. In looking at the high frequency power supply noise attenuation of the 0.18 μm design, it is necessary to look back at (3.19), which predicts the location of the zero. With an approximately 55% reduction in the capacitance per area of the source/drain to bulk capacitance, a shift to the right of the zero is expected; however, the 55% reduction in C_1 is offset by a 50% gain in the transconductance. Therefore, the expected result is that the zero for both technologies stays relatively consistent.

To verify the above predictions, the voltage reference is simulated using the 0.18 μm model file. This is shown in Figure 4.1. Comparison of Figure 4.1 with Figure 3.11 shows that the low frequency noise rejection for both technologies is very similar. Also

Fig. 4.1: *Power supply noise gain vs. frequency for varying channel lengths for the voltage reference design in TSMC 0.18 μm CMOS process.*

in agreement with the 0.25 μm design is that there is almost no noise rejection beyond 100 MHz. Even more important, the location of the zero for both designs remains in approximately the same position. As expected, increasing channel length results in an increase in low frequency power supply noise attenuation, but also a shift to the left of the zero.

Scaling to the 0.18 μm technology node produces no improvement in attenuating power supply noise beyond 100 MHz. Therefore, the same solution is tested: capacitance is added at the output node. Figure 4.2 shows the effect of adding capacitance to the output node. Power supply noise attenuation is plotted across frequency for capacitance values from 0 pF to 2.5 pF in increments of 0.5 pF. Adding only a 0.5 pF capacitor

Fig. 4.2: *Power supply noise attenuation vs. frequency for voltage reference with varying capacitance values added at output node.*

results in a -12 dB increase in attenuation. This result is very similar to results from the $0.25\ \mu\text{m}$ design. Slightly different from the previous design however, is that as the capacitance is gradually increased, greater noise rejection can be achieved in the $0.18\ \mu\text{m}$ design as opposed to the $0.25\ \mu\text{m}$ design.

4.1.2 Comparison of $0.18\ \mu\text{m}$ Design With $0.25\ \mu\text{m}$ Design

Table 4.2 shows a comparison of the effect of adding capacitance to the power supply noise attenuation at different frequencies. It also compares the value of power supply noise in both processes at different frequencies. Not clearly evident from Table 4.2 or the

simulated power supply noise attenuation graphs is the difference in the necessary capacitance to achieve a common level of power supply noise attenuation in both processes. For example, a power supply noise attenuation of -22 dB at 2 GHz in the $0.25\text{ }\mu\text{m}$ design requires 2 pF of capacitance on the output node, whereas only 1 pF is needed in the $0.18\text{ }\mu\text{m}$ design. This result is very desirable since a significant amount of chip area is gained without sacrificing any performance in terms of power supply noise attenuation.

Frequency	Gain in $0.25\text{ }\mu\text{m}$ Process (dB)		Gain in $0.18\text{ }\mu\text{m}$ Process (dB)	
	With No Cap.	With 2pF Cap.	With No Cap.	With 2pF Cap.
1kHz	-59.22	-59.22	-52.84	-52.84
100kHz	-49.55	-49.56	-51.14	-51.14
1MHz	-30.08	-30.21	-36.11	-36.23
10MHz	-10.4	-16.28	-16.31	-21.92
100MHz	0.52	-17.68	-0.47	-22.05
1GHz	-0.29	-21.06	-0.02	-27.9
2GHz	-0.27	-21.14	-0.40	-28.57
10GHz	-0.15	-21.07	-0.29	-28.62

Table 4.2: Comparison of power supply noise attenuation of the $0.25\text{ }\mu\text{m}$ and $0.18\text{ }\mu\text{m}$ designs.

Chapter 5

Conclusion

5.1 Conclusions

With increasing levels of integration and continuously scaled devices, controlling power supply noise will become a major design effort for both package and circuit designers. Switching noise from digital circuits and high frequency noise components from RF circuitry pose great risks to the signal integrity of analog circuits. In particular, a voltage reference output should be isolated as much as possible from power supply noise. This is because the achievable accuracy of a voltage reference is critical to the proper performance of many other analog circuits that reside in the same chip. Current design methods involve placing decoupling capacitors on the package and on-chip to reduce noise levels. Often, however, the number of decoupling capacitors is overestimated for the purpose of ensuring signal integrity. By studying relevant circuits, the mechanisms for power supply noise coupling can be better understood; hence, producing designs with more optimal noise performance and more cost efficient decoupling solutions. To better understand the mechanism of power supply noise in the voltage reference, a model was developed and studied. Also, the effect of technology scaling on the voltage reference was examined.

To begin the analysis, a frequency domain model of the power supply noise coupling in the voltage reference was developed. This model was used as a basis from which to mathematically predict, describe, and explain the resulting performance as seen through circuit simulations. Through simulations backed by the developed model, a number of conclusions can be drawn regarding the behavior of power supply noise in the studied voltage reference.

First, it was determined that there exists a tradeoff between low and high frequency noise rejection and channel length. Low frequency noise rejection increases as channel length is increased. Noise in the range 1 kHz to 100 MHz however, degrades as channel length is increased. Noise components beyond 100 MHz were not attenuated by the designed voltage reference regardless of channel length. Therefore, a solution to this was sought and developed. An on-chip capacitor was added to the output of the voltage reference to improve the attenuation of high frequency noise.

The second major contribution of this study deals with the comparison of two successive technology nodes and how power supply noise is affected. By designing the same voltage reference in two successive technology nodes, a direct comparison of power supply noise performance was made possible. Comparison of the two designs indicated that power supply noise coupling figures as well as solutions for power supply noise rejection remains consistent for both technology nodes. An important result from this study revealed that a smaller capacitance was needed in the 0.18 μm technology node to achieve the same result as a larger capacitance in the 0.25 μm node. In other words, better power supply noise rejection was achieved with less area used. This result

somewhat contradicts predictions that indicate that power supply noise problems will only worsen. Although power supply noise levels may increase due to increased integration, results from the study of this voltage reference show that a circuit's ability to reject power supply noise does not necessarily degrade as technologies scale.

5.2 Future Work

The model presented in this thesis, although accurate, never took into account the effects of body-effect on the overall transfer function. Nor did it ever consider the effects of substrate noise. Also, two scaling factors were necessary for curve fitting. An empirical rule or a physical derivation of the necessary scaling factors would provide more consistent modeling parameters. Fabrication of the designed voltage reference with real measurements would be the best method with which to determine the accuracy of the model in its current form. For further practicality, the study can be extended in a system environment where the voltage reference is actually buffered and distributed for use by other circuits. The system analysis would require an amendment to the developed model to account for added power supply noise while being buffered. The amended model however, would be a more useful model from which to develop global power supply noise modeling tools.

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Appendix A:

Fig. A1: *Comparator circuit used in analysis in section 2.4.*

Appendix B:

Fig. B1: Schematic of Voltage Reference Circuit.

Fig. B2: Layout.