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Rapid thermal processing of polysilicon emitter transistors

Diane Mauersberg

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Rapid Thermal Processing of Polysilicon Emitter Transistors

by
Diane Mauersberg

A Thesis Submitted
in
Partial Fulfillment
of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electrical Engineering

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Rochester, New York
February, 1994
Acknowledgements

The author would like to thank Dr. Renan Turkman, Dr. Lynn Fuller, Professor Rob Pearson, and Dr. Santosh Kurinec for their guidance with this project. The author is also grateful to Cornell University for the use of their facility for RTP and IBM for providing TEM analysis. Special thanks to Scott Blondell, Tom Grimsley and Paul Waldrop for their support and assistance with the fabrication equipment.
Abstract

The recent developments in rapid thermal processing in the past several years have shown it to have much potential in achieving full dopant activation of implanted junctions with a limited amount of junction depth movement. Its application to polysilicon emitter transistors allows for the formation of very shallow emitter-base junctions and narrow base widths with far greater activation capability than conventional furnace processes. A process for polysilicon emitter transistors utilizing rapid thermal annealing has been developed. Furnace processing at 875°C; and rapid thermal processing for 20 seconds at 950°C, 1000°C, and 1050°C was performed to anneal the emitter. Vertical npn transistors with emitter junctions of .1 to .2 microns and base widths smaller than .2 microns were fabricated. The resulting gains were as high as 392 with corresponding Early voltages of 165 volts. TEM analysis was also performed to show the effects of RTP.
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<td>$A_e$</td>
<td>Area of the emitter</td>
</tr>
<tr>
<td>$A_h, A_e$</td>
<td>Modified Richardson constant for holes and electrons</td>
</tr>
<tr>
<td>$BV_{CB}$</td>
<td>Breakdown voltage of C-B junction: $I_s = 0$</td>
</tr>
<tr>
<td>$BV_{CE}$</td>
<td>Breakdown voltage between C-E: $I_B = 0$</td>
</tr>
<tr>
<td>$BV_{BE}$</td>
<td>Breakdown voltage of E-B junction: $I_C = 0$</td>
</tr>
<tr>
<td>C</td>
<td>Heat Capacity</td>
</tr>
<tr>
<td>$D_{pE}$</td>
<td>Diffusion constant for holes in the emitter</td>
</tr>
<tr>
<td>$D_{nB}$</td>
<td>Diffusion constant for electrons in the base</td>
</tr>
<tr>
<td>$d$</td>
<td>Thickness of the wafer</td>
</tr>
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<td>$E_x$</td>
<td>Energy component perpendicular to oxide</td>
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<tr>
<td>$F_r, F_p$</td>
<td>Quasi-Fermi level for holes and electrons</td>
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<tr>
<td>$f_T$</td>
<td>Frequency at which beta equals unity</td>
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<td>$GN_B, GN_E$</td>
<td>Gummel number in the base and emitter</td>
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<td>$h_{FEO}$</td>
<td>Common-emitter current gain with no or an equal amount of bandgap narrowing in base and emitter</td>
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<tr>
<td>$I_{b,e,i}$</td>
<td>Base, collector, and emitter currents</td>
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<tr>
<td>$I_{CEO}$</td>
<td>Collector current with emitter open-circuited</td>
</tr>
<tr>
<td>$I_{CEO}$</td>
<td>Collector current with base open-circuited</td>
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<tr>
<td>$I_{PE}, I_{NE}$</td>
<td>Hole and electron current in the emitter</td>
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<tr>
<td>$\lambda$</td>
<td>Incident radiation intensity</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
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<tr>
<td>$J_d$</td>
<td>Drift-diffusion current density</td>
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<td>$J_{th}$</td>
<td>Thermionic emission current density</td>
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<tr>
<td>$J_p, J_n$</td>
<td>Hole and electron current density</td>
</tr>
<tr>
<td>$J_{pT}, J_{nT}$</td>
<td>Hole and electron tunnel current density</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann’s constant</td>
</tr>
<tr>
<td>$L_{pE}$</td>
<td>Hole diffusion length in the emitter</td>
</tr>
<tr>
<td>$m_h^*$</td>
<td>Effective hole mass</td>
</tr>
<tr>
<td>$m_i^*$</td>
<td>Effective mass in an insulator</td>
</tr>
<tr>
<td>$n_i$</td>
<td>Intrinsic free-carrier density</td>
</tr>
<tr>
<td>$N_A, N_D$</td>
<td>Impurity acceptor and donor concentration</td>
</tr>
<tr>
<td>$N_{Ae}$</td>
<td>Acceptor density in the base</td>
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<tr>
<td>$N_{DE}, N_{DC}$</td>
<td>Donor density in the emitter and collector</td>
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<tr>
<td>$N_{dmax}$</td>
<td>Peak doping level at the interface</td>
</tr>
<tr>
<td>$N_r$</td>
<td>Effective density of states</td>
</tr>
<tr>
<td>$P_{h}, P_{e}$</td>
<td>Hole and electron tunneling probability</td>
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<td>$q$</td>
<td>Electronic charge</td>
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<tr>
<td>$R$</td>
<td>Reflectivity of surface</td>
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<td>$R_e$</td>
<td>Emitter resistance</td>
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<td>$R_S$</td>
<td>Sheet resistance</td>
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<td>$S$</td>
<td>Effective recombination velocity</td>
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<td>$T$</td>
<td>Temperature</td>
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<td>$V_A$</td>
<td>Early voltage</td>
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<tr>
<td>$V_{BE}$</td>
<td>Base-emitter voltage</td>
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<tr>
<td>$V_{cB}, V_{CE}$</td>
<td>Collector-base and collector-emitter voltage</td>
</tr>
<tr>
<td>$V_j, VA$</td>
<td>Externally applied voltage</td>
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\[ \Delta V_{gE}, \Delta V_{gB} \] Bandgap narrowing in the base and emitter

\[ \Delta V_{p}, \Delta V_{n} \] Discontinuity for holes and electrons across the interfacial oxide

\[ V_L, V_R \] Potential barrier height left/right of oxide

\[ W_B, W_E \] Width of base and emitter

\[ X_E \] Width of the emitter

\[ X_{PEB}, X_{PBE} \] Base side depletion width on B-C, E-B junctions

\[ \alpha_\lambda \] Absorption coefficient

\[ \beta_{\max} \] Maximum common-emitter current gain

\[ \gamma \] Emitter efficiency

\[ \delta \] Thickness of the interfacial oxide layer

\[ \epsilon_{sl} \] Permittivity of silicon

\[ \eta \] Base-current non-ideality factor

\[ \mu_n \] Mobility of electrons

\[ \xi \] Difference between the quasi-Fermi level for electrons and the conduction band

\[ \rho \] Resistivity

\[ \rho_b \] Base sheet resistance

\[ \tau \] Auger lifetime

\[ \phi_{bi} \] Built-in potential

\[ \phi_b \] Potential barrier due to dopants at interface

\[ \phi_L, \phi_R \] Quasi-Fermi level separations

\[ \chi_b, \chi_e \] Potential barrier through the oxide for holes and electrons

\[ \psi_s \] Band bending in the monocrystalline region
1.0 Introduction

Doped polysilicon was first used as a diffusion source for shallow emitter junction formation by Takagi in 1972.\textsuperscript{1} The primary concern of this new approach to transistor formation was the creation of shallow junctions and enhanced transistor gains were not reported. It wasn’t until Graul et al. deposited a film of undoped polysilicon for the emitter contact, which was then implanted with arsenic atoms and annealed, that a significant increase in emitter efficiency and current gain was achieved.\textsuperscript{1,2}

Polysilicon emitters are now emerging as a technology to significantly improve the characteristics of bipolar integrated circuits. Traditional bipolar technology, despite its superior electrical characteristics of high speed and high driving capability, has suffered from low packing density, yield problems, and high power consumption.\textsuperscript{1} The use of self-aligned poly structures reduces the large distances between contacts which are responsible for parasitic capacitances.\textsuperscript{3} This reduction improves the packing density and switching speed. As the lateral dimension of the emitter is decreased, a reduction of the vertical dimension is essential as well. This requirement provides for process control in achieving thin base widths\textsuperscript{4} and decreasing the peripheral emitter-base capacitance, both desirable for speed
enhancement. At the same time a reduction of the vertical emitter dimension severely degrades the current gain. In conventional bipolar circuit process design there is a constant dilemma over the choice of base doping and base width. High gains are obtained with a low base doping and narrow base width. A minimum doping level, however, is required to prevent base punchthrough when the collector-base junction is reverse biased, and to prevent high values of base series resistance. Unacceptably, small magnitudes for Early voltages also occur with low base doping because a deeper penetration of the collector-base depletion width occurs. For this reason the normal range of acceptable base Gummel numbers is between $10^{12}$ and $10^{13}$ atoms/cm$^2$. With a requirement on the minimum range for the base doping, the base width is made small to create a shorter minority-carrier transient time across the base to enhance device speed. As the base width is decreased, however, the base doping again needs to be increased in order to prevent punchthrough. A compromise must, therefore, be made between the gain, Early voltage, punchthrough voltage, and speed.

The development of polysilicon emitter technology has allowed for the scaling of both the lateral and vertical emitter bipolar dimensions with high performance. In addition yield improvements are likely from the fact that emitter-base junction formation is made by diffusion from the polysilicon
into undamaged single-crystal silicon.\textsuperscript{2} The presence of the polysilicon contact has shown a clear increase in the common-emitter current gain for a very shallow emitter-base junction depth.\textsuperscript{1,2} The reasons for the increased gain have been a subject of debate for a number of years. The proposed theoretical models can basically be divided into those involving carrier transport through the polysilicon and those concerned with the barrier present from an interfacial oxide and/or dopant segregation at the interface. In the case of digital circuits where higher current gains are not a driving necessity, the enhanced current gain can be traded for an increase in the base doping for increased speed.\textsuperscript{3} These achievements are advantageous for the recent development of BiCMOS integrated circuits, which incorporate the benefits of both bipolar and CMOS technologies.

Rapid thermal processing, although still in its preliminary stages, is proving valuable for annealing such shallow implanted junctions. Measured results from a number of studies have shown that a greater amount of conductivity can be obtained for a given junction depth with RTP, compared to conventional furnace processes.

This project investigates the application of rapid thermal processing to polysilicon emitter transistors in order to develop a single-poly PET process at Rochester Institute of Technology. A separate well for the collector is used for
device isolation and six different base dopings are studied for the determination of an optimum integrated base. Electrical characterization along with transmission electron microscopy for structural analysis of the interfacial layer is performed.
2.0 Background

2.1 Polysilicon Emitter Transistor Structure

The conservation of design area has continued to be of great importance in VLSI technology. While oxide isolation techniques have reduced device size, the distances between the contacts within the devices themselves have still remained rather large.\(^3\) A considerable area of the device has been necessary to allow for mask overlay errors. These inactive areas can be held accountable for device parasitic capacitances and resistances that limit performance. Self-aligned structures, such as PET devices, serve as a solution to the problem.

Polysilicon contacted bipolar transistors can be classified into two distinct groups. Those which utilize the polysilicon to form just the emitter of the transistor belong to the family of single-poly PETs, while those that use a layer of polysilicon to contact the extrinsic base as well as a layer to contact the emitter are known as double-poly PETs.\(^1\) The self-alignment of the poly emitter contact with the emitter diffusion allows the metallization pattern to be offset from the contact.\(^6\) The amount of offset possible is of course limited by the allowable additional series resistance, but this feature is of value. Aluminum spiking of the emitter-base junction and electromigration failure is prevented in the
cases where the metallization is offset; and in the cases where the aluminum and the polysilicon are directly over the junction, spiking is also decreased since silicon from the polysilicon rather than the substrate moves into the aluminum.³

A single-poly npn PET is shown below in Figure 1. After the formation of the collector and base regions of the device, an emitter window is opened in the oxide above the base.

![Single-poly PET diagram](image)

**Figure 2.1 Single-poly PET**

*(after De Graaff and De Groot⁷)*

At this point there are a number of methods for obtaining a heavily doped n+ polysilicon layer over a shallow n-type monocrystalline emitter.⁷ In one method a layer of polysilicon is deposited and the dopant is diffused from the surface and through the polysilicon into the single-crystal
silicon. There is poor control of the impurity profile within the silicon using this method. Another method is in situ doping during the polysilicon deposition followed by a high temperature step to diffuse the dopant into the polysilicon. This technique, when the capability exists, results in very low values of poly sheet resistance which thus helps to yield low emitter resistance, often a major problem with PETs. A third means of obtaining the emitter structure is by conventional implantation of emitter impurities into the single crystal silicon prior to deposition of the polysilicon layer. The polysilicon is then implanted and annealed to drive the dopant atoms into the previously implanted emitter region. This method, however, does not avoid damage to the monocrystalline region from implantation. The most widely accepted means is direct deposition of undoped polysilicon followed by implantation and a thermal diffusion step to form the shallow emitter-base junction in the silicon. Either arsenic or phosphorous is used for the n-type dopant, with phosphorous showing a slightly greater reduction in the amount of recombination in the monocrystalline silicon over arsenic, which will in turn lead to higher gains. For any of the methods using polysilicon as a diffusion source a shallow junction is possible because dopants will diffuse rapidly through the grain boundaries of the polysilicon with dramatic decrease in diffusivity upon entering the monocrystalline
silicon.\textsuperscript{1} Formation of the junction by diffusion into the undamaged single-crystal silicon also has higher yields since it avoids defect generation created by the annealing of traditional implanted junctions.

Of significant interest, is the treatment of the polysilicon-silicon interface for any of the previously mentioned methods.\textsuperscript{8} If an HF dip and DI rinse are used just prior to polysilicon deposition a very thin native oxide layer of approximately 8 Å will be present at the interface. The use of an RCA clean, however, forms an interfacial oxide layer of around 14 Å. This intentionally grown oxide is possible because of the chemical oxidation of silicon in the hydrochloric acid/peroxide and ammonium hydroxide/peroxide solutions used in the RCA clean at low temperatures less than 100°C.\textsuperscript{1,3} Thermally grown oxides or thin thermal nitride layers are also suitable as interfacial layers. This interfacial layer is thought to act as a tunneling barrier to the minority carrier holes injected into the emitter, therefore lowering the base current.\textsuperscript{7} It is believed that the thicker oxides from the RCA clean, compared to the HF dip oxide, create a larger tunneling barrier and, therefore, an increase in current gain. This is just one of the theories behind the increased gains seen with PETs, that will be discussed in a later section.

A double-poly PET is shown below in Figure 2. In this
approach the emitter is self-aligned to the base contacts, which again reduces the total area necessary for the device.3

Figure 2.2 Double-poly PET
(after Tang9)

There are a number of fabrication schemes used for these devices. In some known processes the extrinsic base regions are formed by the diffusion of boron out of the p+ polysilicon. The intrinsic base is then formed by the means of implantation, and lateral diffusion causes the two base regions to make contact. A spacer oxide grows on the sidewalls of the polysilicon, which determines the distance between the base and emitter contacts. The emitter can then be formed with a second layer of polysilicon by one of the previously mentioned methods.
2.2 Electrical Characteristics

2.2.1 Performance Necessity

With the lateral scaling of bipolar devices to below a micron there is a need to decrease the vertical dimension as well. The underlying reason for this is the emitter-base capacitance, which is comprised of the capacitance between the emitter and base planes in combination with the capacitance of the periphery. This peripheral component, which is highest at the surface, needs to be as small as possible. As the emitter base junction depth is reduced, however, it becomes close to the hole diffusion length, \( L_{pE} \), in the emitter. Very little recombination will then occur causing a steep, linear hole distribution in the emitter. This is illustrated in Figure 2.3.

![Minority Hole Distributions](image)

Figure 2.3 Minority Hole Distributions
(after Ashburn²)

The base diffusion current is proportional to the gradient of
this distribution. If a constant doping density in the emitter is assumed and heavy doping effects are neglected for simplicity, this current can be expressed as:

\[ I_b = qA_e n_i^2 \frac{D_{pe}}{N_{dE} X_E} (e^{\frac{qV_{BE}}{kT}} - 1) \]  

(2.1)

where \( A_e \) is the area of the emitter, \( D_{pe} \) the diffusion constant for holes in the emitter, \( N_{dE} \) the donor density in the emitter, \( X_E \) the emitter width, and \( V_{BE} \) the voltage across the base-emitter. An increase in the gradient will, therefore, cause an increase in the base current.

The common-emitter current gain of a bipolar junction transistor is expressed as a ratio of the collector current to the base current.

\[ \beta = \frac{I_c}{I_b} = \frac{G_{NE} D_{pe}}{G_{NB} D_{pE}} \]  

(2.2)

\( G_{NB} \) and \( G_{NE} \) and \( D_{pB} \) and \( D_{pE} \) are the Smedel numbers and the minority carrier diffusion constants in the base and emitter respectively. It is easily realized that a reduction in the base current is beneficial to circuit performance.

The base current of a bipolar junction transistor is essentially comprised of four component currents:

1. the recombination current in the base region itself,
(2) the recombination current in the space charge region of the emitter-base junction,
(3) the recombination current in emitter region, and
(4) the recombination at the silicon surface or contact.
For state of the art transistors where the base width is designed to be quite small to limit recombination, and hence the first component should be minimal. The second component is important at low injection levels. Recombination in the emitter region, the third component, is controlled by the doping level, bandgap narrowing, and hole lifetime in the emitter. For shallow emitter transistors, the final component, surface recombination has a significant influence on the base current.

Referring again to Figure 2.3, the addition of a polysilicon contact has the effect of extending the length of the emitter and thus decreasing the hole profile in the emitter and the base current. In reality the hole density gradient is not linear due to the characteristics of the interface and the polysilicon transport. This yields an even shallower hole profile, resulting in enhanced gain.

Related to the $\beta$ is the emitter efficiency, $\gamma$, which measures the ability of the emitter to inject electrons into the base of the transistor to be received by the collector.
\[ \gamma = \frac{I_{BE}}{I_{nE} + I_{pE}} \approx \frac{1}{1 + \frac{G_N D_{PE}}{G_N E D_{nB}}} \] (2.3)

\( I_{nE} \) is the emitter electron current and \( I_{pE} \) emitter hole current passing through the emitter-base junction. The approximation is only valid if heavy doping effects in the emitter are neglected. In reality heavy doping effects decrease the effective emitter Gummel number, thus reducing the achievable emitter injection efficiency. For a polysilicon emitter, the barrier created at the interface blocks the flow of holes into the emitter yielding a higher emitter efficiency.

A reduction in the emitter depth is, therefore, possible without sacrificing performance. The specific mechanisms behind the gain enhancement are more complex than described here and are discussed in a following section.

### 2.2.2 Comparison to Conventional BJT

The electrical characteristics of polysilicon emitter transistors differ from conventional bipolar junction transistors in a number of ways. These are namely, an increased common-emitter current gain, nonlinear base and collector currents (double "kinks") in relation to base-emitter voltage,
lower temperature sensitivity of current gain, higher emitter resistances, and better frequency performance.\(^1\)

The current gain for devices contacted using three different methods is shown in Figure 2.4. As can be seen the polysilicon contact exhibits much higher gains. Gains as much as seven times greater than BJTs with standard contacts have actually been reported.\(^{12}\)

![Figure 2.4 Current Gain in Relation to Collector Current](image)

**Figure 2.4 Current Gain in Relation to Collector Current**

*(after Ning and Isaac\(^{12}\))*

A Gummel plot illustrating the double "kinks" is shown in Figure 2.5. The nonlinearity at high \(V_{b,e}\), usually attributed to standard high level injection effects, is more severe than in a conventional BJT.
The emitter resistance, $R_E$, for a polysilicon contact has two addtional components compared with the traditional BJT.\(^{14}\)

$$R_E = R_{\text{metal-contact}} + R_{\text{poly-emitter}} + R_{\text{interface}} + R_{\text{mono-emitter}} \quad (2.4)$$

The major contributers to the overall resistance are the resistance present from the metal contact and the interface. While the interface may be beneficial in reducing the base current, it hinders majority carrier electron transport into the base, increasing the emitter resistance and degrading circuit drivability.

Higher switching speeds with $f_T$'s as high as 30 GHz have been achieved using PETs.\(^{7}\) This is usually attributed to a narrow base width and a smaller emitter-base capacitance.
2.2.3 Polysilicon Emitter Models

There has been a great deal of discussion over the exact mechanisms responsible for the remarkable increase in current gain and other electrical peculiarities. One of the first proposed explanations was smaller bandgap narrowing in the polysilicon film. Graul et al. first observed that the current gain of PETs showed a smaller degree of sensitivity to temperature compared to conventional BJTs. They reasoned that since the major contributor to sensitivity of current gain to temperature is traditionally a larger amount of bandgap narrowing present in the more heavily doped emitter compared to the base, bandgap narrowing in polysilicon must somehow be different. For the same amount of doping, polysilicon should show a lesser degree of narrowing than single crystal silicon of the same doping level. If the emitter and base both have uniform doping profiles then the current gain for the PET device can be expressed as:

\[ h_{FE} = h_{FE0} \exp \left[ q \frac{(\Delta V_{gE} - \Delta V_{gB})}{kT} \right] \]  

(2.5)

where \( h_{FE} \) is the gain with an equal or no amount of bandgap narrowing present in the emitter and base. \((\Delta V_{gE} < 0)\) and \((\Delta V_{gB} < 0)\) represent the bandgap narrowing in the emitter and base.
respectively. Graul et al. plotted the results of log current gain as a function of inverse temperature. The slope revealed that the PETs had a $|\Delta V_{gs} - \Delta V_{gb}|$ 26 mV smaller than the conventional bandgap narrowing of 70 mV. The conclusion was, therefore, that a smaller amount of bandgap narrowing occurs in the polysilicon.

Since this time a number of models have substantially questioned the basis for Graul et al.‘s argument. These proposed theoretical models can be generally separated into two groups. The first of these groups are those models based on barrier theories comprised of either thermionic emission or tunneling over oxide films or doping segregation present at the interface, while the second are those based on the transport of the carriers through the polysilicon film. The models discussed are not broken out into these groups, but are instead organized in such a manner as to preserve chronological order of events.

The first of these barrier theories created as an alternative to Graul et al.‘s theory is De Graaff and De Groot’s ‘tunnel emitter’ model. Previous research by Seto on polysilicon films showed that the majority of the dopant atoms lie inside the grains of the polysilicon and not along the grain boundaries. De Graaff and De Groot, therefore, emphasized that the emitter doping ($10^{20}$ cm$^{-1}$) of Graul et al.‘s PETs was high enough to disregard any significant decrease in
bandgap narrowing. Instead, they proposed the existence of a thin interfacial oxide layer between the single crystal emitter and the polysilicon. This layer should behave as a tunneling barrier to carriers. The additional observation of a pile-up of dopant phosphorous atoms at the interface led De Graaff and De Groot to the belief that the doping level in the emitter had to be degenerate. The structure and band diagram for their proposed model is shown in Figure 2.6.

Figure 2.6 Tunnel Emitter Model Structure/Band Diagram
(after De Graaff and De Groot7)
The phosphorous-doped polysilicon is represented by $W_1$, the phosphorous-doped n+ monocrystalline emitter by $W_2$ and the base by $W_b$. The interfacial oxide layer is shown with a width of $\delta$ (20-30 Å). $F_n$ and $F_p$ represent the quasi-Fermi levels with discontinuities of $\Delta V_n$ and $\Delta V_p$, which occur across the oxide layer. The n+ regions, with $F_n$ lying above the conduction band edge, are assumed to be degenerate. Holes and electrons traveling through the oxide will see a potential barrier of $\chi_b$ and $\chi_e$ respectively. Band bending in the monocrystalline region is denoted by $\psi_s$. The externally applied voltage, $V_{be}$, to the device is then the sum of the externally applied voltage $V_e$ and $\Delta V_n$. As can be seen the bands bend downwards at the interfaces of the oxide.

If one assumes that carriers travel through the interfacial oxide by tunneling then the hole tunnel current can be obtained by

\[ J_{\mu T} = \frac{4\pi q m_{th}}{h^3} \int_{-\infty}^{E_x} dE \left( f_1(E) - f_2(E) \right) \int_{-\infty}^{0} P_h(E_x) dE_x. \quad (2.6) \]

In this equation the Fermi-Dirac distribution functions for the holes in both regions are represented by $f_1$ and $f_2$. $P_h$ is the hole tunneling probability, $m_{th}$ is the effective hole
mass, and $E_z$ is the total energy component perpendicular to the oxide layer. Using Boltzmann statistics for the minority carriers in the emitter Eq. (2.6) was approximated to be

$$J_{pt} = q \sqrt{\frac{kT}{2\pi m^*}} \frac{P_h}{N_{D_2}} n_{i_2}^2 \exp\left(\frac{q}{kT}(V_f - \psi_s)\right).$$

(2.7)

$N_{D_2}$ is the impurity concentration at the interface between the monocrystalline silicon and the oxide film with the intrinsic carrier concentration at this same interface being $n_{i_2}$. The hole tunneling probability is a function of the oxide thickness and the barrier height for holes.

$$P_h \approx \exp\left(-\frac{4\pi\delta}{\hbar}\sqrt{2m^*g\chi_h}\right) \approx \exp(-\delta\sqrt{\chi_h})$$

(2.8)

If region $W$ is kept less than .1 micron recombination in that monocrystalline part of the emitter will be negligible and the tunnel current is equal to the injected hole current coming from the base,

$$J_{pt} = \frac{q n_{i_2}^2 \phi D_p \theta}{G_e} \exp\left(\frac{qV_f}{kT}\right)$$

(2.9)

where $G_e$ is the Gummel number in the emitter,
\[ G_e = \frac{N_p}{P_h} \sqrt{\frac{2\pi m_n^*}{kT}} \exp\left(-\frac{q}{kT}(\Delta V_{g2} - \Psi_s)\right) \]  

(2.10)

and the bandgap narrowing in the emitter \( \Delta V_{g2} \) is

\[ \Delta V_{g2} = \left(\frac{kT}{q}\right) \ln\left(\frac{n_{i2}}{n_{i0}}\right)^2. \]  

(2.11)

Similarly the electron current density is given by

\[ J_n = \frac{q n_{i2}^2}{G_b} \exp\left(\frac{qV_j}{kT}\right). \]  

(2.12)

where the base Gummel number, \( G_b \), is

\[ G_b = \int_0^{\psi_b} \left(\frac{n_{i0}}{n_{i_b}}\right)^2 \frac{N_A}{D_n} \, dx. \]  

(2.13)

Expressing \( G_b \) in terms of the base sheet resistance, \( \rho_s \), and the base bandgap narrowing the dependence on temperature can be seen.

\[ G_b = \text{const} \frac{\rho_s}{T} \exp\left(-\frac{q\Delta V_{gb}}{kT}\right) \]  

(2.14)
The maximum current gain is then

\[ h_{FE,\text{max}} = \frac{G_0}{G_b} = \text{const} \frac{V_T}{\rho_b} \exp\left( -\frac{q}{kT} (\Delta V_T - \Delta V_b - \psi_s) \right). \]

(2.15)

From Eq. (2.15) it was, therefore, concluded by De Graaff and De Groot that surface bending \( \psi_s \) is the reason for the decreased sensitivity of current gain to temperature. The enhanced current gains were attributed to the reduced hole tunneling probability created by the interfacial oxide. Experimentally determined values for \( P_h \) were found to range from \( 10^{-2} \) to \( 10^{-3} \). These small values reduce the base current to cause a significant increase in \( h_{FE} \). It should be noted that the interfacial oxide layer also causes a decrease in the electron tunneling probability \( P_e \) and hence an increase in emitter resistance, which is detrimental to device performance.

Soerowirdjo and Ashburn have also consistently supported this theory through experimental data. Devices fabricated using an HF dip prior to polysilicon deposition continually showed base currents larger than those of identically processed devices, except for the replacement of the HF dip with an RCA clean. The ‘tunnel emitter’ model, however, did not consider any of the effects due to interface traps, and recombination at the interface or in the monosilicon. It also
failed to explain the nonlinear I-V characteristics seen with thick interfacial oxides.

Ning and Isaac did not refute the existence of an interfacial oxide, however, they believed that its effect on the common-emitter current gain would be minimal assuming it to be rather transparent to minority carrier holes. Instead, they proposed that the transport of holes in the n+ polysilicon film is different from the transport in n+ silicon with their 'two-region' model.

Three different methods for contacting silicon npn bipolar transistors as shown in Figure 2.7 were investigated.

Figure 2.7 Three Types of Emitter Contacting Schemes
(after Ning and Isaac⁴)
Identical processing was performed up to the contacting of the shallow 200 nm deep emitter. At this point Al contacts were formed by deposition, Pd$_2$Si + Al contacts through deposition and reaction with the silicon, and n+ polysilicon + Al contacts by deposition of n+ polysilicon followed by a 900°C heat cycle. No intentional interfacial oxide was grown and the same 900°C heat cycle was also performed for the first two contacting schemes prior to contact formation.

Nearly ideal I-V characteristics were measured for all devices, leading to the assumption that no significant oxide layer was present between the polysilicon and monosilicon. Comparison of the common-emitter current gain for Al and Pd$_2$Si + Al devices showed a 25 percent lower gain for Pd$_2$Si + Al contacts. This was attributed to a reduction in the effective monosilicon emitter depth due to the silicon consumed during the formation of the silicide. The decrease in gain is understandable because as the emitter-base junction depth is reduced the hole diffusion length ($L_z = .4$ µm) in a heavily doped emitter becomes larger than the emitter width. In this instance, very little recombination occurs in the emitter with the hole distribution being linear, which results in a large hole current density, $J_{p0}$.
In contrast, however the n+ polysilicon + Al contacted devices exhibited current gains several times larger than Al or the Pd₂Si + Al contacted devices.

Ning and Isaac's 'two region' model is shown in Figure 2.8.

\[ J_{po} = \frac{qD_p N_i^2}{N_D W_E} \]  
(2.16)

**Figure 2.8 Two Region Model for Shallow Emitters**

*(after Ning and Isaac*)

The hole tunneling probability was considered to be 1 with δ
equal to 0 to represent an interface transparent to carriers. The ideal hole current density as a function of the emitter Gummel number is expressed as

$$J_p = \frac{q n_i^2}{G_e} \exp \frac{q V_{BE}}{kT}$$

(2.17)

The ratio of the common-emitter current gain for a device with a polysilicon thickness of $W_i$ to one with a thickness of 0 can be related to the emitter Gummel number as shown.

$$K = \frac{G_e(W_i)}{G_e(W_i=0)} = \frac{\beta(W_i)}{\beta(W_i=0)}$$

(2.18)

The hole currents in region I and II are expressed in Eq. (2.19) and (2.20).  

$$J_{p1} = \frac{q D_{p1} p_1}{L_{p1}} \frac{\frac{1}{2}}{\tanh(W_{p1}/L_{p1})}$$

(2.19)

$$J_{p12} = q D_{p2} \frac{(p_{12} - p_1)}{W_{e2}}$$

(2.20)
Solving for the hole distribution with \( L_{p2} > W_2 \) such that \( D_p \frac{d p_n}{d x} \) is continuous at the interface yields \(^4\)

\[
K = 1 + \frac{D_{p2} L_{p1}}{D_{p1} W_2} \tanh \frac{W_1}{L_{p1}}
\]

(2.21)

\[
K = 1 + \frac{D_{p2} L_{p1}}{D_{p1} W_2} \text{ for } W_1 > L_{p1}
\]

(2.22)

It can be seen that if the hole diffusion constant \( D_p \) is significantly smaller in the n+ polysilicon compared to the silicon then the ratio \( K \) will be greater than 1. The hole diffusion constant is related to the mobility through Einstein's relation.

\[
D_p = \left( \frac{kT}{q} \right) \mu_p
\]

(2.23)

Ning and Isaac, therefore, believed that their experimental findings could be explained by a hole mobility that was smaller in the n+ polysilicon than in the n+ monosilicon. The mobility in polysilicon films has been shown to be a function
of the grain size, grain boundary scattering, and heavy dopant concentration in the film by other sources. Actual majority carrier Hall mobilities in polysilicon versus silicon are significantly different.

The consideration of the insensitivity to temperature discovered by Graul et al. was explained by the temperature dependence of the diffusion length.

\[ L_p = \sqrt{kT \mu_p \tau / q} \]  

(2.24)

If the Auger recombination, \( \tau \), and the mobility in silicon, at high dopant concentrations are independent of temperature, the diffusion length should decrease with decreasing temperature. Recombination would then increase in the monocrystalline emitter and at the interface. PETs and conventional BJTs should have about the same gain at lower temperatures, but as the temperature is increased the importance of recombination in the n+ monocrystalline emitter for PETs will decrease and they will appear less sensitive to temperature. Additionally, a comparison of identically processed devices contacted by two different thicknesses of polysilicon showed a higher base current for the thin-polysilicon devices. This dependence on thickness showed clearly that the enhanced gain is not solely influenced by the interface, but by transport properties of
the polysilicon as well.

The 'two region' model does not consider the difference in doping concentrations between regions I and II, and recombination at the silicon-polysilicon interface. Its explanation of current gain dependence on diffusion length is somewhat qualitative. It should also be noted that these devices did not exhibit the nonlinear Gummel plots characteristic of polysilicon emitter transistors with interfacial oxides.

In an attempt to combine several of the proposed effects into one model Eltoukhy and Roulston proposed a 'unified PET' model with the band diagram shown in Figure 2.9.
$J_{nT}, J_{pT}$: Electron and hole tunnel currents, respectively.

$J_{rn}, J_{rd}$: Net recombination current in the neutral region of the emitter and in the e-b space charge region.

$J_{rg}, J_{rb}$: Net recombination current at the grain boundary and net recombination current in the bulk of the grain.

$J_c, J_b$: Collector and base current density, respectively.

**Figure 2.9 Energy Band Diagram for Unified PET Model**

*(after Eltoukhy and Roulston)*

The minority and majority tunneling currents $J_{pT}$ and $J_{nT}$ were first derived.

$$J_{pT} = A_h T^2 e^{-(E_g - \xi)/kT} \frac{e^{-bh}}{1 - C_h kT}$$

$$* \left[ \exp \left( \frac{qV_R}{kT} + \frac{q\Phi_R}{kT} + \frac{qC_h V_o}{2} \right) - \exp \left( \frac{qV_L}{kT} + \frac{q\Phi_L}{kT} - \frac{qC_h V_o}{2} \right) \right]$$

(2.25)
\[ J_{nT} = A e^{T^2 e^{-t/kT} \frac{e^{-be}}{1-C e^{kT}}} \]
\[
* \left[ \exp \left( -\frac{qV_L}{kT} + \frac{qC_eV_o}{2} \right) - \exp \left( -\frac{qV_R}{kT} - \frac{qC_eV_o}{2} \right) \right]
\]

(2.26)

The quantities \( b_n \) and \( C_n \) are found by

\[ b_n = \frac{4\pi\delta}{h} \sqrt{2m^*_iN_n} \]
\[ C_n = \frac{2\pi\delta}{\hbar} \sqrt{\frac{2m^*_i}{N_n}} \cdot \]

(2.27)

The values \( b_s \) and \( C_s \) are found in a similar manner where \( m^*_i \) is the effective mass in an insulator. In Figure 2.9 and Eq. (2.25) and (2.26), \( A \) is the modified Richardson constant, \( V_L \) and \( V_R \) are the potential barrier heights in the depletion regions just to the left and right of the interfacial oxide, \( V_o \) is the voltage drop across the oxide, \( \xi \) is the difference between the quasi-Fermi level for electrons and the conduction band, and \( \phi_L \) and \( \phi_R \) are the quasi-Fermi level separations.

Corresponding equations were written for recombination currents in the monocrystalline and polysilicon regions, taking into account the number of grains, grain size, and density of states at the grain boundary in the polysilicon.
film, as well as the fixed charge at the interface. Eltoukhy and Roulston assumed that the grain boundaries were infinitely thin. They considered the effects of a smaller minority carrier mobility in the polysilicon due to carrier trapping at these boundaries.

Through the consideration of hole and electron current continuity, Eltoukhy and Roulston solved for the voltage across the oxide, \( V_o \), for a given doping profile, oxide thickness, and polysilicon thickness. The complexity of their equations required the use of a fast, numerical program. In general, for polysilicon devices with no oxide interface, the dominant mechanism influencing the injected base current was the transport in the polysilicon, while for devices containing reasonable oxide thicknesses less than 60 Å, tunneling through the oxide and transport through the silicon were the determining factors. If the supply of holes at the interface is small the current was found to be controlled by transport in the silicon emitter and if the supply was large the limiting factor was tunneling. For very thin oxides less than 20 Å the polysilicon thickness was found to determine the current gain, showing the influence of the transport mechanism in the polysilicon. It was also found that for oxide thicknesses greater than 40 Å the benefit for increasing the emitter injection efficiency is lost, because a higher applied voltage is then necessary to produce a substantial
collector current.

This model supported in part the theories for the significant increased gains proposed by Graul et al., De Graaff and De Groot, and Ning and Isaac. Eltoukhy and Roulston were able to show a decrease in the base current at higher $V_{be}$ values due to the oxide potential, however, they were unable to explain the highly nonlinear I-V characteristics seen by DeGraaff and DeGroot.

Other theories that emphasize the transport properties of the polysilicon are Fossum and Shibib’s ‘recombination velocity’ model and Yu-Ricco-Dutton’s model for PETs. Fossum and Shibib considered an effective recombination velocity, S, at the interface between the polysilicon and monosilicon in order to understand the enhanced gain disregarding any effects from an interfacial oxide. Yu, Ricco, and Dutton also focused on this concept, however, they included the effects from the interface into their S expression. They considered two mobilities, one inside the grains of the polysilicon similar to silicon and a smaller mobility in the grain boundary regions. Recombination was allowed inside the grains and in the interface between the grain and the grain boundary region. From their analysis they concluded that both the interface and the characteristics of the polysilicon have the affect of reducing the minority-carrier surface recombination velocity which is directly proportional to the base current.
and hence increases the gain. The doping profile in the emitter was also found to directly determine the maximum, achievable gain increase.

One of the first explanations for the Gummel plot nonlinearities was also proposed by Yu and Dutton. They found nonlinear characteristics only in the case of devices fabricated with a polysilicon contact and no actually diffusion of emitter impurities into the monocrystalline substrate. In this case there is an abnormal distribution of electrons injected on the base side of the interface. In the extreme case at high base-emitter voltages a negative differential resistance region can develop due to a smaller carrier trap density even with "clean" interfaces explaining the kinks in the base current.

The possibility of dopant segregation at the interface between the polysilicon and the monosilicon is also of interest. Impurities in a polysilicon film segregate at the grain boundaries. If the interface between the poly and the silicon is considered to be one large grain boundary then there should be large amount of dopant pile-up in this region. Neugroschel et al. processed devices with differing arsenic concentrations for the polysilicon emitter. Identical "clean" interfaces were used. They showed that the different arsenic profiles led to a difference in the amount of arsenic segregation at the interface. From the base current
measurements, the diffusivity of the minority carriers at this dopant barrier, and a highly disordered layer 10 nm into the polysilicon, was shown to be reduced. It was also concluded that carriers recombine almost entirely in the 30 nm region above the interface. TEM analysis of these samples actually revealed a grain size of 40 nm in the bulk while close to the interface it was approximately 4 nm. The most surprising result from Neugroschel's study was the similarity in electrical characteristics between diodes contacted by metal and diodes contacted by undoped polysilicon. If the polysilicon was doped with arsenic, however, the diode showed significantly lower hole current. Although Neugroschel et al. calculated a much smaller ratio for diffusivities \( \frac{D_{\text{poly}}}{D_{\text{silicon}}} = 5 \times 10^{-3} \) compared to Ning and Isaac \( \left( \frac{D_{\text{poly}}}{D_{\text{silicon}}} = .3 \right) \), both results show the importance of transport in the polysilicon.

Ng and Yang considered the transport of the minority carrier holes over the barrier due to impurity segregation at the interface by the means of thermionic emission.\(^{20}\) At the interface the probability of scattering is small so that the flow of holes is no longer solely controlled by the drift-diffusion process. The current is comprised, instead, of the holes that have enough kinetic energy to travel over the potential barrier. From the application of the hole current continuity equation at the interface, it was determined that
the total hole current, $J_p$, is comprised of the drift-diffusion current in the monosilicon emitter and the thermionic emission current over the dopant barrier at the interface. Figure 2.10 illustrates their relation to the interface.

![Figure 2.10 Potential Distribution in the Emitter](image)

*Figure 2.10 Potential Distribution in the Emitter*  
*(after Ng and Yang\(^{20}\))*

With these two currents in series $J_p$ is expressed as
\[ J_P = \frac{1}{\frac{1}{J_d} + \frac{1}{J_{th}}} \]

(2.28)

where \( J_d \) and \( J_{th} \) are given by

\[ J_d = \frac{qDn_i^2}{Q_e} \left[ \exp \left( \frac{qV_{BE}}{kT} \right) - 1 \right] \]

(2.29)

and

\[ J_{th} = A \cdot T^2 \exp \left( -\frac{q\Phi_B}{kT} \right) \left[ \exp \left( \frac{qV_{BE}}{kT} \right) - 1 \right]. \]

(2.30)

\( Q_e \) represents the charge associated with the majority carrier electron density in the emitter. The potential barrier, \( \Phi_B \), due to the dopant atoms is directly proportional to the peak doping level at the interface and is given by

\[ \Phi_B = \frac{kT}{q} \ln \frac{N_v N_{d_{max}}}{n_i^2} \]

(2.31)

where \( N_{d_{max}} \) is the peak doping level and \( N_v \) is the effective density of states in the valence band. It is, therefore, apparent from this model that the base current injected into
the emitter is determined by peak level of impurity segregation at the interface and the dopant level in the monosilicon emitter. The nonlinear temperature dependence of gain can be explained by the fact that the hole current $J_p$ is closest to the smaller of the two component currents. The ratio of two currents was found to vary with temperature, leading to the nonlinear temperature dependence of $J_p$.

Experimental work performed by Patton et al. and Chen et al. relating to dopant segregation, showed it to be influential on the base current. Chemical concentrations in the polysilicon below $10^{20}$, however, resulted in insufficient segregation at the interface for barrier formation to affect the base current. Concentrations above $10^{22}$ provided a barrier and showed a substantial decline in the base current.

From the studies reviewed it becomes apparent that no one physical property of the PET is responsible for the increases seen in the common-emitter gains of actual fabricated devices. Some general assumptions can be made, however. The interfacial oxide poses a significant barrier to minority carrier holes, and to majority carrier electrons, to some extent. If it is possible for the carriers to overcome this obstacle, the properties of polysilicon, including the thickness and grain characteristics affecting the transport of the minority carriers, now become a limiting factor. All of these mechanisms are beneficial in reducing the minority hole
current, with the devices having thick interfacial oxides exhibiting the highest increases in gain. The concentrations used to dope the polysilicon/monosilicon still have a significant influence on the amount of gain that is possible, in the same way as with the traditional BJT.

2.3 Annealing of the Emitter

2.3.1 Objectives of the Drive-in

After an implantation step the presence of damage in the silicon creates a region of potential recombination centers or traps inside the emitter and base regions, which creates transistor leakage and degrades gain. It is possible to drive impurities past the damage range if deep junctions are permissible. Current technology trends, however, require very shallow junctions.

For a polysilicon emitter, utilizing annealing for implant damage removal is not as critical an issue compared to a conventional emitter. Since the emitter is formed by diffusion into undamaged silicon it is not necessary to move the emitter-base junction past a damaged area. Of interest, is impurity activation and conductivity. Impurities implanted into the polysilicon for emitter formation must undergo a subsequent annealing step for redistribution throughout the entire film and diffusion into the monocrystalline region, as
well as activation for placement onto substitutional lattice positions. The diffusion rate of impurities in polysilicon can be over 100 times greater than that in single-crystal silicon due to the mechanism of grain boundary diffusion.21 As the dopant atoms move along the grain boundaries they diffuse into the grains in a short amount of time where the electrical mechanisms are essentially the same as in single-crystal silicon. Phosphorous and arsenic (highest degree) have been found to precipitate at the grain boundaries, which predominantly occurs at lower anneal temperatures. When the dopants move from the single-crystal regions to the grain boundaries they do not produce free carriers and the resistivity of the film is dramatically increased. Solutions to this problem are to increase the grain size, which decreases the grain boundary density and the associated trapping of free carriers, increase the dopant concentration, and finally use a higher temperature anneal for better activation.

2.3.2 Rapid Thermal Processing

A major dilemma in the use of high temperature processing for device fabrication has been the control of unwanted dopant diffusion.21,22 While some high temperature steps have been successfully substituted with a modified lower temperature
process like low temperature oxidation, other steps continue to use high temperatures, but for much shorter times.\textsuperscript{21} Short duration thermal steps are not possible in traditional furnace systems since the large mass of the wafer boats, furnace walls, and susceptor make it difficult to rapidly increase and decrease temperature. There is also the possibility that wafer slippage or warpage will occur when the wafers change temperature too rapidly in a conventional furnace.

Rapid thermal processing exposes the wafers to high temperatures for just the time necessary to create the required result.\textsuperscript{22} It selectively promotes a desired reaction over an undesired reaction. In the case of arsenic, the activation energy for removing defects is approximately 5 keV, while the energy for diffusion is around 4 keV.\textsuperscript{22,23} From Figure 2.11 it can be seen that a high temperature for a short time provides the optimum conditions for limited diffusion with no dislocations.
Figure 2.11 Optimum Annealing of Defects with Limited Arsenic Diffusion for a 5E15, 100 Kev Implant (after Sedgwick\textsuperscript{22})

In the case of boron, arsenic, and phosphorous, diffusion is
believed to be enhanced in some part by the presence of silicon interstitials existing after ion implantation.\textsuperscript{21} For boron the activation energy of diffusion is 3.4 keV, while the removal of interstitials requires an energy of 4.7 keV.\textsuperscript{22} If the interstitials are removed early at high RTA temperatures, boron diffusion will be limited. The time required to actually place dopant atoms on substitutional sites is quite short compared to the times for significant diffusion. RTA times under one minute are often sufficient, with the amount of dopant activated being dependent upon the temperature used. The end result is a much greater amount of conductivity is possible for a particular junction depth with rapid thermal annealing than with conventional furnace annealing. Although there has been a substantial study of RTA applied to boron and arsenic implants, the amount of research involving phosphorous and antimony implants has been small.\textsuperscript{24}

The original work in RTP with the use of laser sources allowed substrates to be heated to high temperatures in less than a microsecond.\textsuperscript{21} Small laser spot scanning, however, causes localized thermal gradients creating wafer warpage and damage. The switch to the incoherent lamp sources such as tungsten-halogen or arc lamps allowed for the heating of large areas with only a second required to reach the high temperature. Wafers in RTP units are thermally isolated so that the heat they receive is only from radiant sources and
not conductive in nature and also so cooling is easily achieved. The components of a rapid thermal processing unit are shown below in Figure 2.12.

Figure 2.12 Schematic of a Rapid Thermal Processing Unit
(after Sedgewick\textsuperscript{22})

Temperature repeatability and uniformity is one the most
difficult issues concerning RTP. Temperature measurement has to be carefully designed into the systems to provide closed-loop feedback to prevent undershoot and overshoot. Thermocouples in contact with the wafers are common for temperature measurement, however, at high temperatures their composition of metal poses the threat of undesirable reactions in the process chamber that should be avoided. Pyrometers are typically used at high temperatures. They sense the energy emitted from the wafer remotely, which is a function of the wafer temperature. A pyrometer in an RTP unit focuses on the backside of a wafer, but the chamber reflectivity can have some effect. The energy that the pyrometer measures is dependent upon its operating wavelength. Temperature repeatability is affected by the uniformity across and between wafers annealed. It is common for the backside of wafers to lack uniformity since the thickness of deposited films and finishes vary. In a particular case an oxide film 250 nm thick created a 40°C anneal temperature decrease. Polysilicon films especially tend to amplify the emissivity of a wafer by interference effects. Heavily doped wafers also have a higher heating rate than lightly doped wafers due to differing absorption spectra. A measurement of the emissivity or optical property of the backside of the wafer must be made for calibration before annealing of actual device wafers, so that the input power can be adjusted.
The change of a wafer’s temperature with time is shown in Eq. (2.32).^{23}

\[
\frac{dT}{dt} = \frac{(1-R)}{C} \int_0^\infty d\lambda I_\lambda (1-\exp(a_\lambda d))
\]

(2.32)

where \(C\) is the heat capacity, \(I_\lambda\) is the incident radiation intensity, \(R\) is the reflectivity, \(a_\lambda\) is the absorption coefficient, and \(d\) is the wafer thickness. Required temperatures can be reached in less than a second.^{22} Specific times and temperatures for rapid thermal annealing depend upon the effect desired. Times less than 5 seconds in current systems are unacceptable, since they lead to problems with reproducibility from transient effects at the initial start-up of the process.^{26}

2.3.3 Breakup of the Interfacial Oxide

The annealing of the emitter not only redistributes the implanted impurities, it also has a significant effect on the characteristics of the interface. High transmission electron microscopy on fabricated devices has provided conclusive evidence that a breakup of the thin oxide at the interface occurs for temperatures of 900°C and above.^{2,3} Before the high temperature processing step the interfacial oxide is a
continuous layer, with its thickness depending upon the treatment prior to polysilicon deposition. After an anneal at a temperature of just 900°C an HF etched device will have a discontinuous oxide layer, thicker than the original native oxide thickness of approximately 4 to 5 Å in some areas and as thin as 0 Å in other areas.² RCA clean devices with original oxide thicknesses of 14 to 20 Å show little discontinuity. For an anneal temperature of approximately 1000°C HF etched devices can show balls of oxide as large 50 Å in diameter and areas of regrown polysilicon several hundred angstroms in length along the interface. At higher temperatures the RCA clean devices will show the same breakup characteristics as the HF devices. A higher temperature for the same effect is necessary because the initial starting thickness is greater for the RCA clean devices.

Two phenomena are required for oxide balling-up to occur.²⁷ The Si-O bonds must first break and secondly O atom movement along the interface must occur. Segregated arsenic or phosphorous atoms at the interface aid in the bond breaking by diffusing into the interfacial oxide and lowering the glass transition temperature. The stress of the polysilicon and silicon materials then induces O atom movement.

As mentioned in a previous section tunneling through the interfacial oxide by both minority and majority carriers is a significant premise in a number of theories concerning the
unique electrical characteristics of PETs. As the interfacial oxide is broken-up, the tunneling barrier height is decreased or altogether dissolved. Results supporting this have shown that as the anneal temperature increases the base current also increases, but the emitter resistance decreases. Base currents of up to 100 times greater have been found for RCA clean devices annealed at 1100°C compared with corresponding slightly annealed, control devices. Although breaking up the oxide reduces the possible high gains, the reduction in the emitter resistance is beneficial to circuit performance. Rapid thermal annealing has been used for a short time, high temperature anneal adequate to lower the emitter resistance with limited junction depth movement.

2.3.4 Epitaxial Alignment of the Polysilicon

Following the breakup of the interfacial oxide, the areas of the interface where the monosilicon is exposed to the polysilicon provide the opportunity for epitaxial alignment of the polysilicon with the substrate. A single-crystal emitter created in this manner is termed an extended emitter. Some of the advantages of polysilicon emitter transistor circuits are still present with this approach. The depth of the emitter into the substrate is still shallow, thus the peripheral component of the emitter-base capacitance is still small. Additionally, a
larger degree of control and reproducibility exists for the current gain since the uncertainty of the interface influence is diminished.

Epitaxial alignment proceeds in columns growing from the polysilicon-silicon interface towards the device surface at a rate of several hundred Å/min. When temperatures are as high as 1100°C, the original oxide layer is completely broken-up into balls with almost all of the interface being oxide-free. The rate of alignment is influenced directly by the temperature and degree of dopant concentration in the polysilicon. The use of low drive-in temperatures in conjunction with low impurity concentrations such as 1000°C and 10^{19} atoms/cm³, respectively, yield a small amount of epitaxial alignment. High temperatures and impurity concentrations of 1150°C and 5 \times 10^{26} atoms/cm³, respectively, lead to complete epitaxial alignment with a low degree of defects.

When the average grain size of the film exceeds the original polysilicon thickness the degree of epitaxial alignment is determined from the integrated yield, which is the integral of the ion channeling spectrum for the polysilicon thickness over the random spectrum. In devices tested the base current has been found to be independent of the integrated yield. The base current is most likely so dominated by Auger recombination due the high dopant
activation in the emitter that the actual characteristics of the regrown material have little effect. RTA again makes it possible to use the required high temperatures to cause epitaxial alignment with very little emitter-base junction movement.
3.0 Experimental Design

3.1 Test Chip Layout

A polysilicon emitter test chip was designed using Mentor Graphics Chipgraph software on the Apollo workstations at RIT’s Computer Engineering Lab. A PET process was created for layout consisting of the following six levels: collector, base, buried contact, emitter, contact cut, and metal. Vertical npn and lateral pnp transistors as well as parametric structures for characterization were designed.

The chip design includes a series of vertical npn transistors with emitter windows ranging size (width by length) from 6 by 6 microns to 30 by 240 microns, respectively. There is also an extremely large npn transistor with an emitter dimension 100 by 100 microns for inline beta measurement. The collector regions extend past the base no less than 10 microns. This should insure that the collector-substrate and collector-base depletion regions do not come in contact. The base regions extend a minimum of 10 microns past the buried contact level. The polysilicon also overlaps the buried contact by a minimum of 10 microns for any of the designs. 10 microns was chosen as a minimum to allow for alignment tolerances, resist flow during postbake, and resolution in the lithographic steps. Lateral diffusion of the collector should be larger than the base making this extension
somewhat bigger. These dimensions should insure higher yields with an acceptable degree of device parasitics. Contact cuts to the different device regions range from 6 to 10 microns. Their size in a conventional process controls the smallest emitter dimension possible, however, the contact cut of 6 by 6 microns was possible for the 6 by 6 micron emitter since the polysilicon overlaps the buried contact level. Contacts to the collector and the substrate are also designed to be implanted at the same time as the emitter and base, respectively, to form low-resistance ohmic contacts. In order to avoid aluminum spiking of the shallow emitter-base junction during sintering, transistors with contacts to the polysilicon directly over the junction and contacts to the polysilicon offset from the junction were created. Contacting the polysilicon over field oxide regions may add some series resistance.

The lateral pnp transistors were designed with base widths ranging from 2 to 10 microns. The actual base width will be reduced by two times the lateral diffusion of the base. These devices were included to offer additional design options for the developed process, but were not optimized since the lower mobility of the minority carrier holes in the base limits their high speed performance compared to the vertical npn devices. Contact cuts were designed with a minimum dimension of 10 microns.
Parametric structures to aid in characterization were also designed. An array of 6 by 6 micron cross-bridge Kelvin resistor structures, with diffusion region overlaps ranging from 2 to 15 microns, were designed for measuring the contact resistance of metal contacting the emitter, base, and collector, as well as the metal contacting the polysilicon over the thin and thick oxide regions. Van der Pauw sheet resistance structures and resistors of approximately 40, 80, and 266 squares for emitter, base, base pinch, collector, and polysilicon over thin and thick oxides were created. Separate emitter-base and base-collector diode structures also exist. In addition to these, capacitance structures for metal to substrate, collector, base, emitter, and polysilicon; and polysilicon to substrate and collector are also available on the test chip.

Alignment marks were made at the collector and base levels; and alignment verniers and resolution structures were also added for all levels. The actual chip design layout is shown in blocks in Appendix A.
3.2 Device Simulation Using SUPREM

One dimensional process simulation for the vertical npn PETs was performed using Stanford University Process Engineering Model III (SUPREM). The process simulated was a fully implanted isolated collector process. No buried layers or epitaxial layers were used because RIT does not yet have epi capability and once the rapid thermal processor is installed this process should be fully implementable at RIT. Instead an n well was used as the collector. Less area is needed for such a process compared with the standard buried collector process that requires a p-type isolation around each collector. A disadvantage of this approach is a higher value of collector resistance.

Phosphorous $P^{11}$ was chosen as the dopant species for the collector and emitter regions. Its fast-diffusing nature is suitable for formation of the collector well. Arsenic being a slower-diffuser may be more suitable for emitter formation, however, the safety concerns of this source have made it unavailable at RIT. In addition, after a thorough search on RTP material, an extremely limited amount of research was found to exist on rapid thermal processing of phosphorous implants. This work may, therefore, be helpful to others in this respect.

$BF_{17}$ was chosen as the dopant species over $B_{17}^{12}$ for
formation of a shallow base. B$^{11}$ is a light ion and will cause crystalline defect damage instead of amorphous layer damage. This damage must be annealed at a temperatures above 900°C which can cause a large degree of dopant diffusion. BF$_2^+$ has about a five times higher mass than B$^{11}$, The projected range for the same energy is, therefore, much less with BF$_2^+$ (as small as .03 microns). BF$_2^+$ causes a large degree of amorphous damage, which can be annealed at lower temperatures. The amorphous layer also decreases the opportunity for channeling to occur, thus decreasing junction depth.

Six separate cross sections were simulated. These included regions under the emitter, under the extrinsic base, under the polysilicon and extrinsic base, under the collector outside the base, under the collector contact, and outside the collector well. Simulations for electron and hole distributions and base resistance were also performed.

The first objective of the simulations was to determine the best drive-in times for the base and emitter for a range of base doses that would achieve a narrow base width with a large enough integrated base doping to avoid punchthrough of the base at operating voltages of 5 to 10 volts. The Early voltage of a device is known to decrease in magnitude with decreased base doping also, so this had to be taken into consideration. Simulations were performed for base doses between 5E12 to 3E14 ions/cm$^2$. These ranges were based upon
documented work at other research centers, and on an earlier attempt at PETs at RIT, where it was concluded that a base dose of 1E14 ions/cm² for around the same base widths designed in this process, was too high to achieve desirable gains. The transistors of this earlier investigation had Early voltages as large as 417 volts and did not punchthrough. The depletion widths into the base side of the base-collector junction, $X_{pBC}$, and into the base side of the emitter-base junction, $X_{pEB}$, for the planned collector, base, and emitter doping concentrations for an applied voltage, $V_{CE}$, of 5 volts were tabulated. This was done to check for possible punchthrough. The lowest, worst cases for the integrated base were approximated from SUPREM profiles for each different base dose. $V_{BE}$ was assumed to be .7 volts, leaving $V_{CB}$ equal to 4.3 volts. The results are shown in Table 3.1 with the equations used following the table.
Table 3.1 Tabulation for Punchthrough

<table>
<thead>
<tr>
<th>Base Dose ions/cm²</th>
<th>$N_{AB}$ ions/cm³</th>
<th>$N_{DC}$, $N_{DE}$ ions/cm³</th>
<th>$X_{pbc}$ microns</th>
<th>$X_{pbe}$ microns</th>
</tr>
</thead>
<tbody>
<tr>
<td>5E12</td>
<td>1E16</td>
<td>5E15, 9E18</td>
<td>.47</td>
<td>.15</td>
</tr>
<tr>
<td>8E12</td>
<td>3E16</td>
<td>5E15, 9E18</td>
<td>.18</td>
<td>.091</td>
</tr>
<tr>
<td>1E13</td>
<td>5E16</td>
<td>5E15, 9E18</td>
<td>.071</td>
<td>.073</td>
</tr>
<tr>
<td>5E13</td>
<td>8E16</td>
<td>5E15, 9E18</td>
<td>.065</td>
<td>.059</td>
</tr>
<tr>
<td>8E13</td>
<td>9E16</td>
<td>5E15, 9E18</td>
<td>.062</td>
<td>.056</td>
</tr>
<tr>
<td>1E14</td>
<td>1E17</td>
<td>5E15, 9E18</td>
<td>.056</td>
<td>.054</td>
</tr>
<tr>
<td>3E14</td>
<td>3E17</td>
<td>5E15, 9E18</td>
<td>.020</td>
<td>.033</td>
</tr>
</tbody>
</table>
\[ X_{PBC} = \frac{N_{DC}}{N_{AB} + N_{DC}} \sqrt{\frac{2 \varepsilon_s \varepsilon_r}{q} \left( \frac{1}{N_{DC}} + \frac{1}{N_{AB}} \right) \Phi_{bi} - V_A} \]  

(3.1)

\[ X_{DEB} = \frac{N_{DE}}{N_{AB} + N_{DE}} \sqrt{\frac{2 \varepsilon_s \varepsilon_r}{q} \left( \frac{1}{N_{DE}} + \frac{1}{N_{AB}} \right) \Phi_{bi} - V_A} \]  

(3.2)

\[ \Phi_{bi} = \frac{k t}{q} \ln \left( \frac{N_A N_D}{n i^2} \right) \]  

(3.2)

5E12 ions/cm² was determined to be too low a base doping to avoid punchthrough. 8E12 ions/cm² appears a little risky when looking at SUPREM calculated base widths. Expecting wider widths than SUPREM calculated, as has been shown in the past, this dose was still attempted on a few wafers as an extreme case. The actual dopings focused upon were then 8E12, 1E13, 5E13, 8E13, 1E14, and 3E14 ions/cm². All these doses have a simulated integrated base between 1E12 and 5E13 ions/cm². Simulation input files and profiles are shown in Appendix B.

Another difficulty in achieving a shallow base width was the requirement of a suitable oxide thickness grown above the base. This oxide had to be thick enough to prevent etching the bare silicon during the patterning of the polysilicon and the
diffusion of phosphorous into areas where the polysilicon was not over the emitter. LTO could have been chosen for this oxide, but a certain amount of thermal oxide is necessary before LTO can be deposited. LTO is also of poor quality for an interlevel oxide. This oxide growth, however, causes enhanced diffusion, creating a deeper base-collector junction. From simulation it was determined that the phosphorous diffused 300Å into the oxide over the base during the emitter anneal. This was considered in determining the actual base anneal process.

3.3 Device Fabrication

The steps for fabrication of the two process lots will now be described and illustrated. A second lot was started when it was determined from inline process measurements that the base-collector junction depth of the first lot had become too deep to expect high gains. Adjustments were then made to the base drive-in process for the second lot. The majority of the steps for the two separately processed lots are similar. Steps that differ, however, will be clarified. Specific details of the processing steps including control wafer flow are included in Appendix C. Film thicknesses, junction depths, and sheet resistance measurements for controls at each level are included in Appendix D.
The first lot consisting of twelve device wafers and fifteen control wafers and a second lot of twelve device wafers and thirteen controls were scribed for identification. These starting substrates were p-type with a resistivity of 5-15 ohm-cm. The wafers were then four point probed to determine the specific resistivity of each. Prior to the collector masking oxide or field oxide growth a standard RCA clean was performed. Wafers were then oxidized at 1100°C for 110 minutes. A rather thick target of around .7 microns was used to establish a significant step height difference between this oxide and the oxide to be grown over the collector, so that the alignment mark would be clearly visible for later lithography levels.

For all wet oxidation steps, including this one, a method of drip oxidation was utilized. In this method, DI water was dripped through an adjustable pipet and through a hose into a cleanly etched furnace tube with dry O₂ flowing. All apparatus was cleaned prior to use. The drip rate used was 40 drops per minute to achieve saturation in the tube. The goal was to introduce H₂O into the O₂ gas stream without the use of the bubbler method, which is a possible source of contamination. This should help improve the base current non-ideality factor towards a value of 1. Preliminary experiments showed growth rates to be quite similar to the bubbler method. Thickness uniformity results are shown in Appendix D.
Figure 3.1 Cross Section after Field Oxide Growth

Collector regions were then patterned with resist and etched in the oxide, with the photoresist left on to mask the collector implant. Phosphorous P$_{31}$ ions were implanted at a dose of 8E12 ions/cm$^2$ and an energy of 110 KeV. The resist was then removed.
A standard RCA clean was performed on all wafers prior to the collector drive-in. The drive-in was performed for 2800 minutes at 1125°C.
Figure 3.3 Cross Section after Collector Drive-in

Base regions were patterned with resist and etched in the thermal oxide grown over the collector regions. The resist was again left on to mask the implant. Boron BF$_2^+$ at an energy of 35 KeV was then implanted into two wafers for each of the doses 8E12, 1E13, 5E13, 8E13, 1E14, and 3E14 ions/cm$^2$ for the first lot, and into four wafers for each of the doses 8E12, 5E13, and 1E14 ions/cm$^2$ for the second lot. The resist was then removed.
A standard RCA clean was performed on all wafers prior to the base anneal/drive-in. The drive-in was performed for 55 minutes at 900°C for the first lot. Control groove and stain results showed that the base-collector junction depth was over a micron for almost all doses. Simulations did not show such a large degree of diffusion, although previous experience has yielded slightly deeper junctions than SUPREM showed. Oxidation enhanced diffusion was thought to be the problem in part. A requirement of at least 350 Å of oxide is necessary in order to protect the bare silicon on the outer edges of the
wafer from the bull's-eye effect of the RIE during the polysilicon etch step; and to prevent phosphorous diffusion into the areas below this thin oxide under the polysilicon. A certain amount of oxide will be lost at the edges of the wafer, while the polysilicon in the center completely etches in the RIE. This thickness was determined from SUPREM simulation which showed significant phosphorous diffusion into this thin oxide and from experimental inline data after the RIE step (shown in Appendix D). The process was then modified to 50 minutes at 850°C for the second lot. Preliminary experiments showed the oxide grown would be thick enough.

Figure 3.5 Cross Section after Base Drive-in

The buried contact level was then patterned with resist
and etched in the oxide over the base regions and the resist was removed.

![Cross Section Drawing](image)

**Figure 3.6 Cross Section after Buried Contact Formation**

A special RCA clean was then performed on all wafers. The HF dip was the first step and was performed for 15 seconds for the first lot and only 5 seconds for the second lot to avoid unnecessary etch of the thin base oxide. The wafers were then placed in the APM solution for 10 minutes and the HF: solution for 10 minutes to grow the thin interfacial oxide. Polysilicon was deposited at 610°C with a target thickness of 4000 Å. A thick polysilicon thickness was used to prevent any possible onset of junction spiking during sintering and also to limit the base current. Special controls were prepared with
a 1000 Å of oxide in order to measure the thickness of the polysilicon.

Figure 3.7 Cross Section after Polysilicon Deposition

The polysilicon was then implanted with phosphorous P⁺ at an energy of 45 KeV and dose of 4E15 ions/cm² for the first lot and at 40 KeV and 5E15 ions/cm² for the second lot. A special undoped, p-type, silicon control wafer was also implanted as a substitute for future measurement of the thickness of the oxide on top of the polysilicon during the emitter drive-in, which can not be measured on the nanospec. Oxidation rates of this wafer may be slightly greater than that of polysilicon doped to the same level, however, the
ratio of the amount of poly consumed during oxidation to the oxide thickness grown is very similar to that of single crystal oxidation.\textsuperscript{21}

![Figure 3.8 Cross Section after Emitter Implantation](image)

The polysilicon was then patterned with resist and etched in the RIE for just the precise time necessary to clear in order to avoid possible etching of bare silicon areas on the edges. The resist was then removed.
Figure 3.9 Cross Section after Emitter Patterning

A standard RCA clean was then performed. At this point in the process the device wafers were divided into groups for the emitter drive-in. Since the first lot contained two wafers for each base dose, six wafers were annealed with the furnace process of 120 minutes at 875°C, while the other six wafers were rapid thermal processed at 1000°C for 20 seconds. In the second lot three wafers were furnace annealed for 120 minutes at 875°C, while the remaining wafers were rapid thermal processed in groups of three at 950°C, 1000°C, and 1050°C for 20 seconds. The selection of an emitter drive-in processes was based upon SUPREM results and previously performed research.
relating RTP to bipolar devices.\textsuperscript{31,32,33,34} Most previous research on RTP of PETs involves arsenic emitters, so the higher diffusivity rate of phosphorous was considered. A range of RTP temperatures was used to study the affect of temperature on the interfacial oxide and current gain.

Wafers that received the RTP process were first furnace annealed at 800\textdegree C for 40 minutes to grow some thermal oxide to prevent severe surface leakage. This thermal step also served to redistribute the impurities prior to RTP. Low temperature oxide was then deposited on top of the thermal oxide at 400\textdegree C with a target thickness of 3000\text{Å}. The thermal oxide and LTO acted as a capping oxide to prevent outdiffusion in the RTP process. The rapid thermal anneal process also served as the densification step for the LTO.

\begin{center}
\textbf{Figure 3.10 Cross Section after LTO Deposition}
\end{center}
The rapid thermal processing was conducted at Cornell University with an AG Associates Heatpulse 610 RTP. Nitrogen was used as the process gas. The first step performed was to make sure the displayed temperature for the thermocouple wafer inside the process chamber read the same as an external digital multimeter when the program selection was set for thermocouple temperature monitoring. This made sure that the delicate thermocouple wafer was functioning. After this the pyrometer was checked against the thermocouple wafer by displaying the thermocouple temperature reading when the program selection was set for the pyrometer. On average when the pyrometer reached its steady state temperature value set in the program the thermocouple read 13 to 16°C higher.

A major dilemma was to decide which source of temperature measurement was most accurate. Pyrometer readings vary with the backside of the wafer surface. So if one calibrates the pyrometer using the bare undoped thermocouple wafer, an actual device wafer with various backside films will most likely be different. Laying the device wafer on top of the thermocouple wafer is also another possibility. However, the device wafer is not in direct contact with the thermocouple wafer so the temperature of the device wafer is also most likely different from the thermocouple reading. An ideal situation would be to have a thermocouple embedded in the top surface of each device wafer where one is really concerned with the temperature. This
is obviously an unrealistic solution. Some systems, however, come with a thermocouple that makes contact with each individually processed wafer. This was not available with the system used. Lot #1 was processed with the pyrometer and the thermocouple wafer taken out, while lot #2 was processed using the thermocouple by laying each sample on top of the thermocouple wafer. It was also found to take 3-4 seconds to reach the temperature setting after the steady state cycle was started. The actual anneal time in the program was, therefore, set to 25 seconds in order to have 20 seconds of a constant temperature.

Programs are shown in Appendix C. Five parameters set in the program are; T_sw, which is the temperature of the first lamp intensity used to initiate steady state, Gain, the correction factor applied to the lamp intensity to maintain steady state, DGain, the frequency at which the temperature profile signal is looked at in order to avoid overshoot or undershoot, Iwarm, the lamp intensity value of previously processed wafer, and Icold, the first lamp intensity value of steady state for the first wafer processed. The last two parameters are calculated by the unit, while the first three parameter were set based upon previous operation of the unit.

Initially for the first lot of furnace annealed wafers, the large dimension vertical npn transistor for measuring inline beta was measured for the bottom inch of chips on all
device wafers. The oxide on top of all contact areas was first etched off for this bottom inch. One transistor had a measured gain of 17, on the wafer with a base dose of 8E12 ions/cm². However, the severe surface leakage between the probes made bare silicon probing difficult and few working devices were obtained.

Figure 3.11 Cross Section after Emitter Drive-in

The contact cut level was then patterned with resist and etched in the oxide over the emitter, base, collector, and field regions. The resist was then removed.
A standard RCA clean was performed on all wafers. Finally aluminum with 1% silicon to prevent junction spiking was sputtered on the device wafers.
This aluminum metal level was then patterned with resist and etched in phosphoric acid. After inspection a large amount of haze or dust appeared all over the wafers. This was determined to be the 1% silicon left on top of the oxide after the aluminum had been etched away. A polysilicon etch solution was used to remove the haze and the resist was then removed. No blackening of the aluminum pads was noticed so the resist masked the polysilicon etch well. The wafers were first tested before any sintering process. Wafers were then sintered cautiously to avoid spiking of the emitter-base junction.

Figure 3.14 Cross Section of Completed Devices
4.0 Results

4.1 Electrical Characterization Procedure

In order to evaluate the designed process, all wafers from each lot were tested using an HP 4145B Parameter Analyzer. The vertical npn transistors as well as the lateral pnp transistors were examined. All of the different designs for the transistors were tested on at least one of the best yielding wafers to verify the designs themselves. Some of the parametric structures such as the Van der Pauws and diffused resistors and some cross-bridge Kelvin resistor structures were also measured. Additional structures on the test chip that were not tested were provided for future work.

The vertical npn transistors were evaluated on the basis of the maximum common-emitter current gain, the Early voltage, the product of the maximum gain and the Early voltage, breakdown voltages, the base current non-ideality factor, and the collector currents with emitter open-circuited and the base open-circuited.

The common-emitter gain was previously defined in the background section. Its maximum value, \( \beta_{\text{max}} \), is limited at high values of \( I_e \) due to the Kirk effect. At high collector current the density of electrons on the collector side becomes comparable with the collector doping level. This lowers the electric-field gradient in the collector-base junction,
widening the base width and, therefore, decreasing the gain.

The Early voltage, $V_A$, is a measure of the effect of the decreasing base width caused by the encroaching base-collector depletion region in the forward-active mode. This base-width modulation is expressed as

$$V_A = \frac{I_C}{\delta I_C} \cdot \frac{\delta I_C}{\delta V_{CE}}.$$  \hspace{1cm} (4.1)

This value is experimentally obtained by taking the intercept of the characteristics with the $V_{CE}$ axis.

$BV_{EBO}$ is the breakdown voltage of the emitter-base junction when the collector current is 0. $BV_{CBO}$ is the breakdown voltage of the collector-base junction when the emitter current is 0. $BV_{CEO}$ is the breakdown voltage when a voltage is applied between the collector and emitter with the base current equal to 0. The first two breakdown voltages are avalanche limited, while the third is limited by either avalanche or punchthrough. The collector-substrate breakdown voltage is also of importance.

The base current non-ideality factor, $\eta$, is expressed as

$$\eta = \frac{1}{\ln 10} \frac{V_{IB}}{kT}. \hspace{1cm} (4.2)$$

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This gradient of $I_0$ for this equation is obtained from the Gummel plots.

The collector current with the emitter open-circuited, $I_{cbo}$, is also referred to as the collector-base junction saturation current. This leakage current was measured at a collector-base reverse bias of 5 volts.

4.2 Electrical and Final Inline Results

Before mentioning the outcome of electrical test, a summary of the the final inline process data will be made. Appendix D shows the detailed sequential inline process results. The junction depth readings were made as accurate as possible. Do to the nature of groove and stain measurement technique and the shallowness of these junctions, however, there may be some error in the values. In order to determine $X_{jeb}$, the depth of the n+ region into the base was measured which includes the poly and monosilicon. Since the interface between the polysilicon and the monosilicon was not visible, the monosilicon depth is just the depth of the n+ region with the polysilicon thickness subtracted. The polysilicon thickness is known from taking the original deposition
thickness minus the loss of thickness during oxidation. Furnace annealed wafers and RTP wafers have different poly thicknesses. This method is shown in the Appendix D. The groove and stain junction depth values for both lots are shown in Table 4.1 and Table 4.2.
### Table 4.1 Final Junction Depths for Lot #1

<table>
<thead>
<tr>
<th>Base Dose Ions/cm²</th>
<th>Emitter Anneal</th>
<th>Emitter-Base microns</th>
<th>Base-Collector microns</th>
<th>Collector-Substrate microns</th>
</tr>
</thead>
<tbody>
<tr>
<td>8E12</td>
<td>Furnace</td>
<td>.25</td>
<td>.40</td>
<td></td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1000°C</td>
<td>.16</td>
<td>.51</td>
<td></td>
</tr>
<tr>
<td>1E13</td>
<td>Furnace</td>
<td>.22</td>
<td>.59</td>
<td></td>
</tr>
<tr>
<td>1E13</td>
<td>RTP 1000°C</td>
<td>.10</td>
<td>.58</td>
<td></td>
</tr>
<tr>
<td>5E13</td>
<td>Furnace</td>
<td>.14</td>
<td>.66</td>
<td></td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1000°C</td>
<td>.26</td>
<td>-—</td>
<td></td>
</tr>
<tr>
<td>8E13</td>
<td>Furnace</td>
<td>.19</td>
<td>.70</td>
<td></td>
</tr>
<tr>
<td>8E13</td>
<td>RTP 1000°C</td>
<td>.16</td>
<td>.64</td>
<td></td>
</tr>
<tr>
<td>1E14</td>
<td>Furnace</td>
<td>.16</td>
<td>.76</td>
<td></td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1000°C</td>
<td>.15</td>
<td>.73</td>
<td></td>
</tr>
<tr>
<td>3E14</td>
<td>Furnace</td>
<td>.10</td>
<td>.77</td>
<td></td>
</tr>
<tr>
<td>3E14</td>
<td>RTP 1000°C</td>
<td>.20</td>
<td>.71</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Furnace</td>
<td></td>
<td></td>
<td>6.52</td>
</tr>
<tr>
<td></td>
<td>RTP 1000°C</td>
<td></td>
<td></td>
<td>6.46</td>
</tr>
</tbody>
</table>
Table 4.2 Final Junction Depths for Lot #2

<table>
<thead>
<tr>
<th>Base Dose Ions/cm²</th>
<th>Emitter Anneal</th>
<th>Emitter-Base microns</th>
<th>Base-Collector microns</th>
<th>Collector-Substrate microns</th>
</tr>
</thead>
<tbody>
<tr>
<td>8E12</td>
<td>Furnace</td>
<td>.21</td>
<td>.67</td>
<td></td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 950°C</td>
<td>.23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1000°C</td>
<td>.30</td>
<td>.45</td>
<td></td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1050°C</td>
<td>.29</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5E13</td>
<td>Furnace</td>
<td>.19</td>
<td>.87</td>
<td></td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 950°C</td>
<td>.23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1000°C</td>
<td>.14</td>
<td>.64</td>
<td></td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1050°C</td>
<td>.28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1E14</td>
<td>Furnace</td>
<td>.17</td>
<td>.90</td>
<td></td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 950°C</td>
<td>.23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1000°C</td>
<td>.23</td>
<td>.71</td>
<td></td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1050°C</td>
<td>.26</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Furnace</td>
<td></td>
<td></td>
<td>7.18</td>
</tr>
<tr>
<td></td>
<td>RTP 1000°C</td>
<td></td>
<td></td>
<td>7.11</td>
</tr>
</tbody>
</table>
The final control wafer emitter and base sheet resistance measurements for both lots are shown graphically in Figures 4.1 - 4.4. The values are also listed Appendix D.

Figure 4.1 Control Wafer Base Sheet Resistance for Lot #1
Figure 4.2 Control Wafer Base Sheet Resistance for Lot #2

Figure 4.3 Control Wafer Emitter Sheet Resistance for Lot #1
Van der Pauws and differently sized diffused resistors were measured in order to determine sheet resistance on the actual device wafers. The Van der Pauws and resistors appeared to have metal opens problems due to step height coverage over oxide on some structures on some wafers. In these instances the probe had to be positioned on a metal line and not a pad. This was easiest to do for the diffused resistors, so in order to make a valid comparison across both lots for all types, the longest diffused resistor of 266 squares was measured. Collector and base pinch resistors were designed. However, the collector resistor was designed without the n+ poly on top,
unlike the collector contacts so in order to etch deep enough through the field oxide, an over etch of the other contact cuts would have occurred. The collector resistors were found to be open. The base pinch resistors yielded extremely low sheet resistance values, and it was discovered that a design error caused shorting to the poly. These two errors should be fixed on a redesign of the mask set.

A few cross-bridge Kelvin resistors were measured on one wafer in order to get an idea of the contact resistance. These ranged from 55-90 ohms. The contact size was the same as used in the diffused resistors. Contact resistance depends on the contact size and geometry as well as the semiconductor sheet resistance. Therefore, the contact resistance would be different for each different underlying diffusion and on every differently processed wafer. To substract a general average contact resistance for each resistor would be incorrect. Due to testing time constraints and the fact that a long resistor was measured, in depth contact resistance testing was not performed and some small error in the sheet resistance values is acknowledged. The averaged values for these diffused resistors after sinter, which includes the contact resistance, are shown in Tables 4.3 and 4.4. Stars indicate that the resistor characteristic was curved and, therefore, the data may be unreliable.
Table 4.3 Diffused Resistors Rs for Lot #1

<table>
<thead>
<tr>
<th>Base Dose Ions/cm²</th>
<th>Emitter Anneal</th>
<th>Emitter ohms/sq</th>
<th>Base ohms/sq</th>
<th>Poly over Thin Oxide ohms/sq</th>
<th>Poly over Thick Oxide ohms/sq</th>
</tr>
</thead>
<tbody>
<tr>
<td>8E12</td>
<td>Furnace</td>
<td>508</td>
<td>9211</td>
<td>602</td>
<td>553</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1000°C</td>
<td>235</td>
<td>5602</td>
<td>246</td>
<td>249</td>
</tr>
<tr>
<td>1E13</td>
<td>Furnace</td>
<td>549</td>
<td>4925</td>
<td>677</td>
<td>673</td>
</tr>
<tr>
<td>1E13</td>
<td>RTP 1000°C</td>
<td>236</td>
<td>3756</td>
<td>242</td>
<td>247</td>
</tr>
<tr>
<td>5E13</td>
<td>Furnace</td>
<td>391</td>
<td>1132</td>
<td>563</td>
<td>560</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1000°C</td>
<td>230</td>
<td>1086</td>
<td>243</td>
<td>238</td>
</tr>
<tr>
<td>8E13</td>
<td>Furnace</td>
<td>343</td>
<td>620</td>
<td>549</td>
<td>545</td>
</tr>
<tr>
<td>8E13</td>
<td>RTP 1000°C</td>
<td>211</td>
<td>695</td>
<td>249</td>
<td>250</td>
</tr>
<tr>
<td>1E14</td>
<td>Furnace</td>
<td>387</td>
<td>801</td>
<td>699</td>
<td>553</td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1000°C</td>
<td>241</td>
<td>665</td>
<td>303</td>
<td>285</td>
</tr>
<tr>
<td>3E14</td>
<td>RTP 1000°C</td>
<td>244</td>
<td>290</td>
<td>251</td>
<td>256</td>
</tr>
</tbody>
</table>
### Table 4.4 Diffused Resistors Rs for Lot #2

<table>
<thead>
<tr>
<th>Base Dose Ions/cm²</th>
<th>Emitter Anneal</th>
<th>Emitter ohms/sq</th>
<th>Base ohms/sq</th>
<th>Poly over Thin Oxide ohms/sq</th>
<th>Poly over Thick Oxide ohms/sq</th>
</tr>
</thead>
<tbody>
<tr>
<td>8E12</td>
<td>Furnace</td>
<td>56</td>
<td>2541 *</td>
<td>317</td>
<td>380</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 950°C</td>
<td>262</td>
<td>17896 *</td>
<td>267</td>
<td>263</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1000°C</td>
<td>35</td>
<td>29474 *</td>
<td>216</td>
<td>214</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1050°C</td>
<td>5</td>
<td>14248 *</td>
<td>139</td>
<td>136</td>
</tr>
<tr>
<td>5E13</td>
<td>Furnace</td>
<td>247</td>
<td>4060</td>
<td>500</td>
<td>485</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 950°C</td>
<td>235</td>
<td>2876</td>
<td>244</td>
<td>244</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1000°C</td>
<td>138</td>
<td>2962</td>
<td>211</td>
<td>208</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1050°C</td>
<td>106</td>
<td>3000</td>
<td>118</td>
<td>117</td>
</tr>
<tr>
<td>1E14</td>
<td>Furnace</td>
<td>232</td>
<td>2534</td>
<td>402</td>
<td>391</td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1000°C</td>
<td>135</td>
<td>1741</td>
<td>196</td>
<td>192</td>
</tr>
</tbody>
</table>
One way to determine the individual monosilicon emitter sheet resistance is to consider that the measured emitter sheet resistance is the polysilicon sheet resistance in parallel with the monosilicon emitter sheet resistance. Therefore, if one knows the polysilicon sheet resistance over oxide, and if one also knows the combined sheet resistance of the two, then the sheet resistance of the monosilicon emitter alone can be determined using the relation below.

\[
\frac{1}{R_s (\text{poly \& monosilicon emitter})} = \frac{1}{R_s (\text{poly alone})} + \frac{1}{R_s (\text{emitter alone})} \quad (4.3)
\]

The depth of the emitter into the monosilicon can then be found by approximating the phosphorous impurity profile as a step junction. Considering that the concentration of phosphorous in this area is greater than boron by at least three orders of magnitude, the resistivity is found from the following equation if the mobility is read from the relation of mobility versus total impurity concentration.\(^{15}\)

\[
\rho = \frac{1}{q \mu_n n} \quad (4.4)
\]

The thickness of the emitter is then expressed as
Using approximated total impurity concentrations of $9 \times 10^{18}$ and $1 \times 10^{19}$ atoms/cm$^3$, the mobility of electrons was read as 125 and 120 cm$^2$/Vsec for the first and second lots respectively. The resistivity was calculated to be $5.6 \times 10^{-3}$ ohm-cm for the first lot and $5.2 \times 10^{-3}$ ohm-cm for the second lot. The calculated results for monosilicon emitter sheet resistance and junction depth using this calculated resistivity are shown for both lots using the diffused resistor data in Table 4.5 and 4.6.
Table 4.5 Lot #1 Calculated Monosilicon Emitter Sheet Resistance and Junction Depth

<table>
<thead>
<tr>
<th>Base Dose</th>
<th>Emitter Anneal</th>
<th>Emitter Sheet Rho</th>
<th>Junction Depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ions/cm²</td>
<td></td>
<td>ohms/sq</td>
<td>microns</td>
</tr>
<tr>
<td>8E12</td>
<td>Furnace</td>
<td>4195</td>
<td>.013</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1000°C</td>
<td>4483</td>
<td>.012</td>
</tr>
<tr>
<td>1E13</td>
<td>Furnace</td>
<td>2941</td>
<td>.019</td>
</tr>
<tr>
<td>1E13</td>
<td>RTP 1000°C</td>
<td>6424</td>
<td>.009</td>
</tr>
<tr>
<td>5E13</td>
<td>Furnace</td>
<td>1285</td>
<td>.044</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1000°C</td>
<td>5039</td>
<td>.011</td>
</tr>
<tr>
<td>8E13</td>
<td>Furnace</td>
<td>920</td>
<td>.061</td>
</tr>
<tr>
<td>8E13</td>
<td>RTP 1000°C</td>
<td>1353</td>
<td>.041</td>
</tr>
<tr>
<td>1E14</td>
<td>Furnace</td>
<td>1014</td>
<td>.055</td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1000°C</td>
<td>1337</td>
<td>.042</td>
</tr>
<tr>
<td>3E14</td>
<td>RTP 1000°C</td>
<td>6198</td>
<td>.009</td>
</tr>
</tbody>
</table>
Table 4.6 Lot #2 Calculated Monosilicon Emitter Sheet Resistance and Junction Depth

<table>
<thead>
<tr>
<th>Base Dose</th>
<th>Emitter Anneal</th>
<th>Emitter Sheet Rho ohms/sq</th>
<th>Junction Depth microns</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ions/cm²</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8E12</td>
<td>Furnace</td>
<td>67</td>
<td>.78</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 950°C</td>
<td>23143</td>
<td>.002</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1000°C</td>
<td>42</td>
<td>1.24</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1050°C</td>
<td>5.1</td>
<td>10.2</td>
</tr>
<tr>
<td>8E13</td>
<td>Furnace</td>
<td>495</td>
<td>.12</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 950°C</td>
<td>6371</td>
<td>.008</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1000°C</td>
<td>403</td>
<td>.13</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1050°C</td>
<td>1042</td>
<td>.050</td>
</tr>
<tr>
<td>1E14</td>
<td>Furnace</td>
<td>558</td>
<td>.093</td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1000°C</td>
<td>434</td>
<td>.12</td>
</tr>
</tbody>
</table>
It was found that the vertical npn transistors of the first lot yielded much lower gains compared to the second lot. In depth testing was, therefore, primarily focused on the second lot. No working pnp transistors were found on either lot. Almost all of the many different designs for vertical npn transistors tested on two of the best yielding wafers worked. The devices that had aluminum directly over the junction and devices that had the aluminum offset from the junction to prevent spiking both functioned. A few devices that did not work were found to have either a missing contact cut or metal which was left out by mistake at the time the test chip was created.

For the purpose of making a fair comparison of parameters between wafers, independent of the transistor design, one transistor that seemed to consistently yield was tested in depth on all wafers. The designed dimensions of this transistor in microns are an emitter 10 by 100, a base 100 by 155, and a collector 180 by 205. This transistor had aluminum directly over the junction. It is shown in Appendix A with a star next to it.

In order to get all the data before possible destruction during sinter, all the measurements were made for the first lot before sinter. Most of the measurements for the second lot were made before sinter, except for some maximum gains. The transistors did not function for some wafers after sinter for
the second lot so a few maximum gains were not obtainable. In these cases an Early voltage and corresponding gain are still available. The sinter process apparently destroyed some of the transistors, although strangely, the emitter-base diodes appeared to work for these devices. The shallow base-collector junctions which had aluminum directly over the junction may have been spiked instead. The resulting average values for the investigated parameters described in the characterization procedure in Table 4.7 and Table 4.8. Dotted lines indicate that the parameter is not available due to failure of transistor operation for the wafer, while a star indicates that the value is not a maximum gain, but just the best measured gain from a transistor characteristic for the wafer.
Table 4.7 Vertical Npn Parameters for Lot #1

<table>
<thead>
<tr>
<th>Base Dose Ions/cm²</th>
<th>Emitter Anneal</th>
<th>β V</th>
<th>Vₐ</th>
<th>BV_{CEO} V</th>
<th>BV_{CEO} V</th>
<th>BV_{EBO} V</th>
</tr>
</thead>
<tbody>
<tr>
<td>8E12</td>
<td>Furnace</td>
<td>---</td>
<td>---</td>
<td>&gt;100</td>
<td>29.4</td>
<td>2</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1000°C</td>
<td>11.6</td>
<td>129</td>
<td>&gt;100</td>
<td>26.7</td>
<td>7</td>
</tr>
<tr>
<td>1E13</td>
<td>Furnace</td>
<td>20.4</td>
<td>158</td>
<td>&gt;100</td>
<td>31.1</td>
<td>30</td>
</tr>
<tr>
<td>1E13</td>
<td>RTP 1000°C</td>
<td>18.8</td>
<td>128</td>
<td>&gt;100</td>
<td>26.3</td>
<td>7</td>
</tr>
<tr>
<td>5E13</td>
<td>Furnace</td>
<td>4.6</td>
<td>249</td>
<td>&gt;100</td>
<td>27.4</td>
<td>6</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1000°C</td>
<td>14.1</td>
<td>112</td>
<td>&gt;100</td>
<td>24.4</td>
<td>7</td>
</tr>
<tr>
<td>8E13</td>
<td>Furnace</td>
<td>2.6</td>
<td>68.8</td>
<td>&gt;100</td>
<td>18.5</td>
<td>3</td>
</tr>
<tr>
<td>8E13</td>
<td>RTP 1000°C</td>
<td>---</td>
<td>---</td>
<td>&gt;100</td>
<td>25.3</td>
<td>3</td>
</tr>
<tr>
<td>1E14</td>
<td>Furnace</td>
<td>.36</td>
<td>32.1</td>
<td>&gt;100</td>
<td>25.7</td>
<td>4</td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1000°C</td>
<td>4.5</td>
<td>114</td>
<td>&gt;100</td>
<td>25.0</td>
<td>5</td>
</tr>
<tr>
<td>3E14</td>
<td>RTP 1000°C</td>
<td>1.6</td>
<td>154</td>
<td>&gt;100</td>
<td>25.5</td>
<td>4</td>
</tr>
</tbody>
</table>

94
<table>
<thead>
<tr>
<th>Base Dose</th>
<th>Emitter Anneal</th>
<th>$\beta_{max}$</th>
<th>$V_A$</th>
<th>$\beta_{max}$ * $V_A$</th>
<th>$BV_{CEO}, BV_{CEB}, BV_{EBB}$</th>
<th>$I_{CEO}$</th>
<th>$\eta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ions /cm²</td>
<td></td>
<td></td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>A/cm²</td>
<td></td>
</tr>
<tr>
<td>8E12</td>
<td>Furnace</td>
<td>24.0</td>
<td>0.8</td>
<td>*</td>
<td>&gt;100</td>
<td>2.8</td>
<td>3.2E-6</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 950°C</td>
<td>34.8</td>
<td>12.5</td>
<td>435</td>
<td>&gt;100</td>
<td>13.0</td>
<td>1.3E-6</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1000°C</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>&gt;100</td>
<td>8.0</td>
<td>3.2E-6</td>
</tr>
<tr>
<td>8E12</td>
<td>RTP 1050°C</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>&gt;100</td>
<td>1.63</td>
<td>4.6E-6</td>
</tr>
<tr>
<td>5E13</td>
<td>Furnace</td>
<td>392</td>
<td>165</td>
<td>64680</td>
<td>&gt;100</td>
<td>17.4</td>
<td>6.4E-5</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 950°C</td>
<td>7.8</td>
<td>240</td>
<td>1872</td>
<td>&gt;100</td>
<td>23</td>
<td>6.0E-6</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1000°C</td>
<td>7.8</td>
<td>32.1</td>
<td>*</td>
<td>&gt;100</td>
<td>22.5</td>
<td>4.2E-5</td>
</tr>
<tr>
<td>5E13</td>
<td>RTP 1050°C</td>
<td>325</td>
<td>32.7</td>
<td>10628</td>
<td>&gt;100</td>
<td>22.5</td>
<td>9.2E-5</td>
</tr>
<tr>
<td>1E14</td>
<td>Furnace</td>
<td>120</td>
<td>79.1</td>
<td>9492</td>
<td>&gt;100</td>
<td>25.6</td>
<td>2.6E-5</td>
</tr>
<tr>
<td>1E14</td>
<td>RTP 1000°C</td>
<td>58.4</td>
<td>64.1</td>
<td>3743</td>
<td>&gt;100</td>
<td>23.5</td>
<td>8.7E-5</td>
</tr>
</tbody>
</table>
The collector to substrate breakdown voltages were greater than 100 volts for each of the two lots. It should also be mentioned the non-ideality factor in a couple cases is less than 1. This factor should always be 1 or greater, so these values can be assumed to be 1+ since there was most likely some slight error in the way the slope was taken to determine $\eta$.

The best characteristics came from the wafer that had a base dose of $5 \times 10^{13}$ ions/cm$^2$ and was furnaced annealed. The characteristic plots for this wafer will, therefore, be shown at this time. The characteristics for the remaining wafers and raw electrical data are shown in Appendix E.

**Figure 4.5 Best Wafer Transistor Characteristic**
Figure 4.6 Best Wafer Maximum Gain

Figure 4.7 Best Wafer $B_{V_{CBO}}$ and $B_{V_{EBO}}$
Figure 4.8 Best Wafer $BV_{CEO}$

Figure 4.9 Best Wafer Gummel Plot
4.3 TEM Physical Analysis

Four cross section samples containing the interfacial oxide were prepared at IBM East Fishkill for transmission electron microscopy. The samples included interfaces with the 875°C furnace emitter anneal; 950°C, 1000°C, and 1050°C RTP emitter treatment. The following TEM photos below show the effect of temperature on the uniformity of the interfacial oxide.
Figure 4.11 TEM for 875°C Emitter Furnace Anneal

Figure 4.12 TEM for 950°C Emitter RTP Anneal
Figure 4.13 TEM for 1000°C Emitter RTP Anneal

Figure 4.14 TEM for 1050°C Emitter RTP Anneal
5.0 Discussion

The final inline junction depths show that the designed base widths are quite narrow. Subtraction of emitter-base junction depths from the base-collector junction depths show that the base widths range from .15 to .67 microns for the first lot, and .46 to .73 microns for the second lot. The furnace process seems to have a general trend of creating wider bases than RTP for both lots. This could be possible since the high RTP temperature should serve to remove remaining boron interstitials and hinder further movement of the base-collector junction during the emitter anneal as described earlier. The emitter-base depths seem to be on average a little greater than .2 microns for both lots. For the first lot there is no general trend as to which type of anneal, furnace or RTP, caused a deeper emitter-base junction, however, for the second lot the RTP process looks to have created deeper junctions. The collector-substrate junction depth looks reasonable for both lots. All depths are greater than SUPREM calculated and this was somewhat expected. SUPREM simulation showed quite shallow base-collector junctions of no more than .66 microns for the 55 minute 900°C anneal. The actual junctions possibly went deeper than the simulation showed because of implant damage from the base and collector implants present at the time of the base anneal. For the first
lot by looking at earlier inline process data one will see that an error in junction depth measurement was most likely made. With the amount of error possible in the staining technique used to arrive at these depths no generalizing conclusions should be made about this data.

By examining the final inline sheet resistance data in Appendix D as well as Figures 4.1-4.4, one can see that the control wafer base sheet resistance measurements demonstrate the expected relation that as the base dose is increased the base sheet resistance decreases. This is more apparent for the first lot, with the second lot showing a peculiar nonlinear relation. One can also see that the RTP emitter anneal seems to have resulted in a lower base sheet resistance than the furnace emitter anneal, in almost every different base dose case. The results for the emitter sheet resistance after the emitter anneal show another interesting pattern. The RTP anneal at 1000°C appears to have been effective in producing a lower emitter sheet resistance for the first lot. For the second lot, however, the RTP anneal at 950°C anneal was most likely too low a temperature for such a short duration to sufficiently anneal the emitter, since this treatment has the highest sheet resistance. The other two RTP temperatures yield lower results than the furnace anneal. These two temperatures are definitely high enough to breakup the interfacial oxide which lowers the emitter resistance. For the RTP case the
polysilicon over oxide sheet resistance is about half the emitter resistance. The emitter resistance should be lower since it is the parallel combination of the monosilicon emitter resistance and the polysilicon alone resistance. There are no obvious explanations for this. Compared to SUPREM results, the actual furnace sheet resistances are much higher and this was expected because SUPREM assumes full dopant activation and does not model the effects of the interfacial oxide layer. The simulated polysilicon sheet resistance alone was much lower than actual results, while the emitter sheet resistance was much higher than actual results. This happens because SUPREM calculates the polysilicon and monosilicon emitter sheet resistances separately.

The sheet resistance data determined from the diffused resistor data shown in Tables 4.3 and 4.4 is a little higher in value on average when compared to the control wafer data. This may be due to an invalid assumption about the number of squares per resistor, considering the changes in line width caused by lithography, and to some contact resistance. The same relations, however, seem to exist between RTP and furnace anneal results as previously mentioned. The base resistance measurements are extremely high in the case of the base dose 8E12 ions/cm². The base resistor characteristics for the second lot in particular were not linear at this base dose. The base pinch resistance for this dose, based upon these
extrinsic sheet resistance results, would be quite high, making this dose undesirable. The emitter resistance is lower than the polysilicon over oxide sheet resistance as should be expected. For this reason, this electrical test data was used to calculate the monosilicon emitter sheet resistance and junction depth. The junction depths in Tables 4.5 and 4.6 seem to be of the right magnitude, although a little shallow for the first lot and quite deep in just a couple cases for the lowest base dose of the second lot. It should be mentioned that the second lot received a higher phosphorous emitter implant dose. The extremely deep junctions could be explained by a slight error in measuring the emitter resistance which would throw off the parallel combination calculation by a large degree. There may also be problems with this method if epitaxial alignment of the polysilicon has occurred. The thicknesss of the polysilicon would then be different than that used in the calculations.

The vertical npn characteristics for the first lot in Table 4.7 are not too impressive. The second lot was started because it was suspected that the base widths for this lot were too wide due to the base anneal. The inline base-collector junction depth measurements for the first lot after the base anneal showed very deep junctions far greater than 1 micron. The final measurements on the junctions repeated a number of times did not appear as deep. Based on the low gains
achieved, it is expected that the actual junctions are deeper than the final values showed, but probably not as great as the first inline measurements. The highest gains for the first lot occur for one of the lower base doses, 1E13 ions/cm². With such wide base widths at the higher doses, this would be expected. The Early voltages are high enough to be acceptable for analog applications. All collector-base junction breakdown voltages are greater than 100 volts. The breakdown voltages for the emitter-base junction should typically be between 6 and 8 volts. Many of the wafers show too low of values for this parameter, which is possibly related to the shallow emitter junctions. The lower values for the higher base doses are an indication that the drive-in step for the base did not sufficiently reduce the surface concentration of boron, which is directly related to the breakdown voltage. The smallest value, however, occurred for the lowest base dose and this furnace annealed wafer did not have any functioning npn transistors. The wafer with the highest transistor gain also had the highest value for $B_{EE}$: and one of the smaller base doses. This is what should be expected. The values for $B_{EE}$ are fairly high and in order to determine whether breakdown was due to avalanche multiplication or punchthrough, equations 3.1 through 3.3 and SUPREM impurity concentrations were used to calculate the extension of the base-collector depletion width on the base side using the worst case punchthrough
scenario wafers of $BV_{CEO}$ equal to 29.4 and 31.1 volts. The values turn out to be .43 and .27 microns, with the corresponding determined base widths of .15 and .37 microns. This shows that breakdown is due to punchthrough in the first case and avalanche multiplication in the second case.

The vertical npn characteristics for the second lot in Table 4.8 are much better. Clearly the dose of 8E12 ions/cm² was not a good choice, since two of the wafers that even functioned have very low gains and unacceptable Early voltages. The Early voltages are poor because this base dose seems to be too low for such a narrow base width. The set of wafers that received the dose of 5E13 ions/cm² show extremely good gains. The furnaced annealed devices of this dose have the highest maximum gains and second best Early voltages. The product of these two parameters, which shows the effect of the polysilicon emitter alone, is 64680. The RTP 1050°C annealed devices also have good gains, but the Early voltages would barely be acceptable for analog applications. The dose of 1E14 ions/cm² yielded average gains. In this case the furnaced annealed wafers showed the best gains and Early voltages again, but the highest RTP temperature anneal is not available for comparison due to wafer breakage. It should be pointed out that the remarkable gains are not necessarily due to the interfacial oxide since the highest gains were achieved by furnace emitter anneal and RTP at a temperature of 1050°C,
which is high enough to destroy the interfacial oxide. The contributions from the other characteristics of the polysilicon emitter most likely play a role as well.

The collector-base junction breakdown voltages are greater than 100 volts. These are not sharp clean breakdowns in many cases. The emitter-base breakdown voltages for the 8E12 ions/cm² dose are quite high showing very low boron surface concentrations. The rest of the wafers have average BV_{EEO} values. The values for BV_{CEO} are quite low for the 8E12 ions/cm² dose. Since the wafers from this group did not function or had poor gains, it is likely that punchthrough occurred. This was shown to be possible in the calculations made in the experimental design. Equations 3.1 through 3.3 were again used to calculate the extension of the base-collector depletion width on the base side for two likely punchthrough cases. The first case considered was a nonfunctioning wafer with a base of 8E12 ions/cm² and a BV_{CEO} equal to 1.63 volts. X_{PBC} was found to be .10 microns. For the same base dose and BV_{CEO} of 13 volts, X_{PBC} was found to be .29 microns. The base width is not known directly from measurement for these two RTP temperatures, but guessed to be around .15 microns based on the RTP 1000°C junction measurements. Punchthrough is questionable in the first case and likely the cause for breakdown in the second case.

The highest leakage current density for the whole lot was
9.2E-5 Amps/cm², which is low. The non-ideality factors are in general low, showing that the implant damage from the base implant in the base-emitter depletion region was sufficiently annealed. The highest value for each different base dose was the RTP 950°C case, which may not have been a high enough temperature at such a short time to further anneal the base implant. As mentioned before a value less than 1 shows an error in the gradient measurement and must be considered to be slightly greater than 1.

The TEM analysis shows no major difference between any of the four different emitter anneals. The interfacial oxide is present on all four samples and appears to be continuous. The TEM, however, was done at low magnification due to equipment difficulties so the breakup of the oxide may be difficult to see. Breakup of the interfacial oxide should have occurred at the two highest RTP temperatures. The presence of the interfacial oxide at these higher anneal temperatures may have played a role in the gain.
6.0 Conclusions

Of the investigated base implant doses, it appears that a dose of 5E13 ions/cm² or slightly higher yields the best gains and Early voltage characteristics for this shallow emitter process. Rapid thermal processing seems to be quite valuable for lowering the emitter sheet resistance. Breakup of the interfacial oxide appears to be a questionable factor in this. RTP is only useful in the fabrication of PETs, however, if the proper amount of time and temperature is selected in order to drive the impurities far enough. Furnace annealing appears to have better results than RTP if adequate RTP parameters are not used.
7.0 Suggestions for Future Work

Future work at RIT involving bipolar junction transistors utilizing polysilicon emitters, based upon this experimental work, should use a base dose of approximately 7E13 ions/cm². With the anneal times and temperatures used in this investigation, this should increase the magnitude of the Early voltage with a slight decrease in gain. Rapid thermal oxidation/annealing might also be incorporated into the base anneal process in order to accommodate a higher base dose to prevent punchthrough with a still relatively narrow base width.
8.0 References

(1) C. R. Selvakumar, "Theoretical and Experimental Aspects of Polysilicon Emitter Bipolar Transistors," manuscript received by IEEE, November 1988.


(13) C. R. Selvakumar, unpublished work.


(27) T. Maeda et al. "Poly Si-Si Interfacial Oxide Ball-up Mechanism and Its Control of 0.8 um BiCMOS VLSI's," *IEEE Bipolar Circuits and Technology Meeting*, pp. 102-105, 1989.


9.0 Appendix A

Test Chip Design
9.0 Appendix B

SUPREM Simulation Input Files and Profiles
The simulation input files and profiles are arranged in the following order. Only two example input files are included to avoid redundancy.

(1) The input file for the first process lot for the region under the emitter. (The base dose was changed for each of the six cases.)

(2) Six profiles under the emitter for each of the six base doses.

(3) The input file for the second process lot for the region under the emitter, showing the improvement made to the base anneal and the emitter dose and energy. (The input file includes two emitter anneals. One for the furance anneal and a second for the capping oxide growth prior to RTP. One was selected and the other commented out depending upon the simulation. In order to simulate under the extrinsic base and etc., for each different base dose, appropriate sections such as etch steps were commented out.)

(4) Eight profiles for each of the three base doses for the furnace anneal case including; the region under the emitter, under the extrinsic base with no poly on top, under the
extrinsic base with poly on top, under the collector, under the collector contact, under the field, hole and electron profiles, and the base resistance relation.
TITLE **********POLYSILICON EMITTER TRANSISTOR BJT PROCESS**********
COMMENT CREATED BY DIANE MAUERSBERG
COMMENT ELECTRICAL ENGINEERING MASTERS THESIS
COMMENT FILENAME: BJTEBC1.IN
COMMENT DATE 9/1/92
COMMENT SIMULATION UNDER THE EMITTER
$
$************************************************************
$INITIALIZE <100> SILICON RESISTIVITY BORON=8.0 THICKNESS=12.0 DX=.04$
$
$(STEP 1SCRIBE AND FOUR POINT PROBE)$
$
$(STEP 2 RCA CLEAN)$
$
$(STEP 3 COLLECTOR MASKING OXIDE GROWTH)$
$
COMMENT PUSH WAFERS IN AT 900C IN NITROGEN
DIFFUSION TIME=11.4 TEMP=900 T.RATE=17.5 NITROGEN
DIFFUSION TIME=10.0 TEMP=1100 DRYO2
DIFFUSION TIME=10.0 TEMP=1100 WETO2
DIFFUSION TIME=16.0 TEMP=1100 DRYO2
DIFFUSION TIME=6.0 TEMP=1100 T.RATE=6.0 NITROGEN
COMMENT PULL WAFERS OUT AT 1000C IN NITROGEN
PRINT LAYERS ELECTRICAL
$
$MEASURE CONTROL WAFERS FOR OXIDE THICKNESS
$
$(STEP 4 COLLECTOR LITHOGRAPHY)$
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
$
$(STEP 5 COLLECTOR OXIDE ETCH LEAVING RESIST ON FOR IMPLANT)$
ETCH OXIDE ALL
$
$(STEP 6 IMPLANT PHOSPHOROUS SPECIES P31 IN COLLECTOR REGIONS)$
IMPLANT PHOSPHOROUS ENERGY=110 DOSE=8E12
PRINT LAYERS ELECTRICAL
EXTRACT NAME=XRCS NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=CRS E.RESIST LAYER=1 MIN.REGION=2
COMMENT PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLOT.OUT=PL0T1.PLT
$TITLE "REGION UNDER THE EMITTER - POST COLLECTOR IMPLANT"
$LABEL LABEL =" WELL SUBSTRATE JUNCTION DEPTH:" @XRCS" MICRONS"
$LABEL LABEL =" INNER COLLECTOR SHEET RESISTANCE:" @CRS"OHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
$
$(STEP 7 STRIP RESIST (DO NOT ETCH OXIDE) AND RCA CLEAN)$
COMMENT ETCH OXIDE OFF APPROPRIATE CONTROLS
$
$(STEP 8 DRIVE-IN OF COLLECTOR AND GROWTH OF BASE MASKING OXIDE)$
COMMENT PUSH WAFERS IN AT 900C IN NITROGEN
DIFFUSION TIME=12.1 TEMP=900 T.RATE=18.6 NITROGEN
DIFFUSION TIME=60 TEMP=1125 NITROGEN
DIFFUSION TIME=400 TEMP=1125 DRYO2
DIFFUSION  TIME=2340 TEMP=1125 NITROGEN
DIFFUSION  TIME=18.1 TEMP=1125 T RATE=-6.9 NITROGEN
COMMENT  FULL WAFERS OUT AT 100OC
PRINT LAYERS ELECTRICAL
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=CRS E.RESIST LAYER=1 MIN.REGION=2
COMMENT PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLOT.OUT=PLT2.PLT
$+TITLE ="REGION UNDER THE EMITTER - POST COLLECTOR DRIVE-IN"
$LABEL LABEL =" WELL SUBSTRATE JUNCTION DEPTH:" @XJCS" MICRONS"
$LABEL LABEL =" INNER COLLECTOR SHEET RESISTANCE:" @CRS"OHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
$
$ *MEASURE CONTROL WAFERS FOR OXIDE THICKNESS
$ *MEASURE CONTROL WAFERS FOR COLLECTOR JUNCTION DEPTH AND SHEET RESISTANCE
$
$(STEP 9 BASE LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
$(STEP 10 BASE OXIDE ETCH LEAVING RESIST ON FOR IMPLANT)
ETCH OXIDE ALL
$
$(STEP 11 BASE IMPLANT BORON SPECIES BF2)
IMPLANT BF2 ENERGY=35 DOSE=8E12
PRINT  LAYERS ELECTRICAL
EXTRACT NAME=XJBC NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0 X.MIN=@XJBC+.001
EXTRACT NAME=CRS E.RESIST LAYER=1 MIN.REGION=2
EXTRACT NAME=CRS E.RESIST LAYER=1 MAX.REGION=2
COMMENT PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLOT.OUT=PLT3.PLT
$+TITLE ="REGION UNDER THE EMITTER - POST BASE IMPLANT"
$+RIGHT =10
$LABEL LABEL =" BASE-COLLECTOR JUNCTION DEPTH:" @XJBC" MICRONS"
$LABEL LABEL =" WELL-SUBSTRATE JUNCTION DEPTH:" @XJCS" MICRONS"
$LABEL LABEL =" INNER BASE SHEET RESISTANCE:" @BRS"OHMS/SQ"
$LABEL LABEL =" INNER COLLECTOR SHEET RESISTANCE:" @CRS"OHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
$
$(STEP 12 STRIP RESIST AND RCA CLEAN)
$
$(STEP 13 DRIVE-IN OF BASE/ANNEAL AND GROWTH OF EMITTER MASKING OXIDE)
COMMENT  PUSH WAFERS IN AT 900C IN NITROGEN
DIFFUSION TIME=10 TEMP=900 DRY02
DIFFUSION TIME=35 TEMP=900 WET02
DIFFUSION TIME=10 TEMP=900 DRY02
COMMENT  PULL WAFERS OUT AT 900C IN NITROGEN
PRINT  LAYERS ELECTRICAL
EXTRACT NAME=XJBC NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0 X.MIN=@XJBC+.001
EXTRACT NAME=CRS H.RESIST LAYER=1 MIN.REGION=2
EXTRACT NAME=CRS E.RESIST LAYER=1 MAX.REGION=2
COMMENT  PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLOT.OUT=PLT4.PLT
$+TITLE ="REGION UNDER THE EMITTER - POST BASE ANNEAL"
$+RIGHT =10
$LABEL LABEL =" BASE-COLLECTOR JUNCTION DEPTH:" @XJBC" MICRONS"
$LABEL LABEL =" WELL-SUBSTRATE JUNCTION DEPTH:" @XJCS" MICRONS"
$LABEL LABEL =" INNER BASE SHEET RESISTANCE:" @BRS"OHMS/SQ"
$LABEL LABEL =" INNER COLLECTOR SHEET RESISTANCE:" @CRS"OHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
$
$ *MEASURE CONTROL WAFERS FOR OXIDE THICKNESS
$ *MEASURE CONTROL WAFERS FOR COLLECTOR JUNCTION DEPTH AND SHEET RESISTANCE
$ 
$(STEP 14 BURIED CONTACT LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH . PHOTORESIST ALL
$
$(STEP 15 OXIDE ETCH FOR BURIED CONTACTS)
ETCH OXIDE ALL
$
$(STEP 16 STRIP RESIST AND RCA CLEAN NONSTANDARD FOR INTERFACIAL OXIDE)
$
$(STEP 17 DEPOSITION OF POLYSILICON FOR EMITTER)
DEPOSITION POLYSILICON TEMP=610 THICKNESS=.40
$
$ *MEASURE CONTROL WAFERS FOR POLYSILICON THICKNESS
$ *MEASURE CONTROL WAFERS FOR COLLECTOR AND BASE JUNCTION DEPTHS AND SHEET RESISTANCE
$
$(STEP 18 IMPLANT POLYSILICON WITH PHOSPHOROUS SPECIES P31)
IMPLANT PHOSPHOROUS ENERGY=45 DOSE=4E15
PRINT LAYERS ELECTRICAL
EXTRACT NAME=XJBC NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0 X.MIN=XJBC+.001
EXTRACT NAME=PRS E.RESIST LAYER=2 MAX.REGION=1
EXTRACT NAME=BRS H.RESIST LAYER=1 MIN.REGION=2
EXTRACT NAME=CRS E.RESIST LAYER=1 MAX.REGION=2
COMMENT PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
*PLOT NET ACTIVE PLOT.OUT=PLOTS5.PLT
$TITLE ="REGION UNDER THE EMITTER AFTER POLYSILICON IMPLANT"
$RIGHT =10
$LABEL LABEL =" " BASE-COLLECTOR JUNCTION DEPTH: "@XJBC" MICRONS"
$LABEL LABEL =" " WELL-SUBSTRATE JUNCTION DEPTH: "@XJCS" MICRONS"
$LABEL LABEL =" " POLY SHEET RESISTANCE: "@PRS" OHMS/SQ"
$LABEL LABEL =" " INNER BASE SHEET RESISTANCE: "@BRS" OHMS/SQ"
$LABEL LABEL =" " INNER COLLECTOR SHEET RESISTANCE: "@CRS" OHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
$+PAUSE
$
$(STEP 19 EMITTER LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
$****STEP MASKED OUT
$****ETCH PHOTORESIST ALL
$
$(STEP 20 ETCH POLYSILICON FOR EMITTER AND COLLECTOR CONTACTS)
$****STEP MASKED OUT
$****ETCH POLYSILICON ALL
$
$ *MEASURE CONTROL WAFERS FOR OXIDE CONSUMED DURING POLYSILICON ETCH
$
$(STEP 21 RESIST STRIP AND RCA CLEAN)
ETCH PHOTORESIST ALL
$
$(STEP 22 EMITTER ANNEAL)
COMMENT *** RAPID THERMAL ANNEALING CYCLES FOR SELECT WAFERS ***
COMMENT *** CAPPING OXIDE GROWTH PRIOR TO LTO AND RTP CYCLE ***
$****
$**** COMMENT PUSH WAFERS IN AT 800C IN NITROGEN
$**** DIFFUSION TIME=10 TEMP=800 N2
$**** DIFFUSION TIME=25 TEMP=800 WETO2
$**** DIFFUSION TIME=5 TEMP=800 N2
$**** COMMENT PULL WAFERS OUT AT 800C IN NITROGEN
$
$ * * OR * *
*** FURNACE ANNEAL ***

*** FOR SELECT WAFERS NON RTP WAFERS ***

DIFFUSION
TIME=50 TEMP=875 NITROGEN

DIFFUSION
TIME=40 TEMP=875 WETO2

DIFFUSION
TIME=10 TEMP=875 DRYO2

DIFFUSION
TIME=20 TEMP=875 NITROGEN

COMMENT
PULL WAFERS OUT AT 875C IN NITROGEN

PRINT
LAYERS ELECTRICAL

EXTRACT
NAME=XJEB NET ACTIVE X.MIN=0 X.MAX=XJEB+.001

EXTRACT
NAME=XJBC NET ACTIVE X.MIN=0 X.MAX=XJBC+.001

EXTRACT
NAME=PRS E.RESIST LAYER=2 MAX.REGION=3

EXTRACT
NAME=ERS E.RESIST LAYER=1 MIN.REGION=1

EXTRACT
NAME=BRS H.RESIST LAYER=1 MIN.REGION=2

EXTRACT
NAME=CRS E.RESIST LAYER=1 MAX.REGION=2

ASSIGN
NAME=IBASE N.VALUE=ABS(IBASE)

ASSIGN
NAME=BASE N.VALUE=ABS(IBASE)

COMMENT
PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS

PLOT
NET ACTIVE PLOT.OUT=PLOT6.FLT

+TITLE ="FINAL RESULTS UNDER THE EMITTER"

+RIGHT =10

+DEVICE ="HP7550"

LABEL
LABEL ="EMITTER-BASE XJ: "XJEB" MICRONS"

LABEL
LABEL ="BASE-COLLECTOR XJ: "XJBC" MICRONS"

LABEL
LABEL ="WELL-SUBSTRATE XJ: "XJCS" MICRONS"

LABEL
LABEL ="POLY SRHO: "PRS" OHMS/SQ"

LABEL
LABEL ="EMITTER SRHO: "ERS" OHMS/SQ"

LABEL
LABEL ="INNER BASE SRHO: "BRS" OHMS/SQ"

LABEL
LABEL ="INNER COLLECTOR SRHO: "CRS" OHMS/SQ"

LABEL
LABEL ="BASE DOE AND ENERGY: 8E12, 35KEV"

LABEL
LABEL ="BASE ANNEAL TIME/TEMP: 55 MIN, 900C"

LABEL
LABEL ="EMITTER DOE AND ENERGY: 4E15, 45KEV"

LABEL
LABEL ="EMITTER ANNEAL TIME/TEMP: 120MIN, 875C"

LABEL
LABEL ="BASE WIDTH: "BASEW" MICRONS"

LABEL
LABEL ="INTEGRATED BASE: "IBASE"

LABEL
LABEL ="EMITTER" X=1 Y=1E19

LABEL
LABEL ="BASE" X=.8 Y=5E16

LABEL
LABEL ="COLLECTOR" X=1.50 Y=2E15

PLOT
CHEMICAL BORON COLOR=2 LINE=2 ADD

PLOT
CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD

+FAUSE

PLOT
NET ACTIVE PLOT.OUT=PLOT7.FLT

+TITLE ="FINAL RESULTS UNDER THE EMITTER"

+RIGHT =2

+DEVICE ="REGIS"

LABEL
LABEL ="EMITTER-BASE XJ: "XJEB" MICRONS"

LABEL
LABEL ="BASE-COLLECTOR XJ: "XJBC" MICRONS"

LABEL
LABEL ="WELL-SUBSTRATE XJ: "XJCS" MICRONS"

LABEL
LABEL ="POLY SRHO: "PRS" OHMS/SQ"

LABEL
LABEL ="EMITTER SRHO: "ERS" OHMS/SQ"

LABEL
LABEL ="INNER BASE SRHO: "BRS" OHMS/SQ"

LABEL
LABEL ="INNER COLLECTOR SRHO: "CRS" OHMS/SQ"

LABEL
LABEL ="BASE DOE/ ENERGY: 8E12, 35KEV"

LABEL
LABEL ="BASE ANNEAL: 55 MIN, 900C"

LABEL
LABEL ="EMITTER DOE/ENERGY: 4E15, 45KEV"

LABEL
LABEL ="EMITTER ANNEAL: 120MIN, 875C"

LABEL
LABEL ="BASE WIDTH: "BASEW" MICRONS"

LABEL
LABEL ="INTEGRATED BASE: "IBASE"
+PAUSE
$
COMMENT PLOTTING ELECTRON AND HOLE DISTRIBUTIONS
ELECTRICAL ELECTRON HOLE DISTRIBUTION FILE=D.DAT EXTENT=12
BIAS LAYER=1 V=5 DV=0 ABSCISSA
END ELECTRICAL
PLOT FILE=D.DAT ELECTRON PLOT.OUT=PLOTS.PLT
+TITLE ^="ELECTRON AND HOLE DISTRIBUTIONS,BASE DOSE=8E12"
+RIGHT =2 BOTTOM=1E13
+DEVICE ^="REGIS"
PLOT FILE=D.DAT HOLE COLOR=2 LINE=2 ADD
PLOT NET ACTIVE COLOR=3 LINE=3 ADD
+PAUSE
$
COMMENT PLOTTING BASE RESISTANCE
$(SOLVING POISSON'S EQUATION WHEN THE COLLECTOR VOLTAGE IS RAMPED
$ FROM 0 TO 5 VOLTS)
ELECTRICAL EXTENT=3 STEPS=6 FILE=E.DAT
BIAS LAYER=1 REGION=2 V=0 DV=1 ABSCISSA
END ELECTRICAL
PLOT FILE=E.DAT H.RESIST LAYER=1 MIN REGION=2
+PLOT.OUT=PLOT9.PLT
+TITLE ^="BASE RESISTANCE WITH BASE DOSE=8E12"
+BOTTOM =1E0 TOP=3E5 ^y.LOG SYMBOL=1
+DEVICE ^="REGIS"
$ *MEASURE CONTROL WAFERS FOR OXIDE THICKNESS
$ *MEASURE CONTROL WAFERS FOR FINAL COLLECTOR, BASE, AND EMITTER JUNCTION
$ DEPTH AND SHEET RESISTANCE
$
$(STEP 23 CONTACT CUT LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
$
$(STEP 24 OXIDE ETCH FOR CONTACTS)
ETCH OXIDE ALL
$
$(STEP 25 RESIST STRIP AND RCA CLEAN)
$
$(STEP 26 DEPOSITION OF ALUMINUM)
DEPOSITION ALUMINUM THICKNESS=.8
$
$(STEP 27 VARIABLE SINTER MAXIMUM 450C 20 MINUTES IN H2/N2)
$
$(STEP 28 METAL LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
$
$(STEP 29 ALUMINUM ETCH)
ETCH ALUMINUM
$
$(STEP 30 RESIST STRIP)
$
STOP
FINAL RESULTS UNDER THE EMITTER

Figure 9B.1 Lot #1 Base Dose = 8E12 ions/cm²

Figure 9B.2 Lot #1 Base Dose = 1E13 ions/cm²
FINAL RESULTS UNDER THE EMITTER

**Figure 9B.3** Lot #1 Base Dose = 5E13 ions/cm²

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FINAL RESULTS UNDER THE EMITTER

**Figure 9B.4** Lot #1 Base Dose = 8E13 ions/cm²
Figure 9B.5 Lot #1 Base Dose = 1E14 ions/cm²

Figure 9B.6 Lot #1 Base Dose = 3E14 ions/cm²
INITIALIZE <100> SILICON RESISTIVITY BORON=8.0 THICKNESS=12.0 DX=.04

$ (STEP 1 Scribe and Four Point Probe) $

$ (STEP 2 RCA Clean) $

$ (STEP 3 Collector Masking Oxide Growth) $

COMMENT PUSH WAFERS IN AT 900C IN NITROGEN
DIFFUSION TIME=11.4 TEMP=900 T.RATE=17.5 NITROGEN
DIFFUSION TIME=10.0 TEMP=1100 DRY02
DIFFUSION TIME=90.0 TEMP=1100 WET02
DIFFUSION TIME=10.0 TEMP=1100 DRY02
DIFFUSION TIME=16.8 TEMP=1100 T.RATE=-6.0 NITROGEN
COMMENT PULL WAFERS OUT AT 1000C IN NITROGEN
PRINT LAYERS ELECTRICAL
$ *

$ *MEASURE CONTROL WAFERS FOR OXIDE THICKNESS *

$ (STEP 4 Collector Lithography)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
$

$ (STEP 5 Collector Oxide Etch Leaving Resist On For Implant) $
ETCH OXIDE ALL
$

$ (STEP 6 Implant Phosphorus Species P31 In Collector Regions) $
IMPLANT PHOSPHOROUS ENERGY=110 DOSE=8E12
PRINT LAYERS ELECTRICAL
EXTRACT NAME=XJCS NET ACTIVE X. EXTRACT Y=0
EXTRACT NAME=CRS E. RESIST LAYER=1 MIN. REGION=2
COMMENT PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLO1.OUT=PLOT1.PLT
$TITLE =$REGION UNDER THE Emitter POST COLLECTOR IMPLANT"
$LABEL LABEL =" WELL SUBSTRATE JUNCTION DEPTH: " @XJCS" MICRONS"
$LABEL LABEL =" INNER COLLECTOR SHEET RESISTANCE: " @CRS"OHMS/SO"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
$

$ (STEP 7 Strip Resist (Do Not Etch Oxide) and RCA Clean) $
COMMENT ETCH OXIDE OFF APPROPRIATE CONTROLS
$

$ (STEP 8 Drive-In of Collector and Growth of Base Masking Oxide) $
COMMENT PUSH WAFERS IN AT 900C IN NITROGEN
DIFFUSION TIME=12.1 TEMP=900 T.RATE=18.6 NITROGEN
DIFFUSION TIME=400 TEMP=1125 NITROGEN
DIFFUSION TIME=2340 TEMP=1125 NITROGEN
DIFFUSION TIME=18.1 TEMP=1125 T.RATE=-6.9 NITROGEN
COMMENTS PULL WAFERS OUT AT 1000C
PRINT LAYERS ELECTRICAL
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=CRS E.RESIST LAYER=1 MIN_REGION=2
COMMENTS PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLOT.OUT=PLT2.PLT
$TITLE ="REGION UNDER THE EMITTER - POST COLLECTOR DRIVE-IN"
$LABEL LABEL="WELL SUBSTRATE JUNCTION DEPTH: " @XJCS" MICRONS"
$LABEL LABEL="INNER COLLECTOR SHEET RESISTANCE:" @CRS"OMHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD

$ MEASURE CONTROL WAFERS FOR OXIDE THICKNESS
$ MEASURE CONTROL WAFERS FOR COLLECTOR JUNCTION DEPTH AND SHEET RESISTANCE
($STEP 9 BASE LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
($STEP 10 BASE OXIDE ETCH LEAVING RESIST ON FOR IMPLANT)
ETCH OXIDE ALL
($STEP 11 BASE IMPLANT BORON SPECIES BF2)
IMPLANT BF2 ENERGY=35 DOSE=8E12
PRINT LAYERS ELECTRICAL
EXTRACT NAME=XJBC NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0 X.MIN=@XJBC+.001
EXTRACT NAME=BRX H.RESIST LAYER=1 MIN_REGION=2
EXTRACT NAME=CRS E.RESIST LAYER=1 MAX_REGION=2
COMMENTS PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLOT.OUT=PLT3.PLT
$TITLE ="REGION UNDER THE EMITTER - POST BASE IMPLANT"
$RIGHT =10
$LABEL LABEL="BASE-COLLECTOR JUNCTION DEPTH: " @XJBC" MICRONS"
$LABEL LABEL="WELL SUBSTRATE JUNCTION DEPTH: " @XJCS" MICRONS"
$LABEL LABEL="INNER BASE SHEET RESISTANCE:" @BRX"OMHMS/SQ"
$LABEL LABEL="INNER COLLECTOR SHEET RESISTANCE:" @CRS"OMHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
($STEP 12 STRIP RESIST AND RCA CLEAN)
($STEP 13 DRIVE-IN OF BASE/ANNEAL AND GROWTH OF EMITTER MASKING OXIDE)
COMMENTS PULL WAFERS IN AT 850C IN NITROGEN
DIFFUSION TIME=10 TEMP=850 NITROGEN
DIFFUSION TIME=40 TEMP=850 WETO2
COMMENTS PULL WAFERS OUT AT 850C IN NITROGEN
PRINT LAYERS ELECTRICAL
EXTRACT NAME=XJBC NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0 X.MIN=@XJBC+.001
EXTRACT NAME=BRX H.RESIST LAYER=1 MIN_REGION=2
EXTRACT NAME=CRS E.RESIST LAYER=1 MAX_REGION=2
COMMENTS PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLOT.OUT=PLT4.PLT
$TITLE ="REGION UNDER THE EMITTER - POST BASE ANNEAL"
$RIGHT =10
$LABEL LABEL="BASE-COLLECTOR JUNCTION DEPTH: " @XJBC" MICRONS"
$LABEL LABEL="WELL SUBSTRATE JUNCTION DEPTH: " @XJCS" MICRONS"
$LABEL LABEL="INNER BASE SHEET RESISTANCE:" @BRX"OMHMS/SQ"
$LABEL LABEL="INNER COLLECTOR SHEET RESISTANCE:" @CRS"OMHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD

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$ *MEASURE CONTROL WAFERS FOR COLLECTOR JUNCTION DEPTH AND SHEET RESISTANCE *
$ $(STEP 14 BURIED CONTACT LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
$
$(STEP 15 OXIDE ETCH FOR BURIED CONTACTS)
ETCH OXIDE ALL
$
$(STEP 16 STRIP RESIST AND RCA CLEAN NONSTANDARD FOR INTERFACIAL OXIDE) $
$(STEP 17 DEPOSITION OF POLYSILICON FOR EMITTER) 
DEPOSITION POLYSILICON TEMP=610 THICKNESS=.4
$
$ *MEASURE CONTROL WAFERS FOR POLYSILICON THICKNESS
$ $ *MEASURE CONTROL WAFERS FOR COLLECTOR AND BASE JUNCTION DEPTHS AND SHEET RESISTANCE
$
$(STEP 18 IMPLANT POLYSILICON WITH PHOSPHOROUS SPECIES P31)
IMPLANT PHOSPHOROUS ENERGY=40 DOSE=5E15
PRINT LAYERS ELECTRICAL
EXTRACT NAME=XJBC NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0 X.MIN=XJBC+.001
EXTRACT NAME=PRS E.RESIST LAYER=2 MAX REGION=1
EXTRACT NAME=BRs H.RESIST LAYER=1 MIN REGION=2
EXTRACT NAME=CRs E.RESIST LAYER=1 MAX REGION=2
COMMENT PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS
$PLOT NET ACTIVE PLOT.OUT=PLOT5.PLT
$+TITLE ="REGION UNDER THE EMITTER AFTER POLYSILICON IMPLANT"
$+RIGHT =10
$+LABEL LABEL =" BASE-COLLECTOR JUNCTION DEPTH: "@XJBC" MICRONS"
$+LABEL LABEL =" WELL-SUBSTRATE JUNCTION DEPTH: "@XJCS" MICRONS"
$+LABEL LABEL =" POLY SHEET RESISTANCE: "@FRS" OHMS/SQ"
$+LABEL LABEL =" INNER BASE SHEET RESISTANCE: "@BRs" OHMS/SQ"
$+LABEL LABEL =" INNER COLLECTOR SHEET RESISTANCE: "@CRs" OHMS/SQ"
$PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
$PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
$+PAUSE
$
$(STEP 19 EMITTER LITHOGRAPHY) 
DEPOSITION PHOTORESIST THICKNESS=1.2
$****STEP MASKED OUT
$****ETCH PHOTORESIST ALL
$
$(STEP 20 ETCH POLYSILICON FOR EMITTER AND COLLECTOR CONTACTS)
$****STEP MASKED OUT
$****ETCH POLYSILICON ALL
$
$ *MEASURE CONTROL WAFERS FOR OXIDE CONSUMED DURING POLYSILICON ETCH
$
$(STEP 21 RESIST STRIP AND RCA CLEAN)
ETCH PHOTORESIST ALL
$
$(STEP 22 EMITTER ANNEAL)
COMMENT *** RAPID THERMAL ANNEALING CYCLES FOR SELECT WAFERS ***
COMMENT *** CAPPING OXIDE GROWTH PRIOR TO LTO AND RTP CYCLE ***
**** ***
**** COMMENT PUSH WAFERS IN AT 800C IN NITROGEN
**** DIFFUSION TIME=10 TEMP=800 N2
**** DIFFUSION TIME=25 TEMP=800 WET02
**** DIFFUSION TIME=5 TEMP=800 N2
**** COMMENT PULL WAFERS OUT AT 800C IN NITROGEN
$ *

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*** FURNACE ANNEAL ***

*** FOR SELECT WAFERS NON RTP WAFERS ***

PUSH WAFERS IN AT 875C IN NITROGEN

DIFFUSION TIME=50 TEMP=875 NITROGEN
DIFFUSION TIME=40 TEMP=875 WET02
DIFFUSION TIME=10 TEMP=875 DRY02
DIFFUSION TIME=20 TEMP=875 NITROGEN

PULL WAFERS OUT AT 875C IN NITROGEN

PRINT LAYERS ELECTRICAL

EXTRACT NAME=XJEB NET ACTIVE X.EXTRACT Y=0
EXTRACT NAME=XJBC NET ACTIVE X.EXTRACT Y=0 X.MIN=XJEB+.001
EXTRACT NAME=XJCS NET ACTIVE X.EXTRACT Y=0 X.MIN=XJEB+XJBC+.001
EXTRACT NAME=PRS E.RESIST LAYER=2 MAX.REGION=1
EXTRACT NAME=ERS E.RESIST LAYER=1 MIN.REGION=3
EXTRACT NAME=BR S E.RESIST LAYER=1 MIN.REGION=2
EXTRACT NAME=CRS E.RESIST LAYER=1 MAX.REGION=2
EXTRACT NAME=IBASE NET ACTIVE X.MIN=XJEB X.MAX=XJBC LAYER=1 INTEGRAL

ASSIGN NAME=BASEW N.VALUE=ABS(IBASE)
ASSIGN NAME=IBASE N.VALUE=ABS(IBASE)

COMMENT PLOTTING CHEMICAL/ACTIVE DISTRIBUTIONS

PLOT NET ACTIVE PLOT.OUT= PLOT6.PLT

+TITLE = "FINAL RESULTS UNDER THE EMITTER"
+RIGHT = 10
+DEVICE = "HP7550"

LABEL LABEL = " Emitter-Base XJ: " @XJEB " Microns"
LABEL LABEL = " Base-Collector XJ: " @XJBC " Microns"
LABEL LABEL = " Well-Substrate XJ: " @XJCS " Microns"
LABEL LABEL = " Poly SRHO: " 4PRS " Ohms/Sq"
LABEL LABEL = " Emitter SRHO: " 4ERS " Ohms/Sq"
LABEL LABEL = " Inner Base SRHO: " 4BRS " Ohms/Sq"
LABEL LABEL = " Inner Collector SRHO: " 4CRS " Ohms/Sq"
LABEL LABEL = " Base dose/energy: 8E12, 35KeV"
LABEL LABEL = " Emitter anneal time/temp: 50 Min, 850C"
LABEL LABEL = " Emitter dose/energy: 5E15, 40KeV"
LABEL LABEL = " Emitter anneal time/temp: 120 Min, 875C"
LABEL LABEL = " Base Width: " @BASEW " Microns"
LABEL LABEL = " Integrated Base: " @IBASE"

LABEL LABEL = "Emitter" X=.6 Y=1E19
LABEL LABEL = "Base" X=.8 Y=5E16
LABEL LABEL = "Collector" X=1.5 Y=2E15

PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD

+PAUSE

PLOT NET ACTIVE PLOT.OUT= PLOT7.PLT

+TITLE = "FINAL RESULTS UNDER THE EMITTER"
+RIGHT = 2
+DEVICE = "REDIS"

LABEL LABEL = " Emitter-Base XJ: " @XJEB " Microns"
LABEL LABEL = " Base-Collector XJ: " @XJBC " Microns"
LABEL LABEL = " Well-Substrate XJ: " @XJCS " Microns"
LABEL LABEL = " Poly SRHO: " 4PRS " Ohms/Sq"
LABEL LABEL = " Emitter SRHO: " 4ERS " Ohms/Sq"
LABEL LABEL = " Inner Base SRHO: " 4BRS " Ohms/Sq"
LABEL LABEL = " Inner Collector SRHO: " 4CRS " Ohms/Sq"
LABEL LABEL = " Base dose/energy: 8E12, 35KeV"
LABEL LABEL = " Emitter dose/energy: 5E15, 40KeV"
LABEL LABEL = " Emitter anneal: 120 Min, 875C"
LABEL LABEL = " Base Width: " @BASEW " Microns"
LABEL LABEL = " Integrated Base: " @IBASE"

LABEL LABEL = "Emitter" X=.25 Y=1E19
LABEL LABEL = "Base" X=.6 Y=1E15
LABEL LABEL = "Collector" X=1.5 Y=5E14

PLOT CHEMICAL BORON COLOR=2 LINE=2 ADD
PLOT CHEMICAL PHOSPHOROUS COLOR=3 LINE=3 ADD
COMMENT PLOTTING ELECTRON AND HOLE DISTRIBUTIONS
ELECTRICAL ELECTRON HOLE DISTRIBUTION FILE=D.DAT EXTENT=12
BIAS LAYER=1 V=5 DV=0 ABSCISSA
END ELECTRICAL
PLOT FILE=D.DAT ELECTRON PLOT.OUT=PLOT8.PLT
+TITLE "ELECTRON AND HOLE DISTRIBUTIONS, BASE DOSE=8E12"
+RIGHT =2 BOTTOM=1E13
+DEVICE ="REGIS"
PLOT FILE=D.DAT HOLE COLOR=2 LINE=2 ADD
PLOT NET ACTIVE COLOR=3 LINE=3 ADD
+PAUSE

COMMENT PLOTTING BASE RESISTANCE
$ (SOLVING POISSON'S EQUATION WHEN THE COLLECTOR VOLTAGE IS RAMPED
$ FROM 0 TO 5 VOLTS)
ELECTRICAL EXTENT=3 STEPS=6 FILE=E.DAT
BIAS LAYER=1 REGION=2 V=0 DV=1 ABSCISSA
END ELECTRICAL
PLOT FILE=E.DAT H.RESIST LAYER=1 MIN.REGION=2
+PLOT.OUT=PLOT9.PLT
+TITLE "BASE RESISTANCE WITH BASE DOSE=8E12"
+BOTTOM =1E0 TOP=3E5 ^Y.LOG SYMBOL=1
+DEVICE ="REGIS"
$ *MEASURE CONTROL WAFERS FOR OXIDE THICKNESS
$ *MEASURE CONTROL WAFERS FOR FINAL COLLECTOR, BASE, AND EMITTER JUNCTION
$ DEPTH AND SHEET RESISTANCE
$
$
$(STEP 23 CONTACT CUT LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
$
$(STEP 24 OXIDE ETCH FOR CONTACTS)
ETCH OXIDE ALL
$
$(STEP 25 RESIST STRIP AND RCA CLEAN)
$
$(STEP 26 DEPOSITION OF ALUMINUM)
DEPOSITION ALUMINUM THICKNESS=.8
$
$(STEP 27 VARIABLE SINTER MAXIMUM 450C 20 MINUTES IN H2/N2)
$
$(STEP 28 METAL LITHOGRAPHY)
DEPOSITION PHOTORESIST THICKNESS=1.2
ETCH PHOTORESIST ALL
$
$(STEP 29 ALUMINUM ETCH)
ETCH ALUMINUM
$
$(STEP 30 RESIST STRIP)
$
STOP
**FINAL RESULTS UNDER THE EMITTER**

EMITTER-BASE XJ: 9.237E-02 MICRONS  
BASE-COLLECTOR XJ: 0.3263 MICRONS  
WELL-SUBSTRATE XJ: 4.9218 MICRONS  
POLY SRHO: 31.529 OHMS/SQ  
EMITTER SRHO: 840.96 OHMS/SQ  
INNER BASE SRHO: 46843 OHMS/SQ  
INNER COLL. SRHO: 5391.6 OHMS/SQ  
BASE DOSE/ENERGY: 8E12, 35KEV  
BASE ANNEAL: 50 MIN, 850C  
EMITTER DOSE/ENERGY: 5E15, 40KEV  
EMITTER ANNEAL: 120MIN, 875C  
BASE WIDTH: 0.23353 MICRONS  
INTEGRATED BASE: 1.2423E+12

**Figure 9B.7** Lot #2 Furnace Base Dose = 8E12 ions/cm²

**FINAL RESULTS UNDER THE EXTRINSIC BASE**

BASE-COLLECTOR XJ: 0.40706 MICRONS  
WELL-SUBSTRATE XJ: 4.8948 MICRONS  
EXTRINSIC BASE SRHO: 13442 OHMS/SQ  
COLLECTOR SRHO: 5647.3 OHMS/SQ  
BASE DOSE AND ENERGY: 8E12, 30KEV  
BASE ANNEAL TIME/TEMP: 50 MIN, 850C  
EMITTER DOSE AND ENERGY: 5E15, 40KEV  
EMITTER ANNEAL TIME/TEMP: 120MIN, 875C

**Figure 9B.8** Lot #2 Furnace Base Dose = 8E12 ions/cm²
FINAL RESULTS UNDER THE EX. BASE OX/POLY

- BASE-COLLECTOR XJ: 0.32031 MICRONS
- WELL-SUBSTRATE XJ: 4.9217 MICRONS
- EXTRINSIC BASE SRHD: 9702 OHMS/SQ
- COLLECTOR SRHD: 5377.3 OHMS/SQ
- BASE DOSE AND ENERGY: 8E12, 35KEV
- BASE ANNEAL TIME/TEMP: 50 MIN, 850C
- Emitter Dose and Energy: 5E15, 40KEV
- Emitter Anneal Time/Temp: 120 MIN, 875C

Figure 9B.9 Lot #2 Furnace Base Dose = 8E12 ions/cm²

FINAL RESULTS UNDER THE COLLECTOR

- WELL-SUBSTRATE XJ: 4.9127 MICRONS
- OUTER COLLECTOR SRHD: 3987.6 OHMS/SQ
- BASE DOSE AND ENERGY: 8E12, 30KEV
- BASE ANNEAL TIME/TEMP: 50 MIN, 850C
- Emitter Dose and Energy: 5E15, 40KEV
- Emitter Anneal Time/Temp: 120 MIN, 875C

Figure 9B.10 Lot #2 Furnace Base Dose = 8E12 ions/cm²
FINAL RESULTS UNDER THE COLLECTOR CONTACT

WELL-SUBSTRATE XJ: 4.9297 MICRONS
OUTER COLLECTOR SPKO: 837.18 OHMS/SQ
BASE DOSE AND ENERGY: 8E12, 35KEV
BASE ANNEAL TIME/TEMP: 50 MIN, 850C
EMITTER DOSE AND ENERGY: 5E15, 40KEV
EMITTER ANNEAL TIME/TEMP: 120MIN, 875C

Figure 9B.11 Lot #2 Furnace Base Dose = 8E12 ions/cm²

FINAL RESULTS UNDER THE FIELD

BASE DOSE AND ENERGY: 8E12, 35KEV
BASE ANNEAL TIME/TEMP: 50 MIN, 850C
EMITTER DOSE AND ENERGY: 5E15, 40KEV
EMITTER ANNEAL TIME/TEMP: 120MIN, 875C

Figure 9B.12 Lot #2 Furnace Base Dose = 8E12 ions/cm²
**Figure 9B.13** Lot #2 Furnace Base Dose = 8E12 ions/cm²

**Figure 9B.14** Lot #2 Furnace Base Dose = 8E12 ions/cm²
Figure 9B.15 Lot #2 Furnace  Base Dose = 5E13 ions/cm²

Figure 9B.16 Lot #2 Furnace  Base Dose = 5E13 ions/cm²
FINAL RESULTS UNDER THE EX. BASE OX/POLY

BASE-COLLECTOR XJ: 0.4004 MICRONS
WELL-SUBSTRATE XJ: 4.9218 MICRONS
EXTRINSIC BASE SRHO: 1980.3 OHMS/SQ
COLLECTOR SRHO: 5599.2 OHMS/SQ
BASE DOSE AND ENERGY: 5E13, 35KEV
BASE ANNEAL TIME/TEMP: 50 MIN. 850C
EMITTER DOSE AND ENERGY: 5E15, 40KEV
EMITTER ANNEAL TIME/TEMP: 120MIN. 875C

Figure 9B.17 Lot #2 Furnace Base Dose = 5E13 ions/cm²

FINAL RESULTS UNDER THE COLLECTOR

WELL-SUBSTRATE XJ: 4.9127 MICRONS
OUTER COLLECTOR SRHO: 3887.6 OHMS/SQ
BASE DOSE AND ENERGY: 5E13, 35KEV
BASE ANNEAL TIME/TEMP: 50 MIN. 850C
EMITTER DOSE AND ENERGY: 5E15, 40KEV
EMITTER ANNEAL TIME/TEMP: 120MIN. 875C

Figure 9B.18 Lot #2 Furnace Base Dose = 5E13 ions/cm²

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FINAL RESULTS UNDER THE COLLECTOR CONTACT

WELL-SUBSTRATE XJ: 4.9297 MICRONS
OUTER COLLECTOR SRHO: 637.16 OHMS/SQ
BASE DOSE AND ENERGY: 5E13, 35KEV
BASE ANNEAL TIME/TEMP: 50 MIN, 850C
EMITTER DOSE AND ENERGY: 5E15, 40KEV
EMITTER ANNEAL TIME/TEMP: 120MIN, 875C

Figure 9B.19 Lot #2 Furnace Base Dose = 5E13 ions/cm²

FINAL RESULTS UNDER THE FIELD

BASE DOSE AND ENERGY: 5E13, 35KEV
BASE ANNEAL TIME/TEMP: 50 MIN, 850C
EMITTER DOSE AND ENERGY: 5E15, 40KEV
EMITTER ANNEAL TIME/TEMP: 120MIN, 875C

Figure 9B.20 Lot #2 Furnace Base Dose = 5E13 ions/cm²

150
ELECTRON AND HOLE DISTRIBUTIONS, BASE DOSE = 5E13

Distance (Microns)

Figure 9B.21 Lot #2 Furnace Base Dose = 5E13 ions/cm²

BASE RESISTANCE WITH BASE DOSE = 5E13

Potential (Volts)

Figure 9B.22 Lot #2 Furnace Base Dose = 5E13 ions/cm²
Figure 9B.23 Lot #2 Furnace Base Dose = 1E14 ions/cm²

Figure 9B.24 Lot #2 Furnace Base Dose = 1E14 ions/cm²
**FINAL RESULTS UNDER THE EX. BASE OX/POLY**

Figure 9B.25 Lot #2 Furnace Base Dose = 1E14 ions/cm²

**FINAL RESULTS UNDER THE COLLECTOR**

Figure 9B.26 Lot #2 Furnace Base Dose = 1E14 ions/cm²
FINAL RESULTS UNDER THE COLLECTOR CONTACT

**Figure 9B.27** Lot #2 Furnace Base Dose = 1E14 ions/cm²

FINAL RESULTS UNDER THE FIELD

**Figure 9B.28** Lot #2 Furnace Base Dose = 1E14 ions/cm²
Figure 9B.29 Lot #2 Furnace  Base Dose = 1E14 ions/cm²

Figure 9B.30 Lot #2 Furnace  Base Dose = 1E14 ions/cm²
9.0 Appendix C

Detailed Fabrication Description
1. Wafer Selection and Identification Scribe.
   P type Si (Boron) <100> 5-15 ohm-cm
   Lot #1 Device(D1-D12), Controls(C1-C15)
   Lot #2 Device(D1-D12), Controls(C1-C13)

2. Determination of Initial Resistivity.
   Four point probed all wafers

   NH$_4$OH/H$_2$O$_2$/H$_2$O 1:1:5 10 min at ~ 75°C
   Rinse
   H$_2$O/HF (10:1) 1 min
   Rinse
   HCl/H$_2$O$_2$/H$_2$O 1:1:5 10 min at ~ 75°C
   Rinse
   All wafers

4. Field Oxide Growth.
   Temp=900°C    Ambient=N$_2$    Loaded and Ramped
   Temp=1100°C   Time=10 min.    Ambient=Dry O$_2$
   Temp=1100°C   Time=90 min.    Ambient=Dry O$_2$ with Drip H$_2$O
   Temp=1100°C   Time=10 min.    Ambient=Dry O$_2$
   Temp=1000°C   Ambient=N$_2$    Ramped and UnLoaded
   All wafers

5. Measurement of Field Oxide Thickness.
   Nanospec controls

6. Photolithography for Collector Level.
Coat Resist with HMDS and Prebake - Program #3

Exposure Integrated 60mJ/cm²

Develop and Post Bake - Program #2

All device wafers

7. Etching of Oxide.

BHF etch 10 minutes, controls took 8 minutes to pull dry

All device and control wafers

8. Implantation of the Collector.

Energy = 110 KeV Dose = 8E12 ions/cm² Species P³⁺

All device and control wafers


O₂ plasma ash all device wafers

10. Standard RCA clean.

All wafers

11. Collector Drive-in.

Temp = 900°C  Ambient = N₂  Loaded and Ramped

Temp = 1125°C  Time = 60 min.  Ambient = N₂

Temp = 1125°C  Time = 400 min.  Ambient = Dry O₂

Temp = 1125°C  Time = 2340 min.  Ambient = N₂

Temp = 1000°C  Ambient = N₂  UnLoaded

All wafers

12. Measurement of Collector and Field Oxide Thicknesses.

Nanospec collector and field regions

Lot #1  Device(D1,D6,D12), Controls(C1,C7,C8,C15)

Lot #2  Device(D1,D12), Controls(C5)

Oxide etched off controls first till pull dry - 5min
Lot #1 Controls (C8)
Lot #2 Controls (C4)

Oxide left on:
Lot #1 Controls (C1, C2, C15)
Lot #2 Controls (C2, C12, C13)


Lot #1 Controls (C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14)
Lot #2 Controls (C1, C3, C4, C5, C6, C7, C8, C9, C10, C11)

15. Photolithography for Base Level.

Coat Resist with HMDS and Prebake - Program #3
Exposure Integrated 60mJ/cm²
Develop and Post Bake - Program #2
All device wafers

16. Etching of Oxide.

BHF etch long enough to etch field oxide for p+ substrate contacts.
Lot #1 - 10.5 min.    Lot #2 - 12 min.
All device wafers

17. Implantation of the Base.

Species BF₂⁺

<table>
<thead>
<tr>
<th>Lot #1</th>
<th>Energy (KeV)</th>
<th>Dose (ions/cm²)</th>
<th>Wafers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>35</td>
<td>3E14</td>
<td>(D11, D12, C3, C9)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>159</td>
</tr>
</tbody>
</table>
Lot #2  | Energy (KeV) | Dose (ions/cm²) | Wafers
---|---|---|---
35 | 1E14 | (D2, D10, C4, C10) |  
35 | 8E13 | (D1, D9, C5, C11) |  
35 | 5E13 | (D7, D8, C6, C12) |  
35 | 1E13 | (D5, D6, C7, C13) |  
35 | 8E12 | (D3, D4, C8, C14) |  

18. Resist Removal.
O₂ plasma ash all device wafers

All wafers

20. Base Drive-in.

Lot #1  All wafers
Temp=900°C  Ambient=N₂  Loaded
Temp=900°C  Time=10 min.  Ambient=Dry O₂
Temp=900°C  Time=35 min.  Ambient=Dry O₂ with Drip H₂O
Temp=900°C  Time=10 min.  Ambient=Dry O₂
Temp=900°C  Ambient=N₂  UnLoaded

Lot #2  All wafers
Temp=850°C  Ambient=N₂  Loaded
Temp=850°C  Time=10 min.  Ambient=N₂
Temp=850°C  Time=40 min.  Ambient=Dry O₂ with Drip H₂O
Temp=850°C  Ambient=N₂  UnLoaded
   Lot #1  Device(D1,D6,D12)
   Lot #2  Device(D1,D12), Controls(C1,C3,C4)

   Oxide etched off controls first till pull dry - 5min
   Lot #1  Controls(C3,C4,C5,C6,C7,C8)
   Lot #2  Controls(C5,C6,C7)
   Oxide left on:
   Lot #1  Controls(C1,C3,C4,C5,C6,C7,C8,C15)
   Lot #2  Controls(C1,C2,C3,C4,C12)

   Lot #1  Controls(C3,C4,C5,C6,C7,C8)
   Lot #2  Controls(C5,C6,C7)

24. Photolithography for Buried Contact Level.
   Coat Resist with HMDS and Prebake - Program #3
   Exposure Integrated 60mJ/cm²
   Develop and Post Bake - Program #2
   All device wafers

25. Etching of Oxide.
   BHF etch long enough to etch through oxide over collector for n+ collector contact.
   Lot #1 - 6.5 min.    Lot #2 - 8 min.
   All device wafers

O_3 Plasma Ash all device wafers

27. RCA Clean for Interfacial Oxide Growth.
   \( \text{H}_2\text{O}/\text{HF} \ (10:1) \) (short to save thin oxide over base)
   Lot #1 - 15 sec    Lot #2 - 5 sec.
   Rinse
   \( \text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O} \ 1:1:5 \ 10 \text{ min at } \sim 75^\circ\text{C} \)
   Rinse
   \( \text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O} \ 1:1:5 \ 10 \text{ min at } \sim 75^\circ\text{C} \)
   Rinse
   All wafers

   Temp = 610\(^\circ\)C  Target thickness = 4000\(\AA\)
   Lot #1 Device(D1-D12), Controls(C2,C3,C4,C5,C6,C7,
   C8,C9,C10,C11,C12,C13,C14,C15)
   Deposition time - 48 min.
   Lot #2 Device(D1 - D12), Controls(C2,C5,C6,C7,C8,C9,
   C10,C11,C13)
   Deposition time - 46 min.

   Lot #1 Controls(C3,C4,C5,C6,C7,C8)
   Used base implant controls which had close to 1000\(\AA\)
   of oxide as monitors for the polysilicon thickness.
   Lot #2 Special prepared controls with 1000\(\AA\) oxide

30. Implantation of the Polysilicon.
   Lot #1 Device(D1-D12), Controls(C2,C9,C10,C11,C12,
C13,C14,C15)

Energy = 45 KeV Dose = 4E15 ions/cm² Species P³
Lot #2 Device(D1-D12), Controls(C2,C5,C6,C7,C8,C9, C10,C11,C13)

Energy = 40 KeV Dose = 5E15 ions/cm² Species P³

31. Photolithography for Emitter Level.
Coat Resist with HMDS and Prebake -Program #3
Exposure Integrated 60mJ/cm²
Develop and Post Bake -Program #2
All device wafers

32. Etching of Polysilicon.
RIE process: SF₆ = 30 sccm, O₂ = 3 sccm, Forward
Power = 75 watts, Pressure = 75 mTorr
Lot #1 - etch time 2 minutes for all device wafers and
base controls.
Lot #2 - etch time (1 min and 35 sec) to (1 min and 15
sec) for all device wafers, decreased time to prevent
unnecessary etch of base oxide.

33. Resist Removal.
O₂ Plasma Ash all device wafers

34. Measurement of Oxide Thickness Over Base Regions.
Check to see how much was removed by RIE. Nanospec
Lot #1 Device(D1,D7)
Lot #2 Device(D1,D5,D12)

35. Standard RCA Clean.
All wafers

36. Emitter Furnace Drive-in.

Lot #1 Device(D1,D2,D3,D6,D7), Controls(A Halves)

Temp=875°C  Ambient=N₂  Loaded
Temp=875°C  Time=15 min.  Ambient=N₂
Temp=875°C  Time=25 min.  Ambient=Dry O₂ with Drip H₂O
Temp=875°C  Time=5 min.  Ambient=N₂
Temp=875°C  Ambient=N₂  UnLoaded

Etched oxide in BHF for 1 min. off entire part of all wafers in order to probe beta early and continued:

Temp=875°C  Ambient=N₂  Loaded
Temp=875°C  Time=35 min.  Ambient=N₂
Temp=875°C  Time=25 min.  Ambient=Dry O₂ with Drip H₂O
Temp=875°C  Time=10 min.  Ambient=Dry O₂
Temp=875°C  Time=5 min.  Ambient=N₂
Temp=875°C  Ambient=N₂  UnLoaded

Lot #2 Device(D1,D5,D10), Controls(A Halves except C8,C9,C10,C11)

Temp=875°C  Ambient=N₂  Loaded
Temp=875°C  Time=50 min.  Ambient=N₂
Temp=875°C  Time=40 min.  Ambient=Dry O₂ with Drip H₂O
Temp=875°C  Time=10 min.  Ambient=Dry O₂
Temp=875°C  Time=20 min.  Ambient=N₂
Temp=875°C  Ambient=N₂  UnLoaded

37. Measurement of Emitter, Base, Collector, and Field Oxide
Thicknesses for Furnace Drive-in. Nanospec

P type silicon wafer implanted with the same process as polysilicon implant - to measure thickness over poly.

Lot #1  Device(D1,D7)
Lot #2  Device(D5,D10)

38. Thin Thermal Capping Oxide Growth Prior to RTP

Temp = 800°C  Ambient = N₂  Loaded
Temp = 800°C  Time = 10 min.  Ambient = N₂
Temp = 800°C  Time = 25 min.  Ambient = Dry O₂ with Drip H₂O
Temp = 800°C  Time = 5 min.  Ambient = N₂
Temp = 800°C  Ambient = N₂  UnLoaded

Lot #1  Device(D4,D5,D8,D9,D10,D11), Controls (B Halves)
Prior to this step the oxide was etched in BHF for 1 min. off the entire wafer in order to probe beta early.

Lot #2  Device(D2,D3,D4,D7,D8,D9,D12), Controls (B Halves)


P type silicon wafer implanted with the same process as polysilicon implant - to measure thickness over poly. Nanospec

Lot #1  Device(D4,D11) - for thickness over base
Lot #2  Device(D2,D12) - for thickness over base

40. Low Temperature Oxide Deposition.

Temp = 400°C  Target thickness = 3000Å
O₂ = 12%  SiH₄ = 20%

Deposition time - 180 min. 7 dummies in front of boat.
Lot #1  Device(D4,D5,D8,D9,D10,D11)
Lot #2  Device(D2,D3,D4,D7,D8,D9,D12)

41. Measurement of LTO Thickness Over Base Regions.

Nanospec
Lot #1  Device(D4,D5,D8,D9,D10,D11)
Lot #2  Device(D2,D3,D4,D7,D8,D9,D12)

42. Emitter Rapid Thermal Processing.

Program 950°C for Pyrometer:

<table>
<thead>
<tr>
<th>Step</th>
<th>Time/Rate</th>
<th>Gas</th>
<th>Temp</th>
<th>Tsw</th>
<th>Gain</th>
<th>DGain</th>
<th>IWarm</th>
<th>ICold</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Delay</td>
<td>10</td>
<td>N2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Ramp</td>
<td>50</td>
<td>N2</td>
<td>950</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>SState</td>
<td>25</td>
<td>N2</td>
<td>950</td>
<td>100</td>
<td>-60</td>
<td>-60</td>
<td>3018</td>
</tr>
<tr>
<td>4</td>
<td>Ramp</td>
<td>50</td>
<td>N2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Delay</td>
<td>10</td>
<td>N2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The remaining programs were the same except for Ramp up and SState temperatures, and IWarm and ICold.

<table>
<thead>
<tr>
<th>Program</th>
<th>Ramp Temp</th>
<th>SState Temp</th>
<th>IWarm</th>
<th>ICold</th>
</tr>
</thead>
<tbody>
<tr>
<td>950°C TC</td>
<td>950</td>
<td>950</td>
<td>2545</td>
<td>3250</td>
</tr>
<tr>
<td>1000°C Pyro</td>
<td>1000</td>
<td>1000</td>
<td>3478</td>
<td>3600</td>
</tr>
<tr>
<td>1000°C TC</td>
<td>1000</td>
<td>1000</td>
<td>2952</td>
<td>3600</td>
</tr>
<tr>
<td>1050°C Pyro</td>
<td>1050</td>
<td>1050</td>
<td>4034</td>
<td>4000</td>
</tr>
<tr>
<td>1050°C TC</td>
<td>1050</td>
<td>1050</td>
<td>3184</td>
<td>3950</td>
</tr>
</tbody>
</table>

Dummy wafer used at first for each time temperature
changed because overshoot occurs for first wafer.

Lot #1 Device(D4,D5,D8,D9,D10,D11), Controls(B Halves)
Temp = 1000°C 20 sec. Pyrometer Actual SS = 1001°C
Lot #2 Device(D3,D8), Controls(C8B,C9B,C11B)
Temp = 950°C 20 sec. Thermocouple Actual SS = 948°C
Lot #2 Device(D2,D7,D12), Controls(C1B,C2B,C3B,C4B,C5B,
C6B,C7B,C12B,C13B)
Temp = 1000°C 20 sec. Thermocouple Actual SS = 999°C
Lot #2 Device(D4,D9), Controls(C8A,C9A,C10B,C11A)
Temp = 1050°C 20 sec. Thermocouple Actual SS = 1048°C

43. Measurement of Final Emitter-Base, Base-Collector, and Collector-Substrate Junction Depths.
Oxide etched off all controls first till pull dry.
Lot #1 Controls(C1-C15 excluding C2 and C15)
Lot #2 Controls(C1-C13 excluding C2 and C13)

44. Measurement of Final Emitter, Base, and Collector Sheet Resistances.
Lot #1 Controls(C1-C15)
Lot #2 Controls(C1-C13)

45. Photolithography for the Contact Cut Level.
Coat Resist with HMDS and Prebake -Program #3
Exposure Integrated 60mJ/cm²
Develop and Post Bake -Program #2
All device wafers
46. Etching of Oxide.

BHF etch long enough to etch through oxide over all regions including n+ collector and p+ substrate contact, and capacitors with 4000Å of oxide. LTO appeared to be extremely densified by RTP and did not etch that fast.

Furnace Annealed - 5.5 min.   RTP - 7 min.
All device wafers

47. Resist Removal.
O₂ Plasma Ash

48. RCA Clean.

Standard except H₂O/HF (10:1) (30 seconds last step)
All wafers

49. Sputtering of Aluminum / 1% Silicon

Run #1 - Done in two steps because problems developed
Target Thickness = 5000Å   Sputter Time = 5 min.
DC Power =3400 Watts   Pressure =5 mTorr
(continued)   Sputter Time =24 min.
DC Power =1500 Watts   Pressure =5 mTorr
Run #2
Target Thickness = 5000Å   Sputter Time = 18 min.
DC Power =3240 Watts   Pressure =5 mTorr
Run #1 - All Furnace Annealed Device Wafers
Run #2 - All RTP Device Wafers

50. Photolithography for the Metal Level.
Coat Resist with no HMDS and Prebake - Program #30
Exposure Integrated 55mJ/cm²
Develop and Post Bake - Program #2
All device wafers

51. Etching of Aluminum.
Street clear test performed on one wafer first.
Phosphoric acid 3 minutes at 40°C
All device wafers

52. Removal of 1% Silicon Haze.
Etched 20 seconds in polysilicon etch
HNO₃ = 64% : BOE = 3% : DI H₂O = 33%
All device wafers

53. Removal of Resist.
O₂ Plasma Ash

54. Sintering of Aluminum.
In steps to prevent spiking of junction, with wafers tested prior to any sintering.
Maximum temp = 449°C
Maximum time at highest temp = 10 min.
Total sinter time = 20 min
All sinter wafers

55. Testing of Device Wafers.

56. TEM Physical Analysis of Interfacial Oxide.
Lot #2 Controls(C6A,C6B,C10B,C11B)
9.0 Appendix D

Inline Process Data
1. Measurement of Initial Resistivity.
Lot #1  Average of all wafers: 11.8 ohm-cm
Lot #2  Average of all wafers: 7.97 ohm-cm

2. Measurement of Field Oxide Thickness.
Across wafer averages given to show uniformity results
Top refers to wafer flat which was at the top of tube
Lot #1  Average of controls:
<table>
<thead>
<tr>
<th>Top</th>
<th>Center</th>
<th>Bottom</th>
<th>Left</th>
<th>Right</th>
</tr>
</thead>
<tbody>
<tr>
<td>6102Å</td>
<td>6271Å</td>
<td>6503Å</td>
<td>6204Å</td>
<td>6246Å</td>
</tr>
</tbody>
</table>
Lot #2  Average of controls:
<table>
<thead>
<tr>
<th>Top</th>
<th>Center</th>
<th>Bottom</th>
<th>Left</th>
<th>Right</th>
</tr>
</thead>
<tbody>
<tr>
<td>6546Å</td>
<td>6591Å</td>
<td>6610Å</td>
<td>6602Å</td>
<td>6594Å</td>
</tr>
</tbody>
</table>

Lot #1 Center Thickness: Collector  Field
| D1   | 4031Å  | 7459Å |
| D6   | 4031Å  | 7485Å |
| D12  | 4031Å  | 7416Å |
| C1   | 3902Å  |       |
| C7   | 3988Å  |       |
| C8   | 3970Å  |       |
| C15  | 4020Å  |       |
Lot #2 Center Thickness: Collector  Field
| D1   | 3985Å  | 7717Å |
| D12  | 3984Å  | 7696Å |

Lot #1:  C8 = 8.24 microns (measured twice)
Lot #2:  C4 = 6.70 microns (measured twice)


Lot #1:
C3 = 630 ohms/sq  C4 = 610 ohms/sq  C5 = 630 ohms/sq
C6 = 597 ohms/sq  C7 = 625 ohms/sq  C8 = 603 ohms/sq
C9 = 635 ohms/sq  C10 = 591 ohms/sq  C11 = 646 ohms/sq
C12 = 637 ohms/sq  C13 = 682 ohms/sq  C14 = 605 ohms/sq

Lot #2:
C3 = 669 ohms/sq  C4 = 659 ohms/sq
C5 = 695 ohms/sq  C6 = 658 ohms/sq  C7 = 664 ohms/sq
C8 = 678 ohms/sq  C9 = 654 ohms/sq  C10 = 625 ohms/sq
C11 = 637 ohms/sq


Lot #1 Center Thickness:  Base  Collector  Field
D1  940Å  4436Å  7859Å
D6  792Å  4340Å  7804Å
D12 833Å  4354Å  7772Å

Lot #2 Center Thickness:  Base  Collector  Field
D1  425Å  4020Å  7706Å
D12 422Å  4042Å  7711Å
C1  423Å
Lot #1:
C3 = 1.70 microns  C4 = 1.59 microns  C5 = 1.63 microns
C6 = 1.51 microns  C7 = 1.12 microns  C8 = 1.16 microns
Lot #2:
C5 = .42 microns  C6 = .61 microns  C7 = .65 microns

Lot #1:
C3 = 438 ohms/sq  C4 = 483 ohms/sq  C5 = 629 ohms/sq
C6 = 564 ohms/sq  C7 = 853 ohms/sq  C8 = 884 ohms/sq
Lot #2:
C5 = 706 ohms/sq  C6 = 976 ohms/sq  C7 = 643 ohms/sq

Lot #1  Average of controls (C3,C4,C5,C6,C7,C8) placed through out boat:
Top    Center    Bottom    Left    Right
4239Å  4249Å    4229Å    4245Å  4219Å
Lot #2  Average of special prepared controls with 1000Å oxide placed through out boat:
Top    Center    Bottom    Left    Right
3962Å  3984Å    4043Å    4016Å  3975Å

10. Measurement of Oxide Thickness Over Base Regions.
A check to see not to much was removed by RIE.
Lot #1 Center Thickness:                      Base
        D1      760Å
        D7      629Å
Lot #2 Center Thickness:                      Base
        D1      389Å
        D5      301Å
        D12     367Å

11. Measurement of Final Emitter, Base, Collector, and Field
Oxide Thicknesses after Emitter Furnace Drive-in.

Lot #1 Center Thickness:                      Base       Collector       Field
        D1      445Å     3762Å      6998Å
        D7      415Å     3618Å      6873Å
Lot #2 Center Thickness:                      Base       Collector       Field
        D5      800Å     4220Å      7816Å
        D10     798Å     4241Å      7838Å

Special P_type bare silicon phosphorous implanted wafer
for the oxide thickness over emitter poly = 2545Å

12. Measurement of Oxide Thickness after Thermal Capping
Oxide Growth for RTP Wafers.

Lot #1 Base Thickness:                      Top       Center     Bottom
        D4      145Å     161Å      148Å
        D11     155Å     213Å      147Å
Lot #2 Base Thickness:                      Top       Center     Bottom
        D2      293Å     393Å      322Å
        D12     426Å     438Å      393Å
Special P-type bare silicon phosphorous implanted wafer for the oxide thickness over emitter poly = 518Å

Lot #1 was in the front of the boat. Actual LTO thicknesses are obtained by subtracting on average 200Å for Lot#1 and 400Å for Lot#2 for base oxide thickness.
Lot #1 Average of (D4,D5,D8,D9,D10,D11):

<table>
<thead>
<tr>
<th>Top</th>
<th>Center</th>
<th>Bottom</th>
<th>Left</th>
<th>Right</th>
</tr>
</thead>
<tbody>
<tr>
<td>3965Å</td>
<td>3579Å</td>
<td>3611Å</td>
<td>3667Å</td>
<td>3667Å</td>
</tr>
</tbody>
</table>

Lot #2 Average of (D2,D3,D4,D7,D8,D9,D12):

<table>
<thead>
<tr>
<th>Top</th>
<th>Center</th>
<th>Bottom</th>
<th>Left</th>
<th>Right</th>
</tr>
</thead>
<tbody>
<tr>
<td>3267Å</td>
<td>3145Å</td>
<td>3311Å</td>
<td>3322Å</td>
<td>3333Å</td>
</tr>
</tbody>
</table>

Lot #1:
* Emitter-base junction depth approximation
Furnace remaining poly = 4200Å - (.44)(2545Å) = 3131Å
RTP remaining poly = 4200 - (.44)(518Å) = 3982Å
* Xj_ab = Xj_r_base - Poly thickness after oxide growth

<table>
<thead>
<tr>
<th>Furnace</th>
<th>RTP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xj_ab</td>
<td></td>
</tr>
<tr>
<td>C9A = .10 microns</td>
<td>C9B = .20 microns</td>
</tr>
<tr>
<td>C10A = .16 microns</td>
<td>C10B = .15 microns</td>
</tr>
<tr>
<td>C11A = .19 microns</td>
<td>C11B = .16 microns</td>
</tr>
<tr>
<td>C12A = .14 microns</td>
<td>C12B = .26 microns</td>
</tr>
</tbody>
</table>
C13A = .22 microns  C13B = .10 microns
C14A = .25 microns  C14B = .16 microns
Xjtc
C3A = .77 microns  C3B = .71 microns
C4A = .76 microns  C4B = .73 microns
C5A = .70 microns  C5B = .64 microns
C6A = .66 microns  C6B = broken
C7A = .59 microns  C7B = .58 microns
C8A = .40 microns  C8B = .51 microns
Xjce
C1A = 6.52 microns  C1B = 6.46 microns

Lot #2:

* Emitter-base junction depth approximation

Furnace remaining poly = 4000Å-(.44)(2545Å) = 2931Å
RTP remaining poly = 4000-(.44)(518Å) = 3782Å

* Xjeb = Xjn-base - Poly thickness after oxide growth

Furnace  RTP

Xjeb
C5A = .21 microns  C5B = .30 microns
C6A = .19 microns  C6B = .14 microns
C7A = .17 microns  C7B = .23 microns
C8A = .29 microns  C8B = .23 microns
C9A = .28 microns  C9B = .23 microns
C10A = .21 microns  C10B = .28 microns
C11A = .26 microns  
C11B = .23 microns

C1A = .67 microns  
C1B = .45 microns

C3A = .87 microns  
C3B = .64 microns

C4A = .90 microns  
C4B = .71 microns

Xj_{bc}  

C12A = 7.18 microns  
C12B = 7.11 microns

Xj_{cs}


Lot #1:  

<table>
<thead>
<tr>
<th>Component</th>
<th>Furnace</th>
<th>RTP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C9A</td>
<td>347 ohms/sq</td>
<td>149 ohms/sq</td>
</tr>
<tr>
<td>C10A</td>
<td>270 ohms/sq</td>
<td>122 ohms/sq</td>
</tr>
<tr>
<td>C11A</td>
<td>251 ohms/sq</td>
<td>123 ohms/sq</td>
</tr>
<tr>
<td>C12A</td>
<td>297 ohms/sq</td>
<td>127 ohms/sq</td>
</tr>
<tr>
<td>C13A</td>
<td>312 ohms/sq</td>
<td>141 ohms/sq</td>
</tr>
<tr>
<td>C14A</td>
<td>333 ohms/sq</td>
<td>159 ohms/sq</td>
</tr>
<tr>
<td>Base</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C3A</td>
<td>650 ohms/sq</td>
<td>286 ohms/sq</td>
</tr>
<tr>
<td>C4A</td>
<td>700 ohms/sq</td>
<td>665 ohms/sq</td>
</tr>
<tr>
<td>C5A</td>
<td>880 ohms/sq</td>
<td>808 ohms/sq</td>
</tr>
<tr>
<td>C6A</td>
<td>1374 ohms/sq</td>
<td>broken</td>
</tr>
<tr>
<td>C7A</td>
<td>3930 ohms/sq</td>
<td>2522 ohms/sq</td>
</tr>
<tr>
<td>C8A</td>
<td>4647 ohms/sq</td>
<td>3658 ohms/sq</td>
</tr>
<tr>
<td>Collector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C1A</td>
<td>696 ohms/sq</td>
<td>707 ohms/sq</td>
</tr>
<tr>
<td>Collector Contact</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C2A</td>
<td>195 ohms/sq</td>
<td>111 ohms/sq</td>
</tr>
<tr>
<td>Poly over Oxide</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C15A</td>
<td>350 ohms/sq</td>
<td>79 ohms/sq</td>
</tr>
<tr>
<td>Component</td>
<td>Lot #2:</td>
<td>Furnace</td>
</tr>
<tr>
<td>----------------------</td>
<td>-------------------------------------</td>
<td>---------------</td>
</tr>
<tr>
<td>Emitter</td>
<td>C5A = 183 ohms/sq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C6A = 198 ohms/sq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C7A = 233 ohms/sq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C8A = 83 ohms/sq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C9A = 82 ohms/sq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C10A = 204 ohms/sq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C11A = 85 ohms/sq</td>
<td></td>
</tr>
<tr>
<td>Base</td>
<td>C1A = 1749 ohms/sq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C3A = 1969 ohms/sq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C4A = 700 ohms/sq</td>
<td></td>
</tr>
<tr>
<td>Collector</td>
<td>C12A = 668 ohms/sq</td>
<td></td>
</tr>
<tr>
<td>Collector Contact</td>
<td>C13A = 210 ohms/sq</td>
<td></td>
</tr>
<tr>
<td>Poly over Oxide</td>
<td>C2A = 170 ohms/sq</td>
<td></td>
</tr>
</tbody>
</table>

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9.0 Appendix E

Electrical Plots and Data
1. Diffused Resistor (ohms) Raw Average Data

Lot #1:

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Emitter</th>
<th>Base</th>
<th>Collector</th>
<th>B-Pinch</th>
<th>PolyThin</th>
<th>PolyThick</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>91.3E3</td>
<td>165E3</td>
<td>---</td>
<td>788</td>
<td>146E3</td>
<td>145E3</td>
</tr>
<tr>
<td>D2</td>
<td>103E3</td>
<td>213E3</td>
<td>---</td>
<td>922</td>
<td>186E3</td>
<td>147E3</td>
</tr>
<tr>
<td>D3</td>
<td>135E3</td>
<td>2.45E6</td>
<td>---</td>
<td>782</td>
<td>160E3</td>
<td>147E3</td>
</tr>
<tr>
<td>D4</td>
<td>62.6E3</td>
<td>1.49E6</td>
<td>---</td>
<td>372</td>
<td>65.4E3</td>
<td>66.2E3</td>
</tr>
<tr>
<td>D5</td>
<td>62.7E3</td>
<td>999E6</td>
<td>---</td>
<td>365</td>
<td>64.4E3</td>
<td>65.8E3</td>
</tr>
<tr>
<td>D6</td>
<td>146E3</td>
<td>1.31E6</td>
<td>---</td>
<td>894</td>
<td>180E3</td>
<td>179E3</td>
</tr>
<tr>
<td>D7</td>
<td>104E3</td>
<td>301E3</td>
<td>---</td>
<td>850</td>
<td>150E3</td>
<td>149E3</td>
</tr>
<tr>
<td>D8</td>
<td>61.3E3</td>
<td>289E3</td>
<td>---</td>
<td>362</td>
<td>64.7E3</td>
<td>63.4E3</td>
</tr>
<tr>
<td>D9</td>
<td>56E3</td>
<td>185E3</td>
<td>---</td>
<td>406</td>
<td>66.2E3</td>
<td>66.6E3</td>
</tr>
<tr>
<td>D10</td>
<td>64.0E3</td>
<td>177E3</td>
<td>---</td>
<td>431</td>
<td>80.6E3</td>
<td>75.8E3</td>
</tr>
<tr>
<td>D11</td>
<td>65.1E3</td>
<td>77.2E3</td>
<td>---</td>
<td>393</td>
<td>66.7E3</td>
<td>68.2E3</td>
</tr>
</tbody>
</table>

Lot #2

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Emitter</th>
<th>Base</th>
<th>Collector</th>
<th>B-Pinch</th>
<th>PolyThin</th>
<th>PolyThick</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>14.8E3</td>
<td>676E3</td>
<td>---</td>
<td>529</td>
<td>84.3E3</td>
<td>101E3</td>
</tr>
<tr>
<td>D2</td>
<td>9.41E3</td>
<td>7.84E6</td>
<td>---</td>
<td>297</td>
<td>57.4E3</td>
<td>57.0E3</td>
</tr>
<tr>
<td>D3</td>
<td>69.8E3</td>
<td>4.76E3</td>
<td>---</td>
<td>443</td>
<td>71.0E3</td>
<td>70.0E3</td>
</tr>
<tr>
<td>D4</td>
<td>1.31E3</td>
<td>3.79E6</td>
<td>---</td>
<td>211</td>
<td>36.9E3</td>
<td>36.3E3</td>
</tr>
<tr>
<td>D5</td>
<td>65.7E3</td>
<td>1.08E6</td>
<td>---</td>
<td>644</td>
<td>133E3</td>
<td>129E3</td>
</tr>
<tr>
<td>D7</td>
<td>36.6E3</td>
<td>788E3</td>
<td>---</td>
<td>326</td>
<td>56.2E3</td>
<td>55.4E3</td>
</tr>
<tr>
<td>D8</td>
<td>62.6E3</td>
<td>765E3</td>
<td>---</td>
<td>416</td>
<td>64.8E3</td>
<td>64.8E3</td>
</tr>
</tbody>
</table>
2. Cross-bridge Kelvin Resistors (ohms)

Lot #2

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Emitter</th>
<th>Base</th>
</tr>
</thead>
<tbody>
<tr>
<td>D5</td>
<td>55</td>
<td>90</td>
</tr>
</tbody>
</table>

3. Breakdown Voltages (volts)

Lot #1

<table>
<thead>
<tr>
<th>Wafer</th>
<th>BV_{CBO}</th>
<th>BV_{CEO}</th>
<th>BV_{EBO}</th>
<th>Collector-Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>&gt;100</td>
<td>18.5</td>
<td>3</td>
<td>&gt;100</td>
</tr>
<tr>
<td>D2</td>
<td>&gt;100</td>
<td>25.7</td>
<td>4</td>
<td>&gt;100</td>
</tr>
<tr>
<td>D3</td>
<td>&gt;100</td>
<td>29.4</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>&gt;100</td>
<td>26.7</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td>&gt;100</td>
<td>26.3</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>&gt;100</td>
<td>31.1</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>&gt;100</td>
<td>27.4</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>D8</td>
<td>&gt;100</td>
<td>24.4</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>D9</td>
<td>&gt;100</td>
<td>25.3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>D10</td>
<td>&gt;100</td>
<td>25.0</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>D11</td>
<td>&gt;100</td>
<td>25.5</td>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

Lot #2

<table>
<thead>
<tr>
<th>Wafer</th>
<th>BV_{CBO}</th>
<th>BV_{CEO}</th>
<th>BV_{EBO}</th>
<th>Collector-Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>181</td>
</tr>
<tr>
<td>Lot</td>
<td>D1</td>
<td>D2</td>
<td>D3</td>
<td>D4</td>
</tr>
<tr>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td>#2</td>
<td>&gt;100</td>
<td>&gt;100</td>
<td>&gt;100</td>
<td>&gt;100</td>
</tr>
<tr>
<td></td>
<td>2.8</td>
<td>8.0</td>
<td>13.0</td>
<td>1.63</td>
</tr>
</tbody>
</table>

4.0 Leakage Current Before Density Calculation

Lot #2

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$I_{leak}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>500 pA</td>
</tr>
<tr>
<td>D2</td>
<td>711 pA</td>
</tr>
<tr>
<td>D3</td>
<td>333 pA</td>
</tr>
<tr>
<td>D4</td>
<td>720 pA</td>
</tr>
<tr>
<td>D5</td>
<td>9.94 nA</td>
</tr>
<tr>
<td>D7</td>
<td>6.50 nA</td>
</tr>
<tr>
<td>D8</td>
<td>926 pA</td>
</tr>
<tr>
<td>D9</td>
<td>14.3 nA</td>
</tr>
<tr>
<td>D10</td>
<td>4.09 nA</td>
</tr>
<tr>
<td>D11</td>
<td>13.5 nA</td>
</tr>
</tbody>
</table>
Figure 9E.1 Lot#1 - Wafer D1 - Transistor Characteristic

Figure 9E.2 Lot#1 - Wafer D2 - Transistor Characteristic
**Figure 9E.3** Lot#1 - Wafer D3 - Transistor Characteristic

**Figure 9E.4** Lot#1 - Wafer D4 - Transistor Characteristic
Figure 9E.5 Lot#1 - Wafer D5 - Transistor Characteristic

Figure 9E.6 Lot#1 - Wafer D6 - Transistor Characteristic
Figure 9E.7 Lot#1 - Wafer D7 - Transistor Characteristic

Figure 9E.8 Lot#1 - Wafer D8 - Transistor Characteristic
Figure 9E.9 Lot#1 - Wafer D9 - Transistor Characteristic

Figure 9E.10 Lot#1 - Wafer D10 - Transistor Characteristic
Figure 9E.11 Lot#1 - Wafer D11 - Transistor Characteristic

Figure 9E.12 Lot#2 - Wafer D1 - Transistor Characteristic
Figure 9E.13 Lot#2 - Wafer D1 - Gummel Plot

Figure 9E.14 Lot#2 - Wafer D2 - Gummel Plot
Figure 9E.15 Lot#2 - Wafer D3 - Transistor Characteristic

Figure 9E.16 Lot#2 - Wafer D3 - Maximum Gain
Figure 9E.17 Lot#2 - Wafer D3 - Gummel Plot

Figure 9E.18 Lot#2 - Wafer D4 - Gummel Plot

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Figure 9E.19 Lot#2 - Wafer D7 - Transistor Characteristic

Figure 9E.20 Lot#2 - Wafer D7 - Gummel Plot
Figure 9E.21 Lot#2 - Wafer D8 - Transistor Characteristic

Figure 9E.22 Lot#2 - Wafer D8 - Maximum Gain
Figure 9E.23 Lot#2 - Wafer D8 - Gummel Plot

Figure 9E.24 Lot#2 - Wafer D9 - Transistor Characteristic
**GRAPHICS PLOT**

**Figure 9E.25** Lot#2 - Wafer D9 - Maximum Gain

**GRAPHICS PLOT**

**Figure 9E.26** Lot#2 - Wafer D9 - Gummel Plot

<table>
<thead>
<tr>
<th>LINE 1</th>
<th>17.7E+00</th>
<th>56.4E-03</th>
<th>727E-03</th>
<th>131E-15</th>
</tr>
</thead>
<tbody>
<tr>
<td>LINE 2</td>
<td>1.0000</td>
<td>1.000/00</td>
<td>1.000</td>
<td>1.000</td>
</tr>
</tbody>
</table>
Figure 9E.27 Lot#2 - Wafer D10 - Transistor Characteristic

Figure 9E.28 Lot#2 - Wafer D10 - Maximum Gain
Figure 9E.29 Lot#2 - Wafer D10 - Gummel Plot

Figure 9E.30 Lot#2 - Wafer D12 - Transistor Characteristic
Figure 9E.31 Lot#2 - Wafer D12 - Maximum Gain

Figure 9E.32 Lot#2 - Wafer D12 - Gummel Plot