A CMOS monolithic analog multiplier with wide input dynamic range

George Anthony Hadgis
A CMOS Monolithic Analog Multiplier with Wide Input Dynamic Range

by

George Anthony Hadgis

A Thesis Submitted
in
Partial Fulfillment
of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electrical Engineering

Approved by:

Professor P. Mukund
(Thesis Advisor)

Professor Lynn P. Fuller
(Defense Committee Member)

Professor Daniel Perlman
(Defense Committee Member)

Professor R. Unnikrishnan
(Department Head)

DEPARTMENT OF ELECTRICAL ENGINEERING
COLLEGE OF ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY
ROCHESTER, NEW YORK
MAY 1995
Acknowledgment

This thesis was required in partial fulfillment for the Master of Science degree in Electrical Engineering by Rochester Institute of Technology. I would like to take this opportunity to thank my parents, Anthony and Sophie Hadgis, for their support and encouragement over the past years. I would also like to thank my wife, Teresa, for her patience and encouragement, taking care of our daughter, Katherine, while I spent the many evenings required to complete this thesis.

Also, I would like to thank my advisor, Dr. P.R. Mukund, whose help and guidance made completing this thesis a reality. I would also like to thank my supervisors at the Eastman Kodak Company, Dr. James Walling, Mr. David Swift, and Mr. Peter Rudak for giving me time off during the early phases of this project so that I could conduct my research.

Finally, I would like to thank Mr. Fariborz Barman of National Semiconductor who spent several hours investigating and working with me in developing PSpice simulation models for the components used in the discrete implementation of this project.
Abstract

A novel CMOS monolithic analog multiplier capable of operating in two quadrants is described in this thesis. The multiplier incorporates a voltage-controlled variable linear resistor comprised of two FET transistors in the feedback network of an operational amplifier. This novel approach to implementing an analog multiplier results in good linearity and wide input dynamic range when compared to other implementations where an FET is incorporated in the feedback network of an operational amplifier. The analog multiplier, comprised of an operational amplifier and a variable linear resistor, has been designed. PSpice simulation results are given in support of the multiplier. Experimental results of a discrete implementation are also given. A comparison between the analytical model, the simulation results, and the experimental results is presented at the end of this thesis.
# Table of Contents

**Acknowledgment** ii

**Abstract** iii

**Table of Contents** iv

**List of Figures** vi

**List of Tables** xi

## Chapter 1

### Introduction 1

1.1 Background and Application 1

1.2 Application Proposal 5

## Chapter 2

### Previous Work 8

2.1 General 8

2.2 Single Transistor Multiplier Circuit 9

2.3 Two Transistor Variable Linear Resistor 13

2.4 Technology Proposal 15

## Chapter 3

### Analysis and Design 16

3.1 Analysis of a Two Transistor Variable Linear Resistor 17

3.2 Analysis of a Two Transistor Multiplier Circuit 21

3.3 Design of the Cascode Operational Amplifier 26

3.4 Frequency Analysis of the Monolithic Multiplier 33
<table>
<thead>
<tr>
<th>Chapter 4</th>
<th>PSpice Simulation Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Simulation of a Two Transistor Variable Linear Resistor</td>
</tr>
<tr>
<td>4.2</td>
<td>Simulation of the Cascode Operational Amplifier</td>
</tr>
<tr>
<td>4.3</td>
<td>Simulation of the Monolithic Analog Multiplier</td>
</tr>
<tr>
<td>4.4</td>
<td>Simulation of the Discrete 2Q Analog Multiplier</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Chapter 5</th>
<th>Experimental Results</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Chapter 6</th>
<th>Conclusions</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>General</td>
</tr>
<tr>
<td>6.2</td>
<td>Future Work</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>References</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Appendix A</th>
<th>MOSIS 2.0\mu m Process Parameters</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Appendix B</th>
<th>PSpice Simulation Files</th>
</tr>
</thead>
<tbody>
<tr>
<td>B.1</td>
<td>Monolithic Variable Linear Resistor</td>
</tr>
<tr>
<td>B.2</td>
<td>Open-Loop Cascode Operational Amplifier</td>
</tr>
<tr>
<td>B.3</td>
<td>Unity-Gain Cascode Operational Amplifier</td>
</tr>
<tr>
<td>B.4</td>
<td>National Semiconductor's Model for the LMC6062</td>
</tr>
<tr>
<td>B.5</td>
<td>National Semiconductor's Model for the CD4007</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Appendix C</th>
<th>Monolithic Chip Layout</th>
</tr>
</thead>
</table>

v
List of Figures

Chapter 1

1.1 Block Diagram of a Document Scanner. 1
1.2 CCD Output of One Scan Raster of a White Piece of Paper. 2
1.3 Output of CCD Device and Output of Sample and Hold. 3
1.4 CCD Output of One Scan Raster of a White Piece of Paper After DC Clamping. 4
1.5 Multiplication Circuit in the Scanner. 6

Chapter 2

2.1 Schematic of a Non-Inverting Amplifier. 9
2.2 Schematic of Multiplier Circuit Using an FET in Place of $R_g$. 10
2.3a $i_{dMR2}$ vs. $V_{in1}$ of Circuit Shown in Figure 2.2 for $V_{in2} = 5$ V. 11
2.3b $i_{dMR2}$ vs. $V_{in2}$ of Circuit Shown in Figure 2.2 for $V_{in1} = 0.5$ V. 11
2.4a $V_{out}$ vs. $V_{in1}$ of Circuit Shown in Figure 2.2 for $V_{in2} = 5$ V. 12
2.4b $V_{out}$ vs. $V_{in2}$ of Circuit Shown in Figure 2.2 for $V_{in1} = 0.5$ V. 12
2.5a Gain vs. $V_{in1}$ of Circuit Shown in Figure 2.2 for $V_{in2} = 5$ V. 13
2.5b Gain vs. $V_{in2}$ of Circuit Shown in Figure 2.2 for $V_{in1} = 0.5$ V. 13

2.6 Schematic of the Variable Linear Resistor Proposed by Moon, Zaghloul, and Newcomb. 14

2.7 $i_g$ vs. $V_g$ of Circuit Shown in Figure 2.6 for $V_{in2} = 5$ V. 15

Chapter 3

3.1 Schematic of the Variable Linear Resistor Proposed by Moon, Zaghloul, and Newcomb. 17

3.2 Equation 3.12 Compared to Figure 2.7. 20

3.3 Schematic of Analog Multiplier Utilizing the Two Transistor Variable Resistor. 21

3.4a $V_{out}$ vs. $V_{in1}$ of Circuit Shown in Figure 3.3 for $V_{in2} = 5$ V. 24

3.4b $V_{out}$ vs. $V_{in2}$ of Circuit Shown in Figure 3.3 for $V_{in1} = 0.5$ V. 24

3.5a Gain vs. $V_{in1}$ of Circuit Shown in Figure 3.3 for $V_{in2} = 5$ V. 24

3.5b Gain vs. $V_{in2}$ of Circuit Shown in Figure 3.3 for $V_{in1} = 0.5$ V. 24

3.6a $V_{out}$ vs. $V_{in1}$ of Discrete Implementation for $V_{in2} = 5$ V. 25

3.6b $V_{out}$ vs. $V_{in2}$ of Discrete Implementation for $V_{in1} = 0.5$ V. 25
3.7a Gain vs. $V_{in1}$ of Discrete Implementation  
for $V_{in2} = 5$ V.  

3.7b Gain vs. $V_{in2}$ of Discrete Implementation  
for $V_{in1} = 0.5$ V.  

3.8 Schematic of the Two-Stage Cascode Operational Amplifier.  

3.9 Schematic of the Feedback Network.  

3.10 $s$-Domain System Block Diagram.  

Chapter 4  

4.1 Schematic of the Variable Linear Resistor to be Simulated.  

4.2a Level 1 PSpice Simulation of the Variable Linear Resistor  
Circuit of Figure 4.1.  

4.2b Level 3 PSpice Simulation of the Variable Linear Resistor  
Circuit of Figure 4.1.  

4.3a Cascode Operation Amplifier Schematic.  

4.3b Open-Loop Test Circuit for the Cascode Operational Amplifier.  

4.3c Unity-Gain Test Circuit for the Cascode Operational Amplifier.  

4.4a Frequency Response Plot of Open-Loop Cascode Operational Amplifier.  

4.4b Phase Plot of Open-Loop Cascode Operational Amplifier.  

4.5 Output Swing of Open-Loop Cascode Operational Amplifier.
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.6</td>
<td>Output Voltage Swing of Cascode Operational Amplifier Configured for Unity Gain.</td>
</tr>
<tr>
<td>4.7</td>
<td>Slew Rate of Cascode Operational Amplifier.</td>
</tr>
<tr>
<td>4.8</td>
<td>Complete Schematic of Two-Quadrant Analog Multiplier.</td>
</tr>
<tr>
<td>4.9a</td>
<td>$V_{out}$ vs. $V_{in1}$ of the Monolithic Two-Quadrant Analog Multiplier.</td>
</tr>
<tr>
<td>4.9b</td>
<td>$V_{out}$ vs. $V_{in2}$ of the Monolithic Two-Quadrant Analog Multiplier.</td>
</tr>
<tr>
<td>4.10a</td>
<td>Gain vs. $V_{in1}$ of the Monolithic Two-Quadrant Analog Multiplier.</td>
</tr>
<tr>
<td>4.10b</td>
<td>Gain vs. $V_{in2}$ of the Monolithic Two-Quadrant Analog Multiplier.</td>
</tr>
<tr>
<td>4.11</td>
<td>$V_{out}$ vs. $V_{in1}$ for Various Values of $V_{in2}$ for the Monolithic Two-Quadrant Analog Multiplier.</td>
</tr>
<tr>
<td>4.12</td>
<td>10 kHz Sinusoidal Signal Modulated by a 1 kHz Sinusoidal Signal.</td>
</tr>
<tr>
<td>4.13</td>
<td>FFT of Figure 4.12.</td>
</tr>
<tr>
<td>4.14</td>
<td>Normalized Frequency Analysis of Open-Loop Monolithic Operational Amplifier and Monolithic Two-Quadrant Analog Multiplier.</td>
</tr>
<tr>
<td>4.15</td>
<td>Schematic of Discrete Two-Quadrant Analog Multiplier</td>
</tr>
<tr>
<td>4.16a</td>
<td>$V_{out}$ vs. $V_{in1}$ of the Discrete Two-Quadrant Analog Multiplier.</td>
</tr>
</tbody>
</table>
4.16b \( V_{out} \) vs. \( V_{in2} \) of the Discrete Two-Quadrant Analog Multiplier. 56

4.17a Gain vs. \( V_{in1} \) of the Discrete Two-Quadrant Analog Multiplier. 57

4.17b Gain vs. \( V_{in2} \) of the Discrete Two-Quadrant Analog Multiplier. 57

Chapter 5

5.1a \( V_{out} \) vs. \( V_{in1} \) of Circuit Shown in Figure 4.15 for \( V_{in2} = 3 \) V. 58

5.1b \( V_{out} \) vs. \( V_{in2} \) of Circuit Shown in Figure 4.15 for \( V_{in1} = 1 \) V. 58

5.2a Gain vs. \( V_{in1} \) of Circuit Shown in Figure 4.15 for \( V_{in2} = 3 \) V. 61

5.2b Gain vs. \( V_{in2} \) of Circuit Shown in Figure 4.15 for \( V_{in1} = 1 \) V. 61
List of Tables

Chapter 1

Chapter 2

Chapter 3
3.1 Pole Frequency for Various $V_{in2}$ 38

Chapter 4
4.1 Simulation Performance Characteristics of the Open-Loop Operational Amplifier. 44

Chapter 5
5.1 Comparison of $V_{out}$ Slopes for a Fixed $V_{in2}$ 59
5.2 Comparison of $V_{out}$ Slopes for a Fixed $V_{in1}$ 60
5.3 Comparison of Gain Variability for a Fixed $V_{in2}$ 62
5.4 Comparison of Gain Slopes for a Fixed $V_{in1}$ 62

Chapter 6
Chapter 1

Introduction

1.1 Background and Application

![Block Diagram of a Document Scanner](image)

Figure 1.1 - Block Diagram of a Document Scanner

There are many applications in the electrical engineering field for a wide-bandwidth, voltage-controlled variable-gain analog amplifier. One such application is in document image digitization. Figure 1.1 illustrates a block diagram which describes a very common means of digitizing images using a linear charge-coupled device (CCD) [1]. The components of the block diagram are 1) the light source such as a fluorescent lamp, 2) the document being scanned, 3) the lens assembly, 4) the light sensor such as a CCD, 5) the
sample and hold circuit, 6) the DC clamp circuit, 7) the video amplifier, and 8) the analog-to-digital (A/D) converter chip.

Light is emitted by a light source and onto the document being scanned. Rays of light that strike dark regions of the document are not reflected, while rays of light that strike light regions of the document are reflected in proportion to the "whiteness" of the region. The reflected rays of light are focused through the lens assembly onto the photo sites of the CCD. The CCD's photo sites convert the light energy into a proportional amount of electrical energy (charge). The charge in each photo site is then shifted, with an analog shift register, through a charge-to-voltage converter. This creates an analog data stream corresponding to the amount of light striking the array of photo sites at a particular instant in time. The analog data stream for one raster is shown in Figure 1.2 for a plain white document.

![Diagram](image)

**Figure 1.2 - CCD Output of One Scan Raster of a White Piece of Paper**

The voltage of the data is more negative in the center region than at the ends because the fluorescent lamp's light intensity is greater in the middle than at the ends. This is referred to as lamp fall-off. Another contributor to this non-uniform profile is the \( \cos^4\psi \) function of the lens where \( \psi \) is the angle of inclination, normal to the lens axis.
Figure 1.3 shows a magnified view of a few pixels in the center region of Figure 1.2 to illustrate undesired characteristics of the video signal. Specifically, it is desirable to insure that the video signal not exceed input slew rate and bandwidth requirements of the A/D converter. To prevent this condition from occurring, a sample and hold circuit is used. Figure 1.3 illustrates the resultant signal after sample and hold.

![Graph](image)

**Figure 1.3 - Output of CCD Device and Output of Sample and Hold**

Referring back to Figure 1.2, the region to the far left contains a group of pixels which is masked off, preventing any light from striking them. By using a DC clamp circuit, it is possible to set the voltage level of these black pixels to a known value, usually 0V. As a result, the center region of the data stream is also shifted by the same amount as shown in Figure 1.4.

The purpose of the video amplifier is to amplify the signal so that the white region in the center of the data stream is at or near the maximum input voltage of the A/D converter chip. Setting the gain of the amplifier stage so that the maximum input voltage is reached allows the system to take advantage of the maximum dynamic range of the A/D chip. Finally, the digital output data can be output where 0 represents a black pixel and 255 represents a white pixel in an eight-bit system.
It has been shown that the light output of fluorescent lamps vary as a function of time [2]. Specifically, the phosphor of fluorescent lamps discolor with age causing the frequency spectrum of emitted light to change and the overall light output to decrease. Fluorescent lamp output also degrades as a function of temperature. At both high and low temperatures, the amount of light output by a fluorescent lamp is less than a lamp operating at some nominal temperature.

As a result of this, a white piece of paper under a new lamp will produce a certain CCD output voltage for a particular pixel. A few weeks later, the same pixel will have a different voltage level restricting the dynamic range of the system.

To correct this, two things could be done. The first is to change the reference voltage of the A/D chip during a calibration process [3]. In doing so, the reference voltage can be established periodically and, once established, remain fixed until the next calibration. This allows the system to take advantage of the maximum dynamic range of the A/D converter.
Instead of adjusting the reference voltage of the A/D to match the video level, it is also possible to vary the gain of the video amplifier to bring the video levels into the range of the A/D. This approach is described in the following section. Neither implementation, however, allows the system to correct for the lamp fall-off and lens fall-off described earlier.

1.2 Application Proposal

Although both systems described above have been adjusted to take advantage of the full dynamic range of the A/D chip, the digital output data stream is still not uniform and contains information about the lamp fall-off and lens fall-off. To correct for this, a look-up table containing factors which could dynamically compensate for the data stream profile on a pixel by pixel basis could be used. Then, multiplying each pixel by its corresponding factor will result in a uniform output across the CCD. This method of compensation could be done on the digital data. It could also be performed in the analog domain where an analog multiplier is used. In this scenario, a change on one input effectively causes a proportional change in the gain according to the equation

\[ V_o = V_i V_c K \]  

where:  
\( V_o \) = Output voltage  
\( V_i \) = Input voltage  
\( V_c \) = Gain control voltage  
\( K \) = Gain constant of amplifier

The analog multiplier would be controlled by a gain look-up table which contains the factors necessary to correct for the fall-offs discussed above on a pixel by pixel basis. A
D/A chip would be used to generate the multiplication factor voltage. A block diagram of the amplifier stage is shown in Figure 1.5.

![Block Diagram of Amplifier Stage]

**Figure 1.5 - Multiplication Circuit in the Scanner**

This thesis presents a detailed description of the design, simulation, and test of the multiplier stage of the document scanner described above. Chapter 2 describes previous works in detail. Specifically, it reviews a single transistor multiplier and a variable linear resistor. Both circuits are the basis for the development of this novel approach to implementing a wide dynamic range CMOS multiplier.

Chapter 3 describes the analysis and design of the various sub-circuits used in the complete analog multiplier. The analysis first focuses on the variable linear resistor. It then discusses the complete multiplier circuit designed around an operational amplifier. The chapter then discusses the design and analysis of a complete CMOS cascode operational amplifier suitable for a monolithic design which would incorporate the CMOS variable
linear resistor. Finally, this chapter takes a look at the frequency response of the circuit and how the variable linear resistor affects the frequency response of the operational amplifier.

Chapter 4 presents the simulation results for both the monolithic design and the discrete version of the variable linear resistor and the cascode operational amplifier. Finally, the complete simulation results of both implementations are given with comparisons between the simulated and the theoretical.

Chapter 5 examines the experimental results of the discrete implementation of the multiplier circuit. These results are compared to the theoretical and to the simulation results of the discrete version.

Finally, Chapter 6 summarizes the results of the experimental, simulated, and theoretical data. Limitations are discussed as well as areas of improvement and other implementations.
Chapter 2

Previous Work

2.1 General

Analog multipliers serve many useful functions in today's technology. They have application in automatic gain control, communications, neural networks, and frequency translation. The approach taken by this thesis was originally proposed by Beene [4] in which an FET is placed in the feedback network of an operational amplifier in order to achieve an analog multiplier. Patranabis and Ghosh [5] improved on this idea by enabling control of range and sensitivity of the circuit. Approximately one year later, Moon, Zaghloul, and Newcomb [6] disclosed a variable linear resistor with wide dynamic range. The combination of these two approaches was originally selected as the basis for a variable gain amplifier for the application described in Chapter 1. After further analysis and experimentation, it was found that this same new implementation could be expanded to function as a two-quadrant analog multiplier.

Both of these approaches will be examined in more detail in the following sections. Section 2.2 will examine a single FET transistor in the feedback network of an operational amplifier. Limitations of this circuit will also be presented. Section 2.3 will present the analysis of the variable linear resistor and how this implementation can lead to a much wider input dynamic range. Finally, section 2.4 will summarize the implementation which utilizes both approaches to obtain an improved two-quadrant analog multiplier.
2.2 Single Transistor Multiplier Circuit

The development of Patranabis and Ghosh [5] relies on the drain-source conductance of an FET for a given gate voltage. The FET is placed in the feedback network of an operational amplifier. By varying the conductance of the FET via a control signal at the gate, the gain could be adjusted to create a multiplier. However, since a single FET operating in the linear region is used, the input range is limited to approximately ±100mV to maintain a linear relationship in the multiplication process.

![Schematic of a Non-Inverting Amplifier.](image)

**Figure 2.1 - Schematic of a Non-Inverting Amplifier.**

Figure 2.1 is a schematic of a basic non-inverting amplifier. The output voltage of this amplifier circuit is known to be

\[ V_{\text{out}} = (1 + R_f/R_g) \ V_{\text{in1}} \]  

(2.1)

\( V_{\text{out}} \) is therefore linearly related to \( V_{\text{in1}} \) by the gain constant \( (1 + R_f/R_g) \).
Figure 2.2 - Schematic of Multiplier Circuit Using an FET in Place of $R_g$

The technique of Patranabis and Ghosh [5] relies on the basic concept first proposed by Beene [4] which utilizes an FET transistor in place of $R_g$ as illustrated in Figure 2.2. By varying the gate voltage $V_{in2}$, the drain current through $MR_2$ could be controlled. Assuming that $0 < V_{in1} \leq V_{in2} - V_T2$ (MR$_2$ is in the linear mode of operation), the drain current through $MR_2$ is

$$i_{DMR_2(nonsat)} = K'(nonsat)(W_2/L_2)[(V_{in2} - V_T2) - V_{in1}/2]V_{in1}(1 + \lambda_2 V_{in1})$$

(2.2)

where:

- $K' = \mu_0 C_{0X}$
- $\mu_0$ = The surface mobility of the channel for the MOS device.
- $C_{0X}$ = The capacitance per unit area of the gate oxide.
- $W/L$ = Channel width to length ratio of the MOS devices.
- $V_T$ = Threshold voltage of the MOS device.
- $\lambda$ = Channel length modulation parameter for the MOS device.

If $V_{in2} - V_T2 < V_{in1}$ (MR$_2$ is in the saturation mode of operation), then the drain current through $MR_2$ is
\[ i_{DMR2(sat)} = \frac{1}{2}K'_{(sat)} \left( \frac{W_2}{L_2} \right) (V_{in2} - V_T^2)^2 (1 + \lambda_2 V_{in1}) \]  

(2.3)

Figure 2.3a is a plot of the drain current through MR_2 vs. \( V_{in1} \) when \( V_{in2} = 5 \) volts. The drain current is not linear when \( V_{in1} > \sim 1 \)V. This fact, as will be shown shortly, affects the linearity of the circuit with respect to \( V_{in1} \). Close examination of the plot data also shows that MR_2 is in saturation when \( V_{in1} = V_{in2} \), \( V_T^2 = 4.1728 \) volts. Figure 2.3b is a plot of the drain current through MR_2 vs. \( V_{in2} \) when \( V_{in1} = 0.5 \) volts. This plot shows that good linearity is achieved with respect to \( V_{in2} \) provided that \( V_{in2} > V_T^2 \). Appendix A lists the various process parameters from MOSIS for their 2.0\( \mu \)m process, runs N21H, N23Q, N25Y, N27L, and N29T. The averages of these runs were used for this example. The averages were also used for the design of the analog multiplier described later in this text. Design parameters used for this example are \( W_2 = L_2 = 6 \mu m \). \( R_f \) is assumed to be 24 K\( \Omega \).

![Figure 2.3a - \( i_{DMR2} \) vs. \( V_{in1} \) of Circuit Shown in Figure 2.2 for \( V_{in2} = 5 \) V.](image1.png)

![Figure 2.3b - \( i_{DMR2} \) vs. \( V_{in2} \) of Circuit Shown in Figure 2.2 for \( V_{in1} = 0.5 \) V.](image2.png)
The output voltage of the circuit in Figure 2.2 is seen to be

\[ V_{\text{out}} = V_{\text{in}1} + i_{\text{DMR}2} R_f \]  

(2.4)

Figure 2.4a is a plot of \( V_{\text{out}} \) vs. \( V_{\text{in}1} \). The plot shows that \( V_{\text{out}} \) is not linearly related to \( V_{\text{in}1} \) over the entire input range. By examining Equation 2.4, it can be seen that \( V_{\text{out}} \) is a function of \( i_{\text{DMR}2} \) which was previously shown to not be linear. Figure 2.4b is a similar plot of \( V_{\text{out}} \) vs. \( V_{\text{in}2} \). As can be seen, \( V_{\text{out}} \) is linear with respect to \( V_{\text{in}2} \) provided \( V_{\text{in}2} > V_{T2} \).

![Figure 2.4a - \( V_{\text{out}} \) vs. \( V_{\text{in}1} \) of Circuit Shown in Figure 2.2 for \( V_{\text{in}2} = 5 \) V.](image)

![Figure 2.4b - \( V_{\text{out}} \) vs. \( V_{\text{in}2} \) of Circuit Shown in Figure 2.2 for \( V_{\text{in}1} = 0.5 \) V.](image)

Figure 2.5a is a plot of Gain vs. \( V_{\text{in}1} \). This plot shows that the gain of the circuit is not constant over the entire input range. The slope of the gain curve is -0.559. Figure 2.5b is a plot of Gain vs. \( V_{\text{in}2} \). This figure illustrates that MR2 is in the cutoff region when \( V_{\text{in}2} - V_{T2} \leq 0 \). In the cutoff region, no current flows through MR2, and the gain of the circuit is +1.
2.3 Two Transistor Variable Linear Resistor

Independent of analog multiplier design, Moon, Zaghloul, and Newcomb [6] describe a method for implementing a variable linear resistor. The conductance of the variable linear resistor is found to be linear throughout a wide input voltage range. Although this implementation has been tested in a simple voltage divider, it has application in analog multipliers as well.

Moon, Zaghloul, and Newcomb [6] proposed building a variable linear resistor as illustrated in Figure 2.6. Since the gate of MR₁ is connected to the drain of MR₁, MR₁ is kept in saturation (i.e. $V_{GS₁} \leq V_{DS₁}$). Therefore, the current through MR₁ is

$$i_{DMR₁(sat)} = (1/2)K'_{(sat)}(W₁/L₁)(V_g - E - V_{T₁})^2(1 + λ₁(V_g - E))$$

(2.5)
It is necessary for MR\textsubscript{2} to operate in its linear region for this circuit to function properly. This will become evident shortly (i.e. V_{DS2} \leq V_{GS2} - V_{T2}). Therefore, the current through MR\textsubscript{2} is

\[ i_{DMR2(nonsat)} = K'_{(nonsat)}(W_2/L_2)[(V_{in2} - V_{T2}) - V_g/2]V_g(1+ \lambda_2 V_g) \]

(2.6)

Figure 2.6 - Schematic of the Variable Linear Resistor Proposed by Moon, Zaghloul, and Newcomb.

By summing the current-voltage curves of MR\textsubscript{1} and MR\textsubscript{2}, a straight line is achieved illustrating that the conductance of the variable linear resistor is indeed linear and that the input range has been extended. Equations 2.5 and 2.6 are plotted in Figure 2.7 to illustrate the IV characteristics of the FET's that comprise the variable linear resistor shown in Figure 2.6. Also shown in the figure is the summation of Equations 2.5 and 2.6. The data in Appendix A is used to generate the curves of Figure 2.7.
2.4 Technology Proposal

By taking advantage of the wide dynamic range offered by the variable linear resistor of Moon, Zaghloul, and Newcomb [6], an analog multiplier can be realized with good input dynamic range, an improvement to the ±100mV limitation of Patranabis and Ghosh [5]. This is possible by placing the variable linear resistor in the feedback network of an operational amplifier. One advantage of this implementation is that the input dynamic range has been extended while maintaining good linearity throughout this range. Another advantage to this implementation is that few transistors are required, making it ideal for a monolithic implementation.
Chapter 3

Analysis and Design

This chapter will focus on the analysis and design of the two-quadrant analog multiplier. Specifically, the analysis will discuss the various sub-circuits in the multiplier. The assumptions made during the design process will also be presented in support of a reasonably good model of the multiplier. This model will then be compared to a model where no assumptions are made.

The first section, Section 3.1, will detail the analysis of a two transistor variable linear resistor first proposed by Moon, Zaghloul, and Newcomb [6]. This section will also compare the results of the analysis to the Shichman and Hodges model [7].

Section 3.2 will study the implementation of the variable linear resistor of Moon, Zaghloul, and Newcomb [6] in place of the single FET transistor circuit discussed in Chapter 2. This presentation will also illustrate how the new analog multiplier has increased input dynamic range with better gain "flatness".

Section 3.3 will describe the design technique of Allen and Holberg for a cascode operational amplifier [7]. A cascode operational amplifier was selected since it has a relatively high bandwidth compared to a two-stage unbuffered operational amplifier. The process to be used is the Orbit 2μ low noise analog N-well process through MOSIS.
Section 3.4 will examine the frequency response of the complete monolithic multiplier which incorporates the variable linear resistor described in Section 3.1 with the cascode operational amplifier discussed in Section 3.3. The layout for the monolithic multiplier is included in the Appendix C.

### 3.1 Analysis of a Two Transistor Variable Linear Resistor

![Figure 3.1 - Schematic of the Variable Linear Resistor Proposed by Moon, Zaghloul, and Newcomb.](image)

The analysis of the circuit illustrated in Figure 3.1 is presented here. First, assume that $V_g \geq 0$. $MR_1$ is in the saturation region because of the gate-to-drain connection. Therefore the current through $MR_1$, $i_{DMR_1(sat)}$, is:

$$i_{DMR_1(sat)} = \frac{1}{2}K'(sat)(W_1/L_1)(V_{GS1} - V_T1)^2(1 + \lambda V_{DS1})$$

(3.1)

Assuming $\lambda$ is approximately zero implies $(1 + \lambda V_{DS1}) \equiv 1$ and Equation 3.1 becomes:

$$i_{DMR_1(sat)} \equiv \frac{1}{2}K'(sat)(W_1/L_1)(V_g + E - V_T1)^2$$

(3.2)
We also know that MR$_1$ is in the cut-off region if:
\[ i_{DMR_1(cutoff)} = 0 \text{ when } (V_g + E) \leq V_T_1 \quad (3.3) \]

Assuming that MR$_2$ is in the linear region \((V_{in2} \geq V_g + V_T_2)\), the current through MR$_2$ is:
\[ i_{DMR_2(nonsat)} = K'(nonsat)(W_2/L_2)[(V_{GS2} - V_T_2) - V_{DS2}/2]V_{DS2}(1 + \lambda V_{DS2}) \quad (3.4) \]

Assuming \(\lambda\) is approximately zero implies \((1 + \lambda V_{DS2}) \approx 1\) and Equation 3.4 becomes:
\[ i_{DMR_2(nonsat)} = K'(nonsat)(W_2/L_2)[(V_{GS2} - V_T_2)V_{DS2} - V_{DS2}^2/2] \quad (3.4a) \]

Now if \(0 \leq V_g \leq (V_{in2} - V_T_1)\), i.e. if MR$_2$ is in the linear region, Equation 3.4a becomes:
\[ i_{DMR_2(nonsat)} = K'(nonsat)(W_2/L_2)[(V_{in2} - V_T_2)V_g - V_g^2/2] \quad (3.4b) \]

If \((V_T_1 - E) \leq V_g \leq (V_{in2} - V_T_2)\), then:
\[ I_g = i_{DMR_1(sat)} + i_{DMR_2(nonsat)} \quad (3.5) \]

Substituting Equations 3.2 and 3.4b into Equation 3.5 yields:
\[ I_g \equiv (1/2)K'(sat)(W_1/L_1)(V_g + E - V_T_1)^2 + K'(nonsat)(W_2/L_2)[(V_{in2} - V_T_2)V_g - V_g^2/2] \quad (3.6) \]

Expanding Equation 3.6 and combining like terms yields:
\[ I_g \equiv [(1/2)K'(sat)(W_1/L_1) + (1/2)K'(nonsat)(W_2/L_2)]V_g^2 + 
\[ + [(1/2)K'(sat)(W_1/L_1)2E^2 - (1/2)K'(sat)(W_1/L_1)V_T_1 + 
\[ + K'(nonsat)(W_2/L_2)V_{in2} - K'(nonsat)(W_2/L_2)V_T_2)V_g + 
\[ + (1/2)K'(sat)(W_1/L_1)(E^2 + V_T_1^2 - 2EV_T_1)] \quad (3.7) \]
Choosing \( \frac{1}{2}K'(\text{sat})(W_1/L_1) = \frac{1}{2}K'(\text{nonsat})(W_2/L_2) = K \) and substituting into Equation 3.7 yields:

\[
I_g = (2KE - 2KV_T + 2KV_{in2} - 2KV_{T2})V_g + KE^2 + KV_{T1}^2 - 2KEV_T
\]

(3.8)

Choosing \( V_{T1} = V_{T2} = V_T \) and substituting into Equation 3.8 yields:

\[
I_g = (2KE - 4KV_T + 2KV_{in2})V_g + KE^2 + KV_T^2 - 2KEV_T
\]

(3.9)

Let \( \alpha \) equal the coefficient of \( V_g \) and \( \beta \) equal the constant term of Equation 3.9:

\[
\alpha = 2KE - 4KV_T + 2KV_{in2}
\]

(3.10a)

\[
\beta = KE^2 + KV_T^2 - 2KEV_T = K(E - V_T)^2
\]

(3.10b)

\[
I_g = \alpha V_g + \beta
\]

(3.10c)

Choosing \( E = V_T \):

\[
\alpha = 2KV_T - 4KV_T + 2KV_{in2} = 2K(V_{in2} - V_T)
\]

(3.11a)

\[
\beta = 0
\]

(3.11b)

\[
I_g = \alpha V_g
\]

(3.11c)

Substituting Equation 3.11a into Equation 3.11c yields

\[
I_g = 2K(V_{in2} - V_T)V_g
\]

(3.12)

Equation 3.12 is plotted and compared to the summation curve of Figure 2.7 in Figure 3.2. It can be seen that Equation 3.12 is a good approximation to the summation of \( i_{DMR1} \) and \( i_{DMR2} \) (refer to Figure 2.6). The data shown in Appendix A is used to create the plot shown in Figure 3.2.
The discrepancy illustrated in Figure 3.2 can be attributed to the assumption that 
\((1 + \lambda V_{DS1}) \equiv 1\) and \((1 + \lambda V_{DS2}) \equiv 1\). In fact, if \(\lambda = 0\), the two curves of Figure 3.2 are identical provided that \((V_{in2} \geq V_{g} + V_{T2})\) and \(0 \leq V_{g} \leq (V_{in2} - V_{T1})\). This observation verifies the algebra of the above analysis and shows that the assumptions are valid.

![Graph](image)

**Figure 3.2** - Equation 3.12 Compared to Figure 2.7.
3.2 Analysis of a Two Transistor Multiplier Circuit

Recognizing that Equation 3.12 is similar in form to Ohm's Law:

\[ R_{\text{g}} = \frac{l}{2K(V_{\text{in}} - V_T)} \]  

(3.13)

Now the transistor circuit of Figure 3.1 can replace the discrete resistor \( R_{\text{g}} \) of Figure 2.1. The schematic of this circuit is shown in Figure 3.3.

Substituting Equation 3.13 into Equation 2.1 yields

\[ V_{\text{out}} = K' R_f V_{\text{in}} - K' V_{\text{in}} + V_{\text{in}} \]  

(3.14)

Since \( K' \) and \( V_r \) are constant for the technology being used in fabricating the analog multiplier, it is possible to select a value for \( R_f \) which will cause the second term in Equation 3.14 to equal \( V_{\text{in}} \). In other words,

\[ R_f = \frac{l}{K V_T} \]  

(3.15)

Figure 3.3 - Schematic of Analog Multiplier Utilizing the Two Transistor Variable Resistor
Substituting Equation 3.15 into Equation 3.14 causes the second and third terms to drop out and Equation 3.14 becomes the multiplier function sought

\[ V_{\text{out}} = \frac{V_{\text{in}_2} V_{\text{in}_1}}{V_T} \quad \text{when: } V_{\text{in}_2} \geq V_{\text{in}_1} + V_T \]  \hfill (3.16)

Equation 3.16 holds true only when \( V_{\text{in}_2} \geq V_{\text{in}_1} + V_T \) in order to keep MR2 in its linear region. When MR2 is in the saturation region (\( V_{\text{in}_1} \geq V_{\text{in}_2} - V_T \)), the circuit ceases to function as a multiplier. Under this condition, \( V_{\text{out}} \) becomes the voltage across the variable linear resistor, \( V_{\text{in}_1} \), plus the voltage across the feedback resistor:

\[ V_{\text{out}} = V_{\text{in}_1} + I_{R_f} R_f = V_{\text{in}_1} + K V_{\text{in}_1}^2 R_f / 2 + K(V_{\text{in}_2} - V_T)^2 R_f / 2 \quad \text{when: } V_{\text{in}_2} < V_{\text{in}_1} + V_T \]  \hfill (3.17a)

When MR2 is in the cutoff region (\( V_{\text{in}_2} - V_T < 0 \)), \( V_{\text{out}} \) becomes independent of \( V_{\text{in}_2} \) and the circuit once again ceases to function as a multiplier. Under this condition, \( V_{\text{out}} \) is again the voltage across the variable linear resistor, \( V_{\text{in}_1} \), plus the voltage across the feedback resistor:

\[ V_{\text{out}} = V_{\text{in}_1} + I_{R_f} R_f = V_{\text{in}_1} + K V_{\text{in}_1}^2 R_f / 2 \quad \text{when: } V_{\text{in}_2} < V_T \]  \hfill (3.17b)

Figure 3.4a is a plot of \( V_{\text{out}} \) vs. \( V_{\text{in}_1} \). The plot shows that \( V_{\text{out}} \) is now linearly related to \( V_{\text{in}_1} \) over the input range as defined by equation 3.16. Although not obvious in the figure, the curve is defined by Equation 3.17a when \( V_{\text{in}_1} > V_{\text{in}_2} - V_T \). Since \( \lambda \neq 0 \), a slight error exists as illustrated in the figure. When compared with Figure 2.4a, the input dynamic range has been significantly improved while maintaining a reasonable linear relationship. Figure 3.4b is a similar plot of \( V_{\text{out}} \) vs. \( V_{\text{in}_2} \). As can be seen, \( V_{\text{out}} \) is linear with respect to
V_{in2} provided V_{in2} > V_{T2}. Furthermore, we see that the assumption \( \lambda = 0 \) does not affect \( V_{out} \) as a function of \( V_{in2} \) and so the addition of MR\(_1\) does not have a significant effect on the slope of the curve. We can therefore conclude that the addition of MR\(_1\) improves the input dynamic range and linearity without significantly affecting the rest of the circuit.

Figure 3.5a is a plot of Gain vs. \( V_{in1} \). This plot shows that the gain of the circuit is now constant over most of the input range with a slope of 0. Again, since \( \lambda \neq 0 \), there is a slight error illustrated in the figure. The slope in this case is 0.101 which is more than a 5x improvement over the circuit of Figure 2.2 (refer to Figure 2.5a). Figure 3.5b is a plot of Gain vs. \( V_{in2} \). This figure illustrates the effect of MR\(_2\) entering the cutoff region when \( V_{in2} \leq V_{T2} \leq 0 \). In the cutoff region, no current flows through MR\(_2\), and the gain of the circuit is +1. Once again, the addition of MR\(_2\) doesn't seem to significantly effect the performance of the circuit with respect to \( V_{in2} \). We can therefore conclude that the addition of MR\(_1\) improves the gain "flatness" without significantly effecting the rest of the circuit.

Figure 3.6a through Figure 3.7b illustrate the theoretical performance curves of the discrete implementation of the monolithic two-quadrant analog multiplier using the process parameters outlined in Appendix B.5. In this case, \( V_T = 1.6V \), which is defined by the PSpice model for the variable linear resistor transistors used in the discrete implementation. Consistent results are achieved in the discrete case.

In Figures 3.4a, 3.5a, 3.6a, and 3.7a, we noted a sensitivity of \( V_{OUT} \) to the channel length modulation parameter, \( \lambda \), when compared to \( V_{in1} \). This can be explained by examining Equation s 3.1 and 3.4. In both equations, the factor \((1 + \lambda V_{DS})\) illustrates how \( \lambda \) affects the overall IV characteristics of the variable linear resistor and therefore \( V_{OUT} \) vs. \( V_{in1} \). It
does not have an affect on the IV characteristics of the variable linear resistor when \( V_{\text{OUT}} \) is compared to \( V_{\text{in2}} \) since \( V_{\text{in2}} \) (\( V_{\text{GS}} \)) has no effect on the channel length as evident in Figures 3.4b, 3.5b, 3.6b, and 3.7b.

![Figure 3.4a - \( V_{\text{out}} \) vs. \( V_{\text{in1}} \) of Circuit Shown in Figure 3.3 for \( V_{\text{in2}} = 5 \) V.](image1)

![Figure 3.4b - \( V_{\text{out}} \) vs. \( V_{\text{in2}} \) of Circuit Shown in Figure 3.3 for \( V_{\text{in1}} = 0.5 \) V.](image2)

![Figure 3.5a - Gain vs. \( V_{\text{in1}} \) of Circuit Shown in Figure 3.3 for \( V_{\text{in2}} = 5 \) V.](image3)

![Figure 3.5b - Gain vs. \( V_{\text{in2}} \) of Circuit Shown in Figure 3.3 for \( V_{\text{in1}} = 0.5 \) V.](image4)
Figure 3.6a - $V_{out}$ vs. $V_{in1}$ of the Discrete Implementation for $V_{in2} = 5$ V.

Figure 3.6b - $V_{out}$ vs. $V_{in2}$ of the Discrete Implementation for $V_{in1} = 0.5$ V.

Figure 3.7a - Gain vs. $V_{in1}$ of the Discrete Implementation for $V_{in2} = 5$ V.

Figure 3.7b - Gain vs. $V_{in2}$ of the Discrete Implementation for $V_{in1} = 0.5$ V.
3.3 Design of the Cascode Operational Amplifier

The fabrication process selected for this design was Orbit's 2.0μ low noise analog N-well CMOS process through MOSIS. A two-stage cascode operational amplifier was the architecture selected since it has a relatively high bandwidth when compared to a two-stage unbuffered operational amplifier. The cascode operational amplifier shown in Figure 3.8 is comprised of a differential stage (M₁ M₅) followed by the cascode output stage (M₆ M₉, MC₁ MC₃).

The circuit requirements were selected based on typical performance characteristics of a 2.0μ CMOS operational amplifier. Since the purpose of the design is illustrative, reasonable constraints were placed on the design. The circuit requirements are listed below:

**Circuit Requirements**

Supply Voltage: ± 5VDC  
Slew Rate: 5V/μS  
Output Voltage Swing: ± 3V  
Gain Bandwidth: 5MHz  
Open Loop Gain: 5000  
Input Common Mode Range: ± 3V  
Load: 50pF and 10MΩ
Figure 3.8 - Schematic of the Two-Stage Cascode Operational Amplifier

The design of a cascode operational amplifier used for this thesis is based on the design method taught by Allen and Holberg [7]. All calculations are based on the average process parameters shown in Appendix A.

The first step is to determine the sink and source current capability of the operational amplifier. This is accomplished by knowing the desired slew rate for a given capacitive load. This can be determined from:

\[ \tau = R C_L = (V/I) \times C_L \]  \hspace{1cm} (3.18)

Therefore

\[ I_{out} = 5V/\mu S \times 50pF = 250\mu A \]  \hspace{1cm} (3.19)
If the maximum output sinking current is to be equal in magnitude to the maximum output sourcing current, then the width-to-length ratios of the circuit transistors \((S)\) are

\[
S_1 = S_2, \quad S_3 = S_4, \quad S_6 = S_9, \quad S_7 = S_8
\]

(3.20)

Now choosing \(I_5 = 100\mu A\) and knowing that under maximum dynamic conditions all of the current in \(I_5\) will flow through \(M_3\) or \(M_4\), we can apply the current mirror equation as follows:

\[
I_{\text{out}} = (S_6/S_4)I_5
\]

(3.21)

and,

\[
S_6 = S_9 = I_{\text{out}}S_4/I_5 = 2.5 S_4 = 2.5 S_3
\]

(3.22)

Assuming that,

\[
V_{\text{dsC1sat}} = V_{\text{ds7sat}}
\]

(3.23)

Implies that

\[
V_{\text{dsC1sat}} = V_{\text{ds7sat}} = -(V_{ss} - V_{\text{outmax}})/2 = 1V
\]

(3.24)

And the maximum current through \(M_{C1}\) and \(M_7\) is

\[
I_{C1} = I_7 = 250\mu A
\]

(3.25)

Using the saturation equation yields

\[
S_7 = S_{C1} = (2I_7) / (K'_{\text{Nsat}}V_{\text{ds7sat}}^2) = (2I_{C1}) / (K'_{\text{Nsat}}V_{\text{dsC1sat}}^2) = 9.9
\]

(3.26)

From Equation 3.20 above

\[
S_8 = S_7 = 9.9
\]

(3.27)
Similarly

\[ S_6 = S_{C2} = \frac{(2I_6)}{(K'_{\text{psat}} V_{ds_s\text{sat}}^2)} = \frac{(2I_{C2})}{(K'_{\text{psat}} V_{ds_{C2}\text{sat}}^2)} = 27.3 \quad (3.28) \]

From Equation 3.22 above

\[ S_9 = S_6 = 2.5 S_4 = 2.5 S_3 \quad (3.29) \]

Implying

\[ S_4 = S_3 = 10.92 \quad (3.30) \]

For a first order approximation, Allen and Holberg [7] ignore bulk effect for calculating biasing voltages for the output stage. This was found to not be sufficient during simulation and that bulk effect must also be considered.

\[ V_{bp} = V_{dd} - V_{ds_{6\text{sat}}} - V_{ds_{C2\text{sat}}} - V_{t_{C2}} \quad (3.31a) \]

\[ V_{bn} = V_{ss} + V_{ds_{7\text{sat}}} + V_{ds_{C1\text{sat}}} + V_{t_{C1}} \quad (3.31b) \]

where:

\[ V_t = V_{io} + \gamma [\sqrt{2|\phi| V_{eb}} - \sqrt{2|\phi|}] \quad (3.32) \]

The above equations yield

\[ V_{bp} = 1.797 \text{ and } V_{bn} = -2.075 \quad (3.33) \]

Next, the input common-mode range must be considered. To do this, the minimum value for \( S_3 \) is calculated and compared to the value calculated in Equation 3.30.

\[ S_3 \geq 2 I_5 / K'_{\text{psat}}(-V_{in_{\text{max}}} + V_{dd} - |V_{t_{O3}}|_{\text{max}} + V_{t_{l_{\text{min}}}})^2 \quad (3.34) \]
Ignoring bulk effect \((V_{sb} = 0)\) yields:

\[
S_3 \geq 3.04
\]  \hspace{1cm} (3.35)

A larger value for \(S_3\) will yield a larger \(V_{\text{in}_{\text{max}}}\) and therefore \(S_3 = 10.92\) is acceptable:

\[
V_{\text{in}_{\text{max}}} = V_{dd} \cdot \sqrt{(I_5 / K'_{\text{Psat}} S_3) - |V_{\text{to}}|_{\text{max}} + V_{\text{t1}_{\text{min}}}} = 3.23V
\]  \hspace{1cm} (3.36)

The next step is to calculate the value for \(S_1\) (and \(S_2\)). The overall open-loop gain the operational amplifier is equal to the product of the gain of the differential stage and the gain of the output stage:

\[
A_v = A_{v_{\text{diff}}} A_{v_{\text{output}}} = \left(\frac{g_m}{g_{m3}}\right) \left(\frac{g_{m6} + g_{m7}}{R_{||}}\right) / 2
\]  \hspace{1cm} (3.37a)

where:

\[
A_{v_{\text{diff}}} = \frac{g_m}{g_{m3}} \hspace{1cm} (3.37b)
\]

\[
A_{v_{\text{output}}} = \left(\frac{g_{m6} + g_{m7}}{R_{||}}\right) / 2 \hspace{1cm} (3.37c)
\]

\[
g_m = \sqrt{(2 \cdot K_{\text{sat}} I_d S)} \hspace{1cm} (3.37d)
\]

\[
R_{||} = \left(\frac{g_{m_{c2}} r_{dsc6} r_{ds6}}{g_{m_{c1}} r_{dsc7} r_{ds7}}\right) \hspace{1cm} (3.37e)
\]

\[
r_{ds} = 1 / (\lambda I_d) \hspace{1cm} (3.37f)
\]

from the above equations,

\[
g_{m3} = 141.2 \mu S, \quad g_{m6} = 353.6 \mu S, \quad g_{m7} = 353.6 \mu S, \quad R_{||} = 8.4M\Omega \hspace{1cm} (3.38)
\]

and knowing \(A_v \geq 5000\) yields

\[
g_{m1} = g_{m2} \geq 238 \mu S \hspace{1cm} (3.39)
The gain bandwidth requirement also must be used to find an acceptable value for $g_{m1}$ and $g_{m2}$:

\[ GB \geq g_{m1} \left( g_{m6} + g_{m7} \right) / \left( 2 \ g_{m4} \ C_{\parallel} \right) \]  

(3.40a)

where:

\[ C_{\parallel} = \text{the output load capacitance} \]  

(3.40b)

From the above equation,

\[ g_{m1} = g_{m2} = 628.3 \ \mu S \]  

(3.41)

which satisfies Equation 3.39. Using Equation 3.37d yields,

\[ S_1 = S_2 = 78.0 \]  

(3.42)

It is also necessary to verify that the common-mode range, CMR, specification has been met.

\[ V_{\text{in max}} = V_{dd} - \sqrt{\left( I_{d5 \text{sat}} / \beta_3 \right)} - \left| V_{t03} \right|_{\text{max}} \ V_{t_{\text{min}}} = 3.23 \ \text{V} \]  

(3.43a)

\[ V_{\text{in min}} = V_{ss} + \sqrt{\left( I_{d5 \text{sat}} / \beta_1 \right)} + V_{t_{\text{max}}} + V_{ds5_{\text{sat}}} = -3.84 \ \text{V} \]  

(3.43b)

where:

\[ \beta = \left( K' \right) \ W / L = \left( K' \right) \ S \]  

(3.43c)

\[ V_{ds5_{\text{sat}}} = \sqrt{\left( I_{d5 \text{sat}} / K'_{\text{sat}} \ S_5 \right)} = 0.28 \ \text{V} \]  

(3.43d)

The final open-loop gain and gain bandwidth product are found using Equations 3.37a and 3.40a, respectively, to be $A_v = 13,197$ and $GB = 5 \ \text{MHz}$. 
Finally, the bias voltage at the gate of $M_5$ is calculated.

$$V_{bias} = V_{ss} + V_{W5} + V_{ds5_{sat}} = -3.892 \text{ V}$$ (3.44)

Below is a list of the W/L ratios rounded-off for a $2\mu$m process, final performance characteristics, and bias voltage requirements:

- Sink/Source Current: 250$\mu$A
- $S_7 = S_8 = S_{C1}$: 10
- $S_6 = S_9 = S_{C2} = S_{C3}$: 27.5
- $S_3 = S_4$: 11
- Gate Voltage $M_{C1}$: -2.075
- Gate Voltage $M_{C2}$: 1.797
- $S_1 = S_2$: 78
- Gate Voltage $M_5$: -3.892
- Final Open-Lop Gain: 13,197
- Final Gain Bandwidth Product: 5 MHz
3.4 Frequency Analysis of the Monolithic Multiplier

In this section, an analysis of the frequency response of the circuit will be presented. First, the frequency response of the CMOS monolithic open-loop operational amplifier will be studied followed by the frequency response of the variable linear resistor. Finally, the system frequency response will be presented.

Examining Figure 3.8, two nodes will affect the frequency response of the open-loop operational amplifier. The first node is at the output, \( V_{\text{out}} \). Using the process parameters listed in Appendix A, the capacitance at this node is:

\[
C_z = C_{\text{GD}C_1} + C_{\text{GD}C_2} + C_{\text{load}}
\]

\[
\equiv C_{\text{load}} = 50 \text{ pF}
\]

The resistance at this node is:

\[
R_z = R_{\text{load}} \parallel R_T \parallel R_B
\]

\[
= 10 \text{ M}\Omega \parallel 3.56 \text{ M}\Omega \parallel 24.7 \text{ M}\Omega = 2.37 \text{ M}\Omega
\]

where:

\[
R_T = r_{ds6} + r_{dsC2} + g_{mC2} r_{ds6} r_{dsC2}(1 + \eta_{C2})
\]

\[
\equiv r_{ds6} + r_{dsC2} + g_{mC2} r_{ds6} r_{dsC2} = 3.56 \text{ M}\Omega
\]

\[
R_B = r_{ds7} + r_{dsC1} + g_{mC1} r_{ds7} r_{dsC1}(1 + \eta_{C1})
\]

\[
\equiv r_{ds7} + r_{dsC1} + g_{mC1} r_{ds7} r_{dsC1} = 24.7 \text{ M}\Omega
\]

\[
\eta = \frac{g_{mbs}}{g_m} \equiv 0
\]

The dominant pole is therefore:

\[
f_0 = \frac{1}{2\pi C_z R_z} = 1.343 \text{ kHz}
\]
A similar analysis can be done for the second node. This node is at the drain of $M_2$. The resistance at this node is:

$$R_x = r_{ds4} \parallel \frac{1}{g_{m4}} \parallel r_{ds2} \left(1 + g_{m2} r_{ds5}\right)$$

$$\equiv \frac{1}{g_{ds2} + g_{m4}} = 6.933 \text{ k}\Omega$$

Using the large signal model, the capacitances for this node can be calculated [8]. The capacitance at this node is:

$$C_x = C_{ds2} + C_{gb4} + C_{gs4} + C_{gs6} + C_{gsC2}$$

(3.49)

As will be seen later, some of these capacitances are assumed to be zero by PSpice. Therefore, they will also be assumed to be zero for comparison purposes. Equation 3.49 therefore becomes:

$$C_x = C_{gs4} + C_{gs6} + C_{gsC2} \equiv 477.6 \text{ fF}$$

(3.50a)

where:

$$C_{gs4} = \left(C_{gs4} (0) / F2\right) \left(F3 + V_{gs4} / 2 \Phi I_0\right) = 70.8 \text{ fF}$$

(3.50b)

$$C_{gs6} = \left(C_{gs6} (0) / F2\right) \left(F3 + V_{gs6} / 2 \Phi I_0\right) = 194.3 \text{ fF}$$

(3.50c)

$$C_{gs6} (0) = \left(C_{gsC2} (0) / F2\right) \left(F3 + V_{gsC2} / 2 \Phi I_0\right) = 212.5 \text{ fF}$$

(3.50d)

$$C_{gs4} (0) = CGS0 (W_{effM4}) + \left(\frac{2}{3}\right) COX W_{effM4} L_{effM4}$$

(3.50e)

$$C_{gs6} (0) = C_{gsC2} (0) = CGS0 (W_{effM6}) + \left(\frac{2}{3}\right) COX W_{effM6} L_{effM6}$$

(3.50f)

$$W_{eff} = W - 2WD$$

(3.50g)

$$L_{eff} = L - 2LD$$

(3.50h)

$$F2 = (1 - FC)^{1 + m} = 0.34$$

(3.50i)

$$F3 = 1 - FC^{1 + m} = 0.66$$

(3.50j)
The second dominant pole is therefore:

\[ f_1 = \frac{1}{2\pi C_x R_x} = 48 \text{ MHz} \]  

(3.51)

A similar analysis must be done for the variable linear resistor before a system level frequency response can be calculated. Examining Figure 3.9, it can be seen that only one node needs to be considered and is labeled \( V_g \). The capacitance at this node is:

\[ C = C_{gsMR1} \parallel C_{gdMR2} = 1.52 \text{ fF} \]  

(3.52)

where:

\[ C_{gsMR1} = CGS0 (W_{effMR1}) + \left(\frac{2}{3}\right) COX W_{effMR1} L_{effMR1} = 1.52 \text{ fF} \]  

(3.52a)

\[ C_{gdMR2} = [CGD0 + \left(\frac{1}{2}\right) COX L_{effMR2}] W_{effMR2} = 0.00152 \text{ fF} \]  

(3.52b)

Since this capacitance is so small, we can ignore the effects of this circuit on the overall system performance.
The general frequency domain transfer function of the system shown in Figure 3.10 is known to be:

\[ \frac{V_{\text{out}}(s)}{V_{\text{in1}}(s)} = \frac{A(s)}{(1 + A(s) B(s))} \]  

(3.53)

From the previous analysis, it is known that there are two poles associated with the operational amplifier:

\[ A(s) = \frac{A_0}{(1 + s/2\pi f_0)(1 + s/2\pi f_1)} \]  

(3.54)

And a single pole associated with the linear resistor:

\[ B(s) = \frac{B_0}{(1 + s/2\pi f_2)} \]  

(3.55)

From the previous analysis, it was shown that \( f_2 \) is very large. Therefore, Equation 3.55 becomes:

\[ B(s) = B_0 \]  

(3.56)

Substituting Equation 3.54 and 3.56 into 3.53 yields:
\[
V_{\text{out}(s)} \div V_{\text{in1}(s)} = \frac{A_0}{((1 + s/2 \pi f_0) (1 + s/2 \pi f_1) + A_0 B_0)}
\]  
(3.57)

After working through some algebra, the above equation becomes:
\[
V_{\text{out}(s)} \div V_{\text{in1}(s)} = \frac{A_0}{2^2 \pi^2 f_0 f_1 / (s^2 + 2 \pi (f_0 + f_1) s + 2^2 \pi^2 f_0 f_1 (A_0 B_0 + 1))}
\]  
(3.58)

Comparing the above equation to the general second order transfer function of a low-pass system shown below:
\[
V_{\text{out}(s)} \div V_{\text{in1}(s)} = \pm A_0 \omega_n^2 / s^2 + 2 \zeta \omega_n s + \omega_n^2
\]  
(3.59)

It can be seen that the pole frequency of the system is:
\[
f_n = \sqrt{(f_0 f_1 (A_0 B_0 + 1))}
\]  
(3.60)

However, \(B_0\) is a function of \(V_{\text{in2}}\). Therefore, \(f_n\) will vary depending on \(V_{\text{in2}}\). By examining the circuit of Figure 3.9, it can be seen that the gain of the linear resistor is established by the voltage divider circuit comprised of \(R_f\) and \(R_{\text{geq}}\):
\[
B_0 = R_{\text{geq}} / (R_{\text{geq}} + R_f)
\]  
(3.61)

where: \(R_{\text{geq}}\) was defined in Equation 3.13
From this information, a table can be created which describes the pole frequency $f_n$ for a given $V_{in2}$.

<table>
<thead>
<tr>
<th>$V_{in2}$</th>
<th>$R_{seq}$</th>
<th>$B_0$</th>
<th>$f_n$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>114.4 kΩ</td>
<td>0.82</td>
<td>17.2 MHz</td>
</tr>
<tr>
<td>2</td>
<td>16.6 kΩ</td>
<td>0.41</td>
<td>12.2 MHz</td>
</tr>
<tr>
<td>3</td>
<td>9.1 kΩ</td>
<td>0.28</td>
<td>10 MHz</td>
</tr>
<tr>
<td>4</td>
<td>6.3 kΩ</td>
<td>0.21</td>
<td>8.7 MHz</td>
</tr>
<tr>
<td>5</td>
<td>4.7 kΩ</td>
<td>0.16</td>
<td>7.6 MHz</td>
</tr>
</tbody>
</table>

Table 3.1 - Pole Frequency for Various $V_{in2}$
Chapter 4

PSpice Simulation Results

This chapter will discuss the simulation results of the various sub-circuits in the monolithic implementation. Simulation results will also be given for the complete monolithic circuit. A similar set of simulation results will be presented for the complete discrete implementation.

Section 4.1 will illustrate the PSpice simulation results for the monolithic variable linear resistor discussed in Chapter 3. In this section, a level 1 simulation and a level 3 simulation will be compared to the theoretical model developed in the previous section. It will be shown that the level 1 simulation model is very consistent with the analytical model developed in the previous section. A level 3 simulation will also be discussed, illustrating discrepancies between the two models. This will be an important issue when the experimental data of Chapter 5 is reviewed and compared to the analytical model of Chapter 3.

Section 4.2 will discuss the simulation results of the cascode operational amplifier. In this section, the open-loop characteristics will be discussed and compared to the operational amplifier designed in Chapter 3. Unity gain characteristics will also be evaluated. The characteristics of the operational amplifier are tabulated at the end of this section.

Section 4.3 discusses the simulation results of the complete monolithic analog multiplier. The results will be compared to the analytical model described in Chapter 3. Once again, discrepancies between level 1 and level 3 models will be documented.
Finally, Section 4.4 will discuss the simulation results of the discrete version of the analog multiplier. Since the integrated circuit chip was never tested, a discrete implementation was built and tested. The results of this experiment, described in Chapter 5, will be compared to the simulation results of this section.

4.1 Simulation of a Two Transistor Variable Linear Resistor

Figure 4.1 is the schematic of the variable linear resistor used for simulation. This schematic is identical to Figure 3.1 and includes the node numbers used in the PSpice input file. Appendix B.1 is the input file used for the simulation.

![Figure 4.1 - Schematic of the Variable Linear Resistor to be Simulated.](image)
Figure 4.2a - Level 1 PSpice Simulation of the Variable Linear Resistor Circuit of Figure 4.1.

Figure 4.2b - Level 3 PSpice Simulation of the Variable Linear Resistor Circuit of Figure 4.1.
The results of the level 1 simulation are shown in Figure 4.2a. Examining the slope of the total current through both transistors, it can be seen that these results are approximated by the analytical model very well (refer to Figure 2.7). A similar simulation was performed using a level 3 PSpice model for the transistors. The results of this simulation are shown in Figure 4.2b. In this case the discrepancy is quite high. In fact, the error is greater than 2x. These discrepancies can be attributed to two items. The first is that the Shichman-Hodges model used for the PSpice level 1 model is different than the semi-empirical model for level 3 which takes into account process geometries. The other contributor to the error is the assumption that the channel width modulation parameter for the transistor, $\lambda$, is negligible.
4.2 Simulation of the Cascode Operational Amplifier

Figure 4.3a illustrates the schematic of the cascode operational amplifier used for this simulation. It is identical to Figure 3.8 with the addition of the bias voltage circuits and the node identification numbers for the simulation. In order to simplify the simulation, the circuit of Figure 4.3a was implemented as a sub-circuit as illustrated in Appendix B.2 and Appendix B.3. Figure 4.3b illustrates the open-loop test circuit used to evaluate the performance of the cascode operational amplifier. Figure 4.3c illustrates the unity-gain test circuit used to evaluate the performance of the cascode operational amplifier.

![Figure 4.3a - Cascode Operational Amplifier Schematic](image)

![Figure 4.3b - Open-Loop Test Circuit for Cascode Operational Amplifier](image)
Figure 4.3c - Unity-Gain Test Circuit for Cascode Operational Amplifier

Figure 4.4a illustrates the frequency response of the open-loop operational amplifier. Although there is quite a discrepancy between the theoretical and simulated open-loop gains, the original design called for a gain of 5000 (74 dB). Figure 4.4b is the phase response of the circuit. Figure 4.5 shows the output swing of the open-loop operational amplifier. Figure 4.6 illustrates the output voltage swing of the operational amplifier configured as a unity gain amplifier. It can be seen that the linearity of the amplifier is quite good. Figure 4.7 shows the slew-rate of the unity gain amplifier. From these figures, the following characteristics can be obtained:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Theoretical</th>
<th>Simulated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Bandwidth Product</td>
<td>5 MHz</td>
<td>4.5 MHz</td>
</tr>
<tr>
<td>Open-Loop Gain</td>
<td>13197 (82 dB)</td>
<td>5623 (75 dB)</td>
</tr>
<tr>
<td>Dominant Pole</td>
<td>1.343 kHz</td>
<td>1 kHz</td>
</tr>
<tr>
<td>Other Poles</td>
<td>48 MHz</td>
<td>60 MHz</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>± 3 volts</td>
<td>± 4.6 volts</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>5 V/μsec</td>
<td>4.71 V/μsec</td>
</tr>
</tbody>
</table>

Table 4.1 - Simulation Performance Characteristics of the Open-Loop Operational Amplifier
Figure 4.4a - Frequency Response Plot of Open-Loop Cascode Operational Amplifier

Figure 4.4b - Phase Plot of Open-Loop Cascode Operational Amplifier
Figure 4.5 - Output Swing of Open-Loop Cascode Operational Amplifier

Figure 4.6 - Output Voltage Swing of Operational Amplifier Configured for Unity Gain
Figure 4.7 - Slew Rate of Operational Amplifier
4.3 Simulation of the Monolithic Analog Multiplier

Figure 4.8 is the complete schematic of the monolithic two-quadrant analog multiplier. It includes node numbers which correspond to the simulation file. Figure 4.9a shows how $V_{out}$ varies vs. $V_{in1}$. The top curve corresponds to a level 1 PSpice simulation for $V_{in2} = 5$ V. Because of the gain established by the feedback resistor and the variable linear resistor, $V_{in1}$ is restricted to vary between 0 and 600 mV in order to prevent the output from clipping. As will be shown later with the discrete model, a different process with a large $V_T$ yields a smaller gain range. As a result, the inputs can have an even larger dynamic range.

If Figure 4.9a is compared with Figure 3.6a, the top curve of Figure 4.9a (the level 1 simulation) closely approximates the analytical model. This, of course, makes sense since the analytical model was based on level 1 equations. If a first order approximation is acceptable, then the analytical model is a good estimator. If second order effects must be considered, then a level 3 simulation is in order. The bottom curve of Figure 4.9a corresponds to a level 3 simulation. The discrepancies between the analytical model and the level 3 simulation can be attributed to the equations used for the level 3 simulation.

Figure 4.9b illustrates how $V_{out}$ varies as $V_{in2}$ changes for a fixed value of $V_{in1} = 0.5$ V. Once again, the top trace corresponds to a level 1 simulation which corresponds to Figure 3.6b. When compared to Figure 3.6b, we see that the level 1 simulation once again is closely approximated by the analytical model used to plot Figure 3.6b. The bottom trace represents the results of the level 3 simulation. Again, the error is associated with the model used.
Figure 4.10a illustrates the gain of Figure 4.9a as $V_{in1}$ is varied. This plot corresponds to the analytical model used to plot Figure 3.7a. Once again, the upper trace closely approximates the analytical model. Some error is seen in the lower trace which represents the level 3 simulation.

Likewise, Figure 4.10b is the simulation result showing Gain vs. $V_{in2}$ with $V_{in1}$ fixed at 0.5 V. Once again, the top trace is the level 1 simulation while the bottom trace is the level 3 simulation.
Figure 4.9a - $V_{out}$ vs. $V_{in1}$ of the Monolithic 2-Quadrant Analog Multiplier

Figure 4.9b - $V_{out}$ vs. $V_{in2}$ of the Monolithic 2-Quadrant Analog Multiplier
Figure 4.10a - Gain vs. $V_{\text{in}1}$ of the Monolithic 2-Quadrant Analog Multiplier

Figure 4.10b - Gain vs. $V_{\text{in}2}$ of the Monolithic 2-Quadrant Analog Multiplier
Figure 4.11 is a plot illustrating the linearity of the monolithic two-quadrant analog multiplier for various values of $V_{in1}$ and $V_{in2}$ using a level 3 simulation. Figure 4.12 is a plot illustrating the output of the circuit when a 10 kHz sinusoidal signal applied to $V_{in1}$ is modulated by a 1 kHz sinusoidal signal applied to $V_{in2}$. Once again, the simulation level is 3. An FFT analysis was performed on Figure 4.12 to identify the frequency content and is shown in Figure 4.13. Three frequencies were found: the primary frequency of 10 kHz and two sideband frequencies at 9 kHz and 11 kHz, as expected. The same circuit was simulated at higher frequencies and found to perform with similar characteristics. The signals used in this circuit simulation were a 5 MHz sinusoid modulated by a 500 kHz sinusoid. Still higher frequencies (10 MHz modulated by 1 MHz) were simulated, but with output signal quality degradation determined by examination of the FFT results.

Figure 4.11 - $V_{out}$ vs. $V_{in1}$ for Various Values of $V_{in2}$ for the Monolithic 2-Quadrant Analog Multiplier
Figure 4.12 - 10 kHz Sinusoidal Signals Modulated by a 1 kHz Sinusoidal Signal

Figure 4.13 - FFT of Figure 4.12
Figure 4.14 illustrates the normalized frequency response of the monolithic analog multiplier. The open-loop frequency response shown is the normalized frequency response of Figure 4.4a for the operational amplifier circuit (refer to Figure 4.3b). The normalized closed-loop frequency response curve shown corresponds to the complete circuit shown in Figure 4.8. The actual 3-dB cut-off frequency is dependent upon \( V_{in2} \) as illustrated in Table 3.1. In this particular simulation example, the 3-dB cut-off frequency is approximately 6MHz for \( V_{in2} = 3V \). According to Table 3.1, the theoretical 3-dB cut-off frequency should be 10 MHz for \( V_{in2} = 3V \). The discrepancy can be attributed to the approximations used to generate the theoretical model. Once again the theoretical model is based on level 1 PSpice models rather than level 3.

\[
\begin{align*}
\text{Gain} & \quad 100K & \quad 1M & \quad 100M \\
\text{Frequency (Hz)} & \quad 1K & \quad 10K & \quad 100K & \quad 10M
\end{align*}
\]

**Figure 4.14 - Normalized Frequency Analysis of Open-Loop Monolithic Operational Amplifier and Monolithic 2-Quadrant Analog Multiplier**
4.4 Simulation of the Discrete Two-Quadrant Analog Multiplier

Figure 4.15 is a schematic of the discrete version of the analog multiplier. The simulation results of this design are illustrated in this section. Experimental results will be given in Chapter 5. The LMC6062 operational amplifier was selected because it is a CMOS device which has similar characteristics to the CMOS monolithic operational amplifier. The CD4007 device was selected because it was readily available. Since the source of each transistor is internally connected to the substrate, it was necessary to use two individual CD4007 devices. As a result, transistor mismatches are present, affecting performance.

The LMC6062 PSpice model is readily available from National Semiconductor. The CD4007 integrated circuit, on the other hand, is a very old technology and its PSpice model was not directly available from National Semiconductor. After several phone conversations with Fariborz Barman at National, we pieced together what we believed to be an accurate PSpice model for the process. The PSpice model for the LMC6062 and the CD4007 are shown in Appendices B.4 and B.5.

![Figure 4.15 - Schematic of Discrete 2-Quadrant Analog Multiplier](image)
Figure 4.16a - $V_{out}$ vs. $V_{in1}$ of the Discrete 2-Quadrant Analog Multiplier

Figure 4.16b - $V_{out}$ vs. $V_{in2}$ of the Discrete 2-Quadrant Analog Multiplier
Figure 4.17a - Gain vs. $V_{in1}$ of the Discrete 2-Quadrant Analog Multiplier

Figure 4.17b - Gain vs. $V_{in2}$ of the Discrete 2-Quadrant Analog Multiplier
Chapter 5

Experimental Results

This chapter will discuss the experimental data collected and will compare it with the theoretical analysis and simulations. The experimental circuit is shown in Figure 4.15. The operational amplifier used for this circuit is an LMC6062 CMOS operational amplifier from National Semiconductor. The linear resistor circuit is comprised of two N-channel MOS transistors found in the CD4007 integrated circuit also available from National Semiconductor. Due to problems associated with the substrate of the CD4007, it was necessary to use two separate packages so that the sources of each transistor could be isolated from each other and from the substrate.

Figure 5.1a - \( V_{\text{out}} \) vs. \( V_{\text{in1}} \) of Circuit Shown in Figure 4.15 for \( V_{\text{in2}} = 3 \) V.

Figure 5.1b - \( V_{\text{out}} \) vs. \( V_{\text{in2}} \) of Circuit Shown in Figure 4.15 for \( V_{\text{in1}} = 1 \) V.
Figure 5.1a illustrates how V_{out} varies as V_{in1} changes from 0 to 5 volts while maintaining V_{in2} at a constant 3.0 volts. This figure shows that the measured data closely approximates the theoretical. Specifically, the slope of the theoretical curve is 1.875 while the slope of the measured curve is 1.932 yielding a percentage error is 2.95%. Since the power supply voltages are ±5 volts, the operational amplifier clips the output to the rail when \( V_{in1} / V_T > \pm 5V \).

Also shown in Figure 5.1a are the experimental results when a single transistor is used in the feedback loop of the operational amplifier as shown in Figure 2.2 (IQ Measured). In this circuit, the output voltage, V_{out}, is not linear throughout the entire input range of V_{in1}. In fact, it is linear only when V_{in1} is less than approximately 0.6 V. It is non-linear at voltages greater than 0.6 volts.

The simulation results of this circuit are shown in Figure 4.16a and are similar to the experimental results. The slope of the level 1 simulation is approximately 1.5. The slope of the level 3 simulation is approximately 1.75. The percentage error of the level 1 and level 3 simulations to the measured slope are 22% and 9.4%, respectively. Table 5.1 lists the slopes with percentage errors from the experimental results.

<table>
<thead>
<tr>
<th>Description</th>
<th>Slope</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theoretical</td>
<td>1.875</td>
<td>2.95%</td>
</tr>
<tr>
<td>Level 1 Simulation</td>
<td>1.5</td>
<td>22%</td>
</tr>
<tr>
<td>Level 3 Simulation</td>
<td>1.75</td>
<td>9.4%</td>
</tr>
<tr>
<td>Experimental</td>
<td>1.932</td>
<td>n/a</td>
</tr>
</tbody>
</table>

Table 5.1 - Comparison of V_{out} Slopes for a Fixed V_{in2}
A similar experiment can be conducted where $V_{\text{in1}}$ is maintained at 1 volt while varying $V_{\text{in2}}$. This experimental data is shown in Figure 5.1b. The plot shows some errors exist between the theoretical data and the measured data. In this experiment, the slope of the theoretical data curve is 0.604 while the slope of the measured curve is 1.07 (an error of 44%). The results of the level 1 simulation are shown in Figure 4.16b. The slope of this simulation is approximately 0.675 which deviates from the measured value by 36.9%. The slope of the level 3 simulation is approximately 1.0 (an error of approximately 7%). Table 5.2 lists the slopes with percentage errors from the experimental results.

<table>
<thead>
<tr>
<th>Description</th>
<th>Slope</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theoretical</td>
<td>0.604</td>
<td>44%</td>
</tr>
<tr>
<td>Level 1 Simulation</td>
<td>0.675</td>
<td>36.9%</td>
</tr>
<tr>
<td>Level 3 Simulation</td>
<td>1.0</td>
<td>7%</td>
</tr>
<tr>
<td>Experimental</td>
<td>1.07</td>
<td>n/a</td>
</tr>
</tbody>
</table>

**Table 5.2 - Comparison of $V_{\text{out}}$ Slopes for a Fixed $V_{\text{in1}}$**

In both Table 5.1 and Table 5.2, significant errors are noticed both in the theoretical data and the level 1 simulations when compared to the measured data. These errors were expected and are explained in Chapters 3 and 4. To reiterate, the theoretical model is based on the equations used for a level 1 simulation. Furthermore, the channel length modulation parameter, $\lambda$, is assumed to be negligible. For these reasons, there are errors in the theoretical model which may be acceptable if a first order approximation is used. Although the errors are significant, it should be noted that the two-transistor circuit satisfies the requirement of being linear over a wider input range than the one-transistor circuit.
We have compared the experimental and theoretical output voltages of the circuit. It is also interesting to compare gains. Figure 5.2a shows that the gain of the circuit utilizing a single transistor in the feedback loop decreases significantly as $V_{in1}$ increases. This fact can be explained by referring to Figure 3.7. Only one transistor is being used and its IV characteristic is not linear as $V_g$ varies. As a result, the gain of the circuit varies. For example, in this experiment, the gain varies from 1.385 to 2.30, a variability of 0.92. In the two-transistor circuit, the gain of the circuit does not vary as widely as in the one transistor circuit. In this example, the circuit gain varies from 2.5 to 2.187, a variability of 0.313. This represents almost a 3x improvement in gain flatness. The simulation results are shown in Figure 4.17a. From this simulation, the variability of the level 1 simulation is approximately 0.3 over the same input range. The variability of the level 3 simulation is approximately 0.15. Table 5.3 lists the variabilities discussed above.
<table>
<thead>
<tr>
<th>Description</th>
<th>Variability</th>
</tr>
</thead>
<tbody>
<tr>
<td>One Transistor</td>
<td>0.92</td>
</tr>
<tr>
<td>Theoretical</td>
<td>0</td>
</tr>
<tr>
<td>Level 1 Simulation</td>
<td>0.3</td>
</tr>
<tr>
<td>Level 3 Simulation</td>
<td>0.15</td>
</tr>
<tr>
<td>Experimental</td>
<td>0.313</td>
</tr>
</tbody>
</table>

Table 5.3 - Comparison of Gain Variability for a Fixed $V_{in2}$

A similar comparison can be done for $V_{in1}$ equal to 1.0 volt with a variable $V_{in2}$. Table 5.4 lists the relevant slopes with percentage errors from the experimental results.

<table>
<thead>
<tr>
<th>Description</th>
<th>Slope</th>
<th>Slope</th>
</tr>
</thead>
<tbody>
<tr>
<td>One Transistor</td>
<td>1.07</td>
<td>0%</td>
</tr>
<tr>
<td>Theoretical</td>
<td>0.604</td>
<td>44%</td>
</tr>
<tr>
<td>Level 1 Simulation</td>
<td>0.675</td>
<td>36.9%</td>
</tr>
<tr>
<td>Level 3 Simulation</td>
<td>1.0</td>
<td>7%</td>
</tr>
<tr>
<td>Experimental</td>
<td>1.07</td>
<td>n/a</td>
</tr>
</tbody>
</table>

Table 5.4 - Comparison of Gain Slopes for a Fixed $V_{in1}$

Although there are discrepancies between the theoretical, simulated, and experimental data as shown in the above tables, it is more important to note that the variability of the gain in Figures 5.2a and 5.2b has improved over the single transistor implementation. Once again, the errors can be attributed to first order approximations of the circuit, the assumption that the channel length modulation parameter is negligible, and that there may be mismatches between the PSpice process parameters and the actual circuit design. Since the process parameters used are from old technologies though, they are the most up to date available...
from National Semiconductor. Another possible reason for the discrepancies is that there may have also been mismatches between the two transistors used for the variable linear resistor since each transistor was in a separate package.
Chapter 6

Conclusions

6.1 General

A reasonably good first order approximation of a two quadrant analog multiplier was presented in this thesis. The model is consistent with the Shichman and Hodges model used by PSpice for level 1 simulations. Further, some errors are present as a result of neglecting the channel length modulation parameter, λ. In fact, it was found that if the channel length modulation parameter were not ignored, an even better approximation can be achieved.

Larger differences were identified when these results were compared to level 3 PSpice simulation results and experimental results. These discrepancies are explained by the fact that in level 3 simulations, semi-empirical data is used which takes into account process geometries. In fact, the level 3 simulations were much more in line with experimental results.

Although the discrepancies between the first order approximation and the experimental results may be significant, it is important to note that the original goal of a wider input dynamic range has been achieved. This is evident by the gain flatness curves that were discussed in the previous chapters. By incorporating two transistors in the feedback
network of an operational amplifier, it is possible to achieve a multiplier with a wider input dynamic range than that achievable with a more common single transistor implementation.

### 6.2 Future Work

Certainly, it would be desirable to expand the operation of this two quadrant analog multiplier into all four quadrants. Perhaps the switched capacitor implementation of Patranabis and Ghosh [5] could be applied to this design.

The frequency analysis that was conducted in this thesis showed that the pole associated with the variable linear resistor was at a very high frequency. The variable linear resistor and the feedback resistor form a voltage divider with a gain of less than one. Therefore, the pole is negligible assuming that the dimensions of the transistors used are reasonably small. We therefore can conclude that the frequency response of the multiplier is only limited by the operational amplifier’s frequency response.

Based on this observation, it should be possible, using a bi-CMOS process, to design a bipolar operational amplifier with a wide gain bandwidth product and incorporate a CMOS variable linear resistor, taking advantage of the characteristics of CMOS technology to achieve an analog multiplier with wide input dynamic range.

Finally, it may be of interest to further study the sensitivity of the circuit to the channel length modulation parameter, $\lambda$. Perhaps an application such as Maple could be used to accurately solve the complete algebraic equation which describes the circuit characteristics.
References


## Appendix A

### MOSIS 2.0u Low Noise Analog Process Parameters

<table>
<thead>
<tr>
<th>NMOS Run</th>
<th>N21H</th>
<th>N23Q</th>
<th>N25Y</th>
<th>N27L</th>
<th>N29T</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ld</td>
<td>2.50E-07</td>
<td>2.20E-07</td>
<td>2.50E-07</td>
<td>1.00E-07</td>
<td>1.93E-07</td>
<td>2.03E-07</td>
</tr>
<tr>
<td>Tox</td>
<td>4.17E-08</td>
<td>3.75E-08</td>
<td>4.18E-08</td>
<td>4.36E-08</td>
<td>4.15E-08</td>
<td>4.16E-08</td>
</tr>
<tr>
<td>Nsub</td>
<td>9.24E+14</td>
<td>7.62E+14</td>
<td>6.11E+14</td>
<td>5.70E+14</td>
<td>5.84E+15</td>
<td>1.74E+15</td>
</tr>
<tr>
<td>Vto</td>
<td>0.858153</td>
<td>0.81056</td>
<td>0.825008</td>
<td>0.774163</td>
<td>0.8679</td>
<td>0.8271568</td>
</tr>
<tr>
<td>Kp</td>
<td>5.05E-05</td>
<td>5.29E-05</td>
<td>4.92E-05</td>
<td>5.07E-05</td>
<td>4.99E-05</td>
<td>5.06E-05</td>
</tr>
<tr>
<td>Gamma</td>
<td>0.198</td>
<td>0.1819</td>
<td>0.172</td>
<td>0.1737</td>
<td>0.5303</td>
<td>0.25118</td>
</tr>
<tr>
<td>Phi</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>Uo</td>
<td>596.729</td>
<td>605.312</td>
<td>594</td>
<td>640.393</td>
<td>601</td>
<td>607.4868</td>
</tr>
<tr>
<td>Uexp</td>
<td>7.03E-02</td>
<td>8.52E-02</td>
<td>6.82E-02</td>
<td>9.83E-02</td>
<td>1.60E-01</td>
<td>9.64E-02</td>
</tr>
<tr>
<td>Ucrit</td>
<td>1026.7</td>
<td>1467.84</td>
<td>5000</td>
<td>15018.5</td>
<td>8.10E+04</td>
<td>2.518E+04</td>
</tr>
<tr>
<td>Delta</td>
<td>2.7371</td>
<td>1.71295</td>
<td>5.08308</td>
<td>2.56466</td>
<td>4.003</td>
<td>3.220118</td>
</tr>
<tr>
<td>Vmax</td>
<td>65701.4</td>
<td>64128.9</td>
<td>65574.3</td>
<td>60711.9</td>
<td>61580</td>
<td>65533.9</td>
</tr>
<tr>
<td>Xj</td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td>2.50E-07</td>
</tr>
<tr>
<td>Lamda</td>
<td>1.84E-02</td>
<td>1.74E-02</td>
<td>6.64E-03</td>
<td>1.87E-02</td>
<td>2.99E-02</td>
<td>1.82E-02</td>
</tr>
<tr>
<td>Nfs</td>
<td>1.09E+12</td>
<td>1.09E+12</td>
<td>1.98E+11</td>
<td>1.05E+12</td>
<td>4.55E+12</td>
<td>1.59E+12</td>
</tr>
<tr>
<td>Neff</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Nss</td>
<td>1.00E+10</td>
<td>1.00E+10</td>
<td>1.00E+10</td>
<td>1.00E+10</td>
<td>1.00E+10</td>
<td>1.00E+10</td>
</tr>
<tr>
<td>Tpg</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Rs h</td>
<td>28.76</td>
<td>29.39</td>
<td>32.74</td>
<td>31.21</td>
<td>26.63</td>
<td>29.746</td>
</tr>
<tr>
<td>Cgdo</td>
<td>3.10E-10</td>
<td>2.89E-10</td>
<td>3.11E-10</td>
<td>1.91E-10</td>
<td>2.40E-10</td>
<td>2.54E-10</td>
</tr>
<tr>
<td>Cgso</td>
<td>3.10E-10</td>
<td>2.89E-10</td>
<td>3.11E-10</td>
<td>1.91E-10</td>
<td>2.40E-10</td>
<td>2.54E-10</td>
</tr>
<tr>
<td>Cgbo</td>
<td>3.84E-10</td>
<td>4.34E-10</td>
<td>3.85E-10</td>
<td>3.61E-10</td>
<td>4.10E-10</td>
<td>3.95E-10</td>
</tr>
<tr>
<td>Cj</td>
<td>9.00E-05</td>
<td>9.00E-05</td>
<td>9.49E-05</td>
<td>8.19E-05</td>
<td>1.01E-04</td>
<td>9.15E-05</td>
</tr>
<tr>
<td>Mj</td>
<td>0.783638</td>
<td>0.784</td>
<td>0.847099</td>
<td>0.761646</td>
<td>0.8562</td>
<td>0.8065166</td>
</tr>
<tr>
<td>CjsW</td>
<td>5.52E-10</td>
<td>5.53E-10</td>
<td>4.41E-10</td>
<td>5.62E-10</td>
<td>4.65E-10</td>
<td>5.15E-10</td>
</tr>
<tr>
<td>MjsW</td>
<td>0.285064</td>
<td>0.285</td>
<td>0.33406</td>
<td>0.297471</td>
<td>0.343293</td>
<td>0.3089776</td>
</tr>
<tr>
<td>Pbj</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>Delta W</td>
<td>2.40E-07</td>
<td>3.50E-07</td>
<td>2.50E-07</td>
<td>1.00E-07</td>
<td>4.00E-07</td>
<td>2.68E-07</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Median</th>
<th>Std Dev.</th>
<th>Variance</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.203E-07</td>
<td>6.210E-08</td>
<td>3.857E-15</td>
</tr>
<tr>
<td>4.170E-08</td>
<td>1.454E-09</td>
<td>2.113E-18</td>
</tr>
<tr>
<td>7.619E+14</td>
<td>2.294E+15</td>
<td>5.263E+30</td>
</tr>
<tr>
<td>8.250E-01</td>
<td>3.778E-02</td>
<td>1.427E-03</td>
</tr>
<tr>
<td>5.048E-05</td>
<td>1.393E-06</td>
<td>1.939E-12</td>
</tr>
<tr>
<td>1.819E-01</td>
<td>1.564E-01</td>
<td>2.445E-02</td>
</tr>
<tr>
<td>6.000E-01</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>6.010E+02</td>
<td>1.889E+01</td>
<td>3.568E+02</td>
</tr>
<tr>
<td>8.518E-02</td>
<td>3.767E-02</td>
<td>1.419E-03</td>
</tr>
<tr>
<td>1.468E+04</td>
<td>3.145E+04</td>
<td>9.889E+08</td>
</tr>
<tr>
<td>2.737E+00</td>
<td>1.325E+00</td>
<td>1.755E+00</td>
</tr>
<tr>
<td>6.413E+04</td>
<td>2.285E+03</td>
<td>5.222E+06</td>
</tr>
<tr>
<td>2.500E-07</td>
<td>3.553E-15</td>
<td>1.262E-29</td>
</tr>
<tr>
<td>1.843E-02</td>
<td>8.229E-03</td>
<td>6.772E-05</td>
</tr>
<tr>
<td>1.086E+12</td>
<td>1.694E+12</td>
<td>2.868E+24</td>
</tr>
<tr>
<td>1.000E+00</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>1.000E+01</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>2.939E+01</td>
<td>2.341E+00</td>
<td>5.479E+00</td>
</tr>
<tr>
<td>2.888E+10</td>
<td>8.061E+11</td>
<td>6.498E+21</td>
</tr>
<tr>
<td>2.888E+10</td>
<td>8.061E+11</td>
<td>6.498E+21</td>
</tr>
<tr>
<td>3.848E+10</td>
<td>7.269E+11</td>
<td>7.669E+22</td>
</tr>
<tr>
<td>9.000E-05</td>
<td>6.936E-06</td>
<td>4.810E-11</td>
</tr>
<tr>
<td>7.840E-01</td>
<td>4.231E-02</td>
<td>1.790E-03</td>
</tr>
<tr>
<td>5.525E-10</td>
<td>5.691E-11</td>
<td>3.239E-21</td>
</tr>
<tr>
<td>2.975E-01</td>
<td>2.778E-02</td>
<td>7.715E-04</td>
</tr>
<tr>
<td>8.000E-01</td>
<td>1.054E-08</td>
<td>1.110E-16</td>
</tr>
<tr>
<td>2.500E-07</td>
<td>1.155E-07</td>
<td>1.334E-14</td>
</tr>
</tbody>
</table>
# Appendix A

## MOSIS 2.0u Low Noise Analog Process Parameters

<table>
<thead>
<tr>
<th>PMOS</th>
<th>Run</th>
<th>N21H</th>
<th>N23Q</th>
<th>N25Y</th>
<th>N27L</th>
<th>N29T</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ld</td>
<td></td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td>2.27E-07</td>
<td>1.00E-07</td>
<td>3.41E-07</td>
<td>2.34E-07</td>
</tr>
<tr>
<td>Tox</td>
<td></td>
<td>4.18E-08</td>
<td>3.95E-08</td>
<td>4.17E-08</td>
<td>4.36E-08</td>
<td>4.16E-08</td>
<td>4.16E-08</td>
</tr>
<tr>
<td>Nsub</td>
<td></td>
<td>9.31E+15</td>
<td>9.20E+15</td>
<td>1.06E+16</td>
<td>8.83E+15</td>
<td>1.02E+16</td>
<td>9.62E+15</td>
</tr>
<tr>
<td>Vto</td>
<td>-0.889271</td>
<td>-0.971428</td>
<td>-0.937048</td>
<td>-0.971599</td>
<td>-0.9403</td>
<td><strong>-0.9419292</strong></td>
<td></td>
</tr>
<tr>
<td>Kp</td>
<td></td>
<td>1.91E-05</td>
<td>1.92E-05</td>
<td>1.73E-05</td>
<td>1.77E-05</td>
<td>1.84E-05</td>
<td>1.83E-05</td>
</tr>
<tr>
<td>Gamma</td>
<td></td>
<td>0.6289</td>
<td>0.6321</td>
<td>0.715</td>
<td>0.6836</td>
<td>0.701</td>
<td><strong>0.67212</strong></td>
</tr>
<tr>
<td>Phi</td>
<td></td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td><strong>0.6</strong></td>
</tr>
<tr>
<td>Uo</td>
<td></td>
<td>216.28</td>
<td>219</td>
<td>209</td>
<td>223.389</td>
<td>221.4</td>
<td><strong>217.8138</strong></td>
</tr>
<tr>
<td>Uexp</td>
<td></td>
<td>2.18E-01</td>
<td>2.51E-01</td>
<td>2.34E-01</td>
<td>0.245977</td>
<td>0.2558</td>
<td>2.41E-01</td>
</tr>
<tr>
<td>Ucrit</td>
<td></td>
<td>62664</td>
<td>76412.8</td>
<td>47509.9</td>
<td>55425.2</td>
<td>51320</td>
<td><strong>58666.38</strong></td>
</tr>
<tr>
<td>Delta</td>
<td></td>
<td>0.164572</td>
<td>0.554525</td>
<td>1.07179</td>
<td>0.52685</td>
<td>4.665</td>
<td><strong>1.3964344</strong></td>
</tr>
<tr>
<td>Vmax</td>
<td></td>
<td>100000</td>
<td>89217.7</td>
<td>100000</td>
<td>100000</td>
<td>1.00E+06</td>
<td><strong>277823.54</strong></td>
</tr>
<tr>
<td>Xj</td>
<td></td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td>2.50E-07</td>
<td><strong>2.50E-07</strong></td>
</tr>
<tr>
<td>Lamda</td>
<td></td>
<td>5.01E-02</td>
<td>5.37E-02</td>
<td>4.39E-02</td>
<td>5.01E-02</td>
<td>4.49E-02</td>
<td><strong>4.86E-02</strong></td>
</tr>
<tr>
<td>Nfs</td>
<td></td>
<td>9.27E+11</td>
<td>1.00E+11</td>
<td>3.27E+11</td>
<td>9.30E+11</td>
<td>4.56E+12</td>
<td><strong>1.37E+12</strong></td>
</tr>
<tr>
<td>Neff</td>
<td></td>
<td>1.001</td>
<td>1.001</td>
<td>1.001</td>
<td>1.001</td>
<td>1.001</td>
<td><strong>1.001</strong></td>
</tr>
<tr>
<td>Nss</td>
<td></td>
<td>1.00E+10</td>
<td>1.00E+10</td>
<td>1.00E+10</td>
<td>1.00E+10</td>
<td>1.00E+10</td>
<td><strong>1.00E+10</strong></td>
</tr>
<tr>
<td>Tpg</td>
<td></td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td><strong>-1</strong></td>
</tr>
<tr>
<td>Rs0</td>
<td></td>
<td>66.82</td>
<td>65.02</td>
<td>72.96</td>
<td>63.89</td>
<td>61.59</td>
<td><strong>66.056</strong></td>
</tr>
<tr>
<td>Cgdo</td>
<td></td>
<td>3.10E-10</td>
<td>3.28E-10</td>
<td>2.82E-10</td>
<td>1.19E-10</td>
<td>4.25E-10</td>
<td><strong>2.93E-10</strong></td>
</tr>
<tr>
<td>Cgso</td>
<td></td>
<td>3.10E-10</td>
<td>3.28E-10</td>
<td>2.82E-10</td>
<td>1.19E-10</td>
<td>4.25E-10</td>
<td><strong>2.93E-10</strong></td>
</tr>
<tr>
<td>Cgbo</td>
<td></td>
<td>3.73E-10</td>
<td>4.66E-10</td>
<td>5.29E-10</td>
<td>5.47E-10</td>
<td>4.20E-10</td>
<td><strong>4.67E-10</strong></td>
</tr>
<tr>
<td>Cj</td>
<td></td>
<td>2.98E-04</td>
<td>2.03E-04</td>
<td>3.22E-04</td>
<td>3.19E-04</td>
<td>3.18E-04</td>
<td><strong>2.92E-04</strong></td>
</tr>
<tr>
<td>Mj</td>
<td></td>
<td>0.556944</td>
<td>0.4439</td>
<td>0.584956</td>
<td>0.564131</td>
<td>0.5734</td>
<td><strong>0.5446662</strong></td>
</tr>
<tr>
<td>Cjsw</td>
<td></td>
<td>3.00E-10</td>
<td>3.00E-10</td>
<td>2.98E-10</td>
<td>3.29E-10</td>
<td>3.50E-10</td>
<td><strong>3.16E-10</strong></td>
</tr>
<tr>
<td>Mjsw</td>
<td></td>
<td>0.243045</td>
<td>0.243</td>
<td>0.310807</td>
<td>0.273617</td>
<td>0.337596</td>
<td><strong>0.281613</strong></td>
</tr>
<tr>
<td>Pb</td>
<td></td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td><strong>0.8</strong></td>
</tr>
<tr>
<td>Delta W</td>
<td></td>
<td>1.70E-07</td>
<td>4.80E-07</td>
<td>1.14E-06</td>
<td>1.28E-06</td>
<td>4.63E-07</td>
<td><strong>7.07E-07</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Median</th>
<th>Std Dev.</th>
<th>Variance</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.500E-07</td>
<td>8.655E-08</td>
<td>7.491E-15</td>
</tr>
<tr>
<td>4.170E-08</td>
<td>1.454E-09</td>
<td>2.113E-18</td>
</tr>
<tr>
<td>9.309E+15</td>
<td>7.278E+14</td>
<td>5.298E+29</td>
</tr>
<tr>
<td>9.403E-01</td>
<td>3.373E-02</td>
<td>1.137E-03</td>
</tr>
<tr>
<td>1.838E-05</td>
<td>8.254E-07</td>
<td>6.814E-13</td>
</tr>
<tr>
<td>6.836E-01</td>
<td>3.960E-02</td>
<td>1.569E-03</td>
</tr>
<tr>
<td>6.000E-01</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>2.190E+02</td>
<td>5.599E+00</td>
<td>3.135E+01</td>
</tr>
<tr>
<td>2.460E-01</td>
<td>1.519E-02</td>
<td>2.307E-04</td>
</tr>
<tr>
<td>5.543E+04</td>
<td>1.140E+04</td>
<td>1.300E+08</td>
</tr>
<tr>
<td>5.545E-01</td>
<td>1.856E+00</td>
<td>3.443E+00</td>
</tr>
<tr>
<td>5.012E-02</td>
<td>4.079E-03</td>
<td>1.664E-05</td>
</tr>
<tr>
<td>9.267E+11</td>
<td>1.819E+12</td>
<td>3.309E+24</td>
</tr>
<tr>
<td>1.001E+00</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>1.000E+10</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>-1.000E+00</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>6.502E+01</td>
<td>4.300E+00</td>
<td>1.849E+01</td>
</tr>
<tr>
<td>3.098E-10</td>
<td>1.110E-10</td>
<td>1.232E-20</td>
</tr>
<tr>
<td>3.098E-10</td>
<td>1.110E-10</td>
<td>1.232E-20</td>
</tr>
<tr>
<td>4.657E-10</td>
<td>7.300E-11</td>
<td>5.329E-21</td>
</tr>
<tr>
<td>3.185E-04</td>
<td>5.058E-05</td>
<td>2.558E-09</td>
</tr>
<tr>
<td>5.641E-01</td>
<td>5.730E-02</td>
<td>3.283E-03</td>
</tr>
<tr>
<td>3.002E-10</td>
<td>2.336E-11</td>
<td>5.456E-22</td>
</tr>
<tr>
<td>2.736E-01</td>
<td>4.192E-02</td>
<td>1.757E-03</td>
</tr>
<tr>
<td>8.000E-01</td>
<td>1.054E-08</td>
<td>1.110E-16</td>
</tr>
<tr>
<td>4.800E-07</td>
<td>4.784E-07</td>
<td>2.289E-13</td>
</tr>
</tbody>
</table>
Appendix B.1

Monolithic Variable Linear Resistor

CMOS IV FOR FIG. 4.2A - GEORGE A. HADGIS
.OPTIONS LIMPTS=15000 ITL5=0 ITL4=10000 RELTOL=0.02 PIVTOL=1E-16
.WIDTH=80
.MODEL CMOSN NMOS LEVEL=1 ID=0.203U TOX=0.0416U NSUB=1.74E15 VTO=0.8272
  KP=50.6U GAMMA=0.25118 PHI=0.6 UO=607.5 UEXP=0.0964
  UCRIT=25186 DELTA=3.22 VMAX=63534 XJ=0.25U
  LAMBDA=0.0182 NFS=1.59E12 NEFF=1 NSS=1E10 TPG=1
  RSH=29.746 CGDO=254P CGSO=254P CGBO=395P CJ=91.5U
  MJ=0.807 CJSW=515P MJSW=0.309 PB=0.8

*  
* INPUT SIGNAL
*  
VG 12 0 DC 5V

*  
* GAIN CONTROL VOLTAGE
*  
VIN2 400 0 DC 5V

*  
* VOLTAGE CONTROLLED LINEAR RESISTOR
*  
VE 300 0 DC -0.8272V
MR1 12 12 300 300 CMOSN L=6U W=6U
MR2 12 400 0 0 CMOSN L=6U W=6U

*  
* TESTS TO RUN
*  
.OP
.DC VG 0 5 0.25

*  
* OUTPUT SECTION
*  
.PRINT DC V(12) ID(MR1) ID(MR2)
.END
Appendix B.2

Open-Loop Cascode Operational Amplifier

CASCODE OP-AMP OPEN-LOOP FOR FIG. 4.4a, 4.4b AND 4.5 - GEORGE A. HADGIS
.OPTIONS LIMPTS=30000 ITL5=0 ITL4=10000 RELTOL=0.1 PIVTOL=1E-16
.WIDTH=80

.MODEL CMOSN NMOS LEVEL=2 LD=0.203U TOX=0.0416U NSUB=1.74E15 VTO=0.8272
+ KP=50.6U GAMMA=0.25118 PHI=0.6 UO=607.5 UEXP=0.0964
+ UCRIT=25186 DELTA=3.22 VMAX=63534 XJ=0.25U
+ LAMBDA=0.0182 NFS=1.59E12 NEFF=1 NSS=1E10 TPG=1
+ RSH=29.746 CGDO=254P CGSO=254P CGBO=395P CJ=91.5U
+ MJ=0.807 CJSW=515P MJSW=0.309 PB=0.8

.MODEL CMOSP PMOS LEVEL=2 LD=0.234U TOX=0.0416U NSUB=9.62E15 VTO=-0.9419
+ KP=18.3U GAMMA=0.67212 PHI=0.6 UO=217.8 UEXP=0.241
+ UCRIT=58666 DELTA=1.3964 VMAX=277823 XJ=0.25U
+ LAMBDA=0.0486 NFS=1.37E12 NEFF=1.001 NSS=1E10 TPG=-1
+ RSH=66.056 CGDO=293P CGSO=293P CGBO=467P CJ=294U
+ MJ=0.545 CJSW=316P MJSW=0.282 PB=0.8

* POWER SUPPLIES
*
VDD 100 0 DC 5V
VSS 200 0 DC -5V
*
* INPUT SIGNAL
*
VINP 5 0 AC 1V SIN(-88.11UV 0.2V 10KHZ)
*
* CASCODE OP_AMP SUB-CIRCUIT
*
*       Vin+
*            |    Vin-            Vo
*            |    |    |    Vdd
*            |    |    |    |    Vss
*            |    |    |    |    |
*
.SUBCKT CASCODE 5 0 12 100 200
*
M1 6 4 8 200 CMOSN L=4U W=312U
M2 7 5 8 200 CMOSN L=4U W=312U
M3 6 6 100 100 CMOSP L=4U W=44U
M4 7 7 100 100 CMOSP L=4U W=44U
M5 8 3 200 200 CMOSN L=4U W=200U
M6 11 7 100 100 CMOSP L=4U W=110U
M7 13 10 200 200 CMOSN L=4U W=40U
M8 10 10 200 200 CMOSN L=4U W=40U
M9 9 6 100 100 CMOSP L=4U W=110U
MC1 12 2 13 200 CMOSN L=4U W=40U
MC2 12 11 100 CMOSP L=4U W=110U
MC3 10 1 9 100 CMOSP L=4U W=110U

* * BIASING CIRCUIT *
*
MB1 1 1 100 100 CMOSP L=4U W=16U
MB2 1 1 2 200 CMOSN L=4U W=4U
MB3 2 2 3 200 CMOSN L=4U W=26U
MB4 3 3 200 200 CMOSN L=4U W=300U
.ENDS

* * CASCODE INSTANTIATION *
*
XOA 5 0 12 100 200 CASCODE
*
* EXTERNAL LOAD COMPONENTS *
*
CL 12 0 50PF
RL 12 0 10MEG
*
* TESTS TO RUN *
*
.OP
.TF V(12) VINP
.DC VINP -0.05V 0.05V 100UV
.AC DEC 20 100HZ 1GHZ
*
* OUTPUT SECTION *
*
.PRINT AC VP(12) VDB(12)
.PRINT DC V(12)
.END
Appendix B.3

Unity-Gain Cascode Operational Amplifier

CASCODE OP-AMP UNITY GAIN FOR FIG. 4.6 AND 4.7 - GEORGE A. HADGIS

.OPTIONS LIMPTS=30000 ITL5=0 ITL4=10000 RELTOL=0.1 PIVTOL=1E-16
.WIDTH=80

.MODEL CMOSN NMOS LEVEL=2 LD=0.203U TOX=0.0416U NSUB=1.74E15 VTO=0.8272
+ KP=50.6U GAMMA=0.25118 PHI=0.6 UO=607.5 UEXP=0.0964
+ UCRIT=25186 DELTA=3.22 VMAX=63534 XJ=0.25U
+ LAMBDA=0.0182 NFS=1.59E12 NEFF=1 NSS=1E10 TPG=1
+ RSH=29.746 CGDO=254P CGSO=254P CGBO=395P CJ=91.5U
+ MJ=0.807 CJSW=515P MJSW=0.309 PB=0.8

.MODEL CMOSP PMOS LEVEL=2 LD=0.234U TOX=0.0416U NSUB=9.62E15 VTO=-0.9419
+ KP=18.3U GAMMA=0.67212 PHI=0.6 UO=217.8 UEXP=0.241
+ UCRIT=58666 DELTA=1.3964 VMAX=277823 XJ=0.25U
+ LAMBDA=0.0486 NFS=1.37E12 NEFF=1.001 NSS=1E10 TPG=-1
+ RSH=66.056 CGDO=293P CGSO=293P CGBO=467P CJ=294U
+ MJ=0.545 CJSW=316P MJSW=0.282 PB=0.8

* POWER SUPPLIES
 *
VDD 100 0 DC 5V
VSS 200 0 DC -5V
 *
* INPUT SIGNAL
 *
VINP 5 0 AC 1V SIN(-88.11UV 0.2V 10KHZ)
 *
* CASCODE OP_AMP SUB-CIRCUIT
 *
*Vin+  Vin-  Vo  Vdd  Vss
*
*SUBCKT CASCODE 5 4 12 100 200
*
M1 6 4 8 200 CMOSN L=4U W=312U
M2 7 5 8 200 CMOSN L=4U W=312U
M3 6 6 100 100 CMOSP L=4U W=44U
M4 7 7 100 100 CMOSP L=4U W=44U
M5 8 3 200 200 CMOSN L=4U W=200U
M6 11 7 100 100 CMOSP L=4U W=110U
M7 13 10 200 200 CMOSN L=4U W=40U
M8 10 10 200 200 CMOSN L=4U W=40U
M9 9 6 100 100 CMOSP L=4U W=110U
MC1 12 2 13 200 CMOSN L=4U W=40U
MC2 12 1 11 100 CMOSP L=4U W=110U
MC3 10 1 9 100 CMOSP L=4U W=110U
*
* BIASING CIRCUIT
*
MB1 1 1 100 100 CMOSP L=4U W=16U
MB2 1 1 2 200 CMOSN L=4U W=4U
MB3 2 2 3 200 CMOSN L=4U W=26U
MB4 3 3 200 200 CMOSN L=4U W=300U
.ENDS
*
* CASCODE INSTANTIATION
*
XOA 5 0 12 100 200 CASCODE
*
* EXTERNAL LOAD COMPONENTS
*
CL 12 0 50PF
RL 12 0 10MEG
*
* TESTS TO RUN
*
* .OP
.TF V(12) VINP
.DC VINP -0.05V 0.05V 100UV
.AC DEC 20 100HZ 1GHZ
*
* OUTPUT SECTION
*
.PRINT AC VP(12) VDB(12)
.PRINT DC V(12)
.END
Appendix B.4

National Semiconductor’s Model for the LMC6062

* **********COMMON MODE EFFECT********** *
I2  99 50 13U
**Quiescent current
EOS  7  1 POLY(1) 16 49 100E-6 1
*Offset voltage.........^  
R8  99 49 1.25MEG  
R9  49 50 1.25MEG  *
* ***************POLE STAGE*************** *
*  
*Fp=370 KHz  
G3  98 15 9 49 1E-3  
R12  98 15 1K  
C5  98 15 430.15P  *
* ***************POLE STAGE*************** *
*  
*Fp=6.8 MHz  
G5  98 18 15 49 1E-3  
R14  98 18 1K  
C6  98 18 23.405P  *
* **********COMMON-MODE ZERO STAGE********** *
*  
*Fpcm=1 KHz  
G4  98 16 POLY(2) 1 49 2 49 0 2.812E-8 2.812E-8  
L2  98 17 159.2M  
R13  17 16 1K  *
* ***************SECOND STAGE*************** *
*  
EH  99 98 99 49 1  
G1  98 29 18 49 5.5611E-7  
R5  98 29 65.33G  
V2  99 8 1.0  
D1  29 8 DX  
D2  10 29 DX  
V3  10 50 1.0  *
* ***************OUTPUT STAGE*************** *
*  
F6  99 50 VA7 1  
**Dynamic supply current  
F5  99 35 VA8 1  
D3  36 35 DX  
VA7  99 36 0  
D4  35 99 DX  
E1  99 37 99 49 1  
VA8  37 38 0
G6  38  40  49  29  12.5E-3
R16  38  40  119.698
V4   30  40  .77
D5   30  99  DX
V5   40  31  .77
D6   50  31  DX
*Fp1=.034 Hz
C3   29  39  28.57P
R6   39  40  1K
*
******************MODELS USED******************
*
.MODEL DA D(IS=2E-14)
.MODEL DB D(IS=1E-14)
.MODEL DX D(IS=1E-14)
.MODEL MOSFET PMOS(VTO=-2.35 KP=1.6753E-4)
.ENDS
Appendix B.5

National Semiconductor’s Model for the CD4007

*---------------------------------------------------------------------------*
* CD4007 model                                                           *
*---------------------------------------------------------------------------*

*MODEL NMOS NMOS(LEVEL=3 VTO=1.6 KP=2.13E-5 GAMMA=1.161
+ PHI=0.648 W=177.8U L=8.89U
+ CGSO=2.43E-10 CGDO=2.43E-10 RSH=8 CJ=6.90E-5
+ MJ=0.5 CJSW=3.30E-10 MJSW=0.300 TOX=1100E-10
+ NSUB=40.0E14 NFS=1.00E10 XJ=2.27E-6 UO=1200
+ LD=0.190E-6 VMAX=13E4 THETA=0.100 ETA=0.250
+ KAPPA=0.5)

*MODEL PMOS PMOS(LEVEL=3 VTO=-1.6 KP=2.04E-5 GAMMA=0.410
+ PHI=0.540 W=381U L=8.89U
+ CGSO=2.43E-10 CGDO=2.43E-10 RSH=60 CJ=6.90E-5
+ MJ=0.5 CJSW=3.30E-10 MJSW=0.300 TOX=1100E-10
+ NSUB=5E14 NFS=1.00E10 XJ=2.27E-6 UO=670
+ LD=0.190E-6 VMAX=13E4 THETA=0.100 ETA=0.250
+ KAPPA=0.5)
Appendix C

Monolithic Chip Layout