A field emission transistor array for writing applications

Todd C. Sieger

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A FIELD EMISSION TRANSISTOR ARRAY
FOR WRITING APPLICATIONS

by

TODD C. SIEGER

Bachelor of Science
Microelectronic Engineering
Rochester Institute of Technology
(1991)

A Thesis Submitted in Partial Fulfillment
of the Requirements for the Degree of
MASTER OF SCIENCE
in
Electrical Engineering

Approved by:

Prof. Lynn F. Fuller (Thesis Advisor)
Prof. Jon K. Edwards
Prof. R. Unnikrishnan (Department Head)

DEPARTMENT OF ELECTRICAL ENGINEERING
COLLEGE OF ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY
ROCHESTER, NEW YORK
SEPTEMBER, 1992
A Field Emission Transistor Array for Writing Applications

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_________________________________________ Date: Oct. 13, 1992
Abstract

This work involved the development of a unique imaging device utilizing vacuum microelectronic field emitter tip arrays (FEAs) and CCDs. The device offers the potential for higher resolution than any other write head technology (such as LED and laser etc.) currently used in Xerographic copiers and computer printers. In addition, the possibility of true-color output exists. A discussion of the CCD Emitter's applications and advantages over existing devices will be presented.

As part of the development of the device, layouts for a 10-pixel linear array device and other test structures were created as part of a CCD/FEA test chip. The bulk of the work, however, was the development of a process for fabrication of these devices using standard silicon integrated circuit processing techniques. Results of the development of the fabrication sequence, based on RIT's n-well CMOS process, will be presented. Included, will be the presentation of SEM photographs of a finished FEA and the optimization of TMA SUPREM-3 process simulations to match experimental results. The presentation will be summarized by a discussion of the application of the fabrication process in a manufacturing environment and recommendations for future fabrication and testing of the entire CCD Emitter device at RIT.
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<th>Description</th>
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<tbody>
<tr>
<td>&lt;100&gt;</td>
<td>Silicon crystallographic orientation</td>
</tr>
<tr>
<td>°C</td>
<td>Degrees Celsius</td>
</tr>
<tr>
<td>Å</td>
<td>Angstrom ($10^{-10}$ meter)</td>
</tr>
<tr>
<td>β</td>
<td>FEA geometry factor in Fowler-Nordheim equation</td>
</tr>
<tr>
<td>Ω</td>
<td>Ohm</td>
</tr>
<tr>
<td>φ</td>
<td>Work function</td>
</tr>
<tr>
<td>µA</td>
<td>Microampere</td>
</tr>
<tr>
<td>µm</td>
<td>Micrometer or micron ($10^{-6}$ meter)</td>
</tr>
<tr>
<td>A</td>
<td>Constant in Fowler-Nordheim equation or Ampere</td>
</tr>
<tr>
<td>AMU</td>
<td>Atomic Mass Units</td>
</tr>
<tr>
<td>ANOVA</td>
<td>Analysis Of Variance</td>
</tr>
<tr>
<td>B</td>
<td>Constant in Fowler-Nordheim equation</td>
</tr>
<tr>
<td>BCCD</td>
<td>Buried-Channel CCD</td>
</tr>
<tr>
<td>BF₂⁺</td>
<td>Ion created from boron trifluoride</td>
</tr>
<tr>
<td>BOE</td>
<td>Buffered Oxide Etch</td>
</tr>
<tr>
<td>BPSG</td>
<td>BoroPhosphoSilicate Glass</td>
</tr>
<tr>
<td>C₂F₆</td>
<td>Freon 116</td>
</tr>
<tr>
<td>CATS</td>
<td>Computer Aided Transcription Software</td>
</tr>
<tr>
<td>CCD</td>
<td>Charge-Coupled Device</td>
</tr>
<tr>
<td>CHF₃</td>
<td>Freon 23</td>
</tr>
<tr>
<td>CIF</td>
<td>Caltech Intermediate Format</td>
</tr>
<tr>
<td>cm</td>
<td>Centimeter ($10^{-2}$ meter)</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complimentary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>CO₂</td>
<td>Carbon dioxide</td>
</tr>
<tr>
<td>CRT</td>
<td>Cathode Ray Tube</td>
</tr>
<tr>
<td>DI</td>
<td>Deionized water</td>
</tr>
<tr>
<td>dpi</td>
<td>Dots Per Inch</td>
</tr>
<tr>
<td>e</td>
<td>Base of natural log (2.71828)</td>
</tr>
<tr>
<td>E</td>
<td>Exponent - power of 10 (ex. 1E10 = 10¹⁰)</td>
</tr>
<tr>
<td>e-beam</td>
<td>Electron beam</td>
</tr>
<tr>
<td>EDIP</td>
<td>Electron Discrete Image Projector</td>
</tr>
<tr>
<td>eV</td>
<td>Electron volt</td>
</tr>
<tr>
<td>FAX</td>
<td>Facsimile</td>
</tr>
<tr>
<td>FEA</td>
<td>Field Emission transistor Array</td>
</tr>
<tr>
<td>FEC</td>
<td>Field Effect Controlled FEA or Field Emission Cell</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>H₂</td>
<td>Hydrogen gas</td>
</tr>
<tr>
<td>H₂O</td>
<td>Water</td>
</tr>
<tr>
<td>H₂O₂</td>
<td>Hydrogen peroxide</td>
</tr>
<tr>
<td>H₂SO₄</td>
<td>Sulfuric acid</td>
</tr>
<tr>
<td>HCl</td>
<td>Hydrochloric acid</td>
</tr>
<tr>
<td>HF</td>
<td>Hydrofluoric acid</td>
</tr>
<tr>
<td>I.T.O.</td>
<td>Indium Tin Oxide</td>
</tr>
<tr>
<td>in</td>
<td>Inch</td>
</tr>
<tr>
<td>J</td>
<td>Current density</td>
</tr>
<tr>
<td>keV</td>
<td>Thousand electron volts</td>
</tr>
<tr>
<td>KOH</td>
<td>Potassium hydroxide</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
<tr>
<td>LOCOS</td>
<td>Local Oxidation Of Silicon</td>
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**LIST OF SYMBOLS**

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<tr>
<td>LPCVD</td>
<td>Low Pressure Chemical Vapor Deposition</td>
</tr>
<tr>
<td>lpm</td>
<td>Liters Per Minute</td>
</tr>
<tr>
<td>LTO</td>
<td>Low Temperature Oxide</td>
</tr>
<tr>
<td>MCIF</td>
<td>Mentor Graphics utility for creating CIF files from layout data</td>
</tr>
<tr>
<td>MEBES</td>
<td>Manufacturing Electron Beam Exposure System</td>
</tr>
<tr>
<td>min</td>
<td>Minutes</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MOSIS</td>
<td>MOS Implementation Service</td>
</tr>
<tr>
<td>mtorr</td>
<td>millitorr (unit of pressure)</td>
</tr>
<tr>
<td>n/n-type</td>
<td>Electron-rich semiconductor</td>
</tr>
<tr>
<td>N₂</td>
<td>Nitrogen gas</td>
</tr>
<tr>
<td>NH₃</td>
<td>Ammonia</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-channel Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>O₂</td>
<td>Oxygen gas</td>
</tr>
<tr>
<td>oxide</td>
<td>Silicon dioxide</td>
</tr>
<tr>
<td>p/p-type</td>
<td>Hole-rich semiconductor</td>
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<tr>
<td>PMOS</td>
<td>P-channel Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>poly</td>
<td>Polysilicon</td>
</tr>
<tr>
<td>resist</td>
<td>Photoresist</td>
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<td>RGB</td>
<td>Red, Green, Blue</td>
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<tr>
<td>RIE</td>
<td>Reactive Ion Enhanced etching</td>
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<td>Rochester Institute of Technology</td>
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<td>rpm</td>
<td>Revolutions Per Minute</td>
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<td>Rs</td>
<td>Sheet resistance</td>
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<td>SCCD</td>
<td>Surface-Channel CCD</td>
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<td>Symbol</td>
<td>Definition</td>
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<tr>
<td>sccm</td>
<td>Standard Cubic Centimeters Per Minute</td>
</tr>
<tr>
<td>sec</td>
<td>Second (unit of time)</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
</tr>
<tr>
<td>SF₆</td>
<td>Sulfur hexafluoride</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SiH₄</td>
<td>Silane</td>
</tr>
<tr>
<td>SiO₂</td>
<td>Silicon dioxide</td>
</tr>
<tr>
<td>slpm</td>
<td>Standard Liters Per Minute</td>
</tr>
<tr>
<td>sq</td>
<td>Square</td>
</tr>
<tr>
<td>TCA</td>
<td>1,1,1 Tri-ChloroEthane</td>
</tr>
<tr>
<td>TMA</td>
<td>Technology Modeling Associates</td>
</tr>
<tr>
<td>torr</td>
<td>Unit of pressure</td>
</tr>
<tr>
<td>V</td>
<td>Volt</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large Scale Integration</td>
</tr>
<tr>
<td>W</td>
<td>Watt</td>
</tr>
<tr>
<td>Xⱼ</td>
<td>Metallurgical junction depth</td>
</tr>
<tr>
<td>X₀ₓ</td>
<td>Oxide thickness</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

Recent trends in information processing have been toward greater use of electronic image reproduction, manipulation and storage. Users require output from these electronic images be of very high quality. This dictates that output devices be capable of very high resolution and true-color rendering. Current techniques for generating color prints from electronic information includes thermal dye transfer printers, CRT film recorders, and color laser printers. A new type of device has been proposed by Jon Edwards of Eastman Kodak Company (retired). The CCD Emitter is an imaging element, or write head, that offers many advantages over these existing technologies.

Most significant of the CCD Emitter's advantages are the potential for higher resolution than any other write head technology and fast, true-color output. A detailed discussion of the CCD Emitter's applications and advantages over existing devices is presented in section 3.3.

These advantages are inherent in the construction of the CCD Emitter. Each pixel of the device consists of a FEA, for emitting electrons in proportion to the input signal, a four-phase BCCD for transferring the input signal charge to the FEA, and several NMOS transistors for resetting the pixel. Electrons from the FEA travel through a vacuum to strike a phosphor screen backed by a transparent conductor. The phosphor screen is capable of emitting true RGB output. Output is fast due to the choice of a BCCD to transfer the signal as will be discussed in section 3.2.2. Very high resolution is possible because the device, with the exception of the screen, is fabricated by standard silicon processing techniques.
An overview of CCDs and FEAs is presented as they apply to the CCD Emitter. Details of the CCD Emitter device are then presented. The next two sections describe procedures used in the design of a simple ten-pixel device and the development of a process to fabricate this device. Results of the fabrication sequence development follow. Finally, a discussion of the practicality of the fabrication process and some conclusions are presented.
Chapter 2

Historical Review

2.1 CCD Overview

2.1.1 Structure and Operation

The basic unit of a CCD is the MOS capacitor such as the one shown in figure 2.1. When pulsed into deep depletion by a clock signal applied to the gate, the depletion region within the semiconductor behaves as a storage element for minority carriers. The depletion region is often referred to as a potential well because the potential energy barrier is lowered in this region. Information is stored in the device in the form of minority charges in the channel, or inversion layer charge. From MOS studies, it is known that the maximum amount of charge that may be stored by a MOS capacitor is dependent on the insulator, or oxide, thickness and dielectric constant, the surface potential, and the area of the gate among other factors.

A CCD is formed from a closely spaced linear array of MOS capacitors. Spacing is close enough so that the charge stored in one potential well may be transferred to an adjacent one. Transfer of charge is controlled by the voltages applied to the gates of the MOS capacitors. In the case of a MOS capacitor with a p-type silicon substrate, a more positive voltage makes the potential well more attractive for the minority carriers. With reference to figure 2.2b, if the voltage applied to $V_3$ is more positive than that applied to $V_2$, then charge will flow from the potential well under gate 2 to that under gate 3. Charge
may be introduced electrically into the CCD by a diode at one end of the linear array or by generation of minority carriers by incident radiation at any point under the CCD gates. Charge may then be extracted from the CCD with a diode at the other end of the linear array.

![Diagram of MOS capacitor basic structure](image)

**Figure 2.1:** MOS capacitor basic structure.
The number of adjacent gates which comprise the CCD cell determines the number of phases, or clocks, used for the CCD. In a two-phase CCD, every other gate is controlled by the same clock signal. In a three-phase CCD, every third gate is controlled by the same clock, and every fourth gate is tied together in the four-phase CCD. Figure 2.3 shows a cross-sectional view of a four-phase CCD.
Very close spacing between two adjacent gates may be easily achieved by using two or more conductive levels for the gates. By using a different conductor for an adjacent gate, the two gates may actually overlap at their edges and spacing is thus determined by the thickness of the interlevel dielectric. This thickness is on the same order as the thickness of the insulator between the gate and the substrate. For two or four-phase CCDs two conductive levels may be used. Three-phase CCDs require three conductive levels to maintain symmetry of the devices. The arrangement of the gates in the three-phase CCD is shown in figure 2.4. Heavily doped polysilicon, aluminum, or a combination of both may be used for the conductive layers. Typically polysilicon is used since successive fabrication steps are at temperatures higher than the melting point of aluminum.
Since CCDs with symmetrical potential wells require three or more clocks to
determine the signal flow direction, two-phase CCDs must have non-symmetric potential
wells \(^5\). Techniques or producing non-symmetric, or directional, potential wells include
ion-implantation of a region under the gates or using two different oxide thicknesses to
enhance the potential step. These two techniques are shown in figure 2.5.

**Figure 2.4:** Three-phase CCD structure \(^4\).

**Figure 2.5:** Two types of two-phase CCD structures \(^6\).
Minority charges are stored and transferred at the potential energy minimum. This minimum may be at the surface of the semiconductor. Such devices are referred to as surface channel CCDs (SCCDs). Devices which have their potential energy minimum within the bulk of the substrate are referred to as bulk, or buried, channel CCDs (BCCDs). The buried-channel device is produced by doping a thin (approximately 0.5μm) region at the surface of the semiconductor with the opposite polarity of the substrate. Figure 2.6 illustrates the energy band diagrams for both SCCD and BCCD devices. From these diagrams, it can be seen that the potential energy minimum of the SCCD is right at the insulator (SiO₂) - silicon interface. The potential energy minimum of the BCCD device is well within the silicon.

Figure 2.6: Surface and buried-channel CCD energy band diagrams. (a) SCCD structure and its band diagram when empty (b) and with charge signal (c). (d) BCCD structure, empty band diagram, and with a charge signal present (c).
CHAPTER 2. HISTORICAL REVIEW

Because the charge transfer within the BCCD is away from the insulator surface, the interface carrier trapping, and thus signal loss, is reduced. This results in higher transfer efficiencies for BCCDs over SCCDs. Additionally, having the channel away from the interface increases the device speed since carrier mobilities are not degraded as much as in SCCDs by high vertical electric fields. Buried-channel devices do suffer from lower charge handling capability due to lower capacitance, and higher current in the off-state (zero charge). The higher off-state current, or dark current, is due a higher rate of thermal generation of carriers.

2.1.2 Applications

Both digital and analog applications for CCDs exist. A CCD functions as a dynamic shift register, or memory, for information. When working with the presence or absence of a charge at a fixed level, then the CCD is a memory for digital information. Since the amount of charge stored in a CCD's potential well may be varied over a continuous range, then analog information may be represented. Since a dynamic shift register is essentially a delay line, it may be used in signal processing applications. For example, convolution is the multiplication of a time-varying signal by a delayed value of itself.

A CCD imaging array is another analog application of the CCD. Exposed to a focused image, each gate (or pixel) is charged to a level corresponding to the brightness at that location. Picture information is then read, or clocked, out of the shift register to an output stage.

Aside from the applications just described, the inventors of the CCD, Boyle and Smith, in their paper introducing the device, recognized the possibility of using it as a display device. They state that the inverse of reading information could be accomplished "via shift register action and then forward biasing the MIS structure to force minority carriers into the bulk where radiation recombination takes place."
No other mention of the CCD as a writing device has been found in the literature. Perhaps, this idea did not catch on due to the fact that the "radiation recombination" the authors mentioned would not produce visible radiation in silicon based devices. Direct recombination in silicon, which would produce visible radiation, does not occur except in very highly reverse-biased p-n junctions.

2.2 FEA Overview

2.2.1 Structure and Operation

A field emission transistor, or triode, is essentially a microelectronic vacuum tube. The device consists of a cold cathode, which is a source of electrons, a gate, or grid, for controlling the extraction of electrons, and an anode which functions as the target, or collector, for the electrons. These three terminals are analogous to the emitter, base, and collector of a bipolar transistor or the source, gate, and drain of a MOS transistor. The device is operated in a vacuum, just as a vacuum tube, in order to increase the mean free path of the electrons. Figure 2.7 shows a cross-section of a field emission triode.

![Field emission micro-triode](image)

Figure 2.7: Field emission micro-triode.
Unlike a hot cathode, from which electrons are emitted due to thermal excitation, the cold cathode emits electrons due to very high electric fields which result in quantum mechanical tunneling of electrons from the cathode. High fields are achieved with this micro-cathode by defining a very sharp point at the tip of the cathode. The sharpness of the tip, as well as other geometrical factors, influences the current emitted from the tip. This geometrical influence is included in the $\beta$ term of the Fowler-Nordheim equation.

$$J = \frac{A \beta V^2}{\phi} e^{-\frac{B \phi^{3/2}}{\beta V}} \left( \frac{A}{cm^2} \right)$$

where, $A$ and $B$ are constants, $\phi$ is the work function of the cathode material, and $V$ is the grid to cathode voltage. The Fowler-Nordheim plot in figure 2.8 shows how the height of the of the tip with respect to the grid and the grid opening size influence the extracted current. Figure 2.9 demonstrates that the sharper the tip, and the smaller the cone's half-angle, the higher the current. This is done by introducing a figure of merit related to these two quantities.

The plot in figure 2.8 shows currents of 100 to 1000$\mu$A, however, 50 to 100$\mu$A are typical for a single tip. Extraction voltages as low as 10 to 15V have been reported for tips on the order of 1$\mu$m in size. The use of arrays of emitter tips with a common grid results in much higher current densities. In addition, the arrays tend to average the emission which results in devices with greater uniformity of emission from array to array. These concepts lend to the use of FEAs in flat panel display devices. Such a device, fabricated by LETI CENG of France, is shown in figure 2.10. This device uses a conductive screen, coated with a phosphor, as the anode. A separately indexed FEA is used as the electron "gun" for each pixel. The current averaging improves the uniformity of light emission from pixel to pixel while the higher current capability improves image brightness.\(^\text{16}\).
Figure 2.8: Geometrical influence on FEA characteristics \(^{14}\).

\[ f = \frac{V_a}{V} \frac{I}{I_a} \frac{L}{L_a} \sim \frac{r}{r_a} \]

Where \(V, I, L\) are voltage, current & linear dimension of floating sphere geometry.

Figure 2.9: Figure of merit for various cathode shapes. (a) Rounded whisker. (b) Sharpened pyramid. (c) Hemispherical. (d) Pyramidal \(^{15}\).
Figure 2.10: (a) Cross-section of a single FEA tip in a flat-panel display. (b) Matrix structure used for addressing each pixel. 

Several methods exist for fabricating a device with the conical, or Spindt, type of cathode described above. All of the methods are compatible with existing silicon wafer processing equipment and techniques. The LETI CENG technique for producing tips involves the masked deposition of molybdenum to form the cathode. This technique is shown in figure 2.11.

The use of silicon as the tip material results in fabrication techniques which are more compatible with standard integrated circuit processing techniques. Early techniques for producing silicon tips involved wet chemical etching of silicon using potassium hydroxide (KOH). This technique resulted in pyramid shaped tips, as shown in figure 2.11, due to the orientation dependent etching of silicon in KOH. As was shown in figure 2.9, this structure has a low figure of merit, and thus generates low currents.
Figure 2.11: Fabrication sequence of LETI microtips.  

Figure 2.12: SEM photograph of KOH etched silicon pyramids.
By using dry chemical, or plasma, etching of silicon and successive thermal oxidation, a sharp point may be created. The thermal oxidation step serves to sharpen the tip by consuming some of the silicon at the peak of the tip. This processing sequence is outlined in figure 2.13. Figure 2.14 shows a SEM photograph of a finished tip with a 2μm diameter grid opening. In comparing figures 2.12 and 2.14, it is apparent that this process produces much sharper tips, and therefore, devices capable of higher currents.

![Figure 2.13: Fabrication sequence for dry-etched silicon field emitters](image)

Figure 2.13: Fabrication sequence for dry-etched silicon field emitters.
The evaporation of insulator and gate material and lift-off process, steps e-f of figure 2.13, are not the only technique for fabricating the grid part of the device. The masking oxide caps may be removed with HF after the silicon etch (step c of figure 2.13). Next, the tips could be thermally oxidized for sharpening. Following this, BPSG could be deposited and reflowed and then metal sputtered onto the wafer. The metal gate opening would then be defined by lithography, metal etch, and oxide etch. This technique, which was reported by R. Lee, et al., is shown in figure 2.15. Advantages of this method include greater compatibility with standard integrated circuit processing techniques. The drawback of this method is that it requires an extra masking and extra etch steps, thus the self alignment of the lift-off method (figure 2.13) is lost.
2.2.2 Applications

As described earlier, field emission devices have been used in flat panel area displays. The displays reported have been designed using simple matrix addressing schemes and fabrication on glass substrates by the techniques shown in figure 2.11. Full color capability is obtained using a screen such as in figure 2.17. Silicon substrate based FEAs have been fabricated only on uniformly doped substrates with no other circuitry.

Circuitry has been integrated with field emission devices in the implementation of microwave generation and amplification devices. These devices, however, utilize lateral cathode structures such as shown in figure 2.16.
LETI COLOR DISPLAY

TECHNIQUE USED:

(SWITCHED ANODE COLOR CONTROL)

Figure 2.17: LETI anode (screen) configuration for full color flat panel display.
CHAPTER 2. HISTORICAL REVIEW

A device which integrates a field emitter tip with a MOSFET was proposed by A. Ting, et al., of the U.S. Naval Research Laboratory. This device utilizes the FET gate as an extra element of control over the FEA.

"The goal of the FEC cathode is to improve the performance of existing vacuum FEAs and to enable the success of envisioned applications of these field emitters."\textsuperscript{25}

The cathode of the FEA in this device is electrically connected to the drain of the MOSFET as shown in figure 2.18. As of this writing, no details regarding the fabrication of this device were available.

![Figure 2.18: Cross-sectional view of a FET controlled FEA \textsuperscript{26}.](image)
Chapter 3

Theory of CCD Emitter

3.1 Structure

The CCD Emitter device is capable of taking digital or analog image information as input and writing the image to a photosensitive medium one line at a time. Scanning the photosensitive media, such as a piece of film or electrophotographic drum of a copier or printer, across the linear device produces an area image. This concept is shown in figure 3.1. EDIP is another term for the CCD Emitter.

Figure 3.1: Area information from a linear array device.27.
A four-phase CCD is used to transfer the analog or digital data to each pixel of the linear array where an FEA at each pixel acts as a miniature electron gun. Electrons from the FEA strike a phosphor coated, transparent conducting anode resulting in the visible display of the information. A vacuum enclosure is required for operation of the FEAs. This enclosure must be transparent for viewing the visible information. Figure 3.2 shows schematically the proposed arrangement of a complete write head.

![Figure 3.2: CCD Emitter writehead](image-url)
CHAPTER 3. THEORY OF CCD EMITTER

Not shown in figure 3.2, is an optical system for transfer of the image from the phosphor screen to the photosensitive media. This may be required if it is not possible to place the photosensitive media directly on the phosphor screen. One possible choice for such a system is the SELFOC lens array 29.

It is shown in figure 3.2, how the CCD Emitter device utilizes a field effect controlled FEA such as the one of figure 2.18. The source of the Control FET, as it is called, must be set for accepting information from the CCD or for emitting electrons from the FEA at the appropriate times which requires additional transistors for switching. The schematic for the switching circuitry is shown in figure 3.3 and a preliminary layout of two pixels of an entire device, including the switching circuit, is shown in figure 3.4.

![Diagram of CCD Emitter switching circuit](image)

Figure 3.3: CCD Emitter switching circuit 30.
Figure 3.4: CCD Emitter preliminary layout.
3.2 Principles of Operation

3.2.1 CCD Emitter Operation

The following discussion refers to figures 3.3 and 3.4. Prior to introducing data to the device, the FEA (control FET drain), control FET source, and external phase two diffusion (source of S3) are set to V+ (+5V power supply) by closing switches S4, S2, and S3 respectively. Image information is then introduced to the device using the input diode (ID), signal gate (SGC), and storage gate (STC). Data may be digital or analog due to the nature of the CCD as discussed in section 2.1.2. This method of introducing the data results in charge packets which are linearly related to the input signal. A signal inversion on the input (signal gate) is required. The reason for this will be discussed later.

The data is then gated through the CCD gates with the appropriated four-phase clocking. Data is clocked the entire length of the device until each phase two gate, PH2, contains charge information. Next, the information stored under all phase two gates is transferred to the external phase two diffused regions, and thus the gates of the field effect controlled FEAs, by enabling the TGL gates. Switch S3 is off to allow its source (external phase two diffused region) to take on a value other than V+.

Following the transfer of charge, the control FET source is switched to a bias level, which may be set to ground, by closing S1 and opening S2. Current now flows in the control FET at a level which is a function of the image signal charge level (gate voltage). Electron emission from each FEA occurs when the control FET drain is left floating, or S4 is switched off, and the FEA grid (CGL) is set to a positive voltage. Now, the grid functions as the drain for the control FET. Since the control FET gate voltage is a function of the image signal charge and the FEA current emission is related to this gate voltage, then the FEA emission current is a function of the image signal charge.
A positive relationship between image brightness, which is directly related to FEA emission current level, and signal level is desired. A signal inversion at the input of the CCD is required to maintain this relationship because a positive going input signal increases negative charges in an n-channel CCD, which is the type being used. After emission, which is the display of one line of the image information, CGL is set back to the ground state and all the diffused regions are reset to V+ as described in the first paragraph of this section. The cycle then repeats until each line of the image has been written.

3.2.2 Fabrication Technology and Performance Factors

For the CCD block of the CCD Emitter, an NMOS buried-channel technology was chosen. The n-channel devices have the advantage of higher operating speed over p-channel devices due to the higher mobility of electrons over holes. For this same reason, and for compatibility with the CCD, NMOS enhancement type transistors were used for the switches S1 through S4 and the control FET. Higher speed for the CCD is also an advantage of the buried-channel (depletion type) device over the surface-channel (enhancement type) device. In addition, a buried-channel CCD exhibits lower noise than a surface CCD. A double-polysilicon process was chosen for the four-phase CCD with the gates of the S1-S4 switches being either poly1 or poly2, whichever was appropriate for the layout. Double-poly, n-well CMOS processes are typically used for this type of CCD arrangement, therefore, this technology was chosen for the foundation of the CCD Emitter fabrication process.

Plasma etching of silicon with a tip sharpening oxidation was chosen as the technology for creating the emitter tips. These choices are based on the high figure of merit for such a tip and the ease of integration into standard integrated circuit processing techniques as discussed in section 2.2.1. Ease of integration was also the most important
factor in selecting the grid formation process outlined in figure 2.15. Targets for the tip and grid dimensions were chosen to be as follows: 2\(\mu\)m high tip with a 2\(\mu\)m diameter base; tip as sharp as possible; 3\(\mu\)m diameter grid opening; peak of tip level with top of grid; a large array of tips (= 1000), each 4\(\mu\)m from center to center. These choices are also based on the discussion in section 2.2.1. High currents are desired in order to provide high brightness of the image, however, relatively high resolution was desired.

Table 3.1 shows how there is a tradeoff between light output and resolution of the CCD Emitter. In addition, it lists some of the other important factors that influence the devices performance and their effects.

Table 3.1: Factors affecting CCD Emitter performance

<table>
<thead>
<tr>
<th>Factor</th>
<th>Primary Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEA size (number of tips) ↑</td>
<td>Light output ↑</td>
</tr>
<tr>
<td></td>
<td>Resolution ↓</td>
</tr>
<tr>
<td>Charge transfer capability ↑</td>
<td>Light output ↑</td>
</tr>
<tr>
<td>Charge transfer speed ↑</td>
<td>Speed ↑</td>
</tr>
<tr>
<td>Accelerating voltages ↑</td>
<td>Light output ↑</td>
</tr>
<tr>
<td>Phosphor efficiency ↑</td>
<td>Light output ↑</td>
</tr>
<tr>
<td>Phosphor decay time ↑</td>
<td>Speed ↓</td>
</tr>
<tr>
<td>Optical system losses ↑</td>
<td>Light output ↓</td>
</tr>
<tr>
<td>SELFOC lens array</td>
<td>Limits resolution</td>
</tr>
<tr>
<td>Receptor sensitivity ↑</td>
<td>Speed ↑</td>
</tr>
</tbody>
</table>
3.3 Applications and Advantages

The CCD Emitter is perfect for application that require either high resolution or true-color output capability with very fast write times. Such applications include electrostatic, or Xerographic, copying and printing of either black and white or color images. This include FAX and color FAX. The potential for very high resolution exists because the device takes advantage of standard silicon processing techniques, in which the dimensions of devices are always being shrunk with each short generation of the technology. Such high resolutions are possible, greater than 1000 dpi, that photographic quality reproduction of digitally stored photographs on negative or slide film is possible. Using an area array of CCD Emitters, flat panel displays with resolutions exceeding HDTV could be possible.

Current writehead technologies for application in electrostatic printers, copiers, and FAXes, and film writers include LED and laser writeheads. Table 3.2 shows the advantages of the CCD Emitter over these two technologies. Many of these advantages owe to the simple control over the device because of the CCD. The CCD is attributed the advantages of fast write time, simple switching circuitry, analog or digital input, simple modulation of light level, low current, high efficiency, and no additional storage buffer. Standard integrated circuit processing techniques are responsible for many of the other advantages. These include very high resolution, as mentioned above, no moving parts, high reliability, and low cost. The remaining advantages, namely primary color output, parallel color output, and high light intensity are attributed to the use of the FEA with a phosphor screen.
Table 3.2: Writehead technology comparison.~\(^{33}\)

<table>
<thead>
<tr>
<th>Advantage</th>
<th>CCD Emitter</th>
<th>LED Printhead</th>
<th>Laser Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>Very high; &gt;1000 dpi possible</td>
<td>Low; 400-600 dpi</td>
<td>Very high</td>
</tr>
<tr>
<td>Primary colors</td>
<td>Near true</td>
<td>Not true primary</td>
<td>Only with filtering</td>
</tr>
<tr>
<td>Color output</td>
<td>Parallel</td>
<td>Parallel</td>
<td>Sequential</td>
</tr>
<tr>
<td>Write time</td>
<td>Fast; parallel output</td>
<td>Relatively fast; parallel output</td>
<td>Slow</td>
</tr>
<tr>
<td>Switching circuitry</td>
<td>Very simple</td>
<td>Complex</td>
<td>Complex</td>
</tr>
<tr>
<td>Accepts analog and digital information</td>
<td>Yes</td>
<td>Generally only discrete</td>
<td></td>
</tr>
<tr>
<td>Control of output level</td>
<td>Simple modulation of light level</td>
<td>Difficult; modulate light duration</td>
<td>Complex light modulation</td>
</tr>
<tr>
<td>Light intensity</td>
<td>High (tradeoff resolution)</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Moving parts</td>
<td>None</td>
<td>None</td>
<td>Delicate moving parts</td>
</tr>
<tr>
<td>Reliability</td>
<td>High</td>
<td>Average</td>
<td>Low</td>
</tr>
<tr>
<td>Current</td>
<td>Low</td>
<td>Very high</td>
<td>Low</td>
</tr>
<tr>
<td>Efficiency</td>
<td>Very high</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Additional storage buffer required</td>
<td>None</td>
<td>None</td>
<td>Large buffer required</td>
</tr>
<tr>
<td>Cost</td>
<td>Inexpensive; produced in mass quantities</td>
<td>Relatively inexpensive</td>
<td>Expensive</td>
</tr>
</tbody>
</table>
Chapter 4

Design Layout and Maskmaking

4.1 Layout Tools

Circuit layout was accomplished with the use of Mentor Graphics Chipgraph software. This software is installed on the Apollo workstations which reside in the Computer Engineering department’s VLSI lab. Basically a polygon editing tool, this software allows for hierarchical manipulation of the designs. This capability was used extensively in the layouts of these designs. Once layouts were completed, a CIF file was created with the MCIF utility for transferring the design to the fracturing software. Fracturing, accomplished with CATS, will be discussed in section 4.4.

A custom process definition file was generated for the designs because the CCD Emitter technology is not a standard (i.e. NMOS, PMOS, or CMOS) technology. The CMOS process definition file was the basis since the fabrication process is based on a CMOS process, as will be discussed in section 5.1. Several layer names were added. They are: Mesa, Buried_Chan, Poly2, Tip, and Aperature. This process definition, given the name sieger_ccd and residing in the file ccd.bin, is shown in figure 4.1.

Design rules for all the layouts were based on MOSIS Scalable and Generic CMOS Design Rules, Revision 6. A Lambda value of 5µm was used. In cases where no design rules were available, they were based on knowledge of the fabrication process and tools in the RIT wafer fab that will be used to fabricate the device. The layers for which this is the case, are those that are listed above which were added to the process definition file.
The Mesa level, which was included in the design, was not used on the reticles. This level was for an option in the process which will be discussed in section 5.2. This level was drawn wherever an FEA exists. It coincides exactly with the edge of the area defined by the Tip level. Active area overlap of the Tip and Mesa levels was kept at 5\(\mu\)m. The Aperature consists of 3\(\mu\)m circles which are concentric with the 2\(\mu\)m circles that define the tips. Thus, the overlap of the Aperature level to the Tip level is only a half micron, making alignment of these two levels extremely critical. N_Impant, or N_Select, design rules were used for the buried channel level and poly1 design rules were used for the poly2 level. The overlap of poly2 to poly1 in the CCD was taken as 5\(\mu\)m.
4.2 FEA-Only Device

In the development of the CCD Emitter device, not only was the layout of the entire device required, but the development of the process required fabrication, and thus layouts, of only the FEA portion of the device. For this design, a cell was created which is an array 900 tips (30 x 30) which are 2μm in diameter and 4μm from center to center, all of which are within a doped region defined by the Active_Area level. This array is referred to as TIP_ARRAY. The array also includes a 2μm wide strip on each of two adjacent sides of the array. These two structures were included to allow for measurement of silicon etch undercut during the silicon etch experiment. This is discussed in section 6.2.2. Figure 4.2 shows a simplified representation of the tip array.

Figure 4.2: Tip level of the tip array used in the FEA-only device (not to scale).
A single die, titled TIPS_ONLY, is an array of 256 (16 x 16) of the tip array cells for a total size of 3712μm by 3932μm. Large contacts are made to the active region of each array, which are all connected with lines on the metal level. These lines are all connected at one end of the chip to form the cathode connection. Metal lines parallel to the cathode lines and passing over the tips are connected at the other end of the chip to form the grid or gate connection. Both the TIPS_ONLY and TIPARRAY cells are given in Appendix 1.

Alignment marks for the GCA-6700 steppers, which were used for the photolithography steps in the fabrication of the devices, were implemented on each of the six levels of the design in the cell named GCA6700. The inclusion of an alignment mark on each level was for alignment on later levels in case the alignment mark on the first level was not visible due to processing. All marks were shifted 200μm in the negative x direction (GCA-6700 axes) from the previous level's mark.

4.3 CCD/FEA Project Chip

The main focus on the project chip is the CCD Emitter device. Using the hierarchical design approach, a cell, PIXEL, was created which consists of a single four-phase BCCD with 50μm by 50μm gates (cell CCD), a single 30 by 30 tip FEA (cell FEA), and the five transistor switching circuit shown in figure 3.3. Transistors S2, S4, and Control FET have poly1 as their gate material. Transistors S1 and S3 use poly2 for the gates. Additionally, an input cell was created, as INPUT_CELL. This cell includes an input diode (ID), two control BCCD gates (SGC and STC), each 50μm by 50μm, and parallel metal and polysilicon lines for connecting to all the signals on the PIXEL cell. These two cells were designed such that a long line of pixels could easily be obtained by overlapping copies of PIXEL by 5μm and then overlapping INPUT_CELL by 5μm on the left end of the line of pixels. Plots of theses cells and all of the cells referred to in the following discussion may be found in Appendix 1.
Three copies of a single pixel CCD Emitter with probe pads (ONE_PIXEL) are included on the chip, titled TVCHIP. This device was created by including the input cell and one pixel cell. An output diode (OD) was also added to the right side of the pixel for taking out charge from the BCCD if necessary. Also, four copies of a ten-pixel CCD Emitter (PIXELS_10) are implemented. These two different devices will allow for complete testing of the CCD Emitter’s functionality and the scheme for shifting a line of image data into the device.

An array of eight sixteen-pixel long devices is included for testing uniformity of emission from the FEA’s. This device is referred to as PIXEL_ARRAY. The eight lines are wired in parallel such that each line will display the same information. Every other line consists of a line of a vertically mirrored version of the pixel, called PIXEL_90, and a mirrored version of the input cell, INPUTCELL_90. These mirrored versions of the cells described above were designed in a manner as to reduce space required for interconnections. On one end of the cells, the PHL1, PHL2, PHL3, and PHL4 lines may be shared between a cell and its mirrored version. On the other end, the V+ CONTROL and V+/BIAS CTRL B lines may be shared.

All of the building blocks used to create these complex cells were implemented separately for testing purposes. All of these “test” devices were wired to 100µm by 100µm metal pads spaced 100µm apart. This pad arrangement allows for the use of the standard test chip probe card in the RIT Microelectronic Engineering test facility. Included on the project chip are devices that consist of a single 30 by 30 array of field emission tips (FEA_ONLY) and a single four-phase BCCD (CCD_ONLY). Included in the TEST_STRUCT cell, are individual NMOS, PMOS, and BCCD transistors, all with both poly1 and poly2 gates. Also included in TEST_STRUCT, are cross-bridge Kelvin resistors for measuring contact resistance of the 10µm by 10µm contacts used throughout the designs, and Van Der Pauw resistors for measuring sheet resistance of the material layers.
4.4 Maskmaking and Stepper Job

Design fracturing was accomplished with CATS. This package converts the designs to a series of trapezoids. These trapezoids, which only approximate the design, are in a format that is readable by the MEBES I electron beam system. This system writes the patterns, one level at a time, to the resist coated 5x stepper reticles that are used to fabricate the device. Positive e-beam resist was used in the fabrication of all masks and the silicon process is designed to all be done with positive resist. The use of positive resist for both mask and wafer processing means that any drawn area on the layout will be an be a transparent area on the mask, and thus an area on the wafer that is free of resist after exposure and development. Based on this, several of the design levels were reversed.

Since fracturing only approximates the design, complex geometric shapes are not written to the reticle exactly as designed. For these layouts, complex patterns were used only on the Tip and Aperature levels. Fracturing these levels for the standard 0.5μm e-beam spot size, or resolution, resulted in circles (2μm and 3μm diameter) with very rough edges. Final fracturing of these two levels required the 0.25μm spot size. Fracturing at this smaller spot size, however, uses more memory than fracturing at 0.5μm. Data compression was used in order to fit these two fractured patterns on the MEBES magnetic tape. Patterns fractured with this smaller spot size also required higher MEBES write times.

All fracturing was done using the cmos_nw.clay file with the CIFLIB utility. Magnification was set at 5x, height [512], and the orientation used was Mirror90. This orientation causes the design to be right-reading, or as-designed, on the wafer. The extent command was issued only once in order to ensure that each level was centered around the same point to avoid mis-alignment during fabrication. Tables 4.1 and 4.2 summarize the fracturing options used for each layer of the TIPS_ONLY and TVCHIP.
Table 4.1: Design fracturing summary for TIPS_ONLY.

<table>
<thead>
<tr>
<th>Mask Level</th>
<th>Chipgraph Layer #</th>
<th>CATS Layer #</th>
<th>Layer Name</th>
<th>Reverse</th>
<th>Spot Size (µm)</th>
<th>Filename (.cflt)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>254</td>
<td>Active_area</td>
<td>No</td>
<td>0.5</td>
<td>M920609R1_01</td>
<td>No LOCOS.</td>
</tr>
<tr>
<td>2</td>
<td>18</td>
<td>250</td>
<td>Mesa</td>
<td>Yes</td>
<td>0.5</td>
<td>M920609R1_02</td>
<td>Not used.</td>
</tr>
<tr>
<td>3</td>
<td>15</td>
<td>252</td>
<td>Tip</td>
<td>No</td>
<td>0.25</td>
<td>M920609R1_03</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>253</td>
<td>Contact_a</td>
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<td>0.5</td>
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<tr>
<td>5</td>
<td>16</td>
<td>251</td>
<td>Aperature</td>
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<td>0.25</td>
<td>M920609R1_05</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>12</td>
<td>255</td>
<td>Metal2</td>
<td>Yes</td>
<td>0.5</td>
<td>M920609R1_06</td>
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</table>

Table 4.2: Design fracturing summary for TVCHIP

<table>
<thead>
<tr>
<th>Mask Level</th>
<th>Chipgraph Layer #</th>
<th>CATS Layer #</th>
<th>Layer Name</th>
<th>Reverse</th>
<th>Spot Size (µm)</th>
<th>Filename (.cflt)</th>
<th>Comments</th>
</tr>
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<tr>
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<td>G890914TS_01</td>
<td></td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>244</td>
<td>Mesa</td>
<td>Yes</td>
<td>0.5</td>
<td>G890914TS_02</td>
<td>Not used.</td>
</tr>
<tr>
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<td>2</td>
<td>255</td>
<td>Active_area</td>
<td>Yes</td>
<td>0.5</td>
<td>G890914TS_03</td>
<td>N_well compliment.</td>
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<tr>
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<td>Field_Vt</td>
<td>Yes</td>
<td>0.5</td>
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<td></td>
</tr>
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<td>G890914TS_05</td>
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<tr>
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<td>Poly1</td>
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<td>Poly2</td>
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<tr>
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<td></td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>253</td>
<td>Contact_a</td>
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<td>0.5</td>
<td>G890914TS_11</td>
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</tr>
<tr>
<td>11</td>
<td>16</td>
<td>243</td>
<td>Aperature</td>
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<td>0.25</td>
<td>G890914TS_12</td>
<td></td>
</tr>
<tr>
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<td>11</td>
<td>254</td>
<td>Metal1</td>
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<td>0.5</td>
<td>G890914TS_13</td>
<td></td>
</tr>
<tr>
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<td>17</td>
<td>251</td>
<td>Passivation</td>
<td>No</td>
<td>0.5</td>
<td>G890914TS_14</td>
<td></td>
</tr>
</tbody>
</table>
Masks have been completed for all of the designed levels for both parts of the project. For the TIPS\_ONLY design, each level of the chip was repeated in a 3 by 3 array on the reticle. Thus there are five reticles for this design. The advantage of the 3 by 3 array is that it exposes nine die on the wafer per stepper exposure which results in a total wafer exposure time one ninth of that required if only a single die was exposed each stepper exposure. Another advantage is that the stepper job definition was straightforward. Theoretically, a single pass may be used for all levels once the key offsets and shifts have been determined for proper alignment. Shifts must, of course, be determined after confirming that the stepper baseline is set correctly.

A second pass was implemented in the stepper job which is titled TSIEGER and resides on GCA STEPPER01. The second pass allows for the use of the alignment mark from level 3, the Tip level, in case the alignment mark from level 1 is not visible after processing. The alignment mark from level 3 is shifted 400μm in the negative x direction (when using GCA-6700 axes) from the level 1 alignment mark. In order to use this alignment mark, therefor, an additional shift of 0.4mm (400μm) is used in pass 2. The MEBES job decks and GCA stepper job decks are contained in Appendix 2.

The entire stepper job for the TIPS\_ONLY design should be re-written to include a different pass for each level. It was determined late in the processing that different shifts are needed for each level even if baseline is set correctly for the stepper. This is the case because the extent command must have been issued for each level of the design during fracturing.

The MEBES job and stepper job are much more complex for the TVCHIP design. Due to the large number of levels, a reticle for each level would have been too costly. To reduce the number of reticles, four levels were written on each reticle. Thus, levels 1-4 are on one reticle, levels 5-8 on the second, levels 9-12 on the third, and level 13 on the fourth. Figure 4.3 shows the arrangement of the levels on the reticle plates.
The stepper job was written using a separate pass for each of the four positions on the reticle. Levels 1, 5, 9, and 13 use pass 1 of the job; levels 2, 6, and 10 use pass 2; levels 3, 7, and 11 use pass 3; and levels 4, 8, and 12 use pass 4. Key offsets and shifts have been determined and entered into the job deck. The shifts, which are based on using no shifts when exposing the first level, are the same for levels 2 through 13. Therefore, the shifts, which are required when exposing levels 5, 9, and 13 with pass 1, must be removed from pass 1 when exposing level 1. The MEBES and stepper job decks may again be found in Appendix 2.
Chapter 5

Process Design and Simulation

5.1 Process Foundation

Targets for the fabrication of the FEAs were given in section 3.2.2. An additional target of the FEA fabrication was to have the processing steps for the FEA compatible a "standard", i.e. typical for the integrated circuit industry, n-well CMOS process because the n-well CMOS process was chosen as the foundation for the CCD fabrication. Specifically, RIT's n-well CMOS process was chosen as the basis for the work. The important steps of this process are listed in table 5.1. Most of this process typifies an industry CMOS process. Where the steps did not reflect standard CMOS steps, they were modified to reflect more typical processing of CMOS devices. Note that the step numbers are not sequential. This is to allow for the addition of steps for fabrication of the CCD and FEA.

All steps that were modified, added for fabrication of the CCD, or added for fabrication of the FEAs, were simulated and confirmed through processing of those steps on an individual basis. Additional process design targets are related to the buried-channel CCD construction. They are, buried-channel junction depth of 0.5µm and gate oxide thickness of 750Å (under both poly1 and poly2 gates).
**Table 5.1: RIT n-well CMOS process.**

1. **Starting wafers**
   <100>, p-type, boron doped, 5-15 Ω·cm

2. **Alignment oxide growth**
   1000°C, 10min dry O₂ + 55min wet O₂ + 5min dry O₂ + 1150°C, 600min N₂
   Expected oxide thickness: 3300Å

3. **Pattern n-Well - mask level #1**

4. **n-Well implant**
   Phosphorous; 130keV; 6E12 ions/cm²

5. **n-Well drive-in**
   1000°C, 10min dry O₂ + 25min wet O₂ + 5min dry O₂ + 1150°C, 1250min N₂ + 800°C, 400min N₂
   Expected junction depth: 5μm

6. **Pad oxide growth**
   950°C, 30min dry O₂; 200Å

7. **Nitride deposition**
   LPCVD; 790-810°C; 12.5min deposition; 900Å

8. **Pattern Active - mask level #2**

9. **Pattern Field Threshold Adjust - mask level #3**

10. **Field threshold adj. implant**
    Boron 11; 35keV; 2E13-1E14 ions/cm²

11. **Field oxide growth (LOCOS)**
    800°C, 15min dry O₂ + 1100°C, 25min dry O₂ + 950°C, 15min dry O₂ + 380min wet O₂ + 30min N₂
    Expected oxide thickness: 7500Å

12. **Kool oxide growth**
    900°C, 25min dry O₂ + 25min wet O₂ + 35min dry O₂
    Expected oxide thickness: 540Å

13. **Threshold adjust implant**
    Boron 11; 35keV; 1-3E12 ions/cm²

14. **Gate oxide growth**
    950°C, 15min N₂ + 100min dry O₂ + 30min N₂
    Expected oxide thickness: 550Å

15. **Polysilicon deposition**
    LPCVD; 610°C; 56min deposition; 5000Å

16. **Polysilicon doping**
    Emulsitone N-250 spin-on dopant
    950°C, 10min N₂
    Expected sheet resistance: 45 Ω/sq

17. **Pattern Poly gates - mask level #4**

18. **Pattern p+ S/D - mask level #5**

19. **p+ S/D implant**
    BF₂⁺; 55keV; 1E15 ions/cm²
31 Pattern n+ S/D - mask level #6

32 n+ S/D implant
Phosphorous; 35keV; 1E15 ions/cm²

33 Passivation oxidation
900°C, 15min wet O₂; 1000Å

34 Glass deposition
Allied Accuglass 211

35 Densify
900°C, 30min wet O₂; 3000Å

36 Pattern Contacts - mask level #7

37 Aluminum deposition
Sputter 0.5μm

38 Sinter
450°C, 20min forming gas (90% N₂, 10% H₂)

40 Pattern Metal - mask level #8

5.2 Integration of CCD and FEA Technologies

In order to fabricate the buried-channel CCD, steps for defining and implanting a buried-channel region and steps related to the second polysilicon level were added to the n-well CMOS process. These steps are outlined in table 5.2. The parameters for these steps that were determined by simulation and experimentation are indicated. These will be further discussed in chapter 6.

Table 5.2: Process steps added for CCD.

14 Pattern Buried Channel - mask level #4

15 Buried channel implant
Phosphorous; 150keV; 2.5E12 ions/cm²

16 Gate oxide growth
950°C, 15min N₂ + 125min dry O₂ + 30min N₂
Expected oxide thickness: 750Å

17 Polysilicon deposition
LPCVD; 610°C; 73min deposition; 6500Å

20 Gate oxide etchback
To 200Å in regions where poly2 gates will be.

21 First isolation oxidation
950°C, 15min N₂ + 110min dry O₂ w/ TCA + 30min N₂
Expected oxide thickness: 750Å in poly2 gate regions.

22 Polysilicon2 deposition
LPCVD; 610°C; 73min deposition; 6500Å
23 Polysilicon doping
Emulsitone N-250 spin-on dopant
950°C, 10min N₂
Expected sheet resistance: 45 Ω/sq

24 Pattern Poly2 gates - mask level #6

25 Second isolation oxidation
900°C, 25min wet O₂; 1200Å in FEA region.

In addition to the steps that were added for the CCD fabrication, several steps were added or significantly modified for fabrication of the FEA's emitter tips and grid. These steps are outlined in table 5.3. Again, the table reflects the final results which will be discussed in chapter 6.

Table 5.3: Process steps added or significantly modified for FEA.

26 Pattern Tips - mask level #7

27 Oxide etch
RIE: 200W; 170:60:48sccm CHF₃:C₂F₆:CO₂; 150mtorr; 2min

28 Silicon etch
RIE: 190W; 10:4:7sccm SF₆:O₂:CO₂; 73mtorr; 3min
Final depth of etch: 1.9-2.1μm

33 Tip sharpening oxidation
900°C, 75 min wet O₂; 2500Å in valley of FEA.

34 Glass deposition
2000Å undoped LTO + 12000Å BPSG; 420°C.
BPSG: 4% by weight boron, 4% by weight phosphorous.

35 Reflow
900°C, 60 min N₂

39 Pattern Aperature - mask level #11

The steps described listed in table 5.3 result in emitter tips that are 2μm high with the peak of the tip approximately on the same level as the silicon/silicon dioxide interface of the CCD and other circuitry. In order to "planarize" the device, that is to make the base of the tips level with the silicon/silicon dioxide interface of the CCD, another masking and oxide etch and silicon etch step would be required. This option would allow for the use of the lift-off type of grid fabrication sequence (figure 2.13) without an abrupt step where
the FEA ended. In this manner, a single level of metal, the same as used for the grid, could be used to run the CGL (grid control) lines. The masking level, which was included in the designs but not used, is called the Mesa level. This masking step, an oxide etch and silicon etch (2μm deep) could be performed immediately after the n-well drive-in (figure 5.1a-b). The remainder of the processing would be performed as described above. Emitter tips would be defined and etched in the 2μm high mesa with the edges of the mesa coincident with the edges of the FEA. This is illustrated in figure 5.1c-d.

![Figure 5.1: (a) Pattern Mesa level and etch oxide. (b) Etch silicon 2μm deep. (c) Pattern Tip level and etch oxide. (d) Etch silicon 2μm deep.](image-url)
5.3 Process Simulation Using SUPREM-3

All process parameters were derived from simulations using the one-dimensional TMA SUPREM-3 process simulation software. Simulations of each step that was modified from or added to the starting CMOS process was simulated either individually or as part of a sequence of steps to create the appropriate structure. The procedure was to start with the default coefficients and optimize process parameters (time, temperature, etc.) to match the design target. Next, the process step was run in the wafer fab using these parameters. Measurements of the appropriate design target (oxide thickness, sheet resistance, etc.) were then made. The coefficients used by SUPREM-3 were then modified to match the simulations to the measured results. The process step was then re-simulated and re-run to confirm the results of the simulations.

Figure 5.2 shows an output deck from the optimization of the linear oxidation rate coefficient in wet O\textsubscript{2} based on the results from the Kooi oxide growth. This deck shows how an optimization loop was used to obtain the coefficient by setting the optimization target to the measured oxide thickness of 0.0993μm. Table 5.4 lists all the coefficients arrived at in this manner in the form of Ambient statements used by SUPREM-3. These coefficients were used in the simulation of the entire process for which the results may be found in Appendix 3. The first Ambient statement sets up the effect of chlorine on oxidation rate for 950°C in dry O\textsubscript{2} with 5% HCl. The next statement sets up the dry O\textsubscript{2} linear oxidation rate and oxidation rate in the thin oxide regime. The third and fourth statements are the linear oxidation rate and diffusion enhanced oxidation rate for wet O\textsubscript{2}.

Table 5.4: Optimized SUPREM-3 coefficients.

<table>
<thead>
<tr>
<th>Ambient</th>
<th>O\textsubscript{2} Lin.Clde Column=3 Temperature=950 Table(4)=0.9848</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient</td>
<td>O\textsubscript{2} &lt;100&gt; ThinO\textsubscript{2}.0=2.2632E7 H.Lin.0=1.1649E5</td>
</tr>
<tr>
<td>Ambient</td>
<td>H\textsubscript{2}O &lt;100&gt; H.Lin.0=1.5049E6</td>
</tr>
<tr>
<td>Ambient</td>
<td>H\textsubscript{2}O &lt;100&gt; Gamma.0=3813</td>
</tr>
</tbody>
</table>
Figure 5.2: SUPREM-3 coefficient optimization example.

```
SUPREM-3
Version C, Revision 9002
All Rights Reserved

8-SEP-92 09:52:50

Statements input from file OPT_EX.S3I

1. Title          CCD/FEA - Kooi Oxidation Development
2. Comment        Todd Sieger Aug. 5.1992 File: K00IOX_1
3. Initialize     <100> Silicon Resistivity Boron=5
                  Thickness=12 dx=.04
4. $              
5. Loop           Steps=50 Optimize
6. Assign         Name=WOXR N.Value=1E5 Lower=1E5 Upper=3E6 Optimize
7. $              
8. Comment        Set up coefficients for oxidations in O2 & WetO2 (H2O)
9. Comment        ambients based on process results.
10. Ambient       O2 Lin.Cide Column=3 Temperature=950 Table{4}=0.9848
11. Ambient       O2 <100> ThinOx.0=2.2632E7 H.Lin.0=1.1849E5
12. Ambient       H2O <100> H.Lin.0=@WOXR
13. Ambient       H2O <100> Gamma.0=3813
14. $              
15. Comment       Grow Kooi Oxide (1000A).
16. Diffusion     Time=50 Temperature=900 WetO2
17. Comment       Wet O2 turned off after soak.
18. Comment       Pull the wafers out at 900C.
19. Extract       Name=K0X Thickness Layer=2
                  Target=0.0993
20. $              
21. Assign        Name=K0X N.Value=NINT(10000*K0X)
22. $              
23. Stop          End

Input line # 3
Coefficient data group read
File: S3COF0
Date: 28-AUG-92 15:45:55
Documentation from data file:
SUPREM-3 Revision 9002 coefficient initialization

Input line # 20
Optimization successful:
Smooth minimum found.
12 function evaluations in 3 iterations.

RMS error 0.00 %

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<table>
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</table>

Sensitivities: 100 * (% change in target) / (% change in assign)

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*** END SUPREM-3 ***
5.4 Emitter Tip Simulation Using SUPREM-4

Since large geometries (greater than 10\(\mu\)m) were used in the layout of the CCD and switching circuit, one-dimensional simulations at several different points, or cross-sections, accurately simulated the structure. That is, no two-dimensional effects were present in the CCD or switching circuit due to small dimensions. Since the emitter tips were very small (2\(\mu\)m) and were non-planar, two-dimensional simulations were desired. These were necessary in determining the tip sharpening oxidation time due to geometrical effects of the tip.

TMA SUPREM-4 was used of the two-dimensional process simulations. The grid spacing in the vertical direction was matched to that used in the SUPREM-3 simulations for compatibility (to get the same results in large flat areas). Following the grid setup, the profiles of boron and phosphorous in the silicon prior to the tip etch were matched to those obtained from SUPREM-3 at the same point in the process. This was done by using the PROFILE statement in SUPREM-4 with a printout of the concentration at every point obtained from SUPREM-3 with the PRINT CONCENTRATION command. Figures 5.3 and 5.4 demonstrate the matching dopant profiles before the silicon etch.

Next, the tip was etched to the desired dimensions; 2\(\mu\)m deep with an undercut of 0.9\(\mu\)m using a series of etch statements. The curvature was assumed based on experience with dry chemical etching. The resulting structure is shown with the simulation grid in figure 5.5. Figures 5.6 and 5.7 show that following the silicon etch step the SUPREM-3 and SUPREM-4 dopant profiles still match.

Since SUPREM-3 and SUPREM-4 use different models for diffusion and implant, the profiles from both no longer matched following the n+ source/drain (S/D) implant and tip sharpening oxidation. This is shown in figures 5.8 through 5.13. In order to make these simulations meaningful, SUPREM-4's oxidation enhanced diffusion coefficient for
phosphorous, FI, was varied until the oxide thickness grown in the flat region where the silicon was etched 2μm (tip valley region) matched that grown in the SUPREM-3 simulation of the same cross-section. Once this was determined, a time for the tip sharpening oxidation was arrived at by trial and error. The time was varied until a sharp point was created at the peak of the tip. The input deck for the final SUPREM-4 simulation of the tip is given in Appendix 3, page A3-40. Results of this simulation will be given in the next chapter.
CHAPTER 5. PROCESS DESIGN AND SIMULATION

SUPREM-3: FEA Tip Peak Before n+ Implant

Figure 5.3: Dopant profile before tip (silicon) etch for SUPREM-3.

SUPREM-4: FEA Tip Peak Before n+ Implant

Figure 5.4: Dopant profile before tip (silicon) etch for SUPREM-4.
Figure 5.5: SUPREM-4 simulation structure and grid.
SUPREM-3: FEA Tip Valley Before n+ Implant

Figure 5.6: Dopant profile after tip (silicon) etch for SUPREM-3.

SUPREM-4: FEA Tip Valley Before n+ Implant

Figure 5.7: Dopant profile after tip (silicon) etch for SUPREM-4.
CHAPTER 5. PROCESS DESIGN AND SIMULATION

SUPREM-3: FEA Tip Valley After n+ Implant

Figure 5.8: Dopant profile in valley after tip etch and n+ implant for SUPREM-3.

SUPREM-4: FEA Tip Valley After n+ Implant

Figure 5.9: Dopant profile in valley after tip etch and n+ implant for SUPREM-4.
Figure 5.10: Dopant profile in peak after tip sharpening for SUPREM-3.

Figure 5.11: Dopant profile in peak after tip sharpening for SUPREM-4.
Figure 5.12: Dopant profile in valley after tip sharpening for SUPREM-3.

Figure 5.13: Dopant profile in valley after tip sharpening for SUPREM-4.
Chapter 6

Results

6.1 CCD Emitter Process Outline

An outline of the final processing sequence is shown in table 6.1, with details of the process given in Appendix 5. The steps outlined in bold are those which already existed in the RIT n-well CMOS process but were modified. Italicized steps are those added or modified due to the inclusion of the CCD and underlined steps are those added or modified due to the inclusion of the FEA. A detailed discussion of the modifications follows later in this chapter.
Table 6.1: Final CCD Emitter process.

1 Starting wafers  
   <100>, p-type, boron doped, 5-15 Ωcm

2 Alignment oxide growth  
   1100°C, 60min wet O₂  
   + 1150°C, 600min N₂  
   Expected oxide thickness: 6000Å

3 Pattern n-Well mask level #1

4 n-Well implant  
   Phosphorous; 130keV; 6E12 ions/cm²

5 n-Well drive-in  
   1000°C, 10min dry O₂ + 25min wet O₂ + 5min dry O₂  
   + 1150°C, 1250min N₂  
   + 800°C, 400min N₂  
   Expected junction depth: 5μm

6 Pad oxide growth  
   1100°C, 15min dry O₂; 580Å

7 Nitride deposition  
   LPCVD; 790-810°C; 20min deposition; 1500Å

8 Pattern Active - mask level #2

9 Pattern Field Threshold Adjust - mask level #3

10 Field threshold adj. implant  
   Boron 11; 35keV; 3E13 ions/cm²

11 Field oxide growth (LOCOS)  
   800°C, 15min dry O₂  
   + 1100°C, 25min dry O₂  
   + 950°C, 15min dry O₂ + 400min wet O₂ + 30min N₂  
   Expected oxide thickness: 8000Å

12 Kooi oxide growth  
   900°C, 50min wet O₂  
   Expected oxide thickness: 1000Å

13 Threshold adjust implant  
   Boron 11; 35keV; 2E12 ions/cm²

14 Pattern Buried Channel - mask level #4

15 Buried channel implant  
   Phosphorous; 150keV; 2.5E12 ions/cm²

16 Gate oxide growth  
   950°C, 15min N₂ + 125min dry O₂ + 30min N₂  
   Expected oxide thickness: 750Å

17 Polysilicon1 deposition  
   LPCVD; 610°C; 73min deposition; 6500Å

18 Polysilicon doping  
   Emulsitone N-250 spin-on dopant  
   950°C, 10min N₂  
   Expected sheet resistance: 45 Ω/sq

19 Pattern Poly1 gates - mask level #5
20 Gate oxide etchback
To 200Å in regions where poly2 gates will be.

21 First isolation oxidation
950°C, 15min N₂ + 110min dry O₂ w/ TCA + 30min N₂
Expected oxide thickness: 750Å in poly2 gate regions.

22 Polysilicon2 deposition
LPCVD; 610°C; 73min deposition; 6500Å

23 Polysilicon doping
Emulsitone N-250 spin-on dopant
950°C, 10min N₂
Expected sheet resistance: 45 Ω/sq

24 Pattern Poly2 gates - mask level #6

25 Second isolation oxidation
900°C, 25min wet O₂; 1200Å in FEA region.

26 Pattern Tips - mask level #7

27 Oxide etch
RIE; 200W; 170:60:48sccm CHF₃:C₆F₁₄:CO₂; 150mtorr; 2min

28 Silicon etch
RIE; 190W; 10:4:7sccm SF₆:O₂:CO₂; 73mtorr; 3min
Final depth of etch: 1.9-2.1μm

29 Pattern p+ S/D - mask level #8
30 p+ S/D implant
BF₂⁺; 55keV; 1E15 ions/cm²

31 Pattern n+ S/D - mask level #9
32 n+ S/D implant
Phosphorous; 35keV; 1E15 ions/cm²

33 Tip sharpening oxidation
900°C, 75 min wet O₂; 2500Å in valley of FEA.

34 Glass deposition
2000Å undoped LTO + 12000Å BPSG; 420°C.
BPSG: 4% by weight boron, 4% by weight phos.

35 Reflow
900°C, 60 min N₂.

36 Pattern Contacts - mask level #10
37 Aluminum deposition
Sputter 0.5μm
38 Sinter
450°C, 20min forming gas (90% N₂, 10% H₂)

39 Pattern Aperature - mask level #11

40 Pattern Metal - mask level #12
6.2 CMOS Process Modifications

The steps highlighted in bold only are steps which were part of the original RIT n-well CMOS process but were incompatible with the "standard" CMOS, and thus CCD Emitter, process. The first of these is the alignment oxide growth. An thicker oxide was desired in order to increase the step difference of the alignment mark so that it would be visible during later lithography levels. This was necessary because there are 13 masking levels, including bond pad openings in the passivation, versus the 9 masking levels of base CMOS process.

Next, the pad oxide was increased to 580Å and the nitride thickness to 1500Å. This arrangement is more typical of a standard CMOS process. It was also necessary for masking the field threshold implant because the complement of the n-well mask, rather than the n-well complement orred with the active mask, was used as the field threshold adjust mask. A value of 3E13 ions/cm² was chosen for the field threshold adjust implant because it typifies a CMOS process and should be high enough to provide adequate isolation between transistors with the increased field oxide thickness. The field oxide was increased from 7500Å to 8000Å. Another step that was changed to reflect a standard CMOS process was the Kooi oxide growth. This oxide thickness was increased to 1000Å. Finally, the threshold adjust implant was chosen to be 2E12 ions/cm². This value, determined from simulations, provides reasonable threshold voltages (+1V and -2V) with only minor compensation of the phosphorous dopant in the buried-channel.
6.3 CCD Process Steps

The buried-channel implant was determined to be 150keV, 2.5E15 ions/cm² to provide a 0.5µm final junction depth. The gate oxide thickness was changed from 550Å to 750Å by increasing the growth time and using TCA during growth. Polysilicon was deposited to a thickness of 6500Å immediately following the gate oxidation. This thickness was arrived at from simulations. Keeping the polysilicon doping step as it was to get a sheet resistance below 100 Ω/sq required the increased polysilicon thickness to avoid diffusing phosphorous through the gate and into the substrate. The second polysilicon deposition and doping utilized the same parameters as the first. In order to obtain the same gate oxide thickness under the poly2 gates as under the poly1 gates, the oxide in these regions was etched back to 200Å following poly1 patterning and then grown back to 750Å during the first isolation oxidation. This oxidation step was performed in the same ambient as the gate oxide growth to obtain a high quality oxide under the poly2 gates. The second isolation oxide thickness was chosen to provide a sufficient mask for the silicon etching to form the emitter tips. This entire sequence was processed, including successive thermal steps, to confirm that no phosphorous penetrated through the gate from the polysilicon.

6.4 FEA Process Steps

Due to the three-dimensional nature of the emitter tips and the fact that plasma etch processes can not be simulated, the FEA process steps were run in the fab to determine the processing parameters. Fabrication of a subset of the CCD Emitter process, shown in table 6.2, was completed to produce samples for experimentation. The goal was to mimic the conditions (oxide thicknesses, doping levels, etc.) that would be seen in the entire CCD Emitter processing. The final results for these steps are shown in table 6.2.
Table 6.2: FEA-only process.

1 Starting wafers  
<100>, p-type, boron doped, 20-40 $\Omega$·cm

2 Alignment oxide growth  
1100°C, 60min wet $O_2$  
+ 1150°C, 600min $N_2$  
Oxide thickness: 6000Å

3 Pattern n-Well - mask level #1

4 n-Well implant  
Phosphorous; 150keV; 8E12 ions/cm²

5 n-Well drive-in  
950°C, 20min wet $O_2$ + 15min $N_2$  
+ 1125°C, 1920min dry $O_2$  
Junction depth: 6.7µm  
Oxide thickness: 7400Å

26 Pattern Tips - mask level #2

27 Oxide etch  
RIE; 200W; 170:60:48sccm $CHF_3:C_2F_6:CO_2$; 150mtorr; 17min

28 Silicon etch  
RIE; 190W; 10:4:7sccm $SF_6:O_2:CO_2$; 73mtorr; 3min  
Final depth of etch: 1.9-2.1µm

31 Pattern n+ S/D - mask level #3  
Same mask as level 1

32 n+ S/D implant  
Phosphorous; 35keV; 1E15 ions/cm²

33 Tip sharpening oxidation  
900°C, 75min wet $O_2$; 2500Å in valley of FEA.

34 Glass deposition  
2000Å undoped LTO + 12000Å BPSG; 420°C.  
BPSG: 4% by weight boron, 4% by weight phosphorous.

35 Reflow  
900°C, 60min $N_2$

36 Pattern Contacts - mask level #4

37 Aluminum deposition  
Sputter 0.5µm

38 Sinter  
450°C, 20min forming gas (90% $N_2$, 10% $H_2$)

39 Pattern Aperature - mask level #5

40 Pattern Metal - mask level #6
It should be noted that the starting wafer resistivity was 20-40 Ω·cm instead of 5-15 Ω·cm due to wafer availability. Also note that the n-well implant and drive-in parameters are different than those used defined for the CCD Emitter process. Neither of these factors should have a major impact on the experiments performed for determining the silicon etch parameters since the well doping would still be very close to that for wafers processed with the CCD Emitter process. Finally, note that the tip etch masking oxide thickness was 7400Å versus 1200Å in the CCD Emitter process. This should also not have a major impact on the determination of the silicon etch parameters.

6.5 Silicon Etch Determination

Samples were prepared by processing silicon wafers through step 26 (tip patterning) of table 6.2. Next, since a small number of wafers were processed and some would be required for experiments following the silicon etch determination, two wafers were broken up into 11 one inch squares. Each sample was mounted to a dummy wafer with hard-baked resist for the RIE experiments. Oxide etch parameters were obtained from a study of SiO₂ etching at RIT 34. These parameters provide a nearly vertical oxide sidewall, therefore maintaining the 2μm tip mask pattern, and high SiO₂:Si selectivity.

A statistically designed screening experiment was used for determining the etch parameters so that only the 11 samples would be required. Since four factors were varied over three levels each, a full-factorial design would require 81 samples. The starting values for the silicon etch were derived from the development of a trench etching process at RIT 35. The etch gas, SF₆, was maintained at 10sccm and the etch time was maintained at 3min 45sec (determined from a preliminary run) while the diluents, pressure, and power were varied as shown in table 6.3. Table 6.4 shows the experimental matrix and randomized run order.
CHAPTER 6. RESULTS

Table 6.3: Silicon etch variables.

<table>
<thead>
<tr>
<th>Factor</th>
<th>Level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
</tr>
<tr>
<td>O₂ (sccm)</td>
<td>0</td>
</tr>
<tr>
<td>CO₂ (sccm)</td>
<td>0</td>
</tr>
<tr>
<td>Pressure (mtorr)</td>
<td>60</td>
</tr>
<tr>
<td>Power (W)</td>
<td>150</td>
</tr>
</tbody>
</table>

Table 6.4: Screening experiment design and run order.

<table>
<thead>
<tr>
<th>Run #</th>
<th>O₂</th>
<th>CO₂</th>
<th>Pressure</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>6</td>
<td>+</td>
<td></td>
<td>+</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>+</td>
<td></td>
<td>+</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>+</td>
<td></td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>+</td>
<td>+</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>+</td>
<td></td>
<td>+</td>
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<tr>
<td>5</td>
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<td>+</td>
<td>+</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
The results of the etch experiment were evaluated with Alpha-step profilometry and SEMs. Etch depth was measured with the Alpha-step as shown in the example in figure 6.1. This measurement shows an etch depth of 1.85μm. Etch depth was confirmed and undercut was determined using SEM images. The corner of the tips-only device, where the 2μm wide wedges meet, was used in cases where the oxide caps were removed due to too much undercut. Figure 6.2 shows one example of the corner structure in which the undercut is 0.5μm and the etch depth is 1.5μm. Table 6.5 summarizes the results for all the runs. Aspect is the ratio of undercut to vertical etch depth. Figures 6.3 and 6.4 represent the varied results obtained from the experimental matrix. SEM photos of all the samples may be found in Appendix 4.

Figure 6.1: Alpha-step profile of a sample after silicon etch.
Figure 6.2: FEA-only corner structure used for SEM measurements (10000x magnification).

Table 6.5: RS1 table of silicon etch results.
Figure 6.3: Silicon etch results for run number 1 (10000x).

Figure 6.4: Silicon etch results for run number 11 (10000x).
The statistical software package RS1 was used to fit a model to the silicon etch parameters. The response was Aspect and only the linear terms were used since not enough degrees of freedom were available for the interaction and quadratic terms. Table 6.6 shows the resulting model coefficients and the summary ANOVA for the model.

Table 6.6: RS1 model for the silicon etch parameters.

---

**COEFF 5R x 5C**

<table>
<thead>
<tr>
<th>Term</th>
<th>Coeff.</th>
<th>Std. Error</th>
<th>T-value</th>
<th>Signif.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1</td>
<td>0.065958</td>
<td>0.170612</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 -O</td>
<td>0.103966</td>
<td>0.200060</td>
<td>0.52</td>
<td>0.6219</td>
</tr>
<tr>
<td>3 -C</td>
<td>-0.142043</td>
<td>0.200060</td>
<td>-0.71</td>
<td>0.5043</td>
</tr>
<tr>
<td>4 -P</td>
<td>0.107657</td>
<td>0.200060</td>
<td>0.54</td>
<td>0.6099</td>
</tr>
<tr>
<td>5 -W</td>
<td>0.354266</td>
<td>0.200060</td>
<td>1.77</td>
<td>0.1270</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Term</th>
<th>Transformed Term</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1</td>
<td></td>
</tr>
<tr>
<td>2 -O</td>
<td>((O-3)/3)</td>
</tr>
<tr>
<td>3 -C</td>
<td>((C-5)/5)</td>
</tr>
<tr>
<td>4 -P</td>
<td>((P-8e+01)/2e+01)</td>
</tr>
<tr>
<td>5 -W</td>
<td>((W-2e+02)/5e+01)</td>
</tr>
</tbody>
</table>

- indicates factors are transformed.

---

**SUM_ANOVA 5R x 5C**

<table>
<thead>
<tr>
<th>Source</th>
<th>1 df</th>
<th>2 Sum Sq.</th>
<th>3 Mean Sq.</th>
<th>4 F-Ratio</th>
<th>5 Signif.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Total(Corr.)</td>
<td>10</td>
<td>3.265799</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 Regression</td>
<td>4</td>
<td>1.344638</td>
<td>0.336160</td>
<td>1.05</td>
<td>0.4550</td>
</tr>
<tr>
<td>3 Residual</td>
<td>6</td>
<td>1.921161</td>
<td>0.320194</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 Lack of fit</td>
<td>4</td>
<td>1.681137</td>
<td>0.420284</td>
<td>3.50</td>
<td>0.2343</td>
</tr>
<tr>
<td>5 Pure error</td>
<td>2</td>
<td>0.240024</td>
<td>0.120012</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R-sq. 0.4117
R-sq-adj. 0.0196

Model obeys hierarchy. The sum of squares for linear terms is computed assuming nonlinear terms are first removed. F(4,2) as large as 3.502 is not a rare event. => no evidence of lack of fit.
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Using the model developed with RS1, the Aspect response was optimized for a value of 0.45 which corresponds to the desired 2μm etch depth and 0.9μm undercut. The optimum values, shown in table 6.7, were rounded off to 4sccm O₂, 7sccm CO₂, 73mtorr, and 190W. A run was performed with these value for the same time as used in the experiment (3min 45sec). The result was a 2.3μm etch depth and, therefore, too much undercut which caused the removal of the masking oxide caps as shown in figure 6.5. Since the aspect response was optimized and the etch depth varied for different conditions, the software did not care what time was used for the run. Based on this, all that was required to obtain the desired structure, as shown in figure 6.6, was to reduce the time to etch time 3min.

Table 6.7: RS1 optimization of the silicon etch process.

<table>
<thead>
<tr>
<th>Factor, Response or Formula</th>
<th>Range</th>
<th>Initial Setting</th>
<th>Optimal Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Factors</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 O₂</td>
<td>0 to 6</td>
<td>3</td>
<td>3.9247</td>
</tr>
<tr>
<td>3 CO₂</td>
<td>0 to 10</td>
<td>5</td>
<td>7.3522</td>
</tr>
<tr>
<td>4 PRESS</td>
<td>60 to 100</td>
<td>80</td>
<td>72.451</td>
</tr>
<tr>
<td>5 POWER</td>
<td>150 to 250</td>
<td>200</td>
<td>187.22</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 Responses</td>
<td></td>
<td></td>
<td>0.45</td>
</tr>
<tr>
<td>8 ASPECT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Formulas</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 RESP</td>
<td>MIN</td>
<td></td>
<td>1.1561e-09</td>
</tr>
</tbody>
</table>

Converged to a tolerance of 1.65e-09 after 98 steps.
Figure 6.5: Results for first run (3.75min) with optimum etch process (10000x).

Figure 6.6: Results for second run (3min) with optimum etch process (10000x).
6.6 Emitter Tip Sharpening

As discussed in section 5.4, the tip sharpening oxidation was simulated using the two-dimensional SUPREM-4 simulator. The results of these simulations are shown in figures 6.7 and 6.8. From figure 6.8 it is obvious that the device geometry has a noticeable effect on the dopant (phosphorous) distribution within the tip. This effect results in only a minor geometrical influence on oxide thickness. Figures 6.9 and 6.10 show how the results of processing of the tip sharpening step closely match the simulations.

![FEA Tip After Sharpening Oxidation](image)

**Figure 6.7:** Oxide thickness from SUPREM-4 simulation of tip sharpening.
Figure 6.8: Dopant contours from SUPREM-4 simulation of tip sharpening.
Figure 6.9: Results of tip sharpening oxidation; oxide still intact (10000x).

Figure 6.10: Results of tip sharpening oxidation; oxide removed (10000x).
6.7 FEA Grid Formation

Following the tip sharpening oxidation, approximately 1.4μm of silicon dioxide was deposited by LPCVD. The deposition was performed at Eastman Kodak's research lab. First, 2000Å of undoped LTO was deposited. This was followed by approximately 1.2μm of BPSG. The BPSG contained 4% by weight of boron and 4% by weight of phosphorous which allows for reflow of the glass. Reflow was necessary because the glass is conformal as deposited (see figure 6.11). Without reflow, it would be difficult to define a 3μm diameter, 0.5μm thick metal grid over the glass. A low temperature of 800°C was tried for the first attempt at reflow so that dopant redistribution within the device would be minimized. After three hours, however, not enough flow was observed, as shown in figure 6.12. After boosting the reflow temperature to 900°C (for one hour) adequate planarization was observed as shown in figure 6.13.

Figure 6.11: As-deposited BPSG (10000x).
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Figure 6.12: BPSG after 3 hours at 800°C in nitrogen (10000x).

Figure 6.13: BPSG after 1 hour at 900°C in nitrogen (10000x).
The grid metal (aluminum) was deposited 0.5μm thick following the BPSG reflow step. The 0.5μm added to the 1.5μm BPSG/oxide stack results in a grid that has its top surface level with the peak of the tip. After aligning and patterning the device with the Aperature mask, the metal was etched with aluminum etchant then the oxide was removed from the tip with a 8min BOE etch. Lithography problems during the patterning step resulted in poor uniformity of the 3μm diameter grid openings as can be seen in the SEM photo of the finished gated field emitter tip of figure 6.14. Additionally, resist adhesion problems resulted in lifting of the resist during the oxide etch an subsequent attacking of the aluminum. Enough aluminum was removed in some areas to make it not worth finishing the fabrication (namely the metal interconnect patterning). It is apparent from figure 6.14, that the desired structure was obtained.

Figure 6.14: Finished gated field emitter tip array (10000x).
Chapter 7

Future Development

7.1 Device Fabrication

Originally, the goal of this project was to fabricate a working model of the CCD Emitter and test it to demonstrate the concept. It is still desirable for RIT to accomplish this goal in the future. With this project, much of the foundation work has been completed. What remains in the development of the CCD Emitter device is to complete fabrication of the CCD Emitter. First, the FEA-only device must be completed, and tested to get Fowler-Nordheim plots, to determine if the fabricated gated emitter tip arrays provide sufficient current for the application. This requires stripping the aluminum, which was attacked during the aperture etch, and sputtering new aluminum before completing the remainder of the processing steps outlined in table 6.2.

Once the FEA structure has been confirmed to be suitable for the application, the processing of the entire CCD Emitter process, as outlined in Appendix 5, should be completed. A lot of wafers has been started for this process and was processed through the n-well (mask #1) patterning step. Coincident with the CCD Emitter processing, a phosphor coated, transparent, conductive anode must be fabricated. This screen need only have one color phosphor and a common conductor across the entire screen for early work with this device. In the long term, a screen utilizing the three primary color phosphors, such as in figure 2.17, should be developed. In addition, a method for mounting the anode (screen) to the CCD Emitter substrate must be developed.
7.2 Test Apparatus

In order to test the functionality of the CCD Emitter device, and the electrical characteristics of the FEAs, it is necessary to operate the devices in a vacuum. For this reason, a testing apparatus fully contained in a vacuum bell jar must be devised. The requirement for vacuum capability is a pressure of $10^6$ torr at most. Lower pressures, around $10^9$ torr, are typically used when testing FEAs. Since getting to such a high vacuum state requires much time with most vacuum pumps, it is desirable to be able to probe different devices across the wafer without breaking vacuum. To this end, wafer and/or probe manipulator high vacuum feed-throughs would be required. The use of probe cards and wafer manipulators over individual probes is suggested due to the relatively high pin counts for the devices. In addition to a probe station, a video camera and optics would be required in the bell jar with a feed-through to an external monitor would be needed for observing the small pixels.
A process for creating gated field emitter tips has been defined and fabrication of the gated tips has been completed. The processing sequence for the CCD Emitter device has been designed and simulated. Parameters obtained for process steps that deviated from the RIT n-well CMOS process were confirmed through fabrication of the individual step or a subset of the CCD Emitter process steps. Layouts for the CCD Emitter device and test structures representing the building blocks of the CCD Emitter have been completed and reticles for all levels of the layouts have been fabricated for use on GCA-6700 (5x) steppers. Stepper job decks have been written to utilize these reticles. In short, the CCD Emitter process is ready for fabrication of a working model. The fabrication process may be completed by a technician with little or no modification to the steps. It has been demonstrated that this device may be fabricated with reasonable modifications to a "standard" double-poly, n-well CMOS process.
References


6. Ibid.


8. Opcit, p. 36.


REFERENCES


17. Ibid, p. 197.


21. Ibid, p. 27.


REFERENCES

30. Opcit.

31. Ibid.


Device Layouts

Figure A1.1: Legend for layers defined in SIEGER_CCD process.
Figure A1.2: Entire TIPSONLY chip.
Figure A1.3: TIPARRAY cell used in TIPSONLY chip.
Figure A1.4: Entire CCD/FEA project chip (TVCHIP).
Figure A1.5: GCA-6700 alignment mark cell.
Figure A1.6: 8 line by 16 pixel device.
Figure A1.7: Line of 10 pixels.
Figure A1.8: Single pixel (with input cell) device.
Figure A1.9: Four-phase BCCD.
Figure A1.10: Single FEA of 30 by 30 tips.
Figure A1.11: Array of test structures; plots of individual structures follow.
Figure A1.12: NMOS transistor with poly1 gate.
Figure A1.13: NMOS transistor with poly2 gate.
Figure A1.14: PMOS transistor with poly1 gate.
Figure A1.15: PMOS transistor with poly2 gate.
Figure A1.16: Single BCCD transistor with poly1 gate.
Figure A1.17: Single BCCD transistor with poly2 gate.
Figure A1.18: Van Der Pauw - p+ region in p wafer.
Figure A1.19: Van Der Pauw - n+ region in n-well.
Figure A1.20: Van Der Pauw n-well.
Figure A1.21: Van Der Pauw - p+ region in n-well.
Figure A1.22: Van Der Pauw - n+ region in p wafer.
Figure A1.23: Van Der Pauw - n+ region in n-well with 2μm silicon etched away.
Figure A1.24: Van Der Pauw buried channel region (n type) in p wafer.
Figure A1.25: Van Der Pauw - poly1.
Figure A1.26: Van Der Pauw - poly2.
Figure A1.27: Van Der Pauw - poly1 exposed to p+ S/D implant (PMOS poly1 gate).
Figure A1.28: Van Der Pauw - poly2 exposed to p+ S/D implant (PMOS poly2 gate).
Figure A1.29: Van Der Pauw - poly1 exposed to n+ S/D implant (NMOS poly1 gate).
Figure A1.30: Van Der Pauw - poly2 exposed to n+ S/D implant (NMOS poly2 gate).
Figure A1.31: Kelvin'structure - contact to p+ S/D.
Figure A1.32: Kelvin structure - contact to n+ S/D.
Figure A1.33: Kelvin structure - contact to poly1 exposed to p+ S/D implant.
Figure A1.34: Kelvin structure contact to poly2 exposed to p+ S/D implant.
Figure A1.35: Kelvin structure - contact to poly1 exposed to n+ S/D implant.
Figure A1.36: Kelvin structure - contact to poly2 exposed to n+ S/D implant.
Figure A1.37: Input cell for CCD Emitter devices.
Figure A1.38: Mirrored version of the input cell for CCD Emitter devices.
Figure A1.39: Single pixel cell for CCD Emitter devices.
Figure A1.40: Mirrored version of the pixel cell for CCD Emitter devices.
Figure A1.41: FEA cell used in each pixel (30 by 30 tips).
Figure A1.42: Four-phase BCCD cell used in each pixel.
Figure A1.43: Mirrored version of the four-phase BCCD cell; used in each mirrored pixel.
MEBES Job Decks:

Figure A2.1: EMCSIEG1.JB - 0.5μm job deck used for levels 1, 4, and 6 of TIPS_ONLY design.
Figure A2.2: EMCSIEG1B.JB - 0.25µm job deck used for levels 3 and 5 of TIPS_ONLY design.

```
SLICE_EDIT.14
* MTITLE 1.SIEGER LAYER 1
* MTITLE 2.SIEGER LAYER 2
* MTITLE 3.SIEGER LAYER 3
* MTITLE 4.SIEGER LAYER 4
* MTITLE 5.SIEGER LAYER 5
* MTITLE 6.SIEGER LAYER 6
* DTITLE 1,M920609 RI #1
* DTITLE 2,M920609 RI #2
* DTITLE 3,M920609 RI #3
* DTITLE 4,M920609 RI #4
* DTITLE 5,M920609 RI #5
* DTITLE 6,M920609 RI #6
* CHIP 1, (A.XYVERN1-50-01 RC-13),
* ROWS 15000,2,95000/15000,2,95000
* CHIP 2, (1,M920609-R1-01, RC=13),
* $ (2,M920609-R1-02, RC=13),
* $ (3,M920609-R1-03, RC=13),
* $ (4,M920609-R1-04, RC=13),
* $ (5,M920609-R1-05, RC=13),
* $ (6,M920609-R1-06, RC=13)
* ROWS 42336,3,21165/42336,3,21165
* CHIP 3, (A.RITLOGO-25-01 RC=13),
* ROWS 10000/62500
* CHIP 4, (A.GCA6700-FI-01, RC=13),
* ROWS 62500/62500/62500/62500
* CHIP 5, (A.L173634-01-02 RC=13),
* ROWS 20000,2,6000/20000,2,6000
* CHIP 6, (A.XYVERN1-50-02 RC=13),
* ROWS 15000,2,95000/15000,2,95000
END
```
Figure A2.3: EMCSIEG2.JB - 0.5μm job deck used for all level except 7 and 11 of TVCHIP design.

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OPTION AA=0.5, BA=0.5, PA, SA=40, VA=10
MTITLE 1, LEVELS 1 2 3 4
MTITLE 2, LEVELS 5 6 7 8
MTITLE 3, LEVELS 9 10 11 12
MITLE 4, LEVEL 13
DTITLE A, SIEGER THESIS CCD FEA
CHIP 1, (A, XYVERN1-50-01, RC=13)
ROWS 15000, 2, 95000/15000, 2, 95000
CHIP 2,
$ (1, G890914-TS-01, RC=15),
$ (2, G890914-TS-05, RC=15),
$ (3, G890914-TS-09, RC=15),
$ (4, G890914-TS-13, RC=15),
ROWS 85000/40000
CHIP 3,
$ (1, G890914-TS-02, RC=15),
$ (2, G890914-TS-06, RC=15),
$ (3, G890914-TS-10, RC=15),
ROWS 85000/85000
CHIP 4,
$ (1, G890914-TS-03, RC=15),
* $ (2, G890914-TS-07, RC=15),
* (3, G890914-TS-11, RC=15),
7 AND 11 ARE DONE WITH EMGSIEG2B.JB
* 
ROWS 40000/85000
CHIP 5,
$ (1, G890914-TS-04, RC=15),
$ (2, G890914-TS-08, RC=15),
$ (3, G890914-TS-12, RC=15),
ROWS 40000/40000
CHIP 90, (A, RITLOGO-50-01, RC=13)
ROWS 10000/20000
CHIP 91, (A, GCA6700-FI-05, RC=13)
ROWS 62500/50000/120000
CHIP 92, (A, L173634-01-02, RC=13)
ROWS 20000, 2, 85000/62500
ROWS 62500/20000, 2, 85000
CHIP 93, (A, XYVERN1-50-02, RC=13)
ROWS 15000, 2, 95000/15000, 2, 95000
END
```

Figure A2.4: EMCSIEG2B.JB 0.25μm job deck used for levels 7 and 11 of TVCHIP design.

```
SLICE EDIT, 14
OPTION AA=0.25, BA=0.25, PA, SA=10, VA=10
* THIS IS TO PLACE THE .25UM PATTERNS
* WITHOUT PUTTING TITLES OR ANYTHING ELSE
* USE THIS WITH MESES/T
* AS IT IS GOING ON A MASK WITH
* AN EXISTING SERIAL NUMBER
* 
CHIP 4,
$ (2, G890914-TS-07, RC=15),
$ (3, G890914-TS-11, RC=15),
ROWS 40000/85000
END
```
APPENDIX 2. MEBES AND STEPPER JOB DECKS

Figure A2.5: Job specification for Reticle #1 of TVCHIP design (levels 1-4).
Figure A2.6: Job specification for 0.5μm part of Reticle #2 of TVCHIP design (levels 5, 6, and 8).

7/18/92  15:10  MEBES 967
REV. 4.6
SPECIFICATION FILE: JOB:EMGSIE2.JOB
DITITLE: SIEGER THESIS  CCD  FEA
ITITLE: LEVELS 5 6 7 8
STITLE:
CASSSETTE TYPE ID: 14.
LEVEL PLOTTED: 2
JOB SCALE: 1.000000
ADDRESSING: .500000 MICRONS
PLOT SCALE: 1.000 TO 1 CM

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<th>TONE</th>
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<td>5</td>
<td>RITLOGOB0 #1</td>
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<td>2200.00</td>
<td>UNMIRROR</td>
<td>UNMIRROR</td>
<td>NORMAL</td>
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<td>L17363401 #02</td>
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<td>510.00</td>
<td>UNMIRROR</td>
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<td>NORMAL</td>
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<td>7</td>
<td>XYVERN150 #02</td>
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<td>255.00</td>
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Figure A2.7: Job specification for 0.25µm part of Reticle #2 of TVCHIP design (level 7).
Figure A2.8: Job specification for 0.5μm part of Reticle #3 of TVCHIP design (levels 9, 10, and 12).

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Figure A2.9: Job specification for 0.25μm part of Reticle #3 of TVCHIP design (level 11).

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Figure A2.10: Job specification for Reticle #4 of TVCHIP design (level 13).

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<td>XXVERN156.02</td>
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GCA-6700 Stepper Job Decks:

Job deck for TIPS ONLY design (TSIEGER):

```
EDIT TSIEGER

METRIC JOB CREATED: 13:09 08/08/92
UPDATE CREATION DATE? (*Y/N): N
JOB COMMENT:
4", 5 LEVEL, 3X3 FEA ARRAY - TODD SIEGER'S THESIS PART I

TOLERANCE (1,2,*3,4,5,6): 3

SCALE CORRECTIONS
x, PPM (-128<P<+128): 
Y, PPM (-128<P<+128):

ORTHOGONALITY, PPM (-128<P<+128):

LEVELER BATCH SIZE [ 1 - 25 ] : 1
WAFER DIAMETER 100.00000

<< ARRAY PARAMETERS >>

STEP SIZE IN X: 12.70000
*C-OUNT, S-PAN OR A-LL:
HOW MANY COLUMNS? 7

STEP SIZE IN Y: 12.70000
*C-OUNT, S-PAN OR A-LL:
HOW MANY ROWS? 7

TRANSLATE ORIGIN
IN X:
IN Y:

DISPLAY? (Y/*N):
LAYOUT? (Y/*N):

<< ALIGNMENT PARAMETERS >>

STANDARD KEYS? (*Y/N):

RIGHT KEY OFFSET
IN X: -2.58169
IN Y: -1.99086

EPI SHIFT
IN X:
IN Y:
```
<< PASS >>

NAME: 1
PASS COMMENT:
ALIGN LEVELS 2-6 USING THIS PASS AND GCA MARKS FURTHEST INTO CORNER

EXPOSURE (SEC.): 0.350
FOCUS SETTING: 250

DXD BATCH CHARACTERIZATION SIZE (-1=NO DXD): -1
AWA PARAMETER FILE NAME (NO EXTENSION) (NONE)

SHIFT
IN X: 0.05461
IN Y: 0.10210

RETICLE BAR CODE: NONE
XL MASKING APERTURE SETTING: 16.00000
XR MASKING APERTURE SETTING: 16.00000
YF MASKING APERTURE SETTING: 16.00000
YR MASKING APERTURE SETTING: 16.00000

XL MASKING APERTURE OFFSET:
XR MASKING APERTURE OFFSET:
YF MASKING APERTURE OFFSET:
YR MASKING APERTURE OFFSET:

XL RETICLE ALIGNMENT OFFSET:
XR RETICLE ALIGNMENT OFFSET:
Y RETICLE ALIGNMENT OFFSET:

RETICLE ALIGNMENT MARK PHASE (P,*N,X): N
A-ARRAY OR P-LUG: A

DROPOUTS:
R:

<< END PASS SET-UP >>
SAVE PASS? (*Y/N):

<< PASS >>

NAME: 2
PASS COMMENT:
ALIGN LEVELS 4-6 USING MARK FROM LEVEL 3 (SI ETCHED) - 400UM TO LEFT

EXPOSURE (SEC.): 0.350

FOCUS SETTING: 250

DXD BATCH CHARACTERIZATION SIZE (-1=NO DXD): -1

AWA PARAMETER FILE NAME (NO EXTENSION) (NONE)

SHIFT
IN X: 0.45461
IN Y: 0.10210

RETICLE BAR CODE: NONE
XL MASKING APERTURE SETTING: 16.00000
XR MASKING APERTURE SETTING: 16.00000
YF MASKING APERTURE SETTING: 16.00000
YR MASKING APERTURE SETTING: 16.00000

XL MASKING APERTURE OFFSET:
XR MASKING APERTURE OFFSET:
YF MASKING APERTURE OFFSET:
YR MASKING APERTURE OFFSET:

XL RETICLE ALIGNMENT OFFSET:
XR RETICLE ALIGNMENT OFFSET:
Y RETICLE ALIGNMENT OFFSET:

RETICLE ALIGNMENT MARK PHASE (P,*N,X): N

A-ARRAY OR P-LUG: A

DROPOUTS:
R:

<< END PASS SET-UP >>
APPENDIX 2. MEBES AND STEPPER JOB DECKS

Job deck for TVCHIP design (T2SIEGER):

EDIT T2SIEGER

METRIC JOB CREATED: 08103 21/08/92
UPDATE CREATION DATE? (*Y/N):
JOB COMMENT:
TODD SIEGER - MSEE THESIS: CCD/FEA - 4 LEVELS/MASK PLATE

TOLERANCE (1,2,*3,4,5,6): 3

SCALE CORRECTIONS
X, PPM (-128<P<+128):
Y, PPM (-128<P<+128):

ORTHOGONALITY, PPM (-128<P<+128):

LEVELER BATCH SIZE [ 1 - 25 ]: 1

WAFER DIAMETER 100.00000

<< ARRAY PARAMETERS >>

STEP SIZE IN X: 5.86153
*COUNT, S-PAN OR A-LL:
HOW MANY COLUMNS? 17

STEP SIZE IN Y: 6.92727
*COUNT, S-PAN OR A-LL:
HOW MANY ROWS? 14

TRANSLATE ORIGIN
IN X:
IN Y:

DISPLAY? (Y/*N):
LAYOUT? (Y/*N):
ADJUST? (Y/*N):

<< ALIGNMENT PARAMETERS >>

STANDARD KEYS? (*Y/N):

RIGHT KEY OFFSET
IN X: 1.73655
IN Y: -0.76253

EPI SHIFT
IN X:
IN Y:
APPENDIX 2. MEBES AND STEPPER JOB DECKS

<< PASS >>

NAME: 1
PASS COMMENT:
LEVELS 1, 5, 9, 13 (UPPER LEFT ON CHROME SIDE); MAKE SHIFTS=0 FOR LEVEL 1

EXPOSURE (SEC.): 0.350
FOCUS SETTING: 251

DXD BATCH CHARACTERIZATION SIZE (-1=NO DXD): -1
AWA PARAMETER FILE NAME (NO EXTENSION) (NONE)

SHIFT
IN X: 0.01400
IN Y: -0.01881

RETICLE BAR CODE: NONE
XL MASKING APERTURE SETTING: 30.00000
XR MASKING APERTURE SETTING: 30.00000
YF MASKING APERTURE SETTING: 30.00000
YR MASKING APERTURE SETTING: 30.00000

XL MASKING APERTURE OFFSET: 22.50000
XR MASKING APERTURE OFFSET: -22.50000
YF MASKING APERTURE OFFSET: -22.50000
YR MASKING APERTURE OFFSET: 22.50000

XL RETICLE ALIGNMENT OFFSET:
XR RETICLE ALIGNMENT OFFSET:
Y RETICLE ALIGNMENT OFFSET:

RETICLE ALIGNMENT MARK PHASE (P, N, X): N
A-ARRAY OR P-LUG? P

PLUGS:

R:  V

PLUGS:

R:  2  +4.50000
C:  5-13 +4.50000

R:  3-4  +4.50000
C:  3-15 +4.50000

R:  5-10  +4.50000
C:  2-16 +4.50000

R:  11-12  +4.50000
C:  3-15 +4.50000

R:  13  +4.50000
C:  5-13 +4.50000

R:

<< END PASS SET-UP >>

SAVE PASS? (*Y/N):
APPENDIX 2. MEBES AND STEPPER JOB DECKS

<< PASS >>

NAME: 2
PASS COMMENT:
LEVELS 2, 6, 10 (UPPER RIGHT ON CHROME SIDE)

EXPOSURE (SEC.): 0.350
FOCUS SETTING: 251

DXD BATCH CHARACTERIZATION SIZE (-1=NO DXD): -1

AWA PARAMETER FILE NAME (NO EXTENSION) (NONE)

SHIFT
IN X: 0.01400
IN Y: -0.01881
RETICLE BAR CODE: NONE

XL MASKING APERTURE SETTING: 30.00000
XR MASKING APERTURE SETTING: 30.00000
YF MASKING APERTURE SETTING: 30.00000
YR MASKING APERTURE SETTING: 30.00000

XL MASKING APERTURE OFFSET: 22.50000
XR MASKING APERTURE OFFSET: -22.50000
YF MASKING APERTURE OFFSET: 22.50000
YR MASKING APERTURE OFFSET: -22.50000

XL RETICLE ALIGNMENT OFFSET:
XR RETICLE ALIGNMENT OFFSET:
Y RETICLE ALIGNMENT OFFSET:

RETICLE ALIGNMENT MARK PHASE (P,N,X): N
APPENDIX 2. MEBES AND STEPPER JOB DECKS

ARRAY OR P-LUG: P

PLUGS:

R:  V

PLUGS:

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<tbody>
<tr>
<td>2</td>
<td>5-13</td>
<td>3-4</td>
<td>3-15</td>
</tr>
</tbody>
</table>

R:
<< END PASS SET-UP >>

SAVE PASS? (*Y/N):
<< PASS >>

NAME: 3
PASS COMMENT:
LEVELS 3, 7, 11 (LOWER RIGHT ON CHROME SIDE)

EXPOSURE (SEC.): 0.350

FOCUS SETTING: 251

DXD BATCH CHARACTERIZATION SIZE (-1=NO DXD): -1

AWA PARAMETER FILE NAME (NO EXTENSION) (NONE)

SHIFT
IN X: 0.01400
IN Y: -0.01881

RETICLE BAR CODE: NONE

XL MASKING APERTURE SETTING: 30.00000
XR MASKING APERTURE SETTING: 30.00000
YF MASKING APERTURE SETTING: 30.00000
YR MASKING APERTURE SETTING: 30.00000

XL MASKING APERTURE OFFSET: -22.50000
XR MASKING APERTURE OFFSET: 22.50000
YF MASKING APERTURE OFFSET: 22.50000
YR MASKING APERTURE OFFSET: -22.50000

XL RETICLE ALIGNMENT OFFSET:
XR RETICLE ALIGNMENT OFFSET:
Y RETICLE ALIGNMENT OFFSET:

RETICLE ALIGNMENT MARK PHASE (P,N,X): N
ARRAY OR P-LUG: P

PLUGS:

R:  V

PLUGS:

R:  2  -4.50000
C:  5-13  -4.50000
R:  3-4  -4.50000
C:  3-15  -4.50000
R:  5-10  -4.50000
C:  2-16  -4.50000
R:  11-12  -4.50000
C:  3-15  -4.50000
R:  13  -4.50000
C:  5-13  -4.50000

R:

<< END PASS SET-UP >>

SAVE PASS? (*Y/N):
<< PASS >>

NAME: 4
PASS COMMENT:
LEVELS 4, 8, 12 (LOWER LEFT ON CHROME SIDE)

EXPOSURE (SEC.): 0.350

FOCUS SETTING: 251

DXD BATCH CHARACTERIZATION SIZE (-1=NO DXD): -1

AWA PARAMETER FILE NAME (NO EXTENSION) (NONE)

SHIFT
  IN X: 0.01400
  IN Y: -0.01881

RETICLE BAR CODE: NONE
XL MASKING APERTURE SETTING: 30.00000
XR MASKING APERTURE SETTING: 30.00000
YF MASKING APERTURE SETTING: 30.00000
YR MASKING APERTURE SETTING: 30.00000

XL MASKING APERTURE OFFSET: -22.50000
XR MASKING APERTURE OFFSET: 22.50000
YF MASKING APERTURE OFFSET: -22.50000
YR MASKING APERTURE OFFSET: 22.50000

XL RETICLE ALIGNMENT OFFSET:
XR RETICLE ALIGNMENT OFFSET:
Y RETICLE ALIGNMENT OFFSET:

RETICLE ALIGNMENT MARK PHASE (P,N,X): N
A-RRAY OR P-LUG: P
PLUGS:
R:  V

PLUGS:
R:  2  +4.50000  
C:  5-13 -4.50000  

R:  3-4  +4.50000  
C:  3-15 -4.50000  

R:  5-10  +4.50000  
C:  2-16 -4.50000  

R:  11-12  +4.50000  
C:  3-15 -4.50000  

R:  13  +4.50000  
C:  5-13 -4.50000  

R:

<< END PASS SET-UP >>

SAVE PASS? (*Y/N):

<< PASS >>

NAME ( <CR> TO EXIT PASS SETUP):

WRITE TO DISK? (*Y/N):

PURGE EDITED FILES ? (*Y/N):
SUPREM-3

Modular Input Deck

1 Title CCD/FEA Master Process Input Deck
2 Comment Defines all process steps use with table t: determine
3 Comment which lines to comment out for specific cross-sections.
4 Comment Todd Sieger Aug. 31, 1992
5 Comment Wafers are 5-15ohm*cm use 5ohm*cm for simulations.
6 Initialize <100> Silicon Resistivity Boron=5
7 $ Thickness=12 dX=.04
8 $ Comment
9 Comment Set layer numbers for some of the extract statements:
10 Assign Name=LI1XOX N.Value=#
11 Assign Name=LI2XOX N.Value=#
12 Assign Name=LTSXOX N.Value=#
13 Assign Name=LI2XOX N.Value=#
14 $ Comment
15 Assign Name=LTSXOX N.Value=#
16 $ Comment
17 Ambient O2 Lin.Cide Column=3 Temperature=950 Table(4)=0.9848
18 Ambient O2 <100> ThinOx.0=2.2632E7 H.Lin.0=1.1649E5
19 Ambient H20 <100> H.Lin.0=1.5049E6
20 Ambient H2O <100> Gamma.0=3813
21 $ Comment
22 Assign Name=AXOX Thickness Layer=2
23 Print Pattern n-Well M1.
24 Implant Phosphorous Energy=130 Dose=6E12
25 Print Pattern Electrical
26 $ Comment
27 Layer Electrical
28 $ Comment
29 Layer Electrical
30 $ Comment
31 Layer Electrical
32 $ Comment
33 Layer Electrical
34 Print Layers
35 Extract Name=AXOX Thickness Layer=2
36 Assign Name=AXOX N.Value=NINT(10000*#AXOX)
37 $ Comment
38 Pattern n-Well M1.
39 Etch Oxide all
40 $ Comment
41 Layer Electrical
42 Layer Electrical
43 Layer Electrical
44 Layer Electrical
45 Layer Electrical
46 Layer Electrical
47 Layer Electrical
48 Layer Electrical
49 Layer Electrical
50 Layer Electrical
51 Layer Electrical
52 Layer Electrical
53 Layer Electrical
54 Layer Electrical
55 Layer Electrical
56 Layer Electrical
57 Layer Electrical
58 Layer Electrical
59 Layer Electrical
60 Layer Electrical
61 $Comment
62 Layer Electrical
APPENDIX 3. CCD/FEA PROCESS SIMULATIONS

A3.2

62 Comment (Mesa patterning & silicon etch to a depth of 2um
63 Comment would be here for the lift-off process.)
64 $
65 Comment Strip oxide.
66 Etch Oxide all
67 $
68 Comment Grow Pad Oxide (1/3 of nitride thickness - 500A)
69 Diffusion Time=5 Temperature=900 t.rate=16 Nitrogen
70 Diffusion Time=5 Temperature=980 t.rate=15 Nitrogen
71 Diffusion Time=3.462 Temperature=1055 t.rate=13 Nitrogen
72 Diffusion Time=15 Temperature=1100 Dry02
73 Comment Dry 02 turned off after soak. Power off.
74 Diffusion Time=16 Temperature=1100 t.rate=-6.25 Nitrogen
75 Comment Pull the wafers out at 1000C.
76 Print Layers Electrical
77 Extract Name=POX Thickness Layer=2
78 Assign Name=POX N.Value=NINT(10000*POX)
79 $
80 Comment Deposit nitride (1500A) for LOCOS process.
81 Deposition Nitride Thickness=0.15
82 $
83 Comment Pattern Active regions M2.
84 Comment RIE etch nitride from field (isolation) areas.
85 Etch Nitride All
86 $
87 Diffusion Time=5 Temperature=900 t.rate=16 Nitrogen
88 Comment Pull the wafers out at 1000C.
89 Diffusion Time=5 Temperature=950 t.rate=15 Nitrogen
90 Comment Grow Field Oxide (~ 8000A)
91 Diffusion Time=15 Temperature=800 Dry02
92 Diffusion Time=20 Temperature=800 t.rate=15 Dry02
93 Diffusion Time=25 Temperature=1100 Dry02
94 Diffusion Time=30 Temperature=1100 t.rate=5 Dry02
95 Diffusion Time=36.35 Temperature=1100 Dry02
96 Diffusion Time=400 Temperature=950 Wet02
97 Diffusion Time=30 Temperature=950 Nitrogen
98 Diffusion Time=30 Temperature=950 t.rate=-5 Nitrogen
99 Comment Pull the wafers out at 800C.
100 Print Layers Electrical
101 Extract Name=POX Thickness Layer=2
102 Assign Name=POX N.Value=NINT(10000*POX)
103 $
104 Comment Grow Kooi Oxide (~1000A)
105 Diffusion Time=50 Temperature=900 Wet02
106 Comment Wet 02 turned off after soak.
107 Diffusion Time=50 Temperature=900 Wet02
108 Etch Oxide Thickness=0.0300
109 $
110 Comment Strip all oxinitride: 2min in 10:1 HF (rate=150A/min)
111 Etch Oxide Thickness=0.0300
112 $
113 Comment Strip all nitride in hot phosphoric acid.
114 Etch Nitride all
115 $
116 Comment Strip pad oxide.
117 Etch Oxide Thickness=0.0580
118 $
119 Comment Grow Kooi Oxide (~1000A)
120 Diffusion Time=50 Temperature=900 Wet02
121 Comment Wet 02 turned off after soak.
122 Diffusion Time=50 Temperature=900 Wet02
123 Etch Oxide Thickness=0.0580
124 $
125 Comment Grow Kooi Oxide (~1000A)
126 Diffusion Time=50 Temperature=900 Wet02
127 Comment Wet 02 turned off after soak.
128 Comment Pull the wafers out at 900C.
APPENDIX 3.  CCD/FEA PROCESS SIMULATIONS

3.  CCD/FEA PROCESS SIMULATIONS

130  Print  Layers Electrical
131  Extract  Name=KOX Thickness Layer=2
132  Assign  Name=KOX N.Value=NINT(10000*@KOX)
133  $
134  Comment  Threshold implant (blanket; through Kooi oxide).
135  Implant  Boron Energy=35 Dose=2E12
136  Print  Layers Electrical
137  $
138  Comment  Pattern buried channel (protect n-well, enh. n-MOS) - M4.
139  Deposition  Photoresist Thickness=1.2
140  $
141  Comment  Buried channel implant (through Kooi oxide)
142  Implant  Phosphorous Energy=150 Dose=2.5E12
143  Print  Layers Electrical
144  $
145  Comment  Strip resist.
146  Etch  Photoresist all
147  $
148  Comment  Etchback oxide over gate areas (strip Kooi oxide).
149  Etch  Oxide Thickness=0.0993
150  $
151  Comment  Grow Gate Oxide (750A).
152  Comment  Stabilize 15min and anneal 30min in N2.
153  Diffusion  Time=15 Temperature=950 Nitrogen
154  Diffusion  Time=125 Temperature=950 DryO2 HCl%=5
155  Diffusion  Time=30 Temperature=950 Nitrogen
156  Comment  Pull the wafers out at 950C.
157  Print  Layers Electrical
158  Extract  Name=GOX Thickness Layer=2
159  Assign  Name=GOX N.Value=NINT(10000*@GOX)
160  $
161  Comment  Deposit Poly1 (~6500A) IMMEDIATELY after gate oxide.
162  Deposition  Polysilicon Thickness=0.65 Temperature=610
163  $
164  Comment  Dope polysilicon (Emulsitone N-250 spin-on source).
165  Diffusion  Time=10 Temperature=950 Nitrogen Phos=5.031E20
166  $
167  Comment  Pattern poly1 gates M5.
168  Comment  Etch in RIE.
169  Etch  Polysilicon all
170  $
171  Comment  Etch polysilicon on backside with RIE.
172  $
173  Comment  Strip resist.
174  $
175  Comment  Etch back gate oxide to 200A
176  Comment  (so Xox under poly1 = Xox under poly2)
177  Etch  Oxide Thickness=0.0550
178  $
179  Comment  First isolation oxidation
180  Comment  (550A so that Gox under poly2 750A)
181  Comment  (Similar to gate oxidation since this will form part
182  Comment  of the gate oxide under poly2.)
183  Comment  Stabilize 15min and anneal 30min in N2.
184  Diffusion  Time=15 Temperature=950 Nitrogen
185  Diffusion  Time=110 Temperature=950 DryO2 HCl%=5
186  Diffusion  Time=30 Temperature=950 Nitrogen
187  Comment  Pull the wafers out at 950C.
188  Print  Layers Electrical
189  Extract  Name=II1XOX Thickness Layer=0@II1XOX
190  Assign  Name=II1XOX N.Value=NINT(100000@II1XOX)
191  $
192  Comment  Deposit Poly2 (~6500A) IMMEDIATELY after first isol. oxide.
193  Deposition  Polysilicon Thickness=0.65 Temperature=610
194  $
195  Comment  Dope polysilicon (Emulsitone N-250 spin-on source)
196  Diffusion  Time=10 Temperature=950 Nitrogen Phos=5.031E20
197  $
198  Comment  Form part of the gate oxide under poly2.
APPENDIX 3. CCD/FEA PROCESS SIMULATIONS

198 Comment Pattern poly2 gates M6.
199 Comment Etch in RIE.
200 Etch Polysilicon all
201 $ 
202 Comment Etch polysilicon on backside with RIE.
203 $ 
204 Comment Strip resist.
205 $ 
206 Comment Second isolation oxidation (-1000A over poly2):
207 Diffusion Time=25 Temperature=900 Wet02
208 Comment Pull the wafers out at 900C.
209 Print Layers Electrical
210 Extract Name=I2XOX Thickness Layer=@LI2XOX
211 Assign Name=I2XOX N.Value=NINT(10000*$I2XOX)
212 $ 
213 Comment Pattern Tips M7
214 Deposition Photoresist Thickness=1.2
215 $ 
216 Comment Etch oxide in RIE to obtain vertical sidewall.
217 Etch Oxide all
218 $ 
219 Comment RIE silicon to a depth of 2um.
220 Etch Silicon Thickness=2.0
221 $ 
222 Comment Strip resist.
223 Etch Photoresist all
224 $ 
226 Deposition Photoresist Thickness=1.2
227 Etch Oxide all
228 $ 
229 Comment p+ S/D implant into bare silicon.
230 Comment BP3 source for implant.
231 Implant Boron Energy=55 Dose=1E15 Name=BP2
232 Print Layers Electrical
233 $ 
234 Comment Strip resist.
235 Etch Photoresist all
236 $ 
238 Comment Etch off SiO2 caps (for non-liftoff process).
239 Comment (Don't remove caps if using lift-off process.
240 Comment Would then need to implant through oxide.)
241 Deposition Photoresist Thickness=1.2
242 Etch Oxide all
243 $ 
244 Comment n+ S/D implant into bare silicon.
245 Implant Phosphorous Energy=35 Dose=1E15
246 Print Layers Electrical
247 $ 
248 Comment Strip resist.
249 Etch Photoresist all
250 $ 
251 Comment Tip sharpening oxidation / Final anneal.
252 Comment See SUPREM4 simulations for optimization.
253 Diffusion Time=75 Temperature=900 Wet02
254 Comment Pull the wafers out at 900C.
255 Print Layers Electrical
256 Extract Name=TSXOX Thickness Layer=@LTSXOX
257 Assign Name=TSXOX N.Value=NINT(10000*$TSXOX)
258 $ 
259 Comment Deposit 1.35um BPSG by LPCVD (Kodak will do this step)
260 Comment (Evaporate 1.35um SiO for lift-off process.)
261 Deposition Oxide Thickness=1.35
262 $ 
263 Comment Reflow BPS3 to planarize FEA region.
264 Diffusion Time=60 Temperature=900 Nitrogen
265 $
Comment | Pattern Contacts (to Poly1, Poly2, & Active)  M10.
Etch | Oxide all
Comment | Strip resist.
Comment | Deposit Metal (sputter aluminum).
Comment | (Evaporate aluminum if using lift-off process.)
Deposition | Aluminum Thickness=0.5
Comment | Sinter.
Comment | Pattern Aperature  M11.
Comment | (For lift-off process, just do HF:glycerine dip.)
Etch | Aluminum all
Etch | Oxide all
Comment | Strip resist.
Comment | Pattern Metal  M12.
Etch | Aluminum all
Comment | Strip resist.
Comment | Deposit passivation
Comment | (Need glycerine in BOE for oxide etch over aluminum.)
Comment | Strip resist.
Comment | Deposit backside aluminum (sputtered)
Layer parameter extraction and plotting statements specific to each cross-section belonging here.
Table A3.1: Lines to Comment-Out for Specific Cross-Sections

<table>
<thead>
<tr>
<th>Cross-Section</th>
<th>Filename</th>
<th>Line Numbers to Comment-Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCCD Gate Overlap</td>
<td>CCDBCP12</td>
<td>40, 85, 90, 98, 139, 146, 169, 200, 217, 220, 227, 242, 261, 267, 273, 279, 280, 285</td>
</tr>
<tr>
<td>BCCD Poly1 Gate</td>
<td>CCDBCGP1</td>
<td>40, 85, 90, 98, 139, 146, 169, 177, 217, 220, 227, 242, 261, 267, 273, 279, 280, 285</td>
</tr>
<tr>
<td>BCCD Poly2 Gate</td>
<td>CCDBCGP2</td>
<td>40, 85, 90, 98, 139, 146, 200, 217, 220, 227, 242, 261, 267, 273, 279, 280, 285</td>
</tr>
<tr>
<td>NMOS Substrate Contact</td>
<td>CCDNCONT</td>
<td>40, 85, 90, 98, 217, 220, 226, 235, 242, 279, 280</td>
</tr>
<tr>
<td>NMOS Field Region</td>
<td>CCDNFIEL</td>
<td>40, 90, 98, 118, 121, 124, 217, 220, 227, 242, 267, 279, 280, 285</td>
</tr>
<tr>
<td>NMOS Poly1 Gate</td>
<td>CCDNGTP1</td>
<td>40, 85, 90, 98, 169, 177, 217, 220, 227, 241, 249, 261, 267, 279, 280</td>
</tr>
<tr>
<td>NMOS Poly2 Gate</td>
<td>CCDNGTP2</td>
<td>40, 85, 90, 98, 200, 217, 220, 227, 241, 249, 261, 267, 279, 280</td>
</tr>
<tr>
<td>NMOS Source/Drain</td>
<td>CCDNSRCE</td>
<td>40, 85, 90, 98, 217, 220, 227, 241, 249, 279, 280</td>
</tr>
<tr>
<td>N-Well</td>
<td>CCDNWELL</td>
<td>39, 47, 85, 217, 220, 227, 242, 279, 280</td>
</tr>
<tr>
<td>PMOS Well Contact</td>
<td>CCDPCONT</td>
<td>39, 47, 85, 217, 220, 227, 241, 249, 279, 280</td>
</tr>
<tr>
<td>PMOS Field Region</td>
<td>CCDPFIEL</td>
<td>39, 47, 118, 121, 124, 217, 220, 227, 242, 267, 279, 280, 285</td>
</tr>
<tr>
<td>PMOS Poly1 Gate</td>
<td>CCDPGTP1</td>
<td>39, 47, 85, 169, 177, 217, 220, 226, 235, 242, 261, 267, 279, 280</td>
</tr>
<tr>
<td>PMOS Poly2 Gate</td>
<td>CCDPGTP2</td>
<td>39, 47, 85, 200, 217, 220, 226, 235, 242, 261, 267, 279, 280</td>
</tr>
<tr>
<td>PMOS Source/Drain</td>
<td>CCDPSRCE</td>
<td>39, 47, 85, 217, 220, 226, 235, 242, 279, 280</td>
</tr>
<tr>
<td>Emitter Tip Peak</td>
<td>CCDTIPPK</td>
<td>39, 47, 85, 217, 220, 227, 241, 249, 267, 285</td>
</tr>
<tr>
<td>Emitter Tip Valley</td>
<td>CCDTIPVL</td>
<td>39, 47, 85, 214, 223, 227, 241, 249, 267, 279, 280, 285</td>
</tr>
</tbody>
</table>
Table A3.2: Layer Numbers for Extract Statements

<table>
<thead>
<tr>
<th>Filename</th>
<th>LI1XOX</th>
<th>LI2XOX</th>
<th>LTSXOX</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCDBCP12</td>
<td>4</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>CCDBCGP1</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>CCDBCGP2</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>CCDNCONT</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>CCDNFIEL</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>CCDNGTP1</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>CCDNGTP2</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>CCDNSRCE</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>CCDN WELL</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>CCDPCONT</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>CCDPFIEL</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>CCDPGTP1</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>CCDPGTP2</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>CCDPSRCE</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>CCDTIPPK</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>CCDTIPVL</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>
Layer parameter extraction and output for CCDBCP12:

Comment
Find the final junction depths etc.
End

Electrical
Steps=1
End

Extract
Name=XJBC Net Active X.Extract Y=0
Assign
Name=XJBC N.Value=.001*NINT(1000*XRJBC)
Extract
Name=RSBC E.Resistivity Layer=1 Min.region=2
Extract
Name=XP1 Thickness Layer=3
Assign
Name=XP1 N.Value=NINT(10000*XP1)
Extract
Name=RS2 E.Resistivity Layer=5
Extract
Name=XP2 Thickness Layer=5
Assign
Name=XP2 N.Value=NINT(10000*XP2)
$
Comment
Final output.
Print
Layers
Plot
Net Active Device=POSTSCRIPT Plot.out=CCDBCP12.pps
+ Title="CCD/FEA BCCD Gate Overlap"
Plot
Active Boron color=1 line=2 add
Plot
Active Phosphorous color=3 line=3 add
Comment
Label
Label="Alignment Xox: "&AXOX"A"
+ x=0.45
Label
Label="Pad Xox: "&POX"A"
Label
Label="Koo Xox: "&KOX"A"
Label
Label="Gate Xox: "&GOX"A"
Label
Label="Poly1 Thickness: "&XP1"A"
Label
Label="Poly1 Rs: "&RSP1" ohms/sq"
Label
Label="Poly1-Poly2 Xox: "&I1XOX"A"
Label
Label="Poly2 Thickness: "&XP2"A"
Label
Label="Poly2 Rs: "&RSP2" ohms/sq"
Label
Label="2nd Isolation Xox: "&I2XOX"A"
Label
Label="Xox After Tip Sharp: "&TSXOX"A"
Label
Label="Buried Channel Xj: "&XJBC" um"
Label
Label="Buried Channel Rs: "&RSBC" ohm/sq"
Label
Label=""
Label
Label="Net Active" Start.Ri Lx.Finish=1.45 Line.Typ=1
+ Color=1
Label
Label="Boron Active" Start.Ri Lx.Finish=1.45 Line.Typ=2
+ Color=2
Label
+ Color=3
Label
Label="Oxide" x=-1.0 y=3E17 Angle=90
Label
Label="Poly-Si" x=-.56 y=3E17 Angle=90
Label
Label="Oxide" x=-.28 y=3E17 Angle=90
Label
Label="Poly-Si" x=.10 y=3E17 Angle=90
Label
Label="Silicon" x=.50 y=3E17 Angle=90
Layer parameter extraction and output for CCDBCGP1:

Comment: Find the final junction depths etc.

Electrical Steps=1
End
Extract Name=XJBC Net Active X.Extract Y=0
Extract Name=RSBC Resistivity Layer=1 Min.region=2
Extract Name=RSP1 Resistivity Layer=3 Min.region=1
Extract Name=XP1 Thickness Layer=3
Assign Name=XP1 N.Value=NINT(10000*XP1)
Extract Name=NDSURF Net Active X=0 Y.Extract Layer=1
Extract Name=NABULK Net Active X=2.5 Y.Extract Layer=1
Extract Name=NDOSE Net Active X.Min=0 X.Max=XJBC Integral
Assign Name=XJBC N.Value=.001*NINT(1000*XJBC)
Assign Name=NABULK N.Value=ABS(NABULK)
Electrical Steps=21 Vth.Elect Layer=1 Min.region=2
Qss Concentration=5E10 Layer=1
Bias Layer=3 V=-5 DV=.5 Abscissa
End
Electrical Extract Name=THRESH V.thresh $ Comment: Final output.
Print Layers Plot Net Active Device=POSTSCRIPT Plot.out=CCDBCGP1.PS + Right=2.5 X.Absolute + Title="CCD/FEA BCCD Gate w/ Polyl"
Plot Active Boron color=2 line=2 add
Plot Active Phosphorous color=3 line=3 add
Comment Label the plot with the junction depths etc.
Label Label="Alignment Xox: " &AXOX*A"
x=0.6
Label Label="Pad Xox: " &POX*A"
Label Label="Kooi Xox: " &KOX*A"
Label Label="Gate Xox: " &GOX*A"
Label Label="1st Isolation Xox: " &I1XOX*A"
Label Label="2nd Isolation Xox: " &I2XOX*A"
Label Label="Xox After Tip Sharp.: " &TSXOX*A"
Label Label="Buried Channel Xj: " &XJBC* um"
Label Label="Buried Channel Rs: " &RSBC* ohms/sq"
Label Label="Poly1 Thickness: " &XP1*A"
Label Label="Poly1 Rs: " &RSP1* ohms/sq"
Label Label="Surface Donor Conc.: " &NDSURF* /cm^3"
Label Label="Bulk Acceptor Conc.: " &NABULK* /cm^3"
Label Label="Buried Channel Int. " &NDOSE
Label Label="Threshold Voltage: " &THRESH* V"
Label Label=""
Label Label="Net Active" Start.Ri LX.Finish=1.5 Line.Typ=1 + Color=1
Label Label="Boron Active" Start.Ri LX.Finish=1.5 Line.Typ=2 + Color=2
Label Label="Phos. Active" Start.Ri LX.Finish=1.5 Line.Typ=3 + Color=3
Label Label="Oxide" x=-.3 y=3E17 Angle=90
Label Label="Oxide" x=.40 y=3E17 Angle=90
Label Label="Poly-Si" x=.15 y=3E17 Angle=90
Label Label="Silicon" x=.50 y=3E17 Angle=90
Layer parameter extraction and output for CCDBCGP2:

Comment  Find the final junction depths etc.
Electrical  Steps=1
End
Extract  Name=XJBC Net Active X.Extract Y=0
Extract  Name=RSBC E.Resistivity Layer=1 Min.region=2
Extract  Name=RSP2 E.Resistivity Layer=3 Min.region=1
Assign  Name=XP2 Thickness Layer=3
Extract  Name=MDOSURF Net Active X=0 Y.Extract Layer=1
Extract  Name=NABULK Net Active X=2.5 Y.Extract Layer=1
Assign  Name=NABULK N.Value=N.INT(10000*XP2)
Assign  Name=NINT N.VALUE=N.INT(1000*XJBC)
Assign  Name=NABULK N.VALUE=ABS(NABULK)
Electrical  Steps=21 Vth.Elect Layer=1 Min.region=2
Qss  Concentration=5E10 Layer=1
Bias  Layer=3 V=-5 DV=.5 Abscissa
End
Extract  Name=THRESH Vthresh
$Comment  Final output.
Print  Layers
Plot  Net Active Device=POSTSCRIPT Plt.out=CCDBCGP2.PS
+  Right=2.5 X.Absolute
+  Title="CCD/FEA BCCD Poly2 Gate"
Plot  Active Boron color=2 line=2 add
Plot  Active Phosphorous color=3 line=3 add
Comment  Label the plot with the junction depths etc.
Label  Label="Alignment Xox: 
Label  Label="Expand Xox: 
Label  Label="Kooi Xox: 
Label  Label="Gate Xox: 
Label  Label="Isolation Xox: 
Label  Label="Xox After Tip Sharp: 
Label  Label="Buried Channel Xj: 
Label  Label="Buried Channel Rs: 
Label  Label="Poly2 Thickness: 
Label  Label="Poly2 Rs: 
Label  Label="Surface Donor Conc. 
Label  Label="Bulk Acceptor Conc. 
Label  Label="Buried Channel Int. : 
Label  Label="Threshold Voltage: 
Label  Label="Net Active" Start.Ri Lx.Finish=1.6 Line.Type=1
+  Color=1
Label  Label="Boron Active" Start.Ri Lx.Finish=1.6 Line.Type=2
+  Color=2
Label  Label="Phos. Active" Start.Ri Lx.Finish=1.6 Line.Type=3
+  Color=3
Label  Label="Oxide" X=-.27 Y=3E17 Angle=90
Label  Label="Oxide" X=.43 Y=3E17 Angle=90
Label  Label="Poly-Si" Y=.15 Y=3E17 Angle=90
Label  Label="Silicon" X=.53 Y=3E17 Angle=90
Layer parameter extraction and output for CCDNCONT:

Comment  Find the final junction depths etc.
Electrical  Steps=1
End        Electrical
Extract    Name=XJHL Net Active X.Extract Y=-3E15
Extract    Name=RSC H.Resistivity Layer=1 Min.region=1
Assign     Name=NASURF Net Active X=0 Y.Extract Layer=1
$          Print
Comment    Final output.
Plot       Net Active Device=POSTSCRIPT Plot.out=CCDNCONT.PS
+          Title="CCD/FEA NMOS Substrate Contact"
Plot       Active Boron color=2 line=2 add
Plot       Active Phosphorous color=3 line=3 add
Comment    Label the plot with the junction depths etc.
Label      Label="Alignment Xox: 
+          X=1.6"
Label      Label="Pad Xox: 
Label      Label="Kooi Xox: 
Label      Label="Gate Xox: 
Label      Label="1st Isolation Xox: 
Label      Label="2nd Isolation Xox: 
Label      Label="Xox After Tip Sharp: 
Label      Label="High-Low Xj: 
Label      Label="P+ region Rs: 
Label      Label="Surface Acct. Conc.. 
Label      Label="Net Active" Start.Ri Lx.Finish=4.0 Line.Typ=1
+          Color=1
Label      Label="Boron Active" Start.Ri Lx.Finish=4.0 Line.Typ=2
+          Color=2
Label      Label="Phos. Active" Start.Ri Lx.Finish=4.0 Line.Typ=3
+          Color=3
Label      Label="Silicon" x=0.7 y=3E17 Angle=90
Layer parameter extraction and output for CCDNFIEL:

Comment Find the final junction depths etc.
Extract Name=NASURF Net Active X=0 Y.Extract Layer=1
Assign Name=NASURF N.Value=ABS($NASURF)
Electrical Steps=21 Vth.Elect Layer=1
Bias Layer=3 V=10 DV=5 Abscissa
End Electrical
Extract Name=THRESH V.thresh
$
Comment Final output.
Print Layers Electrical
Plot Net Active Device=POSTSCRIPT Plot.out=CCDNFIEL.PS
+ Right=5.0 X.Absolute
+ Title="CCD/FEA NMOS Field Region"
Plot Active Boron color=2 line=2 add
Plot Active Phosphorous color=3 line=3 add
Comment Label the plot with the junction depths etc.
Label Label="Alignment Xox: " &AXOX"A"
+ x=1.0
Label Label="Pad Xox: " &POX"A"
Label Label="Field Xox: " &FOX"A"
Label Label="Kooi Xox: " &KOX"A"
Label Label="Gate Xox: " &GOX"A"
Label Label="1st Isolation Xox: " &I1X0X"A"
Label Label="2nd Isolation Xox: " &I2X0X"A"
Label Label="Xox After Tip Sharp: " &TSXOX"A"
Label Label="Surface Accpt. Conc.: " &NASURF" cm^-3"
Label Label="Threshold Voltage: " &THRESH" V"
Label Label="*
Label Label="Net Active" Start.Ri Lx.Finish=4.0 Line.Type=1
+ Color=1
Label Label="Boron Active" Start.Ri Lx.Finish=4.0 Line.Type=2
+ Color=2
Label Label="Phos. Active" Start.Ri Lx.Finish=4.0 Line.Type=3
+ Color=3
Label Label="Aluminum" x=-1.8 y=3E17 Angle=90
Label Label="Oxide" x=-.35 y=3E17 Angle=90
Label Label="Silicon" x=1.0 y=3E17 Angle=90
APPENDIX 3. CCD/FEA PROCESS SIMULATIONS

Layer parameter extraction and output for CCDNGTP1:

Comment Find the final junction depths etc.
Electrical Steps=1
End
Extract Name=RSPI E.Resistivity Layer=3 Min.region=1
Extract Name=XPI Thickness Layer=3
Assign Name=XPI N.Value=NINT(10000*XP1
Extract Name=NASURF Net Active X=0 Y.Extract Layer=1
Assign Name=NASURF N.Value=ABS(&NASURF)
Electrical Steps=21 Vth.Elect Layer=1
Qss Concentration=5E10 Layer=1
Bias Layer=3 V=0 DV=.5 Abcissa
End
Extract Name=THRESH V.thresh
$
Comment Final output.
Print Layers
Plot Net Active Device=POSTSCRIPT Plot.out=CCDNGTP1.PS
+ Right=2.5 X.Absolute
+ Title="CCD/FEA NMOS Poly1 Gate"
Plot Active Boron color=2 line=2 add
Plot Active Phosphorous color=3 line=3 add
Comment Label the plot with the junction depths etc.
Label Label="Alignment Xox: "&AXOX"A"
+ x=0.5
Label Label="Pad Xox: "&POX"A"
Label Label="Kooi Xox: "&KOX"A"
Label Label="Gate Xox: "&GOK"A"
Label Label="Poly1-Poly2 Xox: "&I1KOX"A"
Label Label="2nd Isolation Xox: "&I2KOX"A"
Label Label="Xox After Tip Sharp: "&TS1XOX"A"
Label Label="Poly1 Thickness: "&XP1"A"
Label Label="Poly1 Rs: "&RSP1" ohms/sq"
Label Label="Surface Acpt. Conc. "&NASURF" /cm^3"
Label Label="Threshold Voltage: "&THRESH" V"
Label Label=" "
Label Label="Net Active" Start.Ri Lx.Finish=1.5 Line.Typ=1
+ Color=1
Label Label="Boron Active" Start.Ri Lx.Finish=1.5 Line.Typ=2
+ Color=2
Label Label="Phos. Active" Start.Ri Lx.Finish=1.5 Line.Typ=3
+ Color=3
Label Label="Oxide" x=-.25 y=3E17 Angle=90
Label Label="Oxide" x=.40 y=3E17 Angle=90
Label Label="Poly-Si" x=.15 y=3E17 Angle=90
Label Label="Silicon" x=.50 y=3E17 Angle=90
Layer parameter extraction and output for CCDNGTP2:

Comment Find the final junction depths etc.
Electrical Steps=1
End
Extract Name=RSP2 E.Resistivity Layer=3 Min.region=1
Extract Name=XP2 Thickness Layer=3
Assign Name=XP2 M.Value=NINT(10000*&XP2)
Extract Name=NASURF Net Active X=0 Y.Extract Layer=1
Assign Name=NASURF N.Value=ABS(&NASURF)
Electrical Steps=21 Vth.Elect Layer=1
Qss Concentration=5E10 Layer=1
Bias Layer=3 V=0 DV=.5 Abscissa
End
Extract Name=THRESH V.thresh
$
\$
Comment Final output.
Print Layers
Plot Net Active Device=POSTSCRIPT Plot.out=CCDNGTP2.PS
+ Right=2.5 X.Absolute
+ Title="CCD/FEA NMOS Poly2 Gate"
Plot Active Boron color=2 line=2 add
Plot Active Phosphorous color=3 line=3 add
Comment Label the plot with the junction depths etc.
Label Label=*Alignment Xox: "&AXOX"A"
+ x=0.5
Label Label=*Pad Xox: "&POX"A"
Label Label=Kooi Xox: "&KOY"A"
Label Label=*Gate Xox: "&K1XOX"A"
Label Label=*2nd Isolation Xox: "&I2XOX"A"
Label Label=Xox After Tip Sharp.: "&TSXOX"A"
Label Label=*Poly2 Thickness: "&XP2"A"
Label Label=*Poly2 Rs: "&RSP" ohms/sq"
Label Label="Surface Acpt. Conc.: &NASURF/cm^3"
Label Label="Threshold Voltage: &THRESH V"
Label Label=""
Label Label="Net Active" Start.Ri Lx.Finish=1.5 Line.Typ=1
+ Color=1
Label Label="Boron Active" Start.Ri Lx.Finish=1.5 Line.Typ=2
+ Color=2
Label Label="Phos. Active" Start.Ri Lx.Finish=1.5 Line.Typ=3
+ Color=3
Label Label="Oxide" x=-.25 y=3E17 Angle=90
Label Label="Oxide" x=.43 y=3E17 Angle=90
Label Label="Poly-Si" x=.15 y=3E17 Angle=90
Label Label="Silicon" x=.53 y=3E17 Angle=90
Layer parameter extraction and output for CCDNSRCE:

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<tr>
<td>Electrical</td>
<td></td>
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<tr>
<td>Extract Name=XJSD Net Active X.Extract Y=0</td>
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<tr>
<td>Extract Name=RSSD E.Resistivity Layer=1 Min.region=2</td>
<td></td>
</tr>
<tr>
<td>Extract Name=NDSURF Net Active X=0 Y.Extract Layer=1</td>
<td></td>
</tr>
</tbody>
</table>

$\begin{align*}
\text{Comment} & \quad \text{Final output.} \\
\text{Print Layers} & \\
\text{Plot Net Active Device=POSTSCRIPT Plot.out=CCDNSRCE.PS} \\
\text{+ Right=5.0 X.Absolute} \\
\text{+ Title="CCD/FEA - NMOS Source/Drain"} \\
\text{Plot Active Boron color=2 line=2 add} \\
\text{Plot Active Phosphorous color=3 line=3 add} \\
\text{Comment Label the plot with the junction depths etc.} \\
\text{Label Label="Alignment Xox: \"&AXOX\"A\"} \\
\text{+ X=1.6} \\
\text{Label Label="Pad Xox: \"&POX\"A\"} \\
\text{Label Label="Kooi Xox: \"&KOX\"A\"} \\
\text{Label Label="Gate Xox: \"&GOX\"A\"} \\
\text{Label Label=\"1st Isolation Xox: \"&I1XOX\"A\"} \\
\text{Label Label=\"2nd Isolation Xox: \"&I2XOX\"A\"} \\
\text{Label Label=\"Xox After Tip Sharp: \"&TSXOX\"A\"} \\
\text{Label Label=\"Source/Drain Xj: \"&XJSD\" um\"} \\
\text{Label Label=\"Source/Drain Rs: \"&RSSD\" ohms/sq\"} \\
\text{Label Label=\"Surface Donor Conc. \"&NDSURF\" /cm^3\"} \\
\text{Label Label=\"Net Active" Start.Ri Lx.Finish=4.0 Line.Typ=1} \\
\text{+ Color=1} \\
\text{Label Label="Boron Active" Start.Ri Lx.Finish=4.0 Line.Typ=2} \\
\text{+ Color=2} \\
\text{Label Label="Phos. Active" Start.Ri Lx.Finish=4.0 Line.Typ=3} \\
\text{+ Color=3} \\
\text{Label Label="Silicon" x=.80 y=3E17 Angle=90} 
\end{align*}$
Layer parameter extraction and output for CCDNWELL:

Comment Find the final junction depths etc.
Electrical Steps=1
End
Extract Name=XJW Net Active X.Extract Y=0
Extract Name=RSW E.Resistivity Layer=1 Min.region=2
Extract Name=NDSURF Net Active X=0 Y.Extract Layer=1
$ Comment Final output.
Print Layers
Plot Net Active Device=POSTSCRIPT Plot.out=CCDNWELL.PS
  + Right=7.5 X.Absolute
  + Title="CCD/FEA N-Well"
Plot Active Boron color=2 line=2 add
Plot Active Phosphorous color=3 line=3 add
Comment Label the plot with the junction depths etc.
Label Label="Alignment Xox: " &AXOX"A"
  + x=2.0
Label Label="Pad Xox: " &POX"A"
Label Label="Kooi Xox: " &K0X"A"
Label Label="Gate Xox: " &G0X"A"
Label Label="1st Isolation Xox: " &I1X0X"A"
Label Label="2nd Isolation Xox: " &I2X0X"A"
Label Label="Xox After Tip Sharp. " &TSXOX"A"
Label Label="Well Xj: " &XJW" um"
Label Label="Well Rs: " &RSW" ohms/sq"
Label Label="Surface Donor Conc.: " &NDSURF" /cm^3"
Label Label="*"
Label Label="Net Active' Start.Ri Lx.Finish=5 Line.Typ=1
  + Color=1
Label Label="Boron Active' Start.Ri Lx.Finish=5 Line.Typ=2
  + Color=2
Label Label="Phos. Active' Start.Ri Lx.Finish=5 Line.Typ=3
  + Color=3
Label Label="Silicon" x=.90  y=3E17 Angle=90
Layer parameter extraction and output for CCDPCONT:

Comment       Find the final junction depths etc.
Electrical     Steps=1
End            Electrical
Extract        Name=XJHL Net Active X. Extract Y=1.3E16
Extract        Name=XJW Net Active X. Extract Y=0
Extract        Name=RSW E.Resistivity Layer=1 Min.region=0
Extract        Name=NDSURF Net Active X=0 Y.Extract Layer=1
$
Comment       Final output.
Print          Layers
Plot           Net Active Device=POSTSCRIPT Plot.out=CCDPCONT.PS
               + Right=7.5 X.Absolute
               + Title="CCD/FEA PMOS N-Well Contact"
Plot           Active Boron color=2 line=1 add
Plot           Active Phosphorous color=3 line=3 add
Comment       Label the plot with the junction depths etc.
Label          Label="Alignment Xox: "&AXOX"A"
               + x=2.0
Label          Label="Pad Xox: "&POX"A"
Label          Label="Kooi Xox: "&KOX"A"
Label          Label="Gate Xox: "&GOX"A"
Label          Label="1st Isolation Xox: "&I1XOX"A"
Label          Label="2nd Isolation Xox: "&I2XOX"A"
Label          Label="Xox After Tip Sharp. "&TSXOX"A"
Label          Label="High-Low Xj: "&XJHL" um"
Label          Label="Well Xj: "&XJW" um"
Label          Label="Well w/ contact Rs: "&RSW" ohms/sq"
Label          Label="Surface Donor Conc.: "&NDSURF" /cm^{-3}"
Label          Label=""
Label          Label="Net Active" Start.Ri Lx.Finish=5 Line.Typ=1
               + Color=1
Label          Label="Boron Active" Start.Ri Lx.Finish=5 Line.Typ=2
               + Color=2
               + Color=3
Label          Label="Silicon" x=0.90 y=3E17 Angle=90
APPENDIX 3.  CCD/FEA PROCESS SIMULATIONS

Layer parameter extraction and output for CCDPFIEL:

Comment Find the final junction depths etc.
Extract Name=NDSURF Net Active X=0 Y.Extract Layer=1
Electrical Steps=21 Vth.Hole Layer=1 Min.region=2
Qss Concentration=5E10 Layer=1
Bias Layer=3 V=-50 DV=-10 Abscissa
End Extract Name=THRESH V.thresh Extract Name=XJW Net Active X.Extract Y=0
$ Comment Final output.
Print Layers Electrical
Plot Net Active Device=POSTSCRIPT Plot.out=CCDPFIEL.PS
+ Right=7.5 X.Absolute
+ Title="CCD/FEA PMOS Field Region"
Plot Active Boron color=2 line=2 add
Plot Active Phosphorous color=3 line=3 add
Comment Label the plot with the junction depths etc.
Label Label="Alignment Xox: "&AXOX"A"
  x=1.5
Label Label="Pad Xox: "&POX"A"
Label Label="Field Xox: "&FOX"A"
Label Label="Kooi Xox: "&KOX"A"
Label Label="Gate Xox: "&GOX"A"
Label Label="1st Isolation Xox: "&I1XOX"A"
Label Label="2nd Isolation Xox: "&I2XOX"A"
Label Label="Xox After Tip Sharp. "&TSXOX"A"
Label Label="Well Xj: "&XJW" um"
Label Label="Surface Donor Conc.: "&NDSURF" /cm^3"
Label Label="Threshold Voltage: "&THRESH" V"
Label Label=" "
Label Label="Net Active" Start.Ri Lx.Finish=4.5 Line.Typ=1
  Color=1
Label Label="Boron Active" Start.Ri Lx.Finish=4.5 Line.Typ=2
  Color=2
  Color=3
Label Label="Aluminum" x=-1.7 y=3E17 Angle=90
Label Label="Oxide" x=-.3 y=3E17 Angle=90
Label Label="Silicon" x=1.2 y=3E17 Angle=90
APPENDIX 3. CCD/FEA PROCESS SIMULATIONS

Layer parameter extraction and output for CCDPGTP1:

Comment Find the final junction depths etc.
End
Extract Name=XJW Net Active X.Extract Y=0
Extract Name=RSPl E.Resistivity Layer=3
Extract Name=XP1 Thickness Layer=3
Assign Name=XP1 N.Value=NINT(10000*XP1)
Extract Name=NDSURF Net Active X=0 Y.Extract Layer=1
Electrical Steps=21 Vth.Hole Layer=1 Min.region=2
Qss Concentration=5E10 Layer=1
Bias Layer=3 V=0 DV=-1 Abscissa
End
Extract Name=THRESH V.thresh
$Comment Final output.
Print Layers
Plot Net Active Device=POSTSCRIPT Plot.out=CCDPGTPl.PS
+ Right=7.5 X.Absolute
+ Title="CCD/FEA PMOS Poly1 Gate"
Plot Active Boron color=2 line=2 add
Plot Active Phosphorous color=3 line=3 add
Comment Label the plot with the junction depths etc.
Label Label="Alignment Xox: "&AXOXA"
+ x=1.0
Label Label="Pad Xox: "&POX"A"
Label Label="Kool Xox: "&KOX"A"
Label Label="Gate Xox: "&GOX"A"
Label Label="Poly1-Poly2 Xox: "&I1OX"A"
Label Label="2nd Isolation Xox: "&I2OX"A"
Label Label="Xox After Tip Sharp. "&TSOX"A"
Label Label="Poly1 Thickness: "&XP1"A"
Label Label="Poly1 Rs: "&RSPl" ohms/sq"
Label Label="Well Xj: "&XJWX&um"
Label Label="Surface Donor Conc.: "&NDSURF" /cm^3"
Label Label="Threshold Voltage: "&THRESH" V"
Label Label=""
Label Label="Net Active" Start.Ri Lx.Finish=4.0 Line.Typ=1
+ Color=1
Label Label="Boron Active" Start.Ri Lx.Finish=4.0 Line.Typ=2
+ Color=2
Label Label="Phos. Active" Start.Ri Lx.Finish=4.0 Line.Typ=3
+ Color=3
Label Label="Oxide" x=-.15 y=3E17 Angle=90
Label Label="Poly-Si" x=.20 y=3E17 Angle=90
Label Label="Oxide" x=.50 y=3E17 Angle=90
Label Label="Silicon" x=0.75 y=3E17 Angle=90
Layer parameter extraction and output for CCDPGTP2:

Comment
Find the final junction depths etc.

Electrical
Steps=1

End

Electrical

Extract
Name=XJW Net Active X. Extract Y=0

Extract
Name=RSP2 E.Resistivity Layer=3

Assign
Name=XP2 N.Value=NINT(10000*XP2)

Extract
Name=NDSURF Net Active X=0 Y.Extract Layer=1

Electrical
Steps=21 Vth.Hole Layer=1 Min.region=2

Qss
Concentration=5E10 Layer=1

Bias
Layer=3 V=0 DV=-1 Abscissa

End

Electrical

Extract
Name=THRESH V.threshold

$ Comment
Final output.

Print
Layers

Plot
Net Active Device=POSTSCRIPT Plot.out=CCDPGTP2.PS

+ Title="CCD/FEA PMOS Poly2 Gate"

Plot
Active Boron color=2 line=2 add

Plot
Active Phosphorous color=3 line=3 add

Comment
Label the plot with the junction depths etc.

Label
Label= "Alignment Xox: " &AXOX"A"

+ x=1.0

Label
Label= "Pad Xox: " &POX"A"

Label
Label= "Kooi Xox: " &KOX"A"

Label
Label= "Gate Xox: " &I1XOX"A"

Label
Label= "2nd Isolation Xox: " &I2XOX"A"

Label
Label= "Xox After Tip Sharp. " &TSXOX"A"

Label
Label= "Poly2 Thickness: " &XP2"A"

Label
Label= "Poly2 Rs: " &RSP2" ohms/sq"

Label
Label= "Well Xj: " &XJW" um"

Label
Label= "Surface Donor Conc.: " &NDSURF" /cm^3"

Label
Label= "Threshold Voltage: " &THRESH" V"

Label
Label= "Net Active" Start.Ri Lx.Finish=4.0 Line.Typ=1

+ Color=1

Label
Label= "Boron Active" Start.Ri Lx.Finish=4.0 Line.Typ=2

+ Color=2

Label
Label= "Phos. Active" Start.Ri Lx.Finish=4.0 Line.Typ=3

+ Color=3

Label
Label= "Oxide" x=-.15 y=3E17 Angle=90

Label
Label= "Poly-Si" x=.20 y=3E17 Angle=90

Label
Label= "Oxide" x=.50 y=3E17 Angle=90

Label
Label= "Silicon" x=.75 y=3E17 Angle=90
APPENDIX 3. CCD/FEA PROCESS SIMULATIONS

Layer parameter extraction and output for CCDPSRCE:

Comment Find the final junction depths etc.
Electrical Steps=1
End
Extract Name=XJSD Net Active X.Extract Y=0
Extract Name=XJW Net Active X.Extract Y=0 X.Min=&XJSD+.05
Extract Name=RSSD H.Resistivity Layer=1 Min.region=3
Extract Name=NASURF Net Active X=0 Y.Extract Layer=1
Assign Name=NASURF N.Value=ABS(&NASURF)
$ Comment Final output.
Print Layers
Plot Net Active Device=POSTSCRIPT Plot.out=CCDPSRCE.PS
+ Right=7.5 X.Absolute
+ Title="CCD/FEA PMOS Source/Drain"
Plot Active Boron color=2 line=2 add
Plot Active Phosphorous color=3 line=3 add
Comment Label the plot with the junction depths etc.
Label Label="Alignment Xox: " &AXOX"A"
Label Label="Pad Xox: " &POX"A"
Label Label="Kooi Xox: " &KOX"A"
Label Label="Gate Xox: " &GOX"A"
Label Label="1st Isolation Xox: " &I1XOX"A"
Label Label="2nd Isolation Xox: " &I2XOX"A"
Label Label="Xox After Tip Sharp: " &TSXOX"A"
Label Label="Source/Drain Xj: " &XJSD" um"
Label Label="Source/Drain Rs: " &RSSD" ohms/sq"
Label Label="Surface Accpt. Conc.: " &NASURF" /cm^3"
Label Label="Well Xj: " &XJW" um"
Label Label=" "
Label Label="Net Active" Start.Ri Lx.Finish=5.0 Line.Typ=1
+ Color=1
Label Label="Boron Active" Start.Ri Lx.Finish=5.0 Line.Typ=2
+ Color=2
Label Label="Phos. Active" Start.Ri Lx.Finish=5.0 Line.Typ=3
+ Color=3
Label Label="Silicon" x=.8 y=3E17 Angle=90
Layer parameter extraction and output for CCDTIPPK:

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<td>Name=RSW E.Resistivity Layer=1 Min.region=2</td>
<td>Name=NDSURF Net Active X=0 Y.Extract Layer=1</td>
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<td>$\text{Comment}$</td>
<td>$\text{Print}$</td>
<td>$\text{Plot}$</td>
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<td>$\text{Final output.}$</td>
<td>$\text{Layers}$</td>
<td>$\text{Title=CCC/FEA Emitter Tip Peak}$</td>
<td>$\text{Active Phosphorous color=3 line=3 add}$</td>
</tr>
<tr>
<td></td>
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<td>$\text{Plot}$</td>
<td>$\text{Plot}$</td>
<td>$\text{Comment}$</td>
<td>$\text{Label}$</td>
</tr>
</tbody>
</table>
|         |            | $\text{Net Active Device=POSTSCRIPT Plot.out=CCDTIPPK.PS}$ | $\text{Active Boron color=2 line=2 add}$ | $\text{Label the plot with the junction depths etc.}$ | $\text{Label}=$
|         |            | $+$ | $+$ | $+$ | $+$ |
|         |            | $\text{Boron Active Start. Ri Lx.Finish=5 Line.Typ=2}$ | $\text{Phos. Active Start. Ri Lx.Finish=5 Line.Typ=3}$ | $\text{Silicon x=.90 y=3E17 Angle=90}$ | $\text{Silicon}$ |
|         |            | $\text{Silicon}$ | $\text{Silicon}$ | $\text{Silicon}$ | $\text{Silicon}$ |
|         |            | $\text{Silicon}$ | $\text{Silicon}$ | $\text{Silicon}$ | $\text{Silicon}$ |
|         |            | $\text{Silicon}$ | $\text{Silicon}$ | $\text{Silicon}$ | $\text{Silicon}$ |
|         |            | $\text{Silicon}$ | $\text{Silicon}$ | $\text{Silicon}$ | $\text{Silicon}$ |
Layer parameter extraction and output for CCDTIPVL:

Comment       Find the final junction depths etc.
Electrical     Steps=1
End            Electrical
Extract        Name=XJHL Net Active X. Extract Y=8E15
Extract        Name=XJW Net Active X. Extract Y=0
Extract        Name=RSW E. Resistivity Layer=1 Min. region=2
Extract        Name=NDSURF Net Active X=0 Y. Extract Layer=1
$              
Comment        Final output.
Print          Layers
Plot           Net Active Device=POSTSCRIPT Plot.out=CCDTIPVL..PS
              + Right=7.5 X. Absolute
              + Title="CCD/FEA - Emitter Tip Valley"
Plot           Active Boron color=2 line=2 add
Plot           Active Phosphorous color=3 line=3 add
Comment        Label the plot with the junction depths etc.
Label          Label="Alignment Xox": "@AXOX"A"
              + x=3.0
Label          Label="Pad Xox": "@POX"A"
Label          Label="Kooi Xox": "@KOX"A"
Label          Label="Gate Xox": "@GOX"A"
Label          Label="1st Isolation Xox": "@I1XOX"A"
Label          Label="2nd Isolation Xox": "@I2XOX"A"
Label          Label="Xox After Tip Sharp": "@TSXOX"A"
Label          Label="High-Low Xj": "@XJHL" um"
Label          Label="Well Xj": "@XJW" um"
Label          Label="Well w/ contact Rs": "@RSW" ohms/sq"
Label          Label="Surface Donor Conc.": "@NDSURF" /cm^3"
Label          Label=""
Label          Label="Net Active" Start.Ri Lx.Finish=6 Line.Typ=1
              + Color=1
Label          Label="Boron Active" Start.Ri Lx.Finish=6 Line.Typ=2
              + Color=2
              + Color=3
Label          Label="Aluminum" x=.80 y=3E17 Angle=90
Label          Label="BPSG" x=1.90 y=3E17 Angle=90
Label          Label="Silicon" x=2.85 y=3E17 Angle=90
SUPREM-3 Final Results:

Figure A3.1: CCD/FEA - BCCD Gate Overlap
Figure A3.2: CCD/FEA - BCCD Gate w/ Poly1

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
1st Isolation Xox: 630A
2nd Isolation Xox: 1512A
Xox After Tip Sharp.: 3553A
Buried Channel Xj: 0.461 um
Buried Channel Rs: 5686.7 ohms/sq
Poly1 Thickness: 4937A
Poly1 Rs: 52.795 ohms/sq
Surface Donor Conc.: 7.38969E+16 /cm^3
Bulk Acceptor Conc.: 2.63504E+15 /cm^3
Buried Channel Int.: 1.51785E+12
Threshold Voltage: -5.6881 V

Net Active——
Boron Active-----
Phos. Active————
Figure A3.3: CCD/FEA - BCCD Poly2 Gate

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
2nd Isolation Xox: 1116A
Xox After Tip Sharp.: 3404A
Buried Channel Xj: 0.509 um
Buried Channel Rs: 5022.7 ohms/sq
Poly2 Thickness: 5002A
Poly2 Rs: 44.651 ohms/sq
Surface Donor Conc.: 7.97106E+16 /cm^3
Bulk Acceptor Conc.: 2.63603E+15 /cm^3
Buried Channel Int.: 1.64401E+12
Threshold Voltage: -6.2411 V

Net Active
Boron Active
Phos. Active
Figure A3.4: CCD/FEA - NMOS Substrate Contact

Alignment Xox: 6289A
Pad Xox: 580A
Koon Xox: 993A
Gate Xox: 750A
1st Isolation Xox: 750A
2nd Isolation Xox: 1210A
Xox After Tip Sharp.: 1449A
High-Low Xj: 1.0227 um
p+ region Rs: 252 ohms/sq
Surface Acceptor Conc.: 2.60558E+18 /cm^3

Net Active
Boron Active
Phos. Active
Figure A3.5: CCD/FEA - NMOS Field Region

Alignment Xox: 6289A
Pad Xox: 580A
Field Xox: 9643A
Kooi Xox: 10038A
Gate Xox: 9159A
1st Isolation Xox: 8713A
2nd Isolation Xox: 8925A
Xox After Tip Sharp.: 9541A
Surface Acceptor Conc.: 9.11076E+15/cm³
Threshold Voltage: 41.199 V

Net Active
Boron Active
Phos. Active

Distance (Microns)

-2.00 -1.00 0.00 1.00 2.00 3.00 4.00 5.00

Surface Accept.
Cone.
Figure A3.6: CCD/F EA - NMOS Polyl Gate

- Alignment Xox: 6289A
- Pad Xox: 580A
- Kooi Xox: 993A
- Gate Xox: 750A
- Polyl-Poly2 Xox: 630A
- 2nd Isolation Xox: 1512A
- Xox After Tip Sharp.: 2982A
- Polyl Thickness: 4523A
- Polyl Rs: 36.421 ohms/sq
- Surface Acceptor Conc.: 1.15472E+16 /cm^3
- Threshold Voltage: 1.0054 V

Net Active  
Boron Active  
Phos. Active  

Distance (Microns)
Figure A3.7: CCD/FEA - NMOS Poly2 Gate

- Alignment Xox: 6289A
- Pad Xox: 580A
- Kooi Xox: 993A
- Gate Xox: 750A
- 2nd Isolation Xox: 1116A
- Xox After Tip Sharp.: 3111A
- Poly2 Thickness: 4640A
- Poly2 Rs: 32.962 ohms/sq
- Surface Acceptor Conc.: 3.19732E+15 /cm^3
- Threshold Voltage: 0.60663 V

Net Active
Boron Active
Phos. Active
Figure A3.8: CCD/FEA - NMOS Source/Drain

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
1st Isolation Xox: 750A
2nd Isolation Xox: 1210A
Xox After Tip Sharp.: 2597A
Source/Drain Xj: 0.65276 μm
Source/Drain Rs: 80.099 ohms/sq
Surface Donor Conc.: 6.79525E+19 /cm^3

Net Active
Boron Active
Phos. Active
Figure A3.9:

CCD/FEA - N-Well

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
1st Isolation Xox: 750A
2nd Isolation Xox: 1210A
Xox After Tip Sharp.: 2436A
Well Xj: 5.0112 μm
Well Rs: 1507.9 ohms/sq
Surface Donor Conc.: 3.70001E+16 /cm³
Figure A3.10: CCD/FEA - PMOS N-Well Contact

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
1st Isolation Xox: 750A
2nd Isolation Xox: 1210A
Xox After Tip Sharp.: 2578A
High-Low Xj: 0.74502 um
Well Xj: 4.9553 um
Well w/ contact Rs: 76.729 ohms/sq
Surface Donor Conc.: 6.51375E+19 /cm^3

Net Active
Boron Active
Phos. Active
Figure A3.11: CCD/FEA - PMOS Field Region

Alignment Xox: 6289A
Pad Xox: 580A
Field Xox: 9647A
Kooi Xox: 10042A
Gate Xox: 9163A
1st Isolation Xox: 8717A
2nd Isolation Xox: 8929A
Xox After Tip Sharp.: 9546A
Well Xj: 4.7631 um
Surface Donor Conc.: 5.29051E+16 /cm^3
Threshold Voltage: -79.1 V

Net Active
Boron Active
Phos. Active

Distance (Microns)

Distance (Microns)
Figure A3.12: CCD/FEA - PMOS Poly1 Gate

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
Poly1-Poly2 Xox: 630A
2nd Isolation Xox: 1511A
Xox After Tip Sharp.: 2454A
Poly1 Thickness: 4755A
Poly1 Rs: 56.692 ohms/sq
Well Xj: 5.1009 um
Surface Donor Conc.: 1.45082E+16 /cm^3
Threshold Voltage: -1.8407 V

Net Active
Boron Active
Phos. Active
Figure A3.13: CCD/FEA - PMOS Poly2 Gate

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
2nd Isolation Xox: 1116A
Xox After Tip Sharp: 2618A
Poly2 Thickness: 4857A
Poly2 Rs: 46.942 ohms/sq
Well Xj: 5.0811 um
Surface Donor Conc.: 1.66748E+16 /cm^3
Threshold Voltage: -2.2965 V

Net Active
Boron Active
Phos. Active
Figure A3.14: CCD/FEA - PMOS Source/Drain

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
1st Isolation Xox: 750A
2nd Isolation Xox: 1210A
Xox After Tip Sharp.: 1449A
Source/Drain Xj: 0.81176 um
Source/Drain Rs: 266.28 ohms/sq
Surface Accpt. Conc.: 2.73578E+18 /cm^3
Well Xj: 5.0017 um

Net Active
Boron Active
Phos. Active
Figure A3.15: CCD/FEA - Emitter Tip Peak

- Alignment Xox: 6289A
- Pad Xox: 580A
- Kooi Xox: 993A
- Gate Xox: 750A
- 1st Isolation Xox: 750A
- 2nd Isolation Xox: 1210A
- Xox After Tip Sharp.: 2578A
- High-Low Xj: 0.74502 um
- Well Xj: 4.9553 um
- Well w/ contact Rs: 76.729 ohms/sq
- Surface Donor Conc.: 6.51375E+19 /cm^3

Net Active
Boron Active
Phos. Active
Figure A3.16: CCD/FEA - Emitter Tip Valley

Alignment Xox: 6289A
Pad Xox: 580A
Kooi Xox: 993A
Gate Xox: 750A
1st Isolation Xox: 750A
2nd Isolation Xox: 1210A
Xox After Tip Sharp.: 2581A
High-Low Xj: 0.70919 um
Well Xj: 2.9552 um
Well w/ contact Rs: 79.095 ohms/sq
Surface Donor Conc.: 6.51958E+19 /cm^3

Net Active
Boron Active
Phos. Active
APPENDIX 3. CCD/FEA PROCESS SIMULATIONS

SUPREM-4

Input Deck

$ CCD/FEA Project Todd C. Sieger 8/31/92
$ Emitter tip formation simulation Graded doping: Profile from Sup.3
$ No oxide cap during tip sharpening oxidation.

OPTION DEVICE=REGIS

$ Set up grid for tip simulation.
LINE X LOCATION=0.0 SPACING=0.8
LINE X LOCATION=0.8 SPACING=0.8
LINE X LOCATION=1.0 SPACING=0.1
LINE X LOCATION=2.0 SPACING=0.1

LINE Y LOCATION=0.0 SPACING=0.04
LINE Y LOCATION=2.4 SPACING=0.04
LINE Y LOCATION=2.44 SPACING=0.03
LINE Y LOCATION=3.0 SPACING=0.08
LINE Y LOCATION=3.5 SPACING=0.16

ELIMINATE ROWS X.MIN=1.3 X.MAX=2.0 Y.MIN=2.24 Y.MAX=2.38
ELIMINATE ROWS X.MIN=1.5 X.MAX=2.0 Y.MIN=2.0 Y.MAX=2.2
ELIMINATE ROWS X.MIN=1.7 X.MAX=2.0 Y.MIN=1.7 Y.MAX=1.9
ELIMINATE ROWS X.MIN=1.8 X.MAX=2.0 Y.MIN=1.5 Y.MAX=1.6
ELIMINATE ROWS X.MIN=1.9 X.MAX=2.0 Y.MIN=1.3 Y.MAX=1.4

ELIMINATE COLUMNS Y.MIN=1.4
ELIMINATE COLUMNS Y.MIN=2.4
ELIMINATE COLUMNS X.MIN=1.7 X.MAX=1.8 Y.MIN=1.7 Y.MAX=2.2
ELIMINATE COLUMNS X.MIN=1.9 X.MAX=2.0 Y.MIN=1.3 Y.MAX=2.2

$ Initialize using doping for p-type wafer (5ohm*cm)
INITIALIZE BORON=0 <100>

Comment Set up coefficients for oxidations in O2 & WetO2 (H2O)
Comment ambients based on process results.
Ambient H2O <100> H.Lin.0=1.5049E6 Gamma.0=3E13
PHOSPHOROUS FI=0.0497

$ Get phosphorous and boron dopant profiles from files generated
$ by TSUPREM-3 using file TIPPROF.S3I
PROFILE PHOSPHOROUS IN.FILE=phosprof.dat
PROFILE BORON IN.FILE=boronprof.dat

$ Deposit masking oxide (don’t need to model growth)
DEPOSIT OXIDE THICK=0.1210

$ Pattern masking oxide (2um dots; 4um center to center).
$ Simulate only one tip.
ETCH OXIDE LEFT P1.X=1.0

$ RIE etch silicon (2um deep; ~0.9um undercut).
ETCH SILICON START X=1.9 Y=0
ETCH SILICON CONTINUE X=1.89 Y=0.1
ETCH SILICON CONTINUE X=1.89 Y=0.2
ETCH SILICON CONTINUE X=1.88 Y=0.3
ETCH SILICON CONTINUE X=1.87 Y=0.4
ETCH SILICON CONTINUE X=1.86 Y=0.5
ETCH SILICON CONTINUE X=1.84 Y=0.6
ETCH SILICON CONTINUE X=1.81 Y=0.7
ETCH SILICON CONTINUE X=1.78 Y=0.8
ETCH SILICON CONTINUE X=1.75 Y=0.9
ETCH SILICON CONTINUE X=1.72 Y=1.0
ETCH   SILICON  CONTINUE   X=1.67   Y=1.1
ETCH   SILICON  CONTINUE   X=1.63   Y=1.2
ETCH   SILICON  CONTINUE   X=1.58   Y=1.3
ETCH   SILICON  CONTINUE   X=1.53   Y=1.4
ETCH   SILICON  CONTINUE   X=1.47   Y=1.5
ETCH   SILICON  CONTINUE   X=1.42   Y=1.6
ETCH   SILICON  CONTINUE   X=1.34   Y=1.7
ETCH   SILICON  CONTINUE   X=1.25   Y=1.8
ETCH   SILICON  CONTINUE   X=1.15   Y=1.9
ETCH   SILICON  CONTINUE   X=1.00   Y=2.0
ETCH   SILICON  CONTINUE   X=0.00   Y=2.0
ETCH   SILICON  DONE      X=0.00   Y=0.0

$ Etch masking oxide caps.
ETCH   OXIDE  RIGHT   P1.X=1.0

$ Mirror structure since the tips are symmetrical.
STRUCTURE   REFLECT

$ Plot grid
OPTION   DEVICE=L/POSTSCRIPT   PLOT.OUT="profgrid.ps"
SELECT   TITLE="SUPREM-4 Grid for FEA Tip"
PLOT.2D   SCALE   GRID

$ Check profile by plotting 1D concentration @ Tip Peak
OPTION   DEVICE=L/POSTSCRIPT   PLOT.OUT="profile1.ps"
SELECT   Z=LOG10(ACTIVE(BORON))   +
           TITLE="SUPREM-4: FEA Tip Peak Before n+ Implant"   +
           LABEL="log(Active Concentration)"
PLOT.1D   X.VALUE=2   BOTTOM=14   TOP=21   LINE.TYP=2   COLOR=2
LABEL   LABEL="Boron  (x=2um)"   X=2.0   Y=15
SELECT   Z=LOG10(ACTIVE(PHOS))
PLOT.1D   X.VALUE=0.5   BOTTOM=14   TOP=21   LINE.TYP=2   COLOR=2   +
           LEFT=2.0
LABEL   LABEL="Phosphorous  (x=0.5um)"   X=2.7   Y=16.2

$ Check profile by plotting 1D concentration in Tip "Valley" area.
OPTION   DEVICE=L/POSTSCRIPT   PLOT.OUT="profile2.ps"
SELECT   Z=LOG10(ACTIVE(BORON))   +
           TITLE="SUPREM-4: FEA Tip Valley Before n+ Implant"   +
           LABEL="log(Active Concentration)"
PLOT.1D   X.VALUE=0.5   BOTTOM=14   TOP=21   LINE.TYP=2   COLOR=2   +
           LEFT=2.0
LABEL   LABEL="Boron  (x=0.5um)"   X=2.7   Y=15
SELECT   Z=LOG10(ACTIVE(PHOS))
PLOT.1D   X.VALUE=0.5   ^AXES  "CLEAR   LINE.TYP=3   COLOR=3
LABEL   LABEL="Phosphorous  (x=0.5um)"   X=2.7   Y=16.2

$ n+ S/D implant
IMPLANT   PHOSPHOROUS   ENERGY=35   DOSE=1E15

$ Check profile by plotting 1D concentration @ Tip Peak
OPTION   DEVICE=L/POSTSCRIPT   PLOT.OUT="profile3.ps"
SELECT   Z=LOG10(ACTIVE(BORON))   +
           TITLE="SUPREM-4: FEA Tip Valley After n- Implant"   +
           LABEL="log(Active Concentration)"
PLOT.1D   X.VALUE=0.5   BOTTOM=14   TOP=21   LINE.TYP=2   COLOR=2   +
           LEFT=2.0
LABEL   LABEL="Boron  (x=0.5um)"   X=2.7   Y=15
SELECT   Z=LOG10(ACTIVE(PHOS))
PLOT.1D   X.VALUE=0.5   ^AXES  "CLEAR   LINE.TYP=3   COLOR=3
LABEL   LABEL="Phosphorous  (x=0.5um)"   X=2.7   Y=16.2

$ Oxidize and plot result
METHOD   COMPRESS   TWO.DIM
$ Total time = 10 min.
DIFFUSION TIME=10 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5

$ Total time = 20 min.
DIFFUSION TIME=10 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5

$ Total time = 30 min.
DIFFUSION TIME=10 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5

$ Total time = 40 min.
DIFFUSION TIME=10 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5

$ Total time = 50 min.
DIFFUSION TIME=10 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5

$ Total time = 60 min.
DIFFUSION TIME=10 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5

$ Total time = 65 min.
DIFFUSION TIME=5 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5

$ Total time = 70 min.
DIFFUSION TIME=5 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5

$ Total time = 75 min.
DIFFUSION TIME=5 TEMPERATURE=900 WET02
SELECT Z=1.0
PRINT.1D LAYERS X.VALUE=0.5
SELECT Z=1.0
PRINT.1D LAYERS Y.VALUE=0.2

$ Save and plot the structure with oxide still on.
STRUCTURE OUT.FILE="proftipo.stc"

OPTION DEVICE=POSTSCRIPT PLOT.OUT="proftip.ps"
SELECT TITLE="FEA Tip After Sharpening Oxidation"
PLOT.2D SCALE
COLOR OXIDE COLOR=13
LABEL X=2.0 Y=0.2 LABEL="Oxide" CENTER
LABEL X=2.0 Y=2.2 LABEL="Silicon" CENTER
$ Etch all oxide for plotting purposes only.
ETCH OXIDE ALL

$ Plot the structure with oxide removed.
OPTION DEVICE=POSTSCRIPT PLOT.OUT="profcont.ps"
SELECT Z=LOG10(ACTIVE(PHOS)) +
  TITLE="Phosphorous Contours After Sharpening Oxidation"
PLOT.2D SCALE T.SIZE=0.35
FOREACH X (16 TO 21 STEP 1)
  COLOR MIN.V=X MAX.V=( X + 1) COLOR=( X 2)
END
PLOT.2D ^AXES ^CLEAR
LABEL X=2.8 Y=0.6 LABEL="Log10(Phos)" SIZE=0.3
LABEL X=3.25 Y=0.85 LABEL="20-21" SIZE=0.3 C.RECT=18 W.R=0.4 H.R=0.4
LABEL X=3.25 Y=1.05 LABEL="19-20" SIZE=0.3 C.RECT=17 W.R=0.4 H.R=0.4
LABEL X=3.25 Y=1.25 LABEL="18-19" SIZE=0.3 C.RECT=16 W.R=0.4 H.R=0.4
LABEL X=3.25 Y=1.45 LABEL="17-18" SIZE=0.3 C.RECT=15 W.R=0.4 H.R=0.4
LABEL X=3.25 Y=1.65 LABEL="16-17" SIZE=0.3 C.RECT=14 W.R=0.4 H.R=0.4

$ Check profile by plotting 1D concentration @ Tip Peak
OPTION DEVICE=L/POSTSCRIPT PLOT.OUT="profile4.ps"
SELECT Z=LOG10(ACTIVE(BORON)) +
  TITLE="SUPREM-4: FEA Tip Peak After Sharpening"
PLOT.1D X.VALUE=2 BOTTOM=14 TOP=21 LINE.TYP=2 COLOR=2
LABEL LABEL="log(Active Concentration)" X.VALUE=2 BOTTOM=14 TOP=21 LINE.TYP=2 COLOR=2
SELECT Z=LOG10(ACTIVE(BORON))
PLOT.1D X.VALUE=2 ^AXES ^CLEAR LINE.TYP=3 COLOR=3
LABEL LABEL="Phosphorous (x=2um)" X.VALUE=2 BOTTOM=14 TOP=21 LINE.TYP=2 COLOR=2

$ Check profile by plotting 1D concentration in Tip "Valley" area.
OPTION DEVICE=L/POSTSCRIPT PLOT.OUT="profile5.ps"
SELECT Z=LOG10(ACTIVE(BORON)) +
  TITLE="SUPREM-4: FEA Tip Valley After Sharpening"
PLOT.1D X.VALUE=0.5 BOTTOM=14 TOP=21 LINE.TYP=2 COLOR=2 +
  LEFT=2.0 LABEL LABEL="Boron (x=0.5um)" X.VALUE=2 BOTTOM=14 TOP=21 LINE.TYP=2 COLOR=2 +
SELECT Z=LOG10(ACTIVE(BORON))
PLOT.1D X.VALUE=0.5 ^AXES ^CLEAR LINE.TYP=3 COLOR=3
LABEL LABEL="Phosphorous (x=0.5um)" X.VALUE=2 BOTTOM=14 TOP=21 LINE.TYP=2 COLOR=2

STOP
Silicon Etch Experiment Raw Data

Table A4.1: RSI table of silicon etch results.

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<th>Press.</th>
<th>Power</th>
<th>Vert_Etch</th>
<th>Undercut</th>
<th>Aspect</th>
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<td>(sccm)</td>
<td>(mtorr)</td>
<td>(um)</td>
<td>(um)</td>
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<td>1.000</td>
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<td>6</td>
<td>0</td>
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<td>150</td>
<td>2.500</td>
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</tr>
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<td>0.700</td>
<td>0.500</td>
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<td>0</td>
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<td>250</td>
<td>0.400</td>
<td>0.200</td>
<td>0.500000</td>
</tr>
<tr>
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<td>6</td>
<td>10</td>
<td>60</td>
<td>150</td>
<td>0.670</td>
<td>0.000</td>
<td>0.000000</td>
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<td>0</td>
<td>10</td>
<td>100</td>
<td>150</td>
<td>0.600</td>
<td>0.133</td>
<td>0.231667</td>
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<td>0.200</td>
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<td>250</td>
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<td>1.667</td>
<td>0.635047</td>
</tr>
</tbody>
</table>

Figure A4.1: Silicon etch results for run number 1 (10000x).
Figure A4.2: Silicon etch results for run number 2 (10000x).

Figure A4.3: Silicon etch results for run number 3 (10000x).
Figure A4.4: Silicon etch results for run number 4 (10000x).

Figure A4.5: Silicon etch results for run number 5 (10000x).
Figure A4.6: Silicon etch results for run number 6 (10000x).

Figure A4.7: Silicon etch results for run number 7 (10000x).
Figure A4.8: Silicon etch results for run number 8 (10000x).

Figure A4.9: Silicon etch results for run number 9 (10000x).
15. Pattern Active - mask level #2

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 2; Reticle: Sieger II, Levels 1-4 (Serial# 310488)

Development and post-bake: Wafertrac line 2, program 2.

16. Nitride etch

Plasmatherm RIE; 200W; -80V DC bias; 30 sccm SF₆; 90 mtorr.

Determine etch time from a dummy wafer from nitride deposition step.

17. Photoresist strip

Oxygen plasma.

18. Pattern Field Threshold Adjust - mask level #3

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 3; Reticle: Sieger II, Levels 1-4 (Serial# 310488)

Development and post-bake: Wafertrac line 2, program 2.

19. Field threshold adjust implant

Boron: 11 AMU; 35keV; 3E13 ions/cm²

All device wafers; NO control wafers

20. Photoresist strip

Oxygen plasma.
21. **RCA clean**

22. **Field oxide growth (LOCOS)**

   Furnace tube: #13
   Push: 800°C; 12 in/min; 4 lpm N₂
   Soak: 800°C; 15 min; 4 lpm dry O₂
   Ramp up: 800°C to 1100°C; 4 lpm dry O₂
   Soak: 1100°C; 25 min; 4 lpm dry O₂
   Ramp down: 1100°C to 950°C; furnace power on; 4 lpm dry O₂
   Soak: 950°C; 15 min; 4 lpm dry O₂
   Soak: 950°C; 400 min; 4 lpm wet O₂
   Soak: 950°C; 30 min; 4 lpm N₂
   Ramp down: 950°C to 800°C; furnace power off; 4 lpm N₂
   Pull: 800°C; 12 in/min; 4 lpm N₂

   Expected oxide thickness: ≈ 8000Å

23. **Oxi-nitride etch**

   10:1 H₂O:HF; until hydrophobic in active regions (= 2 min.)

   All device wafers and control wafers C1-C6.

24. **Nitride strip**

   Phosphoric acid; 160°C; 30 min.

   All device wafers and control wafers C1-C6.
25. Oxide etch (pad oxide strip)

10:1 H₂O:HF; 4 min (etch rate is =150Å/min).

All device wafers.

Etch all control wafers bare.

26. RCA clean

27. Kooi oxide growth

Furnace tube: #13

Push: 900°C; 12 in/min; 4 lpm wet O₂

Soak: 900°C; 50 min; 4 lpm wet O₂

Pull: 900°C; 12 in/min; 4 lpm wet O₂

Expected oxide thickness: 1000Å

28. Threshold adjust blanket implant

Boron; 11 AMU; 35keV; 2E12 ions/cm²

All device wafers and all control wafers.

29. Pattern Buried Channel - mask level #4

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 4; Reticle: Sieger II,

Levels 1-4 (Serial# 310488)

Development and post-bake: Wafertrac line 2, program 2.
30. Buried channel implant

Phosphorous: 31 AMU; 150keV; 2.5E12 ions/cm²

All device wafers and control wafers C9 and C10.

31. Photoresist strip

Oxygen plasma.

32. Oxide etch (Koi oxide strip)

10:1 H₂O:HF; 6 min 40 sec (etch rate is ≈150Å/min).

All device wafers and all control wafers.

33. RCA clean

34. Gate oxide growth

Furnace tube: #12
TCA tube clean: 950°C; 30 min; 4 lpm dry O₂; 190 sccm TCA
Push: 950°C; 12 in/min; 4 lpm N₂
Stabilize: 950°C; 15 min; 4 lpm N₂
Soak: 950°C; 125 min; 4 lpm dry O₂; 190 sccm TCA
Anneal: 950°C; 30 min; 4 lpm N₂
Pull: 950°C; 12 in/min; 4 lpm N₂
Expected oxide thickness: 750Å in poly1 gate regions.
35. Polysilicon deposition (poly1)

LPCVD; 610°C; 73 min deposition; 6500Å.

MUST BE DONE IMMEDIATELY AFTER GATE OXIDE GROWTH!

Include control wafers C5, C10, C11, and C13.

36. Four-point probe and groove-and-stain

Control wafer C9.

Expected sheet resistance: $= 6100 \, \Omega /\text{sq}$

Expected junction depth: $= 0.42 \mu\text{m}$

37. Phosphorous pre-deposit of polysilicon

All wafers; spin-on dopant only on device wafers and control wafers C5, C10, C11, and C13.

Dopant: Emulsitone N-250 spin-on dopant; 3000rpm, 10 sec; 185°C, 15min convection oven pre-bake.

Furnace tube: #13

Push: 950°C; 12 in/min; 4 lpm N$_2$

Soak: 950°C; 10 min; 4 lpm N$_2$

Pull: 950°C; 12 in/min; 4 lpm wet O$_2$

38. Oxide etch (spin-on dopant de-glaze)

BOE; until hydrophobic (4 min.)

All device wafers and control wafers C5, C10, C11, and C13.
39. **Four-point probe**

All device wafers and control wafers C5, C10, C11, and C13.

Expected sheet resistance: \( = 45 \, \Omega/\text{sq} \)

40. **Pattern Poly1 gates - mask level #5**

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 1; Reticle: Sieger II, Levels 5-8 (Serial# 310535)

Development and post-bake: Wafertrac line 2, program 2.

Post-bake must be at 140°C or resist will not withstand RIE etch.

41. **Polysilicon etch**

Plasmatherm RIE; 75W; 30 sccm SF₆, 3 sccm O₂; 75 mtorr.

Etch both back side and front side of wafer - 75 sec each.

Confirm etch completion with Nanospec measurement.

42. **Photoresist strip**

Piranha 3:1 \((\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2)\); 15min.

43. **Oxide etch (Gate oxide etchback)**

10:1 \(\text{H}_2\text{O}:\text{HF}\); 3 min 40 sec (etch rate is \(=150\AA/\text{min}\)).

All device wafers and all control wafers.

Check that final oxide thickness is 200Å in regions where poly2 gates will be.

44. **RCA clean**

Do NOT include 10:1 \(\text{H}_2\text{O}:\text{HF}\) step.
45. First isolation oxide growth

Furnace tube: #12
TCA tube clean: 950°C; 30 min; 4 lpm dry O₂; 190 sccm TCA
Push: 950°C; 12 in/min; 4 lpm N₂
Stabilize: 950°C; 15 min; 4 lpm N₂
Soak: 950°C; 110 min; 4 lpm dry O₂; 190 sccm TCA
Anneal: 950°C; 30 min; 4 lpm N₂
Pull: 950°C; 12 in/min; 4 lpm N₂
Expected oxide thickness: 750Å in poly2 gate regions.

46. Polysilicon deposition (poly2)

LPCVD: 610°C; 73 min deposition; 6500Å.

MUST BE DONE IMMEDIATELY AFTER FIRST ISOLATION OXIDE GROWTH!

Include control wafers C6, C10, C12, and C13.

47. Phosphorous pre-deposit of polysilicon

All wafers; spin-on dopant only on device wafers and control wafers C6, C10, C12, and C13.

Dopant: Emulsitone N-250 spin-on dopant; 3000rpm, 10 sec;
185°C, 15min convection oven pre-bake.

Furnace tube: #13
Push: 950°C; 12 in/min; 4 lpm N₂
Soak: 950°C; 10 min; 4 lpm N₂
Pull: 950°C; 12 in/min; 4 lpm wet O₂
APPENDIX 5. CCD/FEA PROCESS OUTLINE

48. Oxide etch (spin-on dopant de-glaze)

BOE; until hydrophobic (4 min.)

All device wafers and control wafers C6, C10, C12, and C13.

49. Four-point probe

All device wafers and control wafers C6, C10, C12, and C13.

Expected sheet resistance:  = 45 Ω/sq

50. Pattern Poly2 gates - mask level #6

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 2; Reticle: Sieger II,

Levels 5-8 (Serial# 310535)

Development and post-bake: Wafertrac line 2, program 2.

Post-bake must be at 140°C or resist will not withstand RIE etch.

51. Polysilicon etch

Plasmatherm RIE; 75W; 30 sccm SF₆, 3 sccm O₂; 75 mtorr.

Etch both back side and front side of wafer - 75 sec each.

Confirm etch completion with Nanospec measurement.

52. Photoresist strip

Piranha 3:1 (H₂SO₄:H₂O₂); 15min.

53. RCA clean
54. **Second isolation oxide growth**

Furnace tube: 

#13

Push: 

900°C; 12 in/min; 4 lpm wet O₂

Soak: 

900°C; 25 min; 4 lpm wet O₂

Pull: 

900°C; 12 in/min; 4 lpm wet O₂

Expected oxide thickness: 1200Å in FEA region.

55. **Pattern Tips - mask level #7**

Resist coating and pre-bake: Wafertrak line 3, program 3.

Exposure: 

Stepper 01; Job T2SIEGER, Pass 3; Reticle: Sieger II, Levels 5-8 (Serial# 310535)

Development and post-bake: Wafertrak line 2, program 2.

Post-bake must be at 140°C or resist will not withstand RIE etch.

Correct exposure and development is critical since tip patterns consist of 2µm circles which must be precisely 2µm prior to the next step.

56. **Oxide etch**

All device wafers and control wafer C4.

Plasmatherm RIE; 200W; 170 sccm CHF₃, 60 sccm C₂F₆, 48 sccm CO₂; 150 mtorr; 2 min each wafer (etch all oxide).

Etch rate is approximately 635Å/min; confirm with a dummy wafer before committing device wafers.
57. Silicon etch

All device wafers and control wafer C4.

Plasmatherm RIE; 190W; 10 sccm SF₆, 4 sccm O₂, 7 sccm CO₂; 73 mtorr; 3 min each wafer.

Final depth of etch should be 1.9-2.1µm; confirm with Alpha-Step measurement on first patterned wafer etched before proceeding.

It is recommended that a device wafer be sacrificed for SEM confirmation of the tip structure.

58. Photoresist strip

Piranha 3:1 (H₂SO₄:H₂O₂); 15 min.

59. Pattern p+ S/D - mask level #8

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 4; Reticle: Sieger II.

Levels 5-8 (Serial# 310535)

Development and post-bake: Wafertrac line 2, program 2.

60. Oxide etch

BOE; until hydrophobic in p+ S/D regions.

All device wafers and control wafers C3, C5, C6, and C7.

61. p+ S/D implant

BF₂⁺; 55keV; 1E15 ions/cm²

All device wafers and control wafers C3, C5, C6, and C7.
62. Photoresist strip

Piranha 3:1 (H₂SO₄:H₂O₂); heated if necessary; 15min.

63. Pattern n+ S/D - mask level #9

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure:
Stepper 01; Job T2SiEGER, Pass 1; Reticle: Sieger II,

Levels 9-12 (Serial# 310538)

Development and post-bake: Wafertrac line 2, program 2.

64. Oxide etch (remove oxide caps from tips)

BOE; until hydrophobic in n+ S/D regions (2 min at most).

All device wafers and control wafers C2, C4, C8, C11, C12, and C13.

65. n+ S/D implant

Phosphorous; 31 AMU; 35keV; 1E15 ions/cm²

All device wafers and control wafers C2, C4, C8, C11, C12, and C13.

66. Photoresist strip

Piranha 3:1 (H₂SO₄:H₂O₂); heated if necessary; 15min.

67. RCA clean
68. **Tip sharpening oxidation**

Furnace tube: #13
Push: 900°C; 12 in/min; 4 lpm wet O₂
Soak: 900°C; 75 min; 4 lpm wet O₂
Pull: 900°C; 12 in/min; 4 lpm wet O₂

Expected oxide thickness: 2500Å in valley of FEA.

69. **Glass deposition**

Submit device wafers only to Dr. Fuller for deposition of 1.4μm of BPSG/undoped LTO at Eastman Kodak Research Labs.

Kodak's process is as follows:

2000Å undoped LTO + 12000Å BPSG deposited at 420°C.

Kodak does **not** perform a flow step immediately following deposition.

BPSG has 4% by weight boron, 4% by weight phosphorous.

70. **Reflow**

Furnace tube: #14
Push: 900°C; 12 in/min; 4 lpm N₂
Soak: 900°C; 60 min; 4 lpm N₂
Pull: 900°C; 12 in/min; 4 lpm N₂

71. **Oxide etch**

BOE; until hydrophobic.

ALL control wafers only.
72. Four-point probe and Nanospec polysilicon thickness

Control wafers C5, and C11 (poly1).

Expected sheet resistance: $= 15 \ \Omega/sq$

Expected poly thickness: $= 5100\AA$

Control wafers C6, C10, C12, and C13 (poly2).

Expected sheet resistance: $= 50 \ \Omega/sq$

Expected poly thickness: $= 3900\AA$

73. Polysilicon etch

Polysilicon wet etchant in Wet Etch II area; until all poly is removed.

Control wafers C5, C6, C10, C11, C12, and C13 only.

74. Oxide etch

BOE; until hydrophobic.

Control wafers C5, C6, C10, C11, C12, and C13 only.

75. Four-point probe and Nanospec polysilicon thickness

Control wafers C10, and C13 (poly1).

Expected sheet resistance: $= 15 \ \Omega/sq$

Expected poly thickness: $= 5100\AA$

76. Polysilicon etch

Polysilicon wet etchant in Wet Etch II area; until all poly is removed.

Control wafers C10, and C13 only.
77. **Oxide etch**

BOE; until hydrophobic.

Control wafers C10, and C13 only.

78. **Four-point probe groove-and-stain**

See process simulation results for expected final junction depths and sheet resistances. An equivalence table is given below.

Table A5.1: Control wafer and SUPREM-3 cross-section equivalence.

<table>
<thead>
<tr>
<th>Control Wafer</th>
<th>Cross Section</th>
<th>Comparable SUPREM-3 Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>n-well</td>
<td>CCDNWELL</td>
</tr>
<tr>
<td>C2</td>
<td>n+ contact to n-well</td>
<td>CCDPCONT</td>
</tr>
<tr>
<td>C3</td>
<td>p+ S/D</td>
<td>CCDPSRCE</td>
</tr>
<tr>
<td>C4</td>
<td>FEA valley</td>
<td>CCDTIPVL</td>
</tr>
<tr>
<td>C5</td>
<td>PMOS poly1 gate</td>
<td>CCDPGTP1</td>
</tr>
<tr>
<td>C6</td>
<td>PMOS poly2 gate</td>
<td>CCDPGTP2</td>
</tr>
<tr>
<td>C7</td>
<td>p+ contact to p wafer</td>
<td>CCDNCONT</td>
</tr>
<tr>
<td>C8</td>
<td>n+ S/D</td>
<td>CCDNSRCE</td>
</tr>
<tr>
<td>C9</td>
<td>BCCD poly1 gate</td>
<td>CCDBCGP1</td>
</tr>
<tr>
<td>C10</td>
<td>BCCD poly2 gate</td>
<td>CCDBCGP2</td>
</tr>
<tr>
<td>C11</td>
<td>NMOS poly1 gate</td>
<td>CCDNGTP1</td>
</tr>
<tr>
<td>C12</td>
<td>NMOS poly2 gate</td>
<td>CCDNGTP2</td>
</tr>
<tr>
<td>C13</td>
<td>NMOS poly2 over poly1</td>
<td>CCDBCP12 without buried channel</td>
</tr>
</tbody>
</table>

Control wafers C5, C6, C10, C11, C12, and C13 will show if any phosphorous diffused through the gate from the polysilicon. C5 and C6 should only have the lightly doped well, C10 only the buried channel and should thus have very close to the same $R_s$ and $X_j$ as C9. C11-C13 should not show evidence of any junction.
79. Pattern Contacts - mask level #10

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 2; Reticle: Sieger II, Levels 9-12 (Serial# 310538)

Development and post-bake: Wafertrac line 2, program 2.

80. Oxide etch

BOE; until contacts are free of oxide (~25 min); etch rate of BPSG is approximately 615Å/min.

All device wafers; NO control wafers.

81. Photoresist strip

Piranha 3:1 (H$_2$SO$_4$;H$_2$O$_2$); 15min.

82. RCA clean

Only 10 sec. dip for 10:1 H$_2$O:HF step.

83. Aluminum deposition

CVC 601 sputterer; 350V, 9A; 11.5 min deposition time; 0.5μm.

84. Sinter

Furnace tube: #14

Push: 450°C; 12 in/min; 4 lpm N$_2$

Soak: 450°C; 20 min; 4 lpm forming gas (90% N$_2$, 10% H$_2$)

Pull: 450°C; 12 in/min; 4 lpm N$_2$
85. Pattern Aperature - mask level #11

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 3; Reticle: Sieger II, Levels 9-12 (Serial# 310538)

Development and post-bake: Wafertrac line 2, program 2.

Correct exposure and development is critical since aperture patterns consist of 3μm circles which must be precisely 3μm in the final device.

Alignment to the 2μm tips is CRITICAL.

86. Aluminum etch

Transene aluminum etchant; 40°C; etch until 3μm circles are clear; minimize overetch.

All device wafers; NO control wafers

87. Oxide etch (clear oxide from peaks of tips)

BOE:glycerine 5:2; 8 min (should expose approximately 0.5μm of the tip).

All device wafers; NO control wafers

88. Photoresist strip

Piranha 3:1 (H₂SO₄:H₂O₂); 15min.

89. Pattern Metal - mask level #12

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SIEGER, Pass 4; Reticle: Sieger II, Levels 9-12 (Serial# 310538)

Development and post-bake: Wafertrac line 2, program 2.
90. Aluminum etch

Transene aluminum etchant; 40°C; until metal clears (takes longer to clear in 3µm holes than in large open areas).

All device wafers; NO control wafers

91. Photoresist strip

Piranha 3:1 (H$_2$SO$_4$;H$_2$O$_2$); 15min.

92. Glass deposition

LPCVD; 400°C; 100 min deposition; 20% SiH$_4$, 12% O$_2$; 2000Å.

93. Pattern Passivation (bond pads) - mask level #13

Resist coating and pre-bake: Wafertrac line 3, program 3.

Exposure: Stepper 01; Job T2SieGGER, Pass 1; Reticle: Sieger II,

Levels 13 (Serial# 310536)

Development and post-bake: Wafertrac line 2, program 2.

94. Oxide etch (clear oxide from bond pads and FEA)

BOE:glycerine 5:2; until pads are free of glass (= 3 min; etch rate lower than straight BOE).

All device wafers and control wafers

95. Photoresist strip

Piranha 3:1 (H$_2$SO$_4$;H$_2$O$_2$); 15min.
96. Aluminum deposition

CVC 601 sputterer; 350V, 9A; 11.5 min deposition time; 0.5μm.

Deposit on BACK SIDES of wafers.

97. Test

Make measurements of test structures and individual transistors using HP-4145 Semiconductor Parameter Analyzer.

FEA and CCD/FEA must be tested in vacuum chamber at or below 10⁻⁶ torr.
Figure A4.10: Silicon etch results for run number 10 (10000x).

Figure A4.11: Silicon etch results for run number 11 (10000x).
Figure A4.12: Silicon etch confirmation experiment - wafer #3: 10:4:7 sccm $\text{SF}_6$:$\text{O}_2$:CO$_2$, 73mtorr, 190W, 3min (10000x).

Figure A4.13: Silicon etch confirmation experiment - wafer #5: 10:3:5 sccm $\text{SF}_6$:$\text{O}_2$:CO$_2$, 80mtorr, 200W, 3min (10000x).
Figure A4.14: Silicon etch confirmation experiment - wafer #6: 10:3:0sccm SF$_6$:O$_2$:CO$_2$, 60mtorr, 250W, 2min (10000x).

Figure A4.15: Silicon etch confirmation experiment - wafer #7: 10:6:0sccm SF$_6$:O$_2$:CO$_2$, 100mtorr, 150W, 2min (10000x).
CCD/FEA Process Outline

1. Obtain and scribe starting wafers

   Silicon, 4" diameter, 500-550µm thick, <100>, p-type, boron doped, 5-15 Ω·cm.

   Ten device wafers labeled D1-D10; thirteen control wafers labeled C1-C13.

2. RCA clean

3. Alignment oxide growth

   Furnace tube: #13
   Push: 900°C; 12 in/min; 4 lpm N₂
   Ramp up: 900°C to 1100°C; 4 lpm N₂
   Soak: 1100°C; 60 min; 4 lpm wet O₂
   Ramp up: 1100°C to 1150°C; 4 lpm N₂
   Soak: 1150°C; 600 min; 4 lpm N₂
   Ramp down: 1150°C to 1000°C; furnace power off; 4 lpm N₂
   Pull: 1000°C; 12 in/min; 4 lpm N₂
   Expected oxide thickness: 6000Å

4. Pattern n-Well - mask level #1

   Resist coating and pre-bake: Wafertrak line 3, program 3.
   Exposure: Stepper 01; Job T2SIEGER, Pass 1; Reticle: Sieger II, Levels 1-4 (Serial# 310488)
   NOTE: Shifts set to 0 for pass 1 for this first level.

   Development and post-bake: Wafertrak line 2, program 2.
5. Oxide etch

BOE: until hydrophobic (6.5 min.)

All device wafers and control wafers C1-C6.

6. n-Well implant

Phosphorous; 31 AMU; 130keV; 6E12 ions/cm²

All device wafers and control wafers C1-C6.

7. Photoresist strip

Oxygen plasma.

8. RCA clean

9. n-Well drive-in

Furnace tube: #16
Push: 1000°C; 12 in/min; 4 lpm N₂
Soak: 1000°C; 10 min; 4 lpm dry O₂
Soak: 1000°C; 25 min; 4 lpm wet O₂
Soak: 1000°C; 5 min; 4 lpm dry O₂
Ramp up: 1000°C to 1150°C; 4 lpm dry O₂
Soak: 1150°C; 1250 min; 4 lpm N₂
Ramp down: 1150°C to 800°C; furnace power on; 4 lpm N₂
Soak: 800°C; 400 min; 4 lpm N₂
Pull: 800°C; 12 in/min; 4 lpm N₂

Expected oxide thickness: = 2181Å over the well
= 7065Å over p-type substrate
10. **Oxide etch**

BOE; until hydrophobic (= 15 min.)

All device wafers and all control wafers

11. **Four-point probe and groove-and-stain**

Control wafer C1.

Expected sheet resistance: = 1350 \(\Omega/\text{sq}\)

Expected junction depth: = 5.15\(\mu\text{m}\)

12. **RCA clean**

13. **Pad oxide growth**

Furnace tube: #13

Push: 900°C; 12 in/min; 4 lpm \(\text{N}_2\)

Ramp up: 900°C to 1100°C; 4 lpm \(\text{N}_2\)

Soak: 1100°C; 15 min; 4 lpm dry \(\text{O}_2\)

Ramp down: 1100°C to 1000°C; furnace power off; 4 lpm \(\text{N}_2\)

Pull: 1000°C; 12 in/min; 4 lpm \(\text{N}_2\)

Expected oxide thickness: 580Å

14. **Nitride deposition**

LPCVD; 790-810°C profile; 20 min deposition; 1500Å.

Include control wafers C1-C6.