Design and fabrication of structured roughnesses in microchannels with integrated MEMS pressure sensors

Tushara Pasupuleti
DESIGN AND FABRICATION OF STRUCTURED ROUGHNESSES IN MICROCHANNELS WITH INTEGRATED MEMS PRESSURE SENSORS

By

Tushara Pasupuleti

A Thesis Submitted
In Partial Fulfillment
of the Requirements for the Degree of
Master of Science

In

Microelectronic Engineering

Approved by:

Prof. ______________________
Dr. Satish G. Kandlikar (Thesis Advisor)

Prof. ______________________
Dr. Karl Hirschman (Thesis Co-Advisor)

Prof. ______________________
Dr. James Moon (Committee Member)

Prof. ______________________
Dr. Robert Pearson (Program Director)

Prof. ______________________
Dr. Sohail A. Dianat (Head of the Department)

ELECTRICAL AND MICROELECTRONIC ENGINEERING DEPARTMENT
COLLEGE OF ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY
ROCHESTER, NEW YORK
MAY 2010
DESIGN AND FABRICATION OF STRUCTURED ROUGHNESSES IN MICROCHANNELS WITH INTEGRATED MEMS PRESSURE SENSORS

By

Tushara Pasupuleti

I, Tushara Pasupuleti, hereby grant permission to the Wallace Library, of Rochester Institute of Technology, to reproduce this document in whole or in part, with the knowledge that any reproduction will not be for commercial use or profit.

___________________________   _________________________
Tushara Pasupuleti     May 21st, 2010
As the demand for cooling is increased for high-density powered electronic devices, researchers have proposed solutions to improve the efficiency of the microchannel liquid cooling system to meet these requirements. Introducing roughness in the microchannels is one of the approaches to enhance the heat transfer. The fluid flow behavior needs experimental investigation before exploring the heat transfer efficiency. A test structure consisting MEMS pressure sensors were fabricated along the length of the microchannel. Smooth microchannels and rough microchannels with structured roughness were fabricated. A fabrication process flow has been developed to fabricate the microchannel and the pressure sensor on the same silicon wafer. The fabrication process challenges were solved to achieve the required test structure design. The process characterization of Microspray\textsuperscript{TM} SU-8 has been one of the key features to define uniform coating on the silicon wafer. A packaging technique was developed on the fabricated test structures and was successfully implemented in some cases. An experimental setup was designed to test the fabricated test structure. The fabricated MEMS pressure sensors were calibrated and the experimental setup was validated using a smooth microchannel.
# Table of Contents

Title Page .................................................................................................................................................. i

Abstract .................................................................................................................................................. iii

Table of Contents .................................................................................................................................... iv

List of Figures ......................................................................................................................................... vii

List of Tables .......................................................................................................................................... xi

Acknowledgements ................................................................................................................................... xii

Chapter 1 .................................................................................................................................................. 1

   Introduction .......................................................................................................................................... 1

Chapter 2 .................................................................................................................................................. 5

   Background .......................................................................................................................................... 5

      2.1. Experiments with Single Chip Module (SCM) ......................................................................... 5

      2.2. Roughness Effects in Microchannels and Minichannels .............................................................. 9

      2.2.1. Surface Roughness Effects in Microchannels and Minichannels ........................................... 9

      2.2.2. Structured Roughness Effects in Minichannels ..................................................................... 12

      2.2.3. Pressure drop in Single Phase Liquid Flow .......................................................................... 12

      2.3. Objectives .................................................................................................................................. 14

Chapter 3 .................................................................................................................................................. 15

   Test Structure Design and Fabrication ............................................................................................... 15

      3.1. Designed Fabrication Process ................................................................................................. 19
3.2. Mask Design ................................................................................................... 31
   3.2.1. Fluid Conduit Design ............................................................................... 31
   3.2.2. Design of Electrical Connections .............................................................. 33
   3.2.3. Pressure Sensor Design ............................................................................ 34

Chapter 4 ........................................................................................................................... 37

Fabrication & Packaging Results ..................................................................................... 37
   4.1. Modified Fabrication Process ........................................................................ 37
   4.1.1. Development for Lithography Level I ......................................................... 37
   4.1.2. Development for Lithography Level II ....................................................... 43
   4.1.3. Development for Lithography Level III, IV and V ..................................... 45
   4.1.4. Development for Lithography Level VI & VII ......................................... 46
   4.2. SEM Images of Microchannels ...................................................................... 49
   4.3. Microchannel Geometry and Surface Analysis ............................................. 52
   4.4. Packaging ....................................................................................................... 55
   4.4.1. Reference Pressure Chamber Packaging .................................................. 55
   4.4.2. Microchannel Packaging .......................................................................... 56
   4.4.3. Packaging Results ..................................................................................... 57

Chapter 5 ........................................................................................................................... 60

Experimental Setup & Results ....................................................................................... 60
   5.1. Experimental Testing Setup ............................................................................ 60
5.2. Results ..................................................................................................................... 64

5.2.1. Pressure Sensor Calibration .............................................................................. 64

5.2.2. Validation of Experimental Setup Using Smooth Microchannel ................. 65

Chapter 6 ......................................................................................................................... 68

Conclusions .................................................................................................................... 68

References .................................................................................................................... 70

Appendix A ..................................................................................................................... 72

Appendix B ..................................................................................................................... 74
### List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>SEM image of (a) Plain or continuous microchannels (b) Enhanced or staggered fin type microchannels [9]</td>
<td>2</td>
</tr>
<tr>
<td>1.2</td>
<td>Components of Single Chip Module [8]</td>
<td>6</td>
</tr>
<tr>
<td>1.3</td>
<td>Microchannel Cooler in a SCM [8]</td>
<td>6</td>
</tr>
<tr>
<td>1.4</td>
<td>Variation in thermal resistance at different locations of the chip.</td>
<td>7</td>
</tr>
<tr>
<td>1.5</td>
<td>Comparing refrigerant cooled system and water cooled system</td>
<td>8</td>
</tr>
<tr>
<td>1.6</td>
<td>Tu and Hrnjak test section to measure pressure drop using pressure tap holes [20].</td>
<td>11</td>
</tr>
<tr>
<td>1.7</td>
<td>Strain gauge pressure sensors integrated along channel length [21].</td>
<td>12</td>
</tr>
<tr>
<td>2.1</td>
<td>(100) and {111} planes in a (100)-oriented silicon wafer</td>
<td>15</td>
</tr>
<tr>
<td>2.2</td>
<td>Schematic of the trapezoidal microchannel with structured roughness features</td>
<td>17</td>
</tr>
<tr>
<td>2.3</td>
<td>Cross-sectional view of the test structure after level I.</td>
<td>21</td>
</tr>
<tr>
<td>2.4</td>
<td>Cross-sectional view of the test structure before Lithography level II.</td>
<td>22</td>
</tr>
<tr>
<td>2.5</td>
<td>Cross-sectional view of the test structure before polysilicon deposition step</td>
<td>23</td>
</tr>
<tr>
<td>2.6</td>
<td>Cross-sectional view of the test structure after polysilicon deposition step</td>
<td>24</td>
</tr>
<tr>
<td>2.7</td>
<td>Backside alignment marks on the diaphragm level II and polysilicon resistor level III</td>
<td>25</td>
</tr>
<tr>
<td>2.8</td>
<td>Cross-sectional view of the test structure after 1 µm TEOS deposition</td>
<td>26</td>
</tr>
<tr>
<td>2.9</td>
<td>Cross-sectional view of the test structure after etching the metal layer</td>
<td>27</td>
</tr>
<tr>
<td>2.10</td>
<td>Cross-sectional view of the test structure before etching the ProTEK™ layer</td>
<td>28</td>
</tr>
<tr>
<td>2.11</td>
<td>Cross-sectional view of the test structure after etching the ProTEK™ layer and the adhesion layer</td>
<td>28</td>
</tr>
<tr>
<td>2.12</td>
<td>Aerosol container of Microspray™ SU-8 resist (MicroChem Corporation Product)</td>
<td>29</td>
</tr>
<tr>
<td>2.13</td>
<td>Cross-sectional view of the smooth microchannel test structure.</td>
<td>30</td>
</tr>
</tbody>
</table>
Figure 3.14 Cross-sectional view of the test structure with SU-8 roughness feature inside the microchannels.

Figure 3.15 Mask design of the fluid conduit on the backside of the wafer.

Figure 3.16 Magnified image of the roughness features inside the microchannels.

Figure 3.17 Design of the electrical connections on the front side of the wafer.

Figure 3.18 Pressure sensor design.

Figure 3.19 Mask design of the test structure.

Figure 3.20 Mask design with all the test structures design and alignment marks.

Figure 4.1 (a) The design of the alignment mark on the mask and (b) the alignment mark on the wafer after KOH etch seen under microscope (10X).

Figure 4.2 The backside of the wafer with manually coated photoresist on the alignment marks and directional arrows.

Figure 4.3 Cracks formed on the nitride layer.

Figure 4.4. Cross-sectional view of the test structure after lithography level Ia.

Figure 4.5 Cross-sectional view of the test structure before lithography level Ib.

Figure 4.6 Cross-sectional view of the test structure after lithography level Ib and manual PR coat on alignment marks.

Figure 4.7 Cross-sectional view of the test structure after silicon etching in hot KOH solution.

Figure 4.8 Cross-sectional view of the test structure with TEOS layer on backside of the wafer to protect the nitride layer from getting etched in LAM490 tool.

Figure 4.9 Cross-sectional view of the test structure with wet oxide grown as a stress relief layer for the thin diaphragm.

Figure 4.10 Cross-sectional view of the test structure defining the diaphragm region after the lithography level Ib.

Figure 4.11 Back side of the test structure.

Figure 4.12 Front side of the test structure.

Figure 4.13 SEM image of 500 µm wide smooth microchannel.
Figure 4.14 SEM image of back side of the wafer near the pressure sensor diaphragm. ..................................................................................................................................................50

Figure 4.15 SEM image of 500 µm wide microchannel with roughness features of 40 µm pitch. .............................................................................................................................................................51

Figure 4.16 SEM image of 160 µm wide microchannel with roughness features of 160 µm pitch. .................................................................................................................................................................51

Figure 4.17 SEM image (top-view) of 160 µm wide microchannel with roughness features of 160 µm pitch. ..........................................................................................................................................................52

Figure 4.18 Smooth microchannel dimension results obtained using Wyko tool. ........53

Figure 4.19 Contour plot of rough microchannel obtained using Wyko tool. ............54

Figure 4.20 (a) Lexan™ plate with drilled holes, (b) Kapton™ tape with punched holes, (c) packaged front side of the test structure, (d) packaged backside of the test structure and, (e) packaged backside of test structure with hose fittings. ........................................57

Figure 4.21 Cross section of the different test structures cases used to verify the packaging technique. The proposed packaging technique worked for case (i) and (ii) but not for case (iii) . ............................................................................................................59

Figure 5.1 Schematic of the test section block. .................................................................................................................................61

Figure 5.2. Basic components of the experimental test setup loop. ........................................................................................................62

Figure 5.3 Schematic of the probe card holder assembly. ................................................................................................................63

Figure 5.4 Schematic of the Labview program used to collect the data. .........................................................................................63

Figure 5.5 Work place in Thermal Micro-fluidics and Fuel Cell Laboratory where experiments were conducted. ......................................................64

Figure 5.6 Graph plotted to calibrate the fabricated MEMS pressure sensors. ...........65

Figure 5.7 Plot validating the experimental setup using microchannel of 155 µm hydraulic diameter. .................................................................................................................................66
## List of Tables

Table 3.1 Summary of the rough and smooth microchannels dimensions being fabricated.................................................................................................................................18

Table 3.2 Location of pressure taps along the channel length. ..........................................................32

Table 3.3 Dimensions of the pressure sensor..................................................................................34

Table 4.1 Details of 50 µm thick SU-8 coat parameters..................................................................47

Table 4.2 Thickness of SU-8 layer obtained at different test structures.........................................48

Table 4.3 SU-8 coat parameters for roughness features. .................................................................48

Table 4.4 Smooth microchannel dimension and roughness............................................................53

Table 4.5 Smooth microchannel dimensions of a fabricated test structure along the channel length. .................................................................................................................................54
Acknowledgements

I would like to thank the following people for helping me sail through my Master’s degree:

- My advisor, Dr. Kandlikar, for giving me an opportunity and motivation to work on the exciting research.
- My co-advisor, Dr. Hirschman, for providing constant support and valuable guidance during the thesis work.
- My committee member, Dr. Moon, for being on the committee and providing valuable suggestions.
- Semiconductor Microsystems Fabrication Laboratory staff members for providing the assistance during the fabrication of the test structures.
- Mechanical Engineering Machine Shop staff members for their help during the machining of the experimental test setup components.
- Members of Thermal Analysis and Microfluidics Fuel Cell Laboratory for their support during the course of the work.
- My teacher, parents, husband, in-laws and sister for their endless support and encouragement to pursue my goals.
Chapter 1

Introduction

Continued advancements in IC technology facilitate shrinking the device dimensions, thereby reducing the total area occupied by an electronic chip. Each working device generates heat that needs to be dissipated, otherwise the temperature of the electronic chip will increase and eventually lead to failure. A cooling system helps to dissipate the heat generated and maintains the temperature suitable for operation of the devices. A microchannel cooling system has been an attractive and very effective way to cool high-power density devices. It reduces the thermal resistance between the chip surface and the coolant. In addition, microchannels provide a substantial surface area-to-volume ratio which increases the heat transfer rate.

Kandlikar and Grande have classified the dimensions of the microchannels to be in the range of 10 µm to 200 µm, minichannels to be in the range of 200 µm to 3 mm, and conventional channels as greater than 3 mm [1]. The application of a microchannel cooling system for electronic chip cooling was initiated three decades ago by Tuckerman and Pease [2]. The efficiency of the microchannel cooling system has been explored by changing the geometry and dimensions of the channels. The pattern of the microchannels can be continuous and staggered fin type. Continuous fin type or plain microchannels have uninterrupted flow along the length of the channel, whereas staggered fin type or enhanced microchannels have fins placed at fixed intervals with an offset which provides continuous mixing of the flow. This mixing of the fluid occurs as the developing flow
profile continuously forms and breaks inside the microchannel which results in a very high heat transfer coefficient. Enhanced microchannels have proven to exhibit better heat transfer performance as compared to plain microchannels [3-8]. Figure 1.1 illustrates the SEM images of plain microchannel and enhanced microchannels respectively [9].

Figure 1.1 SEM image of (a) Plain or continuous microchannels (b) Enhanced or staggered fin type microchannels [9].

Colgan et al. designed a unit known as Single Chip Module (SCM) considering the various assumptions of the actual working conditions [8]. A microchannel cooler and
a thermal chip were packaged together in an SCM. Water was used as the working fluid to study the performance of the SCM. However, water cannot be used for practical reasons inside an electronic device. Alternative working fluids like refrigerants should be considered [10]. **Chapter 2** presents the details of the experiments performed on an SCM at the Thermal Analysis Micro-fluidics and Fuel Lab, RIT. Refrigerant R-123 was used as the working fluid to study the thermal performance of the SCM and to compare a refrigerant-cooled system with a water-cooled system [11]. It was found that the refrigerant cooling system was efficiently able to cool 80 W/cm² of heat flux by maintaining the chip temperature at 60°C. It was also observed that the pressure drop across the test section *i.e.*, SCM was large for the refrigerant R-123 cooling system when compared to the data obtained by Colgan *et al.* for a water-cooled system. This needs investigation, but only two pressure measurements at inlet and outlet are available, which are not sufficient for the analysis. Having the knowledge of the pressure drop along the test section could have been beneficial to understand the fluid flow behavior in detail.

Another way of enhancing the heat transfer rate in the microchannels is by increasing the surface area of the channel. This can be achieved by increasing the surface roughness of the channel. Understanding the fluid flow in the microchannels is important as various factors are dominant at microscale levels which are negligible at macroscale. **Chapter 2** contains the literature review on the study of roughness effects in minichannels and microchannels. It mainly focuses on the experimental work performed in silicon channels for the laminar flow region. In the end of Chapter 2, objectives of the research are defined.
Chapter 3 describes the details of the test section design and the proposed fabrication process flow using the tools available at Semiconductor and Microsystems Fabrication Laboratory, RIT. Chapter 4 illustrates the problems faced during the fabrication and how they were solved in detail. It presents the Scanning Electron Microscope (SEM) images and surface scan analysis of the test section fabricated. The advantages and disadvantages of the packaging methodology used to close the microchannels and the reference pressure chamber of pressure sensor are also described. Chapter 5 provides the details of the experimental setup used for fluidic and electrical connections. It explains the testing procedure adopted to measure the pressure as the fluid flows in the microchannel. Chapter 6 presents the concluding remarks of the current research performed.
Chapter 2

Background

A microchannel cooling system has proven to be remarkably effective at dissipating heat from the high density power devices. Researchers have experimentally investigated the different types of microchannel designs to maximize the thermal performance of the microchannel cooling system. Generally, water has been considered as the working fluid or coolant for most of the experiments. But for practical implementation of the microchannel cooling system in an active electronic device, water cannot be used as working fluid, as any small leak can lead to system failure. Refrigerants are the other alternative working fluids that can be used in the cooling system. To study the refrigerant cooled system and compare it with a water-cooled system, the Single Chip Module (SCM) has been selected as the test section.

2.1. Experiments with Single Chip Module (SCM)

The Single Chip Module is a packaged unit designed to cool individual microprocessors. The different components present in a SCM are two manifold blocks, thermal chip, microchannel cooler, gasket and ceramic substrate. Figure 2.1 illustrates the various components of the SCM. The microchannel cooler consists of a channel chip with staggered fin type pattern and a manifold chip with inlet and outlet ports to define the flow path. Figure 2.2 shows a three dimensional view of a microchannel cooler in a SCM.
The design of the SCM transforms the flow from one inlet and outlet port to four inlets and outlets in a way that there are six parallel heat exchanger zones [8].

Figure 2.1 Components of Single Chip Module [8].

Figure 2.2 Microchannel Cooler in a SCM [8].
Unit thermal resistance has been used to compare different cooling systems in electronics cooling industry. The performance of the cooling system is considered good if the value of unit thermal resistance is low. The unit thermal resistance is given by equation (1) where $T_{chip}$ is the chip temperature, $T_{inlet}$ is the inlet fluid temperature and $q''$ is the heat flux.

$$\theta = \frac{T_{chip} - T_{inlet}}{q''}$$ \hspace{1cm} (1)

Previous work has been performed on the SCM using water as the working fluid [8]. The thermal performance of the SCM using refrigerant R-123 has also been studied [11]. The details of the R-123 experimental test setup and procedures are illustrated in Pasupuleti and Kandlikar’s work [11]. Figure 2.3 illustrates the thermal resistance of each temperature sensor located on the thermal chip. It can be clearly seen that at a constant flowrate all the sensors are at relatively the same temperature, which implies that the heat is dissipated uniformly from the active area of the chip.

![Thermal Resistance vs Flowrate](image)

**Figure 2.3** Variation in thermal resistance at different locations of the chip.
The comparison of the R-123 refrigerant-cooled system and water-cooled system is performed on the basis of the unit thermal resistance. Figure 2.4 shows the comparison of the unit thermal resistance offered by the two working fluids (refrigerant R-123 and water). The values are lower for the water-cooled system as compared to the refrigerant-cooled system. As the flowrate is increasing, the rate at which unit thermal resistance is decreasing for R-123 cooling system is high. The thermal performance is more comparable at high flowrates as the two cooling systems exhibit approximately similar unit thermal resistance. However, experimental data is not available beyond 0.7 lpm flowrate for the refrigerant-cooled system because of the inefficiency of the pump. Also, pressure drop losses of the refrigerant system were quite high as compared to the water-cooled system. No significant conclusions were drawn, but the initial tests show promising results to extend the work at higher flowrates [11].

![Figure 2.4 Comparing refrigerant cooled system and water cooled system](image-url)
2.2. Roughness Effects in Microchannels and Minichannels

Researchers have been studying the effects of surface roughness on fluid flow in channels. In 1937, Nikuradse performed an extensive study on the effects of roughness in channels of diameter 25-100 mm and defined relative roughness of < 3% using sand [13]. It was concluded that roughness has no effects on laminar flow. However, the channel dimensions considered in this experiment were conventional channels (> 3 mm). As the channel diameter is decreased, the surface area-to-volume ratio increases which enhances the surface roughness, thereby affecting the fluid flow. As a result, at the macroscopic level surface roughness does not play a major role, but at the microscopic level surface roughness affects the fluid flow properties.

2.2.1. Surface Roughness Effects in Microchannels and Minichannels

Experimental work to study the roughness effects in minichannels and microchannels was carried out on different materials such as silicon, fused silica and stainless steel tubes. In this research, the focus is to study the effects of roughness in silicon minichannels and microchannels using incompressible working fluids in laminar flow region.

In 1990, Pfahler et al. studied the pressure drop across etched silicon microchannels of hydraulic diameter 1.5 µm, 3.3 µm and 76 µm [14]. He observed that the friction coefficient for the 76 µm microchannel roughly agrees with the theory whereas the other two microchannels disagree. Jiang et al. performed experiments in etched silicon microchannels of hydraulic diameter 8-68 µm with roughness < 0.15 µm (i.e., relative roughness < 0.5%) [15]. He concluded that the experimental laminar friction
factor was less than the theoretical friction factor. Mala and Li’s results show that the experimental friction factor is greater for fused silica microtubes of diameter 50-254 µm [16]. They also noticed early transition from laminar flow. The surface roughness reported for the microtubes was ± 1.75 µm. It was observed that the value of friction factor increases as the diameter decreases. Similarly, Qu et al. noticed the same behavior on friction factor as diameter decreases [17]. They used silicon microchannels of hydraulic diameter 51-169 µm with relative roughness < 2.8% and concluded by stating that the early transition from laminar flow and high friction factor values are due to effects of roughness. Wu and Cheng performed experiments in silicon microchannels with relative roughness < 0.6% and found that the friction factor is more for high values of relative roughness [18].

The above discussion clearly indicates that earlier researchers were trying to understand the deviation of experimental friction factor from the theoretical friction factor in laminar and transitional flow by measuring the pressure drop across the channel length. Celeta et al. adopted a method to obtain the pressure drop inside the channel using two microtubes of same diameter but of different lengths [19]. Figure 2.5 illustrates the testing procedure used to measure the pressure drop along the channel length. The pressure drop across the shorter microtube was used to analyze the pressure drop inside the larger microtube.

Tu and Hrnjak introduced two pressure taps inside the channel to measure the pressure along the channel length as shown in Figure 2.6 [20]. Similarly, Baviere and Ayela measured the local pressure in the microchannel with integrated micromachined strain gauges as illustrated in Figure 2.7 [21]. Although these experiments resulted in a
better understanding of the pressure drop across the channel, they were performed for relative roughness $< 5\%$. In order to enhance the heat transfer a relative roughness of $> 5\%$ is desired [22]. However, experiment data in microchannels that supports this theory has not been reported and hence is the focus of this work.

![Figure 2.5 Test section to measure pressure loss distribution along the channel length [19].](image)

![Figure 2.6 Tu and Hrnjak test section to measure pressure drop using pressure tap holes [20].](image)
2.2.2. Structured Roughness Effects in Minichannels

A Moody diagram explains the nature of the fluid flow with respect to Reynolds’s number for a given relative roughness. This diagram describes the transition from laminar to turbulent flow in conventional channels. However, the diagram is found to be invalid for flow in minichannels and microchannels [14-22]. Kandlikar et al. proposed a modified Moody diagram based on the constricted flow diameter of the channel which accommodates the deviation in the friction factor [23]. Brackbill et al. verified the modified Moody diagram for minichannels with relative roughness ranging from 4% to 25% [24, 25]. However, the modified Moody diagram is not yet verified for microchannels.

2.2.3. Pressure drop in Single Phase Liquid Flow

The non-dimensional parameter to measure the pressure drop is friction factor $f$. Fanning friction factor and Darcy friction factor are two different ways of defining the
friction factor. In this work, friction factor will be defined in terms of Fanning friction factor.

As the fluid flow enters the microchannel, the velocity profile of the fluid is developing and eventually becomes fully developed. The length of the developing flow profile in laminar flow is known as hydrodynamic developing length $L_h$ (also known as entrance length) and is given by

$$L_h = 0.05ReD_h$$  \hspace{1cm} (2)

Equation (3) defines the Reynolds number $Re$ where $m$ is mass flowrate, $D_h$ is the hydraulic diameter of the channel, $A$ is the cross-sectional area and $\mu$ is the dynamic viscosity of the fluid.

$$Re = \frac{mD_h}{A\mu}$$  \hspace{1cm} (3)

The flow is fully developed when microchannel flow length $L > L_h$. In a fully developed laminar flow, the theoretical friction factor for a rectangular channel is provided by Shah and London [26]. In equation (4), aspect ratio $\alpha_c$ is defined as the ratio of the shorter side to the longer side of the channel.

$$f = \frac{24}{Re} (1 - 1.3553\alpha_c + 1.9467\alpha_c^2 - 1.7012\alpha_c^3 + 0.9564\alpha_c^4 - 0.2537\alpha_c^5)$$  \hspace{1cm} (4)

The experimental Fanning friction factor is computed by substituting the measured outlet pressure $P_o$ and inlet pressure $P_i$ along with the other parameters (density $\rho$, velocity $V$ and channel length $L$) in the equation (5).

$$f_{\text{expt}} = \frac{(P_o - P_i)D_h}{2\rho V^2 L}$$  \hspace{1cm} (5)
2.3. Objectives

Enhanced heat and mass transfer processes are in demand for micro-fluidics applications. By introducing structured roughness in the microchannels heat transfer process can be increased due to the increase in the surface area, but experimental validation is critical.

At the microscale level, as the magnitude of the properties decrease the error associated with the property increases. It is very essential at microscale level to consider the factors which were neglected at the macroscale level. The measurement of pressure drop along the microchannel length is the critical part of the experiment to understand the fluid flow behavior in detail. This can be done by connecting a commercial pressure sensor with the test section using connectors or pipe. However, the distance and number of the connecters used between the channel and the sensor should be as small as possible to avoid loss of data due to damping or filtering. Also as discussed in the previous section, measuring the pressure drop at inlet and outlet of the test section is insufficient for an accurate understanding of the fluid flow behavior in the channel. Therefore it is essential to measure the pressure drop along the channel length.

The objective of the present work is to design and fabricate structured roughness features in microchannels with integrated MEMS pressure sensors along the channel length. This is a pioneering effort to fabricate a test section which can be used for the study of fluid dynamics in microchannels with structured roughness.
Chapter 3

Test Structure Design and Fabrication

A test structure is required to experimentally study the roughness effects in microchannels. In this research, a test structure is defined as a microchannel with structured roughness and a series of pressure sensors along the microchannel length. The silicon microchannels designed and fabricated in this research were formed by chemically etching silicon wafers in potassium hydroxide (KOH) solution. The etch rates of the various planes of a silicon crystal in KOH solution are different, and the (100) plane etches faster than the {111} plane. (100)-oriented silicon wafer has the {111} plane at an angle of 54.74° from the surface (100) plane, as shown in Fig. 3.1. Hence, the cross sectional shape of the microchannel is trapezoidal (or triangular if etched deeply enough for the {111} planes to meet).

![Figure 3.1](image)

Figure 3.1 (100) and {111} planes in a (100)-oriented silicon wafer.

The hydraulic diameter is dictated by the shape of the microchannel. In this research, for all the test structures, the range of hydraulic diameter that has been considered is between 125 µm to 225 µm with the length of the microchannel set as 1 cm.
As discussed in the previous chapter, one of the methods of increasing the heat transfer in a microchannel is to enhance the surface area by introducing structured roughness features. This surface area is characterized by the pitch $\lambda$ and height $h$ of the roughness features. The width $w$ of the roughness feature has been chosen to be same in all the test structures. Figure 3.2 illustrates the uniform roughness features inside the trapezoidal microchannel of height $H$ and length $L$. The height of the roughness features has been selected to achieve relative roughness greater than 5%. Relative roughness $\varepsilon/D_h$ is defined as the ratio of the height of the roughness feature $h$ (or $\varepsilon$) to the hydraulic diameter of the microchannel.

Table 3.1 summarizes the test matrix that is generated using the combination of three hydraulic diameters and three roughness pitches and resulting into three smooth microchannels and nine rough microchannels. The microchannels with the presence of roughness features are referred to as rough microchannels and without the roughness features are smooth or plain microchannels. Please note that the height of the microchannel and width of the roughness feature are kept constant for all the test structures.
Figure 3.2 Schematic of the trapezoidal microchannel with structured roughness features.
Table 3.1 Summary of the rough and smooth microchannels dimensions being fabricated.

<table>
<thead>
<tr>
<th>Test Structure</th>
<th>Roughness Feature (width, $w=20\ \mu m$)</th>
<th>Microchannel (Length, $L=1\ \text{cm}$)</th>
<th>Aspect Ratio $H/W_1$</th>
<th>Hydraulic Diameter $D_h\ \mu m$</th>
<th>Relative Roughness $\epsilon/D_h$</th>
</tr>
</thead>
<tbody>
<tr>
<td>I Rough</td>
<td>40 20 2</td>
<td>500 350 150</td>
<td>0.30</td>
<td>224.92</td>
<td>8.89%</td>
</tr>
<tr>
<td>II Rough</td>
<td>40 20 2</td>
<td>250 100 150</td>
<td>0.60</td>
<td>171.27</td>
<td>11.68%</td>
</tr>
<tr>
<td>III Rough</td>
<td>40 20 2</td>
<td>160 10 150</td>
<td>0.94</td>
<td>126.68</td>
<td>15.79%</td>
</tr>
<tr>
<td>IV Rough</td>
<td>100 20 5</td>
<td>500 350 150</td>
<td>0.30</td>
<td>224.92</td>
<td>8.89%</td>
</tr>
<tr>
<td>V Rough</td>
<td>100 20 5</td>
<td>250 100 150</td>
<td>0.60</td>
<td>171.27</td>
<td>11.68%</td>
</tr>
<tr>
<td>VI Rough</td>
<td>100 20 5</td>
<td>160 10 150</td>
<td>0.94</td>
<td>126.68</td>
<td>15.79%</td>
</tr>
<tr>
<td>VII Rough</td>
<td>160 20 8</td>
<td>500 350 150</td>
<td>0.30</td>
<td>224.92</td>
<td>8.89%</td>
</tr>
<tr>
<td>VIII Rough</td>
<td>160 20 8</td>
<td>250 100 150</td>
<td>0.60</td>
<td>171.27</td>
<td>11.68%</td>
</tr>
<tr>
<td>IX Rough</td>
<td>160 20 8</td>
<td>160 10 150</td>
<td>0.94</td>
<td>126.68</td>
<td>15.79%</td>
</tr>
<tr>
<td>X Smooth</td>
<td>0 0 0</td>
<td>500 350 150</td>
<td>0.30</td>
<td>224.92</td>
<td>0.00%</td>
</tr>
<tr>
<td>XI Smooth</td>
<td>0 0 0</td>
<td>250 100 150</td>
<td>0.60</td>
<td>171.27</td>
<td>0.00%</td>
</tr>
<tr>
<td>XII Smooth</td>
<td>0 0 0</td>
<td>160 10 150</td>
<td>0.94</td>
<td>126.68</td>
<td>0.00%</td>
</tr>
</tbody>
</table>
3.1. Designed Fabrication Process

In this section, the fabrication process for introducing structured roughness in microchannels with MEMS pressure sensors will be explained. The process has been defined by using the available tools in the Semiconductor and Microsystems Fabrication Laboratory at RIT. The test structure was designed such that the electrical connections are on the opposite side of the wafer when compared to the fluidic connectors. Seven lithography levels have been performed using 1X contact lithography. Microspray\textsuperscript{TM} SU-8, a negative resist, was used in this process to define the fluid flow from the microchannel to the pressure sensor region. Also, this resist was sprayed on the wafer to define the roughness features inside the microchannels.

The starting point of the fabrication process was to select the appropriate silicon wafers. Since the dimensions of the microchannels were relatively large and process steps were performed on both sides of the wafer, double-sided polished, (100) crystal oriented, 6” silicon wafers of 300 µm thickness were selected. The first step in the process was to remove the organic contaminants, thin oxide and ionic contaminants. Hence, the wafers were cleaned using RCA clean process. This was followed by growing dry oxide of 500 Å at 1000ºC in the Bruce furnace. Then, a nitride layer of 1500 Å was deposited at 810ºC and 260 mT with 159 sccm of dichlorosilane (H\textsubscript{2}SiCl\textsubscript{2}) and 37 sccm of ammonia (NH\textsubscript{3}). As the nitride layer induces tensile stress on the wafer, the oxide layer grown before depositing the nitride layer acts as a stress relief layer. The nitride layer acts as the masking layer during the wet chemical etch of silicon in the hot potassium hydroxide (KOH) solution. The next step was to define the microchannel region on the wafer. Using the standard coat recipe in
the SSI track tool, photoresist (PR) was coated on the back side of the wafer. Using Level 1 Mask on Karl Suss MA140 exposure tool, 1X contact lithography was performed. The photoresist was developed using the standard develop recipe in the SSI track. This step was followed by etching the nitride layer using LAM490 at 260 mT with RF power of 125 W in the presence of 200 sccm sulfur hexafluoride (SF₆). The layer of oxide was etched in 10:1 buffered oxide etch (BOE) solution. The photoresist was stripped in Branson asher tool using 6” hard ash recipe. With the above-described hard mask, 100 µm deep silicon microchannels were formed by etching the silicon in a 20% KOH solution at 75°C.

Due to the fact that alkali contaminants (i.e., potassium) are a major portion of the residual components of the KOH etch, decontamination clean is performed after etching the silicon, as these contaminants could affect the fabrication and performance of other devices (e.g., metal-oxide-semiconductor). This clean is performed in a solution of deionized (DI) water, hydrogen peroxide (H₂O₂) and hydrochloric acid (HCl) at 70°C for 20 mins. The remaining nitride was etched in hot phosphoric acid solution at 175°C and the oxide was etched in 10:1 BOE solution. Figure 3.3 represents the cross-sectional view of the test structure with the microchannel. Please note that all the cross-sectional views presented for explaining the fabrication process are not to scale.
After defining the channel, the next step in the process was to define the diaphragm. In order to achieve this goal, the silicon wafers with the 100 µm deep trench microchannels were loaded in the furnace to grow 500 Å of dry oxide (to act as stress relief layer). In order to protect the microchannels that were fabricated on the backside of wafer during the KOH etch of the diaphragm, a nitride layer of 1500 Å was deposited. The nitride layer on the front side of the wafer was etched in the LAM490 dry etch tool. Before etching the nitride from the front side of the wafer, photoresist was coated on the edge of the wafer using a Q-tip and baked on a hot plate for 1 min at 140°C. This application of photoresist on the edges of the wafer prevents the etching of the nitride from the edge while etching the nitride from the front side of the wafer. Hence this nitride layer protects the edge of the silicon during the silicon etching in KOH solution. After the blanket nitride etch from the front side of the wafer, the dry oxide from the front side of the wafer was etched away in 10:1 BOE solution. The nitride layer on the backside of the wafer protects the oxide under it. Hence after etching nitride and oxide from the front side of the wafer, the photoresist on the edge of the wafer was stripped in the solvent stripper. Baker PRS-2000 resist stripper was used at 90°C to remove the photoresist.
Using the above process, a thin diaphragm was fabricated. In order to protect these thin diaphragms from deforming due to stress, 5000 Å of oxide was grown by wet oxidation at 1000°C in the Bruce furnace. Figure 3.4 illustrates the cross-sectional view of the test structure before the lithography level II.

![Cross-sectional view of the test structure before Lithography level II.](image)

The diaphragm region was defined on the backside of the wafer in lithography level II by aligning to the first lithography level I. Using SSI track and Karl Suss MA140 tools, the lithography step was performed. At this stage, edges of the wafer were again protected by photoresist which was applied using Q-tip. Before the nitride layer was etched, the oxy-nitride etch was performed in 10:1 BOE solution. Please note that the front side of the wafer which had only the oxide layer was not protected by photoresist or any other masking layer. As a result, during this etch step, a portion of the oxide layer on the front side gets etched. The nitride layer from the backside of the wafer was etched in the LAM490 dry etch tool and then oxide was etched in 10:1 BOE solution. As the oxide again gets etched from the front side of the wafer, approximately 4000 Å of oxide was present on the front side of the wafer. The photoresist was stripped from the edges of the wafers in the solvent stripper. Figure 3.5 shows the cross-sectional view before the polysilicon deposition.
The next step in the fabrication process was to create polysilicon resistors for the pressure sensors. A polysilicon layer was deposited on the front and back side of the wafer at 610°C and 300 mT in the presence of silane (SiH₄) gas (50 sccm). The thickness of polysilicon was targeted for 6000 Å. After the deposition, N250 spin-on-glass was coated on the front side of the wafer at 3000 rpm for 45 secs which was followed by an oven bake at 200°C for 20 mins to vaporize the dissolved solvents in the spin-on-glass. The wafers were loaded in the furnace for diffusing the phosphorus dopants into the polysilicon layer. This diffusion process was carried out at 1000°C in the presence of nitrogen gas for 15 mins which was followed by 5 mins of soak in oxygen and hydrogen. The additional soak was performed to grow wet oxide between the polysilicon layer and spin-on-glass. This oxidation facilitates the removal of the spin-on-glass after the diffusion process in 5.2:1 BOE solution for 7 mins. After stripping the spin-on-glass, the sheet resistance of the wafer was measured. The cross-sectional view after the deposition of polysilicon layer is shown in Fig. 3.6.
Figure 3.6 Cross-sectional view of the test structure after polysilicon deposition step.

The polysilicon resistors were patterned on the front side of the wafer in lithography level III using backside alignment technique described below. This step is critical as the response of the pressure sensors with the diaphragm deflection relies on the accurate alignment between the polysilicon resistors level and diaphragm level. The front side of the wafer was coated with photoresist using the standard coat recipe in the SSI track. On the Karl Suss MA140 exposure tool, the backside of the wafer was aligned with the mask of the level II (diaphragm level) using the alignment marks patterned on the wafer in lithography level II. Once the backside of the wafer and mask (level II) were aligned, the wafer chuck in the exposure tool was lowered. Using a transfer pipet, a very small drop of water was put on the backside of the wafer (i.e. on the side of the wafer which faces the mask). At this point, the chuck was moved up towards the mask and, due to the presence of the small drop of water, the wafer and mask adheres to each other. After verifying the alignment between the mask and the wafer and making any necessary adjustments for any misalignments, the mask was released from the mask holder by switching off the vacuum that holds the mask in the mask holder. Carefully, the mask was placed on a table with the wafer adhered to the mask facing up (i.e., towards the operator). The polysilicon resistor mask level III was placed on the wafer aligning with the backside alignment marks present at the corners of the mask. Figure 3.7 illustrates the
backside alignment marks which were present on the mask corners of lithography level II (diaphragm) and level III (polysilicon resistors). Once the two masks were aligned using the backside alignment marks, both the masks were clamped together using clamps. A microscope was used to check the alignment at the four corners of the mask. This clamped assembly was placed in the exposure tool and the wafer was exposed for the standard exposure time. After the completion of exposure, the wafer was carefully separated from the mask level II and developed on the SSI track using the standard develop recipe. At this point, the polysilicon was etched using the LAM490 in the presence of 15 sccm oxygen and 140 sccm sulfur hexafluoride (SF₆) at 325 mT pressure and 140 W RF power which was followed by stripping the photoresist in the solvent stripper.

The next step in the process was to fabricate the contact cuts. The front side of the wafer was coated with a 1 µm thick layer of tetraethyl orthosilicate (TEOS) and the cross sectional view of the test structure through this step is shown in Fig. 3.8. The TEOS layer

Figure 3.7 Backside alignment marks on the diaphragm level II and polysilicon resistor level III

The next step in the process was to fabricate the contact cuts. The front side of the wafer was coated with a 1 µm thick layer of tetraethyl orthosilicate (TEOS) and the cross sectional view of the test structure through this step is shown in Fig. 3.8. The TEOS layer
isolates the polysilicon resistor layer and aluminum metal layer. A lithography step was performed to define the contact cut region in the TEOS layer to connect the resistors and metal layer. This lithography level IV (contact cut level) was aligned with the polysilicon resistor level. The standard coat recipe, exposure time, and develop recipe are used to process this lithography level on the front side of the wafer. Then the required TEOS was etched in 10:1 BOE solution to achieve the contact cuts and the photoresist was stripped in the solvent stripper.

![Cross-sectional view](image)

Figure 3.8 Cross-sectional view of the test structure after 1 μm TEOS deposition.

The wafers were next cleaned using an RCA clean process after the completion of the previous lithography step. An extra process step of 20 secs dip in the 50:1 hydrofluoric acid (HF) bath was introduced in the clean recipe to remove any oxide present near the interface of the resistor and metal (contact cut region). Aluminum metal of 1 μm thickness was deposited on the front side of the wafer using the CVC 601 tool. The metal was deposited in the presence of argon gas at 20 psi, vacuum pressure of 1.3e-6 Torr and RF power 2000 W. The next lithography was performed to define the metal lines and metal contact pads using the level V mask. Again, standard coat recipe, exposure time and develop recipe were used to perform the metal lithography level V. A
wet etch process was performed to etch aluminum metal to pattern the metal layer. The metal etchant for Fujifilm Electronic Materials contains phosphoric acid, acetic acid and nitric acid. After etching the metal, photoresist was stripped in the solvent stripper. Figure 3.9 illustrates the cross sectional view after etching the metal.

In order to define the contact pads on the front side of the wafer a layer of TEOS of 1 µm was deposited to act as the ProTEK™ adhesion layer. ProTEK™ is a spin-on film that is a polymer which protects the devices fabricated on the wafer from the hot KOH solution during silicon etching. ProTEK™ B3 primer was coated first on the front side of the wafer at 1500 rpm for 1 min and baked on a hot plate at 140°C for 1 min. Then, ProTEK™ B3 was spin coated at 1500 rpm for 1 min and baked on a hot plate at 140°C for 1 min. An oven bake is performed to vaporize the dissolved solvents in the layer at 200°C for 30 mins. The wafer is etched in the hot KOH solution to etch away the silicon to achieve a diaphragm of ~25 µm thickness. Decontamination clean is performed after the silicon etching to remove alkali contaminants from transferring to other clean room tools. ProTEK™ is removed in a solvent known as ProTEK remover 100 and isopropylene (IPA) rinse is performed followed by DI water rinse and dry. The TEOS oxide
layer which was deposited as the ProTEK™ adhesion layer is etched in a pad etch bath which is an ammonium fluoride mixture. Figure 3.10 represents the cross-sectional view of the test structure before etching the ProTEK™ layer. Figure 3.11 represents the cross-sectional view of the test structure after the pad etch is performed.

The next step was to define the fluid path from the microchannel region to the pressure sensor region. Microspray™ SU-8, a negative photoresist was used to define this feature. Due to the topography of the backside of the wafer, spin coating of a resist didn’t give a uniform and complete coverage of the wafer. As a result, Microspray SU-8 resist
was used as it could be sprayed on the wafer. Figure 3.12 shows the aerosol container of the Microspray™ SU-8 which is a product of MicroChem Corporation. SU-8 resist was sprayed on the wafer to coat a 50 µm thick resist layer. Lithography level VI mask was performed to pattern the SU-8 layer which was aligned to the first lithography level I (channel level) using a UV filter in the Karl Suss MA150 contact aligner tool. Then the resist was developed in SU-8 developer. The schematic of the test structure is illustrated in Fig. 3.13. This completes the fabrication process for the smooth microchannel test structures.
Figure 3.13 Cross-sectional view of the smooth microchannel test structure.

The rough microchannel with structured roughness was defined in the lithography level VII which was aligned to the channel level I. SU-8 resist is used for defining the roughness features. The thickness of SU-8 resist sprayed was targeted to be 20 µm which was the height of the roughness feature inside the microchannel. The photoresist was exposed using a UV filter in the Karl Suss exposure tool and developed in the SU-8 developer. The schematic of the test structure cross section is illustrated in Figure 3.14.

Figure 3.14 Cross-sectional view of the test structure with SU-8 roughness feature inside the microchannels.
3.2. Mask Design

The following section describes the various masks that were used in the above fabrication process. The masks for the above-described fabrication process was designed using Mentor Graphics IC station. This design was made for a 5” X 5” mask and has seven levels for 1X contact lithography. There are nine test structures designed on one 6” wafer which have been divided into three equal sets of varying hydraulic diameter (225 µm, 170 µm and 125 µm). In each set of test structure with same hydraulic diameter, the roughness pitch was varied (40 µm, 100 µm and 160 µm).

3.2.1. Fluid Conduit Design

![Figure 3.15 Mask design of the fluid conduit on the backside of the wafer.](image)
The fluidic path is defined on the backside of the wafer by using four mask levels as shown in Figure 3.15. The two header regions of the channel, the inlet and the outlet, were defined in level I. The diaphragm region is defined using level II. The pressure taps along the channel length were defined using level VI. As shown in Table 3.2, there are two pressure taps in the inlet and outlet header region and eight pressure taps along the channel length. For the rough microchannels, the roughness features were defined using level VII. Figure 3.16 depicts the roughness features that are defined by level VII.

Table 3.2 Location of pressure taps along the channel length.

<table>
<thead>
<tr>
<th>Sensor Location along the 1 cm long channel</th>
<th>P₁</th>
<th>P₂</th>
<th>P₃</th>
<th>P₄</th>
<th>P₅</th>
<th>P₆</th>
<th>P₇</th>
<th>P₈</th>
<th>P₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inlet header</td>
<td>500 μm</td>
<td>1000 μm</td>
<td>2000 μm</td>
<td>3000 μm</td>
<td>4000 μm</td>
<td>5000 μm</td>
<td>6000 μm</td>
<td>8000 μm</td>
<td>Outlet header</td>
</tr>
</tbody>
</table>

Figure 3.16 Magnified image of the roughness features inside the microchannels.
3.2.2. Design of Electrical Connections

Figure 3.17 Design of the electrical connections on the front side of the wafer.

The electrical connections for the test structure were designed on the front side of the wafer. Figure 3.17 illustrates the mask design of the electrical connections. The polysilicon resistors were defined using level III. The location of these polysilicon resistors has been defined with respect to the diaphragms on the backside of the wafer. Levels IV and V define the contact cut region and metal lines, respectively. The metal bond pads have been designed with respect to a 48 pin probe card.
3.2.3. Pressure Sensor Design

In the proposed test structure, a piezo-resistive bulk micromachined pressure sensor is illustrated in Figure 3.18. The design of the pressure sensor was based on the previous work done by Fuller and Sudirgo [28]. In this process, the silicon substrate was used as the diaphragm of the pressure sensor. Polysilicon resistors were used to measure the diaphragm deflection. In order to maximize the sensitivity of the sensor, the resistors were placed on the diaphragm where the stress is highest. Researchers have found that in a square-shaped diaphragm, the maximum stress is at the center of the four sides of the square diaphragm [28]. As a result, in this design eight polysilicon resistors of equivalent resistance were placed as a pair of two on each side of the diaphragm. The dimensions of resistors are listed in Table 3.3 along with the diaphragm dimensions. The mask design of the test structure with all the levels is illustrated in Fig. 3.19. The mask design on the 5” X 5” mask for 1X lithography with all the test structures and backside alignment marks is shown in Figure 3.20.

<table>
<thead>
<tr>
<th>Table 3.3 Dimensions of the pressure sensor.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor length</td>
</tr>
<tr>
<td>Resistor width</td>
</tr>
<tr>
<td>Targeted thickness of diaphragm</td>
</tr>
<tr>
<td>Dimensions of diaphragm defined on the backside of the wafer</td>
</tr>
<tr>
<td>Dimensions of diaphragm after 275 µm deep silicon etch</td>
</tr>
</tbody>
</table>
Figure 3.18 Pressure sensor design.

Figure 3.19 Mask design of the test structure.
Figure 3.20 Mask design with all the test structures design and alignment marks.
Chapter 4

Fabrication & Packaging Results

This chapter describes the various challenges faced during the fabrication as well as packaging of the proposed test structures and how they were addressed using the tools available at SMFL, RIT. Some of the factors that governed the need for investigating alternate process flow were caused due to the fragile nature of the wafers (the process wafers were less than half the thickness of standard wafers), the need for protecting the layers on both sides of the wafer, and the constraints in the capabilities of the tools present in the SMFL. The following section describes the modified fabrication process.

4.1. Modified Fabrication Process

This section describes the modified process flow employed to fabricate the test structure and also provides the metrology results obtained during the process. It also provides details on the individual process parameters (e.g., etch time, process duration time) that were selected using the test wafers during the fabrication process.

4.1.1. Development for Lithography Level I

The fabrication challenges faced during lithography level I were disappearance of the alignment marks and cracks formed in the nitride layer. The following section
addresses how these problems were identified and solved. In the end of this section, a brief summary of the modified process is explained.

The fabrication process was started as proposed by cleaning the wafers, growing 527 Å of dry oxide and depositing 1550 Å of silicon nitride. The thickness of the layers grown and deposited was measured on both sides of the wafer throughout the fabrication process. The first lithography level I was performed on the backside of the wafer and followed by the nitride etch for 2.5 secs and oxide etch for 1.5 secs. The etch time of the layers was calculated by using a bare silicon wafer with a blanket layer of oxide. The photoresist was stripped in the Branson Asher tool. The wafers were etched in hot 20% KOH solution for 2 hrs 10 mins to define 108 µm deep microchannels. After performing the decontamination clean, the wafers were inspected. There was a small etch rate variation in the hot bath as the depth of the microchannels varied from top to bottom varied as 101.4 µm, 111.8 µm and 112.9 µm. The measurements were taken using the Tencor P2 profilometer to obtain the step height of the microchannels. After inspecting the wafer, it was observed that the channels were etched as desired but the alignment mark outlines were completely etched as shown in Figure 4.1. Hence, these alignment marks could not be used to align any further lithographic levels. Now, the process demanded modification to protect these alignment marks from being etched.
The process was modified by adding a few more steps to maintain the alignment mark geometry and also etch the microchannels in the hot KOH solution. After etching the nitride and oxide layer to open the channel region in silicon, a dry etch of silicon for 10 secs was performed to transfer the pattern of level I (from here on referred to as lithography level Ia) onto the wafer using the LAM490 tool. Then, the nitride and oxide layers were completely etched in hot phosphoric acid and 10:1 BOE solution, respectively. Now, the backside of the silicon wafer has the pattern of level I transferred onto the wafer along with alignment marks. This pattern is ~2000 Å deep on the wafer which was measured using the Tencor P2 profilometer. Again, 500 Å of dry oxide was grown and 1500 Å of silicon nitride was deposited on the wafer. The lithography level I (from here on referred to as lithography level Ib) was repeated on the backside of the wafer (i.e., the coat, exposure and develop process). Using a Q-tip dipped in photoresist, a manual coat of photoresist was applied on the wafer where the alignment marks and
directional arrows were located as shown in Figure 4.2. Also, a coat of photoresist was applied on the edge of the wafer to protect the nitride layer from getting etched in the LAM490.

![Figure 4.2 The backside of the wafer with manually coated photoresist on the alignment marks and directional arrows.](image)

After the manual photoresist coat on the alignment marks and on the edge of the wafer, a hot plate bake at 140°C was performed for 1 min. This was followed by the nitride etch and oxide etch to open the channel region while protecting the alignment marks region with photoresist. After stripping the photoresist, the KOH-based silicon etch was performed for 2 hrs 10 mins to define 100 µm deep microchannels.

During the inspection of the wafer after the hot KOH etch, it was observed that the channels were etched as desired and also that the alignment mark geometry was protected and hence retained for aligning subsequent lithography levels.

However, in the regions where the manual photoresist coat was applied, cracks were formed on the nitride layer as shown in Figure 4.3. Due to the fact that these cracks were localized to the thick photoresist regions, it was concluded that these cracks could have been caused due to the stress induced in the thick photoresist layer. After etching the complete layer of nitride and oxide, it was seen that the silicon was attacked in these
areas, resulting in small holes or small lines etched in the silicon. The cracks in the nitride layer provided an access path for the hot KOH solution to attack the underlying silicon. This problem of cracks in the nitride layer was eliminated by depositing a layer of TEOS on top of the nitride layer before the lithography level Ib.

![Figure 4.3 Cracks formed on the nitride layer.](image)

The following sub-section summarizes the above-described modifications from the commencement of the fabrication process to the successful fabrication of 100 μm microchannels on the back side of the wafer.

As illustrated in Figure 4.4, on the bare silicon wafers oxide was grown and nitride was deposited. This step was followed by lithography level Ia. In this level Ia, the pattern of the mask level I was transferred onto the backside of the wafer. This pattern was further transferred to the nitride and oxide layers by dry etch and wet etch process, respectively. Silicon dry etch was performed to transfer the pattern onto the silicon surface of the wafer. Then, the nitride and oxide layers were completely etched. At this point, the silicon surface had the pattern of mask level I etched on the surface. Again a new layer of dry oxide was grown and nitride layer was deposited. A layer of TEOS of
1 µm was deposited on the backside of the wafer as shown in Figure 4.5. Lithography level Ib was performed on the backside of the wafer. Manual coat of photoresist using Q-tip was done on the alignment marks, directional arrows and edge of the wafer. PR coat was followed by a hot plate bake. Figure 4.6 illustrates the cross-sectional view of the test structure with manual PR coat on the alignment marks. Then, TEOS etch, nitride etch and oxide etch were performed to open the microchannel region, but the alignment region was protected by the PR. After stripping the PR, the wafer was etched in hot KOH solution to create the microchannels. The resulting microchannels have trapezoidally-shaped cross section as shown in Figure 4.7. Decontamination clean was performed to avoid alkali contaminant transfer to clean room tools. Complete nitride layer and oxide layer was etched using wet etch process as the TEOS layer was etched in hot KOH solution.

Figure 4.4. Cross-sectional view of the test structure after lithography level Ia.

Figure 4.5 Cross-sectional view of the test structure before lithography level Ib.
4.1.2. Development for Lithography Level II

The fabrication challenges faced during the lithography level II were to protect the backside nitride layer from getting etched in the tool and to obtain a consistent coating of the photoresist on the backside of the wafer. The following section addresses how these problems were identified and solved.

After the completion of etched microchannels on the silicon wafer, the next stage was to define the diaphragm regions on the backside of the wafer. Dry oxide was grown and nitride layer was deposited. While etching the nitride layer from the front side of the wafer, it was observed that the back side nitride layer gets etched near the wafer...
periphery as the plasma in the LAM490 tool gets under the wafer. To protect the nitride layer on the backside of the wafer, a 1 µm TEOS layer was deposited on the backside of the wafer as shown in Figure 4.8. The wafer edge was coated with PR to protect the nitride layer. Hence, the nitride layer was etched successfully without etching the backside nitride layer. After PR strip, the oxide etch was performed in 10:1 BOE solution which etched dry oxide from the front side and TEOS from the back side. A layer of oxide was grown by wet oxidation on the front side of the wafer (as nitride inhibits the oxide growth on the back side of the wafer). While coating the PR on the backside of the wafer for lithography level II, it was observed that the standard recipe in SSI track gives an incomplete coverage of PR on the wafer due to the topography of the microchannels. To avoid any cracks on the backside nitride layer, a layer of TEOS (2000 Å) was deposited on the backside of the wafer. Figure 4.9 illustrates the cross-sectional view before lithography level II. The backside of the wafer was exposed in lithography level II in which a thick layer of PR was coated; hence, the exposure time was increased to 30 secs and the resist was developed using the standard recipe. Additional PR coat was performed using a Q-tip to protect the nitride layer on the edges of the wafers which was followed by hot plate bake. TEOS and oxy-nitride etches were performed in 10:1 BOE solution followed by nitride etch. Before the oxide etches, PR was stripped in hot solvent bath. Then, the oxide was etched from the backside and also, the TEOS layer was etched simultaneously since PR had been stripped. This reduces the loss of wet oxide from the front side of the wafer. Hence diaphragm region was defined in the nitride and oxide layer on the back side of the wafer as shown in Figure 4.10.
4.1.3. Development for Lithography Level III, IV and V

The fabrication challenges faced during lithography levels III, IV and V were to compute the silicon etch time in hot KOH bath for thin diaphragm and to measure polysilicon sheet resistance. The following section provides the details of these process parameters.
The polysilicon deposition was performed as proposed and dopants were introduced using spin-on-glass. After the thermal diffusion of dopants, spin-on-glass was stripped. The measured sheet resistance of the polysilicon layer was 58 Ω/square. Lithography level III was performed on the front side of the wafer. Level III was aligned to level II on the backside of the wafer using a backside alignment technique. After the polysilicon etch to define the resistors, a TEOS layer was deposited to define the contact cut regions using lithography level IV. An aluminum layer was deposited and patterned using lithography level V. A ProTEK™ adhesion layer, i.e., TEOS layer was deposited on the front side of the wafer. ProTEK™ was coated to protect the front side of the wafer from hot KOH solution. After a 6.5 hour-long silicon etch in hot KOH solution, a thin diaphragm of ~25-30 µm was achieved. After the decontamination clean, ProTEK™ strip and TEOS etch were performed.

4.1.4. Development for Lithography Level VI & VII

The fabrication challenges faced during lithography levels VI and VII were to characterize the process for consistent coating of Microspray™ SU-8 resist. The following section details the processing steps for the SU-8 resist.

On the front side of the wafer, the pressure taps are fabricated using 50 µm thick SU-8 resist. By performing repeated experiments, the process to spray coat the SU-8 resist to obtain the required thickness has been developed. Microspray™ SU-8 negative resist has been spray coated on the wafer three times and during each coat two perpendicular passes were made on the wafer. Each coat of resist was followed by hot plate bake at two different temperatures. Table 4.1 lists the details of the resist coat and
soft bake. The exposure of the SU-8 was carried out on a Karl Suss MA140 tool using UV filter for 3.5 mins. This lithography level VI was aligned to level I. The post-exposure bake was carried out at two different temperatures: the former one was at 65°C for 1 min and latter one was at 95°C for 7 mins. The SU-8 layer was developed in a SU-8 developer for 10 mins followed by IPA rinse, DI water rinse and dry. Table 4.2 lists the step height obtained on the various test structures using a Tencor P2 profilometer to measure the thickness of the SU-8 resist. This completes the fabrication of the smooth microchannel test structures.

The fabrication of the structured roughness features of 20 µm height was carried out in lithography level VII. Microspray™ SU-8 has been used to define these features and the process has been developed on a polished silicon wafer. This lithography level VII was aligned to level I. Table 4.3 lists the coat process for the defining the roughness features. Here also, one coat is referred to as the two perpendicular passes on the wafer. The exposure was carried out for 2.5 mins using UV filter in a Karl Suss MA140 exposure tool. The resist was developed in SU-8 developer for 5 mins followed by IPA rinse, DI water rinse and dry. When this process was performed on the actual test structure wafers, the roughness feature height was equivalent to the channel height. So, the coat process was limited to only one coat rather than two coats. This completes the fabrication process of the rough microchannel test structures.

<table>
<thead>
<tr>
<th>COAT</th>
<th>Delay</th>
<th>Bake 65°C</th>
<th>Bake 95°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>10 mins</td>
<td>2 mins</td>
<td>10 mins</td>
</tr>
<tr>
<td>II</td>
<td>7 mins</td>
<td>2 mins</td>
<td>10 mins</td>
</tr>
<tr>
<td>III</td>
<td>7 mins</td>
<td>2 mins</td>
<td>16 mins</td>
</tr>
</tbody>
</table>

Table 4.1 Details of 50 µm thick SU-8 coat parameters.
Table 4.2 Thickness of SU-8 layer obtained at different test structures.

<table>
<thead>
<tr>
<th>Test structure</th>
<th>SU-8 thickness (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>53.11</td>
</tr>
<tr>
<td>2</td>
<td>50.67</td>
</tr>
<tr>
<td>3</td>
<td>41.01</td>
</tr>
<tr>
<td>4</td>
<td>44.08</td>
</tr>
<tr>
<td>5</td>
<td>51.08</td>
</tr>
<tr>
<td>6</td>
<td>55.81</td>
</tr>
<tr>
<td>7</td>
<td>52.24</td>
</tr>
<tr>
<td>8</td>
<td>44.28</td>
</tr>
<tr>
<td>9</td>
<td>45.70</td>
</tr>
</tbody>
</table>

Table 4.3 SU-8 coat parameters for roughness features.

<table>
<thead>
<tr>
<th>COAT</th>
<th>Delay</th>
<th>Bake 65°C</th>
<th>Bake 95°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>10 mins</td>
<td>2 mins</td>
<td>10 mins</td>
</tr>
<tr>
<td>II</td>
<td>10 mins</td>
<td>2 mins</td>
<td>10 mins</td>
</tr>
</tbody>
</table>

The wafers were diced into nine test structure dies using a KS 780 dicing saw. Figure 4.11 illustrates the back side of the test structure and Figure 4.12 illustrates the front side of the test structure.
4.2. SEM Images of Microchannels

Using a scanning electron microscope (SEM), smooth and rough microchannel images were taken to inspect the fabricated test structures. Figure 4.13 illustrates the images of a smooth microchannel test structure. In the SEM image, it shows that the SU-8 layer is well cured over the test structure. The small misalignment of the level VI (fluid flow) with respect to level I (channel) is also seen. It can be also observed that the incomplete coverage of the photoresist lithography during level II led to silicon etching near the walls of the header region. Figure 4.14 illustrates an image near the diaphragm region of the pressure sensor on the back side of the wafer. This image is shown to represent the SU-8 layer when it is not completely cured. When the same test structure is observed under the microscope the SU-8 layer was found to be cracked at various locations, whereas the test structure shown in Figure 4.13 had no such cracks in the SU-8 layer.
The SEM images of the rough microchannels with structured roughness are illustrated in Figure 4.15. In this figure, it can be observed that the roughness feature height is equivalent to the channel height. After observing these images, the coat process in lithography level VII was modified. Figure 4.16 and Figure 4.17 illustrates the images.
of the rough microchannels. It can be observed that the pattern of the roughness feature has been transferred but the height of the roughness is more than desired, which would obstruct the fluid flow significantly in the microchannels.

Figure 4.15 SEM image of 500 µm wide microchannel with roughness features of 40 µm pitch.

Figure 4.16 SEM image of 160 µm wide microchannel with roughness features of 160 µm pitch.
4.3. Microchannel Geometry and Surface Analysis

This section presents the data obtained by using a Wyko optical profiler tool. Using an interferometry technique, the tool scans the surface and measures the step height of the feature. The smooth microchannel 160 µm wide was scanned to measure the width and height of the microchannel as shown in Figure 4.18. On the left side of the figure, a contour plot of the scanned feature is given. It can be seen that the Wyko tool cannot scan inclined surfaces and hence surface roughness of channel walls are unknown. Table 4.4 lists the microchannel dimensions of a 160 µm wide microchannel scanned along the channel length. Table 4.5 lists the microchannel dimensions of 500 µm wide microchannel. It can be seen that the channel width obtained is more than the designed value. This may be due to the lateral silicon etch in KOH solution which was not taken into consideration during the design of the geometry.

Figure 4.19 illustrates the contour plot of a rough microchannel with structured roughness features inside the microchannel. It was noticed in the SEM images that the
top surface of the roughness features was like a bow type and not flat. Hence, the Wyko tool was unable to scan the inclined surfaces of the roughness features.

Table 4.4 Smooth microchannel dimension and roughness.

<table>
<thead>
<tr>
<th>Location along the channel length</th>
<th>Width (µm)</th>
<th>Height (µm)</th>
<th>Roughness, Ra (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>164.9</td>
<td>147.9</td>
<td>0.63</td>
</tr>
<tr>
<td>2</td>
<td>160.7</td>
<td>151.2</td>
<td>0.79</td>
</tr>
<tr>
<td>3</td>
<td>152.9</td>
<td>147.7</td>
<td>3.62</td>
</tr>
<tr>
<td>4</td>
<td>155.8</td>
<td>145.4</td>
<td>1.07</td>
</tr>
<tr>
<td>5</td>
<td>157.8</td>
<td>157.4</td>
<td>2.59</td>
</tr>
<tr>
<td>6</td>
<td>158.7</td>
<td>145.8</td>
<td>1.92</td>
</tr>
</tbody>
</table>

Figure 4.18 Smooth microchannel dimension results obtained using Wyko tool.
Table 4.5 Smooth microchannel dimensions of a fabricated test structure along the channel length.

<table>
<thead>
<tr>
<th>Location along the channel length</th>
<th>Width (µm)</th>
<th>Height (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>546.7</td>
<td>124.2</td>
</tr>
<tr>
<td>2</td>
<td>547.7</td>
<td>128.8</td>
</tr>
<tr>
<td>3</td>
<td>548.7</td>
<td>140.0</td>
</tr>
<tr>
<td>4</td>
<td>536.0</td>
<td>132.7</td>
</tr>
<tr>
<td>5</td>
<td>539.9</td>
<td>130.6</td>
</tr>
<tr>
<td>6</td>
<td>533.0</td>
<td>141.6</td>
</tr>
<tr>
<td>7</td>
<td>523.2</td>
<td>139.7</td>
</tr>
</tbody>
</table>

Figure 4.19 Contour plot of rough microchannel obtained using Wyko tool.
4.4. Packaging

The two major components of the test structure, i.e., the microchannel and the pressure sensor, needed packaging to seal the microchannel and to create a reference pressure chamber for the pressure sensor. The packaging was first carried out for the reference pressure chamber and then microchannels were sealed. This section explains the packaging performed on the two sides of the test structure.

4.4.1. Reference Pressure Chamber Packaging

The front side of the test structure where the electrical connections of the pressure sensor are fabricated was used to create the reference pressure chamber for the pressure sensor. One of the major constraints while designing the packaging on the front side was to close the small gap between the metal bond pads and probes of the probe card. The components used for packaging on the front side of the test structure are ImageOn Resist (negative resist) and plastic with thermosetting glue.

ImageOn resist is 50 µm thick negative film type resist. The mask used to pattern the photoresist was made using Microsoft Visio and was printed on a clear transparency. The required size of resist film was cut using scissors to cover the front side of the test structure. By peeling the mylar film from the non-shiny side of the resist, the resist film was glued to the front side of the test structure. A hot plate bake was performed at 70°C for 45 secs while applying pressure on it. Once the film is adhered to the test structure, the top mylar layer is also removed. One more layer of resist was applied to create 100 µm thick reference chambers. The bake procedure was repeated again. The resist was
exposed in a Karl Suss MA140 tool for 30 secs. Once the exposure was completed, the top mylar film of the resist was removed and developed in CD-26 developer.

The plastic cover with the thermosetting glue on one side was used to close the reference chamber. The required size of the plastic cover was cut and was placed on the top of the ImageOn resist on the test structure. Using a heat gun, heat and pressure were simultaneously applied for the adhesion of plastic and resist film. This completed the packaging of the front side of the test structure, i.e., enclosing the reference pressure chamber of the pressure sensor.

4.4.2. Microchannel Packaging

The back side of the test structure was packaged to close the microchannel, pressure taps and the sensors. The various components used for packaging were a 5 cm X 5 cm X 0.24 cm polycarbonate plastic (Lexan\textsuperscript{TM}), 2” wide double sided polyimide tape (Kapton\textsuperscript{TM} tape), hose fittings (Swagelok NY-305-2 and NY-405-2) and Loctite\textsuperscript{TM} clear epoxy.

Lexan\textsuperscript{TM} plastic acted as the cover plate in which 1/8” holes were drilled corresponding to the header regions and sensor fluid port region. The double-sided Kapton\textsuperscript{TM} tape was cut to the dimensions of the test structures and holes were punched through it corresponding to the cover plate holes. The holes were punched using a hole puncher. One side of the double-sided tape was applied to the Lexan\textsuperscript{TM} plate and then the other adhesive side was attached to the test structure while applying pressure. Once the test structure got adhered to the tape, then Loctite\textsuperscript{TM} epoxy was applied on the edges of the test structure. The hose fitting were glued to the Lexan\textsuperscript{TM} plate using the Loctite\textsuperscript{TM}
epoxy. Figure 4.20 illustrates the various packaging components and packaged images of the test structure.

![Images](image1.png)

Figure 4.20 (a) Lexan™ plate with drilled holes, (b) Kapton™ tape with punched holes, (c) packaged front side of the test structure, (d) packaged backside of the test structure and, (e) packaged backside of test structure with hose fittings.

### 4.4.3. Packaging Results

The packaging technique used to create the reference pressure chambers for the pressure sensors was successfully implemented. The packaging technique used for closing the microchannel was successful for two cases but not for one case. In case (i),
the packaging technique was applied for a test structure which has a layer of oxide and nitride with the microchannel etched in the silicon wafer. In this case, the technique worked well to hold 50 kPa of pressure drop across the test structure. In case (ii), the packaging technique was implemented on a test structure in which a layer of 50 µm thick SU-8 resist was coated on a polished silicon wafer. In the SU-8 layer, mask level VI was patterned in which a microchannel with pressure taps leading to the pressure sensor regions was present. In this case (ii), it was checked whether the packaging technique can provide a good seal when DI water was passed through the microchannel and prevent internal flooding from occurring (i.e., between any two pressure taps, between channel header and pressure taps, between any two sensor fluid ports, etc.). It was successfully verified that no internal flooding occurs in the test structure when DI water passes through the microchannel. In the case (iii), the packaging technique was implemented on the fabricated test structure with the microchannels and pressure sensors. It was observed that there was internal flooding between pressure taps, header region to pressure taps, etc. The inadequate sealing in case (iii) might have resulted due to the non-uniformities on the test structure. The case (iii) test structure was subjected to different processing techniques such that the non-uniformity on the test structure could not be compensated by the polyimide tape which was used as the interface material between the Lexan™ plate and test structure. The same interface material was able to conform to the SU-8 coated surface on the polished silicon wafer in case (ii). The cross-sectional views of the different cases (i), (ii) and (iii) used to verify the packaging technique is represented in Figure 4.21.
Figure 4.21 Cross section of the different test structures cases used to verify the packaging technique. The proposed packaging technique worked for case (i) and (ii) but not for case (iii).
Chapter 5

Experimental Setup & Results

This chapter explains the components used for setting up the experimental loop for characterizing the fabricated MEMS pressure sensor. Experiments were also performed to validate the experimental setup designed using smooth microchannels. The first section describes the fluidic components and electrical components in the experimental setup. Special emphasis was placed on the various parts that were designed and machined to hold the test structure and other components. The second section explains the results that were obtained while calibrating the pressure sensors and from smooth microchannels.

5.1. Experimental Testing Setup

The experimental setup designed for testing the fabricated test sections consists of the following major components: syringe pump, two commercial pressure sensors, two thermocouples, two reservoirs of DI water, 48 pin probe card, 48 pin edge card, a bread board and a data acquisition system.

A test section block was designed and machined to hold the packaged test structures in fixed place while performing the experiments. Figure 5.1 illustrates the schematic of the test section block designed to be fixed on an x-y stage. The test structure is placed in the slot on the top piece of the test section block with the front side facing up.
Insulation tape was used to anchor the test structure in the top part of the test section block.

![Figure 5.1 Schematic of the test section block.](image)

Figure 5.1 Schematic of the test section block.

Figure 5.2 illustrates the block diagram of the experimental setup used for testing the test structure. The syringe pump, commercial pressure sensor and temperature sensors at the inlet and outlet of the test structure, and a reservoir were all connected using Clippard 3814-6 clear tubing. For the electrical connection to the test structure, the metal bond pads on the test structure were connected via the probes of the 48 pin probe card which was fixed on a z stage. During the course of testing, a microscope was used to align the probes to the bond pads by adjusting the x-y stage. Once the alignment was done, the probe card was lowered using the z stage. To anchor the probe card on the z stage, a probe card holder has been designed and machined using aluminum material. Figure 5.3 illustrates the probe card holder assembly which consists of a T-section plate mounted on the z stage and two arms of the T-section plate to hold the probe card. A 48-
pin edge card was connected with the probe card and wires were soldered to the edge card. The voltage supply wires and output signal were separated on a breadboard. A voltage of +5 V was supplied using a power supply to all the pressure sensors (MEMS fabricated pressure sensors and commercial power sensors). The output signal was recorded using a data acquisition system. A NI-SCXI 1000 chassis was used with a NI-SCXI 1300 card for reading the output signals of pressure sensors and a NI-SCXI 1303 card for reading the temperature of the thermocouple. The schematic of the Labview program used to acquire the data is shown in Figure 5.4. The program was written to acquire voltage data when the calibration of the sensors was carried out and to acquire pressure data when the experiments were conducted. Figure 5.5 represents the workplace where the experiments were performed.

Figure 5.2. Basic components of the experimental test setup loop.
Figure 5.3 Schematic of the probe card holder assembly.

Figure 5.4 Schematic of the Labview program used to collect the data.
5.2. Results

5.2.1. Pressure Sensor Calibration

As the packaging technique was inadequate to provide a good seal for the test structure, the fluidic experiments were not conducted on them. The internal leak inside the test structure did not prevent the calibration of the fabricated pressure sensors.

All the sensor fluid ports and outlet header port were closed. The pressure sensor calibrator was connected to the inlet header port. The voltage was supplied using the power supply to the sensor and the voltage drop across the resistor network was recorded.
The pressure was increased in fixed intervals and the change in voltage was recorded. Figure 5.6 represents the graph plotted to calibrate the MEMS pressure sensors. It can be observed that the slope of the plot increases up to 35 kPa but then decreases. The experiments could not be extended beyond 45 kPa as the silicon die in the test structure cracked and started leaking. This may be due to the incomplete packaging of the test structure.

![Graph](image)

Figure 5.6 Graph plotted to calibrate the fabricated MEMS pressure sensors.

5.2.2. Validation of Experimental Setup Using Smooth Microchannel

The experiment setup that had been designed and assembled was validated by using a smooth microchannel test structure. A 500 μm wide and 100 μm deep trapezoidal channel was considered for performing the experiments. This channel with hydraulic diameter of 155 μm was packaged and experiments were performed at room temperature.
(23°C). Only the inlet and outlet pressure sensors were monitored for the pressure drop across the test section. The non-dimensional pressure measurement parameter, friction factor, was considered to compare the experimental data with the theoretical equation line. The study was limited only to fully developed laminar flow. This was monitored by continuously checking entrance region length to the microchannel length \((L_h < L)\) for a given mass flow rate. Using equation (4), the theoretical line of Fanning friction factor was plotted for different Reynolds number. The pressure drop results obtained were used to compute the experimental friction factor using equation (5). Figure 5.7 illustrates the graph plotted using experimental friction factor data and theoretical friction factor data.

![Figure 5.7 Plot validating the experimental setup using microchannel of 155 µm hydraulic diameter.](image-url)
The data obtained is a good match to the theoretical behavior; however, the theoretical equation used for the friction factor is for rectangular channels and the microchannel used for experiments has a trapezoidal cross section. This leads to some variation between the experimental data and theoretical behavior. As the trend of the experimental results matches with the theoretical data, the experimental setup is hence validated for future experiments.
Chapter 6

Conclusions

The integration of semiconductor fabrication techniques for understanding the fluid dynamics in the microscale level has been the prime focus of this research. The following objectives have been achieved during the course of this pioneering work.

- A test structure with MEMS pressure sensors along the microchannel length has been designed to understand pressure losses occurring in smooth and rough microchannels.

- A fabrication process flow has been developed to fabricate the test structure with the available tools in the SMFL at RIT. The challenges encountered during the fabrication process have been successfully identified and rectified to achieve the desired results. Some of these challenges include the disappearance of alignment marks, cracking of the nitride layer and protecting both sides of the wafer during the process.

- The fabrication of smooth microchannels and rough microchannels (with structured roughness) along with the MEMS pressure sensors has been successfully accomplished.

- One of the key features of the fabrication process was to use Microspray™ SU-8 resist for defining pressure taps and roughness features. The process characterization was done to achieve the target thicknesses using SU-8 resist.
- A packaging technique using Kapton™ double-sided tape has been proposed and successfully implemented for some test structures with different layers on the silicon substrate. The packaging technique did not work for the fabricated smooth and rough test structures, but possible failures modes have been identified.

- An experimental setup consisting of fluidic and electrical components has been designed and implemented to test the fabricated test structure. Validation of the experimental setup has been performed using a smooth microchannel etched on the silicon surface.

The fabrication of the roughness features in microchannels provides a solid foundation towards the understanding of the roughness effects at microscale level. In order to study the fluid flow behavior in the rough microchannels, this research can be further extended by investigating appropriate leak-proof packaging techniques for the fabricated test structure.
References


Appendix A

RIT Microelectronics Engineering
Test Section Block - Bottom part

Tushara Pasupuleti
Date 09/24/09

All the dimensions are in cm

Scale 0.25
Drawing no. 1

#8-32 screw
RIT
Microelectronics Engineering

Test Section Block - Top part

Tushara Pasupuleti
Date 09/24/09

All the dimensions are in cm

Scale 0.25  Drawing no. 2

#8-32 screw

0.3125

0.1360

0.164

0.20

1.00

5.20

4.00

8.00

1.00

8.00

5.20

4.00

1.00

3.50

1.00

0.60

1.40

1.00
Appendix B

RIT Microelectronics Engineering

Probe Card Holder - Middle part

Tushara Pasupuleti
Date 09/24/09

All the dimensions are in cm

Scale 0.20 Drawing no. 3