6-1-1971

An Audio Oscillator Triggering Circuit for the EG&G 501 High Speed Stroboscope; with Integrated Digital Timing

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AN AUDIO OSCILLATOR TRIGGERING CIRCUIT FOR THE EG&G 501 HIGH SPEED STROBOSCOPE; WITH INTEGRATED DIGITAL TIMING

by

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A thesis submitted in partial fulfillment of the requirements for the degree of Bachelor of Science in the School of Photographic Science in the College of Graphic Arts and Photography of the Rochester Institute of Technology

June, 1971

Thesis Advisor: Dr. Schumann

ACKNOWLEDGMENTS

I would like to express my deep appreciation to all the people who have assisted me in the execution of this research project.

I thank Professor John F. Carson for informing me of the need for this instrumentation. Also for his assistance during my endeavor.

I thank Dr. Schumann for his patience and co-operation during my endeavor.

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ABSTRACT

A timing generator was designed and built for an EG&G 501 High Speed Stroboscope. The generator delivers a burst of one, two, four or eight pulses at a selected repetition rate from .5HZ to 20KHZ; upon initiation by a start signal. An Unijunction Transistor (UJT) oscillator provides the basic repetition rate and Integrated Circuit (IC) Digital Logic is used to count and gate the output pulses. The circuit diagrams and construction details are given.

INTRODUCTION

High speed photography has been around for quite some time, but new and improved methods of operational systems are constantly being sought. Presently with the EG&G 501 High Speed Stroboscope operating times are determined by mechanical switching, an event delay switch is used in conjunction with camera monitoring. The camera monitoring system utilizes a relay type switch which opens and closes to apply a signal which fires the 501 unit. There are those who would say that this is beautiful, because of the synchronizing between picture frame and flash exposure; do to the action of the camera monitoring system. The year is now 1971 and this type of system is obselete. Relay contact arms float, more often than not, at high spatial frequencies. At any rate, the EG&G 501 system cannot begin to operate with an output of one, two, four or eight pulses at any frequency within the audio region. It has been my objective to add this capability to the system; only solid state components have been used. This

intricate timing has only become feasible with the introduction of digital circuitry; both discrete and intergrated.

The High Speed Stroboscope type 501 is designed to produce high-intensity light flashes at rates up to 6000 flashes per second, with a minimum flash duration of 1.2 microseconds. This type of lighting is admirably suited to applications which demand that motion be virtually stopped on film, as in the qualitative study of fast moving phenomena as shock waves and the flight of projectiles. High-speed motion pictures of rapid events obtained with electronic flash apparatus can have greater definition than films of the same events obtained with continuous lighting. In addition, the filming of subjects susceptible to damage by heat is sometimes allowed due to the relative coolness of stroboscopic lighting.[1]

The operation of the system is given in the section entitled " Instrumentation ". Within this section are eight diagrams which explain the basic operation of the system.

The oscillator and its power supply were assemblied first. Then came the IC pack division module power supply along with the division module. The final stage was one of setting up the required array of electrical events.

INSTRUMENTATION

Two seperate power supplies were needed, one for the unijunction oscillator circuit (figure 1), the other for the IC pack. The IC pack power supply is shown in, figure 2.

Within the unijunction oscillator power supply resistor R1 (carbon) can vary the output voltage,under load, from 34 volts at its minimum resistance of zero, to 15 volts at its maximum value of 10K ohms. The oscillator has only a voltage criteria; with the current required for oscillation being quite low (less than 30 milli amperes). This fact allows the value of capacitor C1 to be small (470 microfarads). In contrast, within the IC pack power supply a value of 6200 microfarads was necessary. The equation for power supply capacitance is allways a function of filtering and output current required for the specific load. Within the IC pack division module (figure 4) each IC draws at least 30 milli amperes at its operating point. This sets a minimum power supply output current of 120 milli amperes, which is critical. An IC pack can be destroyed at 8 volts or current on the order of 50 milli

amperes.

The output from the oscillator circuit (point 1, figure 3) is fed into point A of the IC pack division module (figure 4). The output from point 1 is a good first order approximation to a positive Dirac delta function. Point A is one lead of a computer logic nand gate. The nand gate results from the cascading of the computer not plus and logic. Assuming the IC pack module is receiving its correct power, point A requires a minimum voltage of 3 volts for correct logic operation. This 3 volt requirement must be met for all operating frequencies. Also, for a fixed output voltage to the oscillator circuit, the voltage at point 1 decreases with increasing frequency. The frequency is increased by decreasing resistor R1 (figure 3, 500K ohms maximum, zero minimum). The nature of the unijunction transistor accounts for the decrease in output voltage with increasing frequency; for any set oscillator supply voltage. Fortunately, with the minimum voltage output from the oscillator power supply and a operating frequency of 5KHZ, resistor R2 (figure 3) can be adjusted to meet the minimum criteria of point A

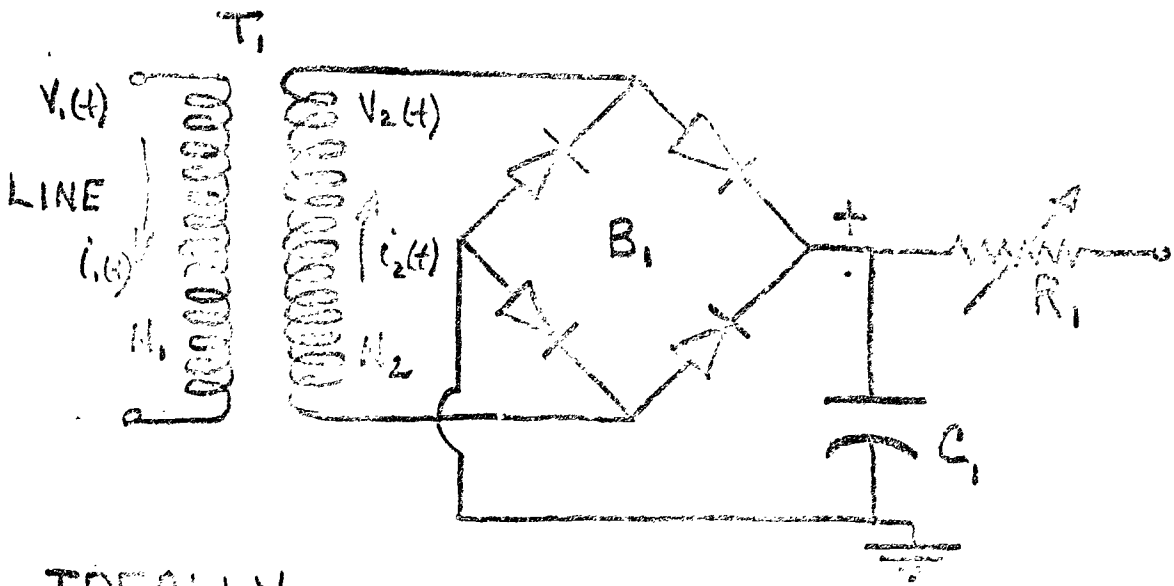
(figure 4). This means that the system can operate properly throughout the entire audio region at an oscillator power supply output voltage less than the maximum obtainable.

The IC pack division module (figure 4) is the heart of the counting system. There are four seperate IC packs within the division module. Each is of the fourteen pin dual inline type. Within the division module are 3 Texas Instruments ICs and 1 manufactured by Stromberg Carlson (Rochester). Stromberg Carlson list there ICs as SC number. Texas Instruments list there ICs as SN number. IC's used are SC 1046, a quad two input nand gate; along with 1 SN74H73 and 2 SN74H78 ICs. All 3 Texas Instrument ICs are Dual J-K Master-Slave Flip-Flops. The division module is most readily understood on a mathematical plane. When point B (figure 4) is at logical 1 (approximately Vcc) and point A is receiving the required positive Dirac delta function, a negative Dirac delta function is present at point C. This is a necessary condition for the operation of the division module. Each division stage alternates it's output from

logical 1 to logical zeroin a binary manner; with the point C criteria being met. Each division output represents a frequency of the reciprocal of 2 to an exponent. The first division output frequency is 1 over 2 to the zero power (1) multiplied by the input frequency at point C, or the oscillator frequency. The next division output equation incorporating 2 to the first power resulting in a division output frequency of one half the oscillator frequency. In this manner 1, 2, 4 and 8 pulses to the EG&G 501 unit may be obtained. The order of an array of electrical events becomes imperative at this point. The clear bus (figure 4), when momentarily shorted to ground, returns all of the division outputs to logical zero. The clear bus and reset switch are tied together, therefore pushing the reset switch is equivalent to pushing the clear bus. Both actions are accomplished simultaneously. The start button when pushed, intiates the digital timing operation. With the oscillator signal present at point A (figure 4) the operational sequence is as follows: the start button is pushed, point B goes to logical one; point C is producing

a negative Dirac delta function, the EG&G 501 unit is being fired and depending on which position switch S1 is in the division output will not change from logical zero to logical 1 until 1, 2,4 or 8 pulses have reached the EG&G 501 unit. Assume that switch S1 is in position 4. This implies that after 8 pulses of energy have entered the 501 unit , position 4 of switch S1 will suddenly change from logical zero to logical 1. This point is connected to the anode gate of a silicon controlled rectifier (SCR). Therefore when position 4 of S1 is at logical 1 (approximately Vcc) the SCR will immediately short to ground. This will place point B at logical zero. which immediately stops signals C and D. To stop the SCR from heavy conduction the reset button is pushed. It is mandatory that this last operation be done immediately. Remembering that the reset and clear lines are tied together; pushing the reset button places a logical zero state on the SCR anode gate, due to the clear bus action, and also places point B at logical zero; due to the flip-flop action of the set reset system. This flip-flop action, which results from the cross coupling of 2 nand gates, is explained in figure 6.

(Figure 1)



IDEALLY

$$\frac{V_1(t)}{V_2(t)} = \frac{N_1}{N_2} = \frac{i_2(t)}{i_1(t)}$$

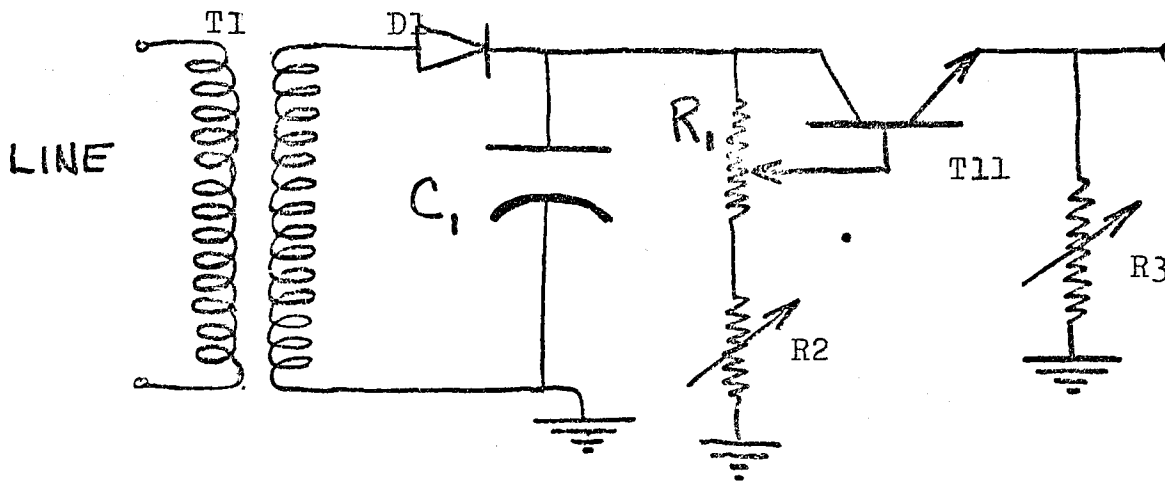
T1 - Primary 55A , 117V Secondary 24v (eff) 1A

B1 Motorola Integrated Bridge

C1 470 micro farads

R1 0-10K ohm (carbon)

(Figure 2)



T1 Primary 117V 60 HZ Secondary 6.3V (eff) 1.2A

R1, R2, R3, 0-10K ohm(Carbon)

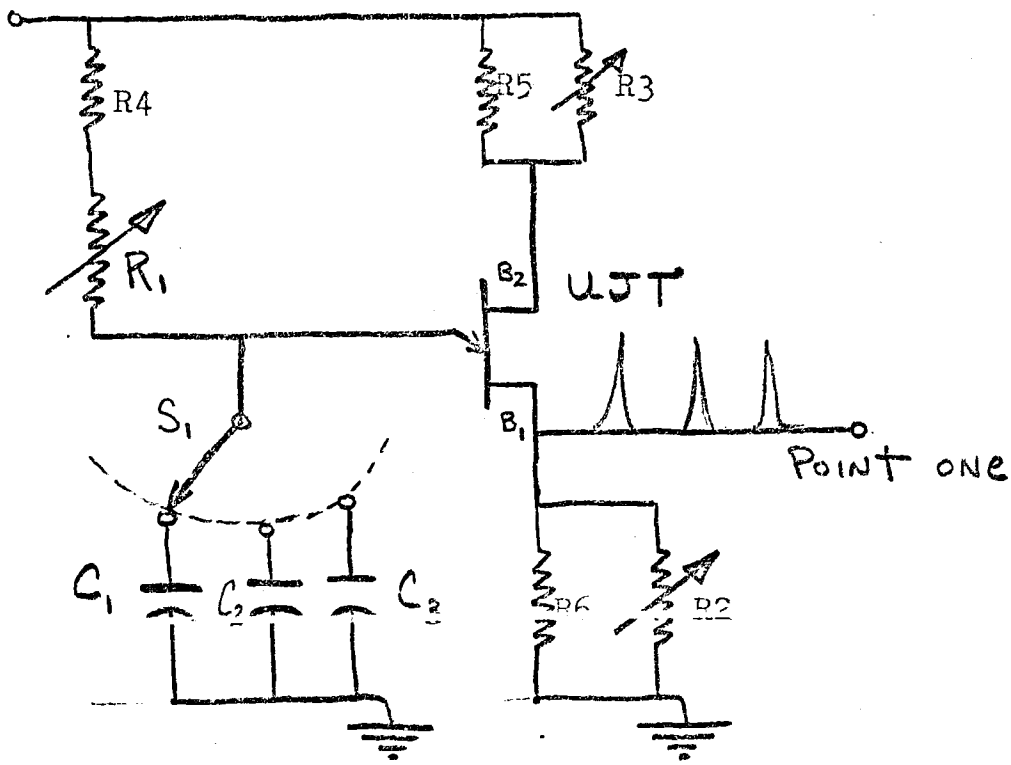
R3 - Quasi load

R1 - varies the conduction of T1

R2 - set minimum conduction of T1

T11 - power transistor , CALE CTRO K4- 526

(Figure 3)



R4-.2200 ohms

R1- 0 - 500K ohms
R5 - 820 ohms

R3 - 0- 10K ohms

R6 - 30 ohms

R2 - 0- 1k ohms

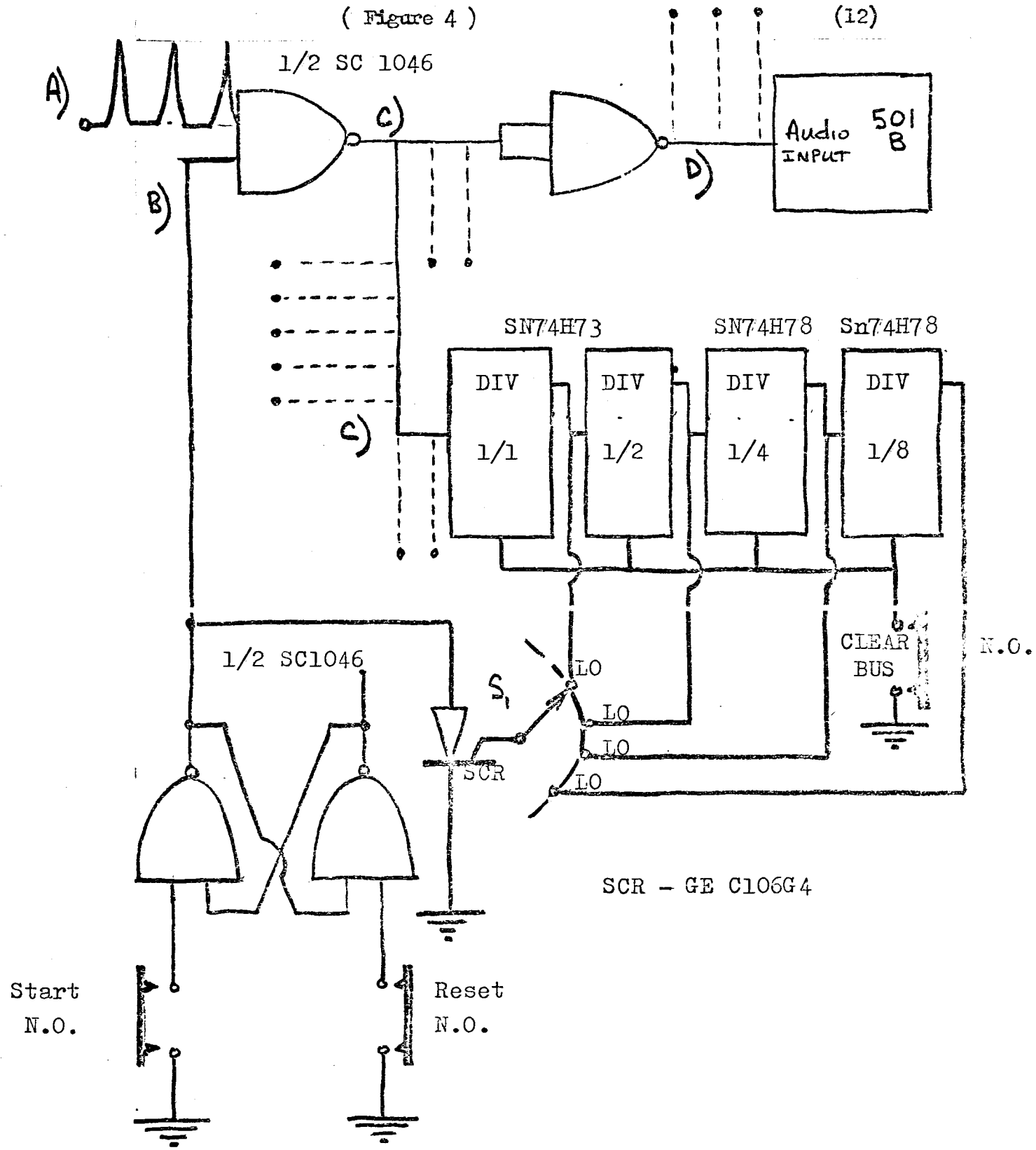
UJT-2n491 Texas Instruments

C1-.2micro farads (low frequencies)

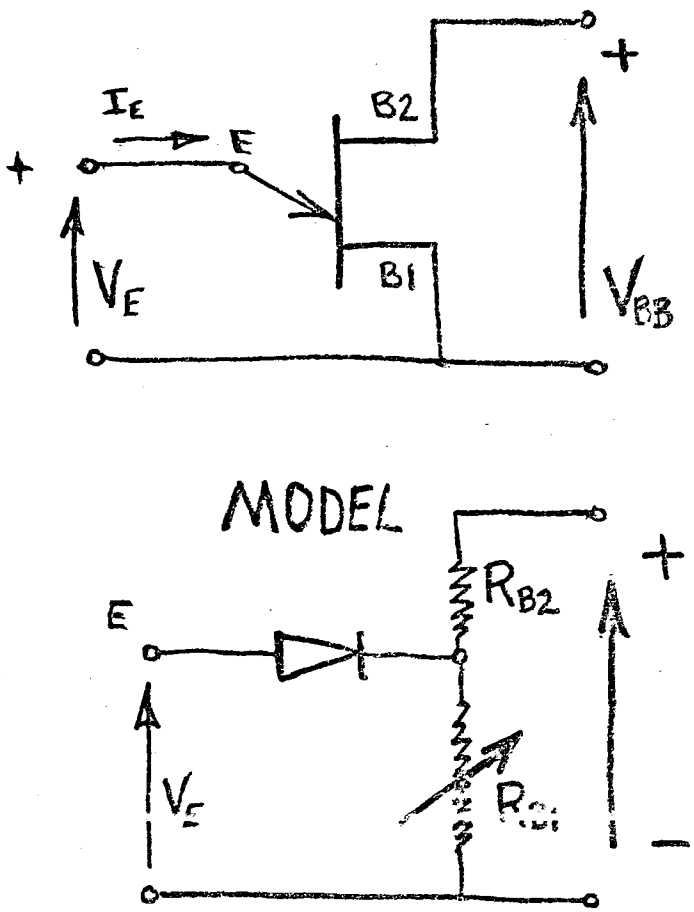
C2 - 0.1 micro farads (mid band)

C3 - 0.02 micro farads (high audio)

(Figure 4)

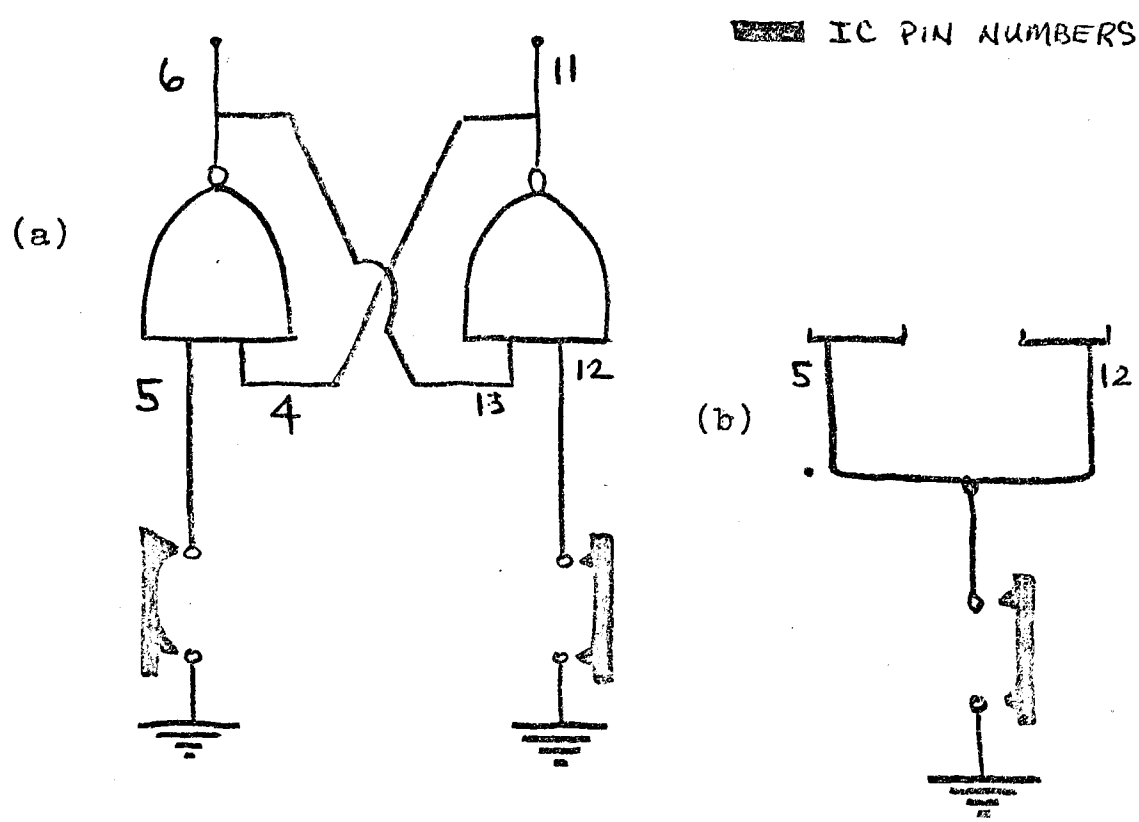

A)
1/2 SC 1046
C)
B)
D)
Audio INPUT
501 B
SN74H73
SN74H78
Sn74H78
DIV 1/1
DIV 1/2
DIV 1/4
DIV 1/8
C)
1/2 SC1046
S1
LO
LO
LO
LO
CLEAR BUS
N.O.
SCR
SCR - GE C106G4
Start N.O.
Reset N.O.

(Figure 5)



When a positive potential at point E forward biases D1 an output will result. Refer to oscillator circuit (figure 3). Each capacitor, C1 thru C3, when connected (seperately) forms a RC time constant which determines the minimum time to reach the forward bias potential needed at point E to obtain an output. In this manner the audio frequency region is scanned.

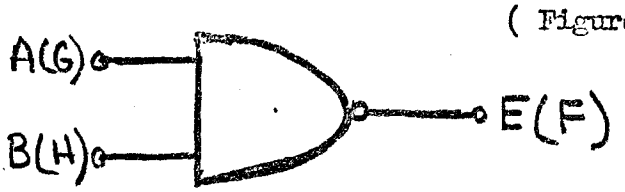
(Figure 6)



Circuit a is a basic flip flop, obtained from the cross coupling of two nand gates.

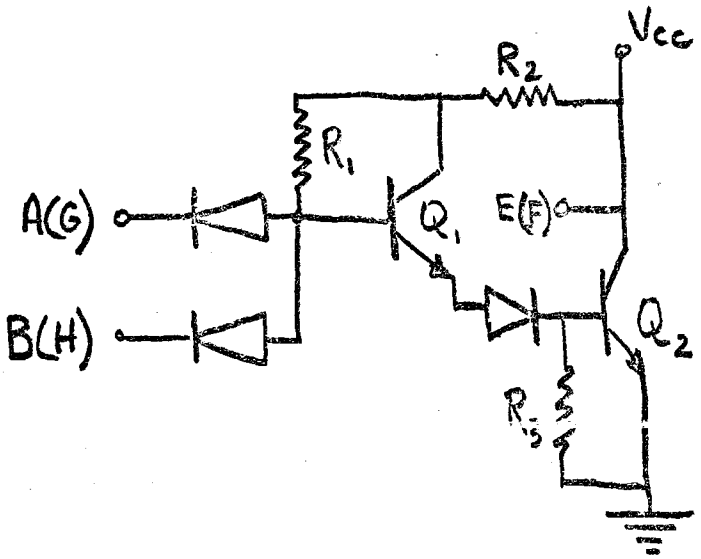
Circuit b is basically the same circuit as in a except two leads have been tied together so that binary divison will result when a signal is applied to the common input (open and close the switch) This is commonly seen as the clock input on many ICs and is sometimes denoted as the toggle lead.

(Figure 7)



$E = \overline{A \cdot B} \Rightarrow E = \text{NOT } A \& B$

$F = \overline{G \cdot H} \Rightarrow F = \text{NOT } G \& H$



TRUTH TABLE

A	B	E
G	H	F
1	1	0
0	1	1
1	0	1
0	0	1

(Figure 8)

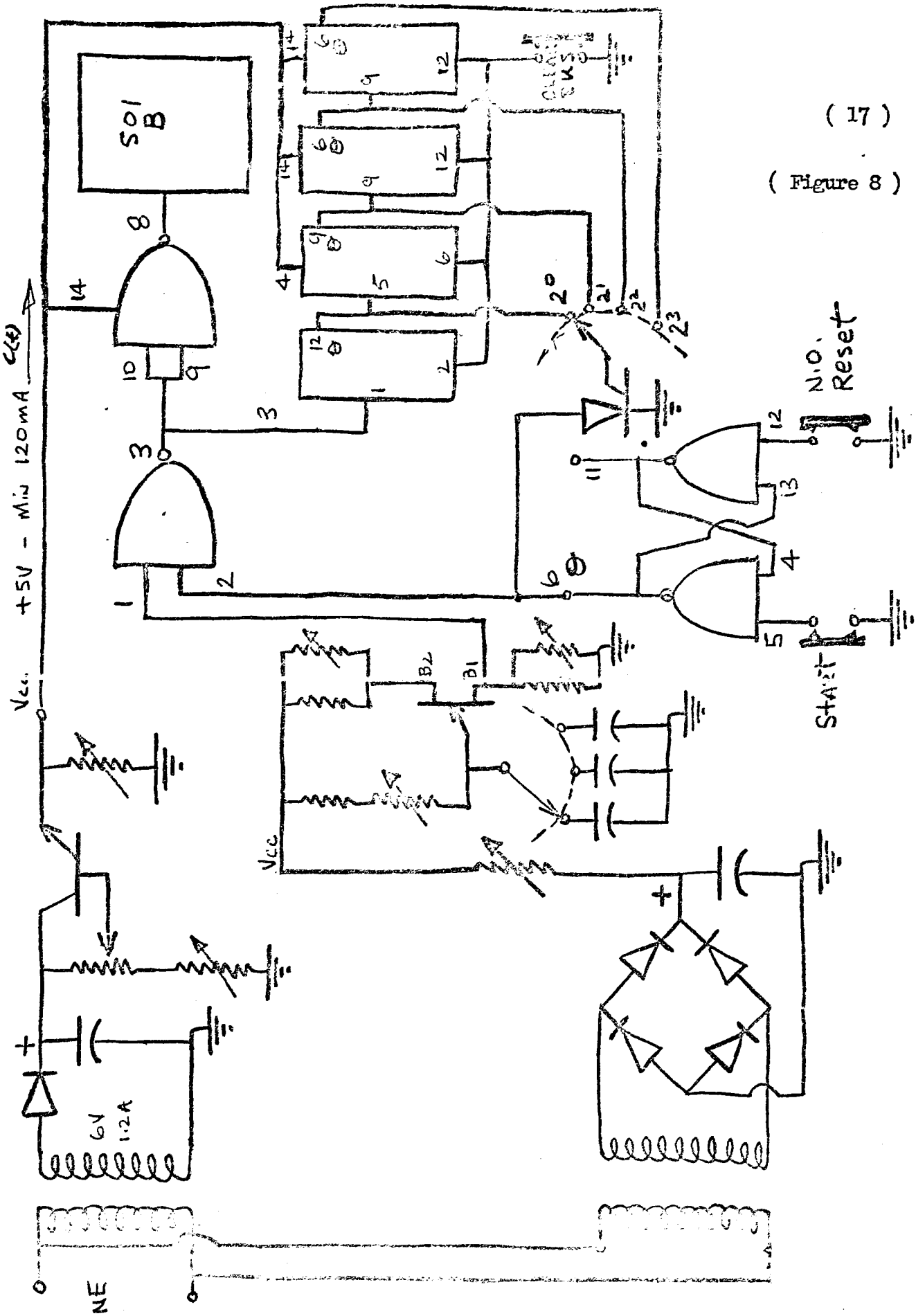


FIGURE EIGHT

RESULTS

Positive proof of system operation is not available;for lack of time.

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BIBLIOGRAPHY

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Wiesmer, Patrick E. "PRACTICAL TRANSISTOR THEORY" Howard W. Sams & Co., Inc.

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APPENDIX 1

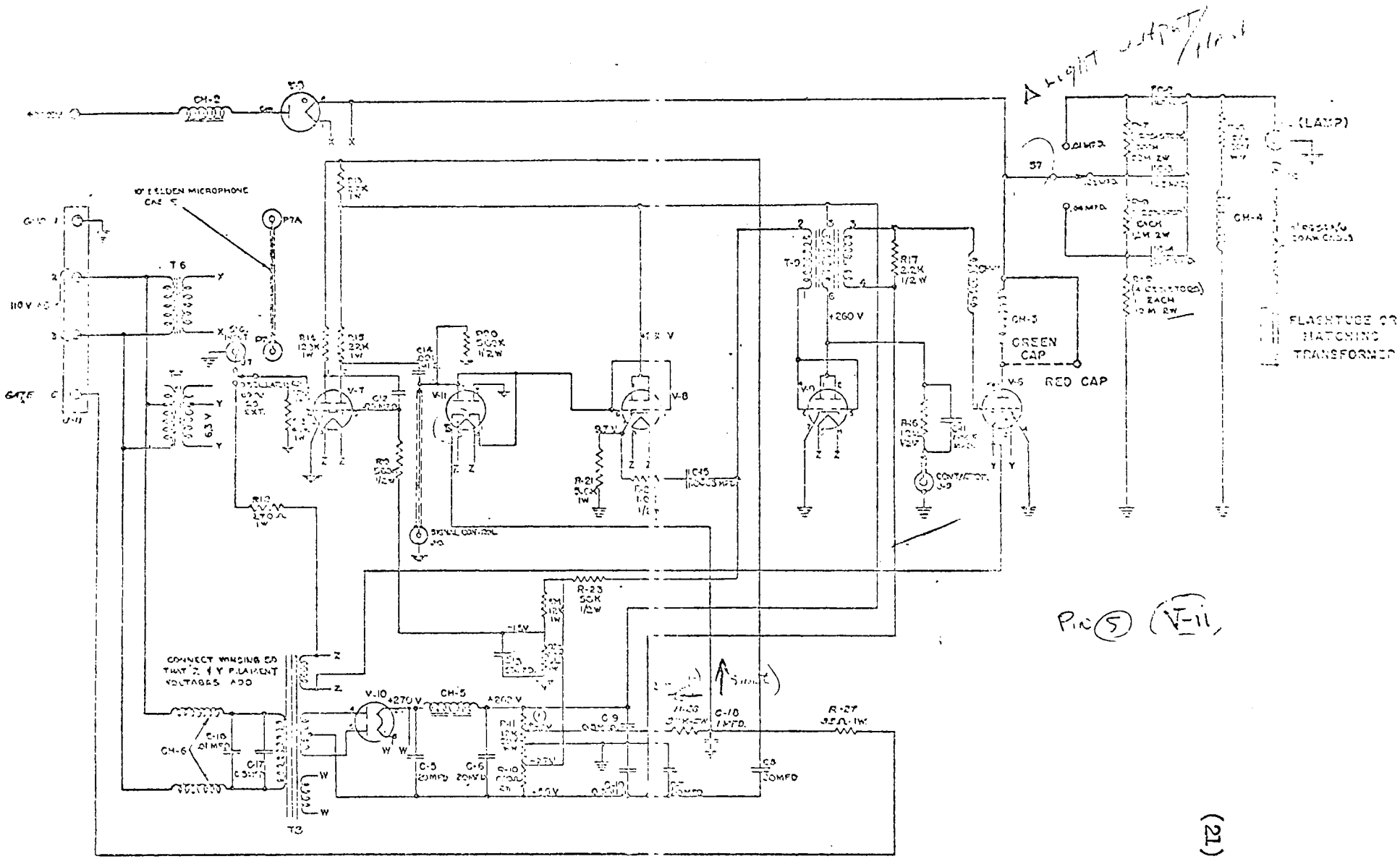
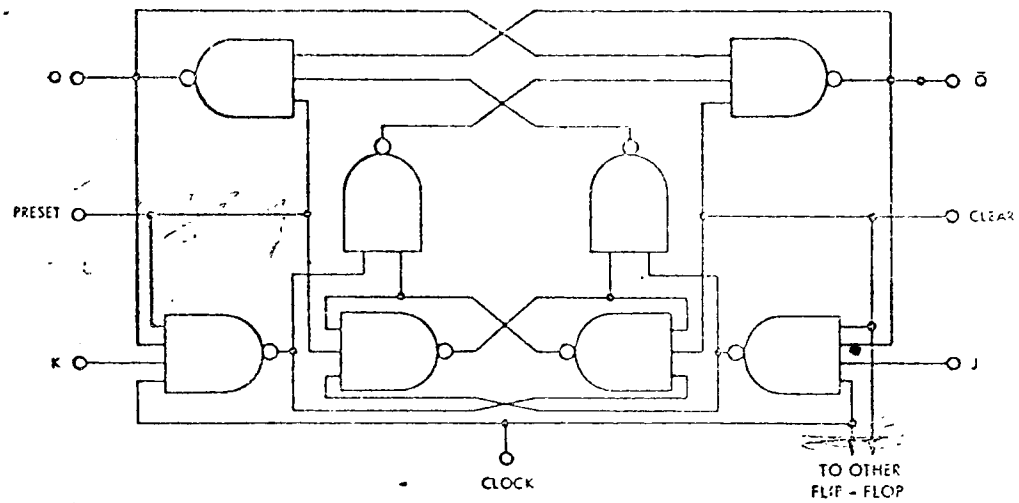
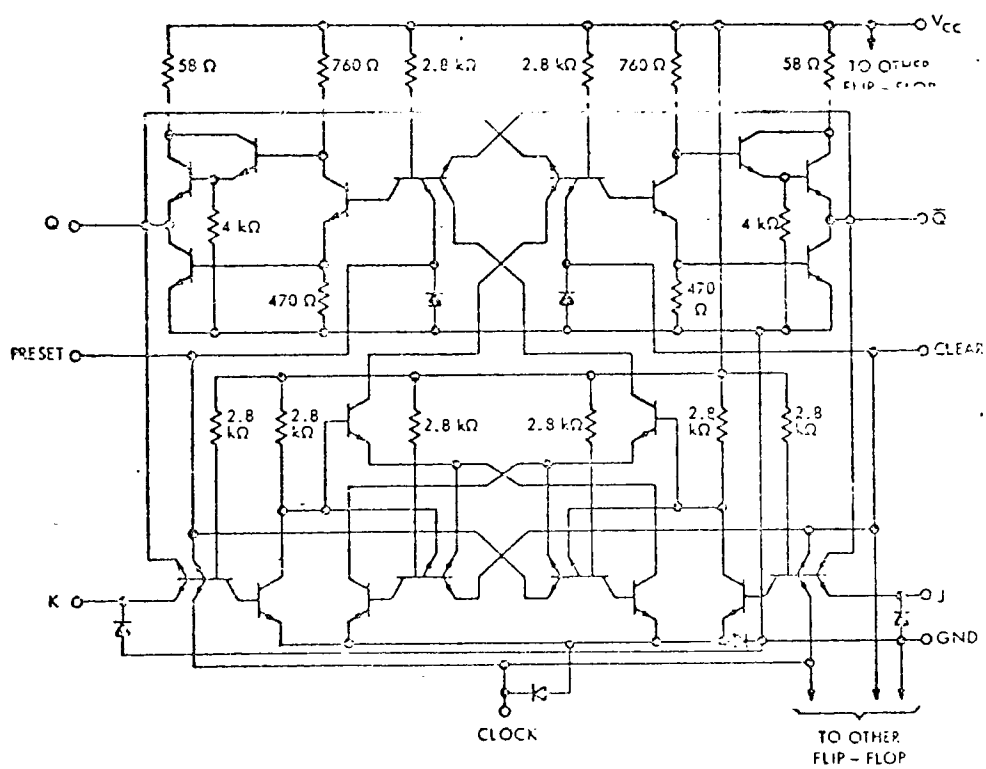


Fig. 2 Schematic Diagram - Modulator Unit, High Speed Stroboscope Type 501

functional block diagram (each flip-flop)

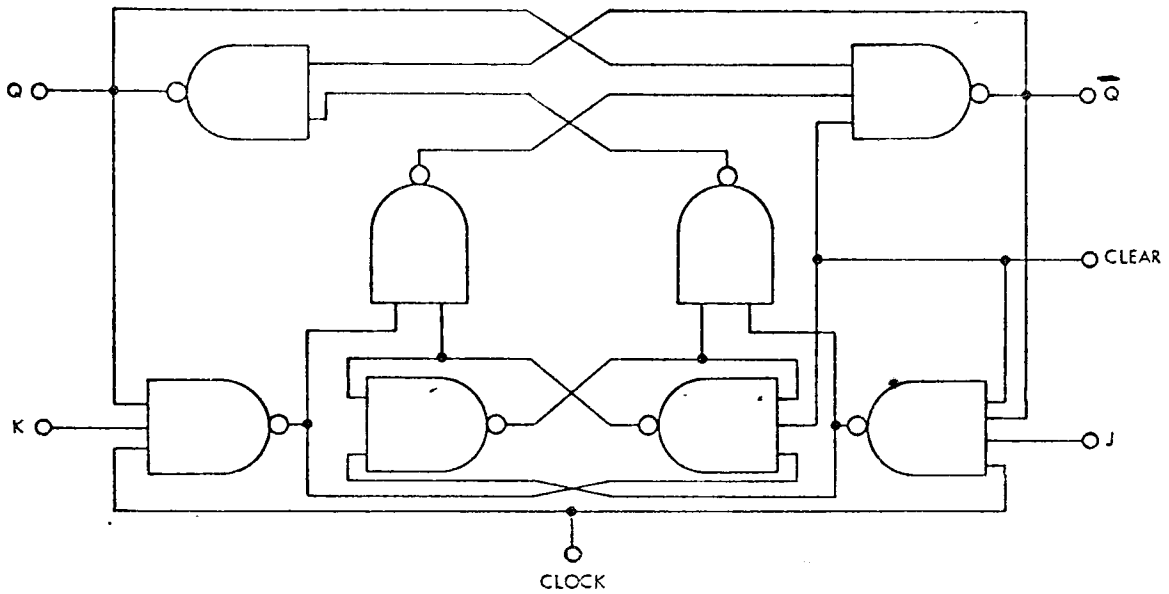


schematic (each flip-flop)

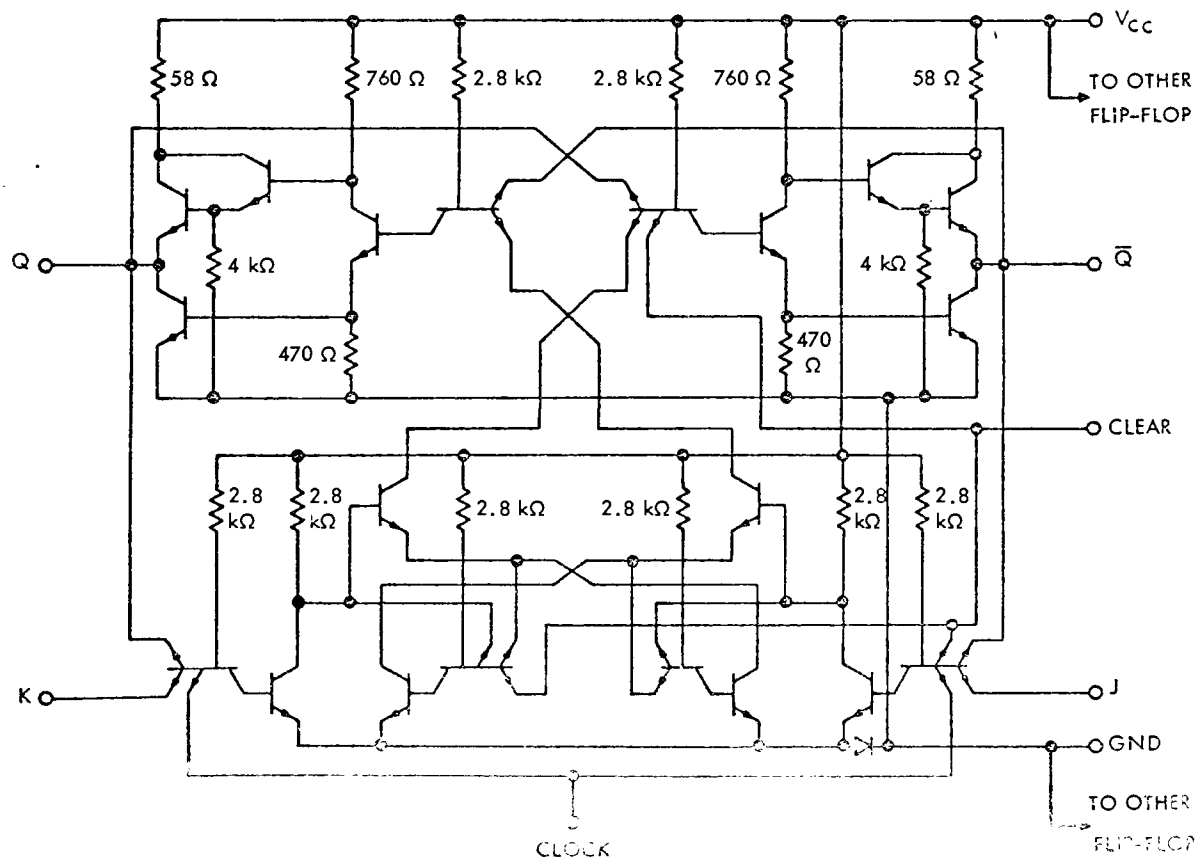


Component values shown are nominal.

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP §	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	57 and 58	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	57 and 58	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	57	V_{CC} = MIN,	I_{load} = −500 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	58	V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	59	V_{CC} = MAX,	V_{in} = 0.4 V			−2	mA
$I_{in(0)}$	Logical 0 level input current at clear	59	V_{CC} = MAX,	V_{in} = 0.4 V			−4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	60	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	60	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	60	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{os}	Short-circuit output current‡	61	V_{CC} = MAX,	V_{in} = 0	−40		−100	mA
I_{CC}	Supply current	60	V_{CC} = MAX			32	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	68	C_L = 25 pF,	R_L = 280 Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	69	C_L = 25 pF,	R_L = 280 Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	69	C_L = 25 pF,	R_L = 280 Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	68	C_L = 25 pF,	R_L = 280 Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	68	C_L = 25 pF,	R_L = 280 Ω		22	27	ns

— SEE ORDERING INSTRUCTIONS PAGE 1504 —

APPENDIX 2

Industry does sell defective IC packs; the novice should be aware of this fact.

Anyone who plans to work with IC packs should become familiar with negative masking, from which one can make his own printed circuit boards.