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Statistical SPICE parameter extraction for an n-well CMOS process

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Statistical SPICE Parameter Extraction for an N-Well CMOS Process

By

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A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Masters of Science in Computer Engineering Rochester Institute of Technology

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Abstract

The purpose of this thesis is to demonstrate one method of statistical parameter extraction and show some of the advantages of statistical models. The method of extraction discussed, parameter domain statistics, is ideal for use in the classroom, due to its simplicity and ease of implementation. Another advantage is the minimal statistical knowledge required to understand this process. The test chip design was a modification of the test chip designed by Bert Berends. An N-Well CMOS lot was processed and models extracted using IC-CAP. From these models, parameter domain statistics were performed - the model parameters were used to create an average and ±3σ models. Additionally, the process was simulated with TSUPREM 4 and models were extracted from simulation and compared to the average models measured from silicon.

Through use of a threshold adjustment implant split, wafers were fabricated with symmetrical NMOS and PMOS threshold voltages. The threshold voltages followed the trends predicted by simulation, and mobility was determined to be independent of threshold adjustment implant dose. Lastly, the buried channel, PMOS device parameters exhibited a larger variation than the NMOS parameters.
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Glossary

**BSIM** - Berkley short-channel IGFET model for SPICE. (p 1)

**Data Domain Statistics** - A method of extracting parameters from each data point of the set of measured I-V curves and then extracting parameters from the resulting statistical I-V curves. (p 3)

**IC-CAP** - A model parameter extraction and simulation software package from Hewlett-Packard. (p 1)

**LPCVD** - Low pressure chemical vapor deposition. (p 17)

**LOCOS** - Localized oxidation of silicon. (p 15)

**LTO** - Low temperature oxide. (p 17)

**MEDICI** - A 2-D device simulation program, by Technology Modeling Associates. (p 19)

**NSUB** - Substrate doping concentration. (p 20)

**N-Type** - Silicon doped in a manor which causes it to be a conductor, in which the majority carrier is electrons. (p 6)

**N-Well CMOS** - A method of fabricating NMOS and PMOS transistors on the same wafer, by manufacturing the NMOS transistors in the base P-type wafer and creating the PMOS transistors in N-type regions called N-Wells. (p 1)

**Parameter Domain Statistics** - A method of extracting parameters from each measured I-V curve and performing basic statistics on the extracted parameters. (p 3)

**P-Type** - Silicon doped in a manner which causes it to be a conductor, in which the majority carrier is holes. (p 5)

**RCA Clean** - A method of cleaning particulates (both organic and metal) from wafers developed at RCA. (p 25)

**R.I.E.** - Reactive ion etch - a method of etching by using a plasma. (p 28)

**RTA** - Rapid thermal anneal: a method of annealing implant damage by heating the wafer to a high temperature very quickly. (p 31)
SPICE - Simulation Program with Integrated Circuit Emphasis, a commonly used circuit simulator first developed at the University of California. (p 1)

SRD - Spin rinse dry. (p 25)

THETA - Mobility modulation factor. (p 20)

TSUPREM IV - A process simulation program, by Technology Modeling Associates. (p 19)

U0 - Surface mobility. (p 20)

VT0 - Zero body bias threshold voltage. (p 20)
Introduction

Simulation is a critical process in engineering today. With today’s emphasis on time to market and minimizing costs, simulation has become a vital part of the design process. It is no longer possible to create a prototype and work out the bugs on the prototype. In circuit simulation the use of models such as SPICE (Simulation Program with Integrated Circuit Emphasis, a commonly used circuit simulator first developed at the University of California) and BSIM have become common place. Designers are typically given models of the devices they will be using in their designs, but may not know how the model was developed, i.e. how the particular model parameter values were arrived at. The goal of this project is to explore a process by which Level 3 SPICE models, for NMOS and PMOS devices, are derived for an N-Well CMOS process, with an emphasis on simplicity and incorporation into the classroom.

There are many methods of extracting model parameters. One example is extracting the threshold voltage from measured drain current (Id) vs. gate voltage (Vg) data. The Vg axis intercept of the straight line through the data points in the linear region (see figure 1.2 in the MOS Device Theory section for a diagram of this). IC-CAP, a model parameter extraction and simulation software package from Hewlett-Packard, provides the user with two basic methods of model development: 1) direct extraction of model parameters and 2) optimization of a subset of parameters for
improved I-V curve fitting. Extracting a model from a single device allows for accurate simulation of that single device, but the model may not be particularly accurate for simulating other devices, fabricated using the same process, on different wafers or even on the same wafer. The reason behind this shortfall is the inherent variability in the processing of the wafers. Variability not only exists from wafer to wafer, but exists even on the same wafer. Despite the best efforts of process engineers, some variation will remain, which is critical in today’s advanced designs and ever-shrinking device dimensions, where even small variations can be critical to the successful operation of the circuit. Statistical parameter extraction arises, out of a need to account for this variability.

McFeely and Pham, who describe methods of generating statistical device models in their paper, *Generating Statistical Models in IC-CAP* [2], give three business factors, which result in the need for statistical modeling. They are high yield, fast time to market, and quality [2]. This project will examine one of two easily implemented methods of statistical parameter extraction described by McFeely and Pham. These methods were chosen for their simplicity, so as to be incorporated into a classroom environment, such as a VLSI design course or an upper level, processing course, where process variability is examined. Two methods of statistical parameter extraction are parameter domain and data domain. Parameter domain statistics consists of extracting parameters from each measured I-V curve and performing basic statistics on the extracted parameters [2]. Data domain statistics consists of
performing statistics on each data point of the set of measured I-V curves and then extracting parameters from the resulting statistical I-V curves [2]. Each method results in a set of statistical model parameter cards. The designer would then be given a set of statistical model cards, consisting of a nominal, +3σ, and -3σ parameter cards. Having these model decks allows the designer to simulate the circuit under the worst case conditions of process variability. These methods will be discussed in further detail later. Other statistical methods exist, which produce more accurate models, but these methods are significantly more complex, and are left for future work. Some examples of more sophisticated methods of statistical parameter include factor analysis and sensitivity analysis, see the McFeely and Pham reference for more information on these methods. The simplicity of the parameter domain technique makes it ideal for quick implementation in an educational setting, and has therefore been chosen as the engine for examining statistical parameter extraction. Additionally, parameter domain statistics lends itself toward using the more accurate factor analysis, than does data domain statistics [2]. This is because factor analysis deals with reducing the parameter set to a smaller number of parameters through the use of multivariable statistical analysis of the parameter set. The reduced parameter set may then be used to help determine a worst-case model much more easily, than the larger original set of parameters.

The understanding of statistical parameter extraction techniques and the effects of process variations on model variation requires the understanding of the
device models and the dependence of the model parameters on the fabrication process.

It is important to have some understanding of how process parameters affect the model parameters and how variations in those process parameters cause variations in the model parameters. It is these relationships which drives the need for statistical modeling and simulation, for successful worst case design of a manufacturable product. With this in mind, the natural progression of the following theory section is formed.
Theory

MOS Device Theory

Metal-Oxide-Semiconductor device theory covers a wide range of complexity, from simple first order effects up through extremely detailed descriptions. To avoid some of this complexity, most texts on MOS VLSI design techniques use the simplified MOS device equations. A basic understanding of MOS device operation will be assumed, although a brief review follows. What is important to understand when extracting model parameters is how the particular parameters relate to not only the model, but also how they relate to the physical device itself. Circuit designers may be content with using a model, without knowledge of the physical aspects of the device, or with using models which are not directly related to any physical part of the device.

Figure 1.1 shows the basic structure of an n-channel MOS transistor. The transistor is made up of a P-type substrate, two N+ doped regions, called the drain...
and the source, and a gate region between the drain and source regions, which is insulated from the substrate by a thin layer of oxide. There are three very important physical dimensions of the transistor, the gate oxide thickness, $\text{TOX}^1$, the length of the space between the drain and the source, $L$, and the width of the transistor, $W$ (see figure 1.1).

The basic operation of the NMOS transistor is that the source and bulk are typically tied together to a point of low potential, such as ground, and the drain is tied to a point of higher potential, such as a positive supply voltage. While the gate voltage remains below a certain potential, called the threshold voltage, $V_T$, no current flows between the drain and source regions of the transistor. Once the gate voltage crosses the threshold voltage, an inversion charge is built up at the surface of the substrate between the drain and source, this region is called the channel. This channel is no longer P-type, but has been changed to N-type, thus it is also called the inversion layer and the device is now in a state of inversion. The reason that this occurs, is that the oxide between the gate and the substrate forms a structure similar to a capacitor, and as a potential is applied to the gate, a potential forms at the substrate surface, called the surface potential, $\psi_s$. Additionally, charge collects at the surface of the substrate forming the inversion layer. The surface potentials at each end of the channel are affected by the drain and source potentials, and it is the difference in the surface potentials at the ends of the channel that cause current to flow from drain to

---

$^1$SPICE parameter names will be used to describe variables, where applicable.
source. PMOS transistors work in the same way, except that the drain and source are P'-type, the substrate is N-type, and the applied voltages are all inverted. The source is connected to a potential higher than the drain, and as the gate potential is decreased, the channel is formed and current flows. This is a very simplified description of what happens, but gives the reader a general idea of what occurs. Tsividis covers the operation of MOS transistors in great detail and is recommended for those who wish to learn about MOS transistors in depth [8]. The remainder of this section will discuss the threshold voltage and mobility model parameters in greater detail, including how they relate to the device structure and materials.

Threshold voltage is one of the most misleading parameters used in modeling of MOS devices. Its usage implies that when the device is “off” no current flows, when the gate-to-source voltage, $V_{GS}$, is less than the threshold voltage (for NMOS). Correspondingly, when the device is “on”, current flows linearly when the gate-to-source voltage is greater than the threshold voltage. In reality, the $I_D$ vs. $V_{GS}$ curve is similar to the one shown in figure 1.2, and the threshold voltage is actually the x-intercept of the slope of the linear region of the curve.
The threshold voltage can also be calculated from knowledge of the process parameters. An equation for $V_T$ is given in (1.1) below [8]:

$$V_T = V_{T0} + \gamma (\sqrt{\phi_B + V_{SB}} - \sqrt{\phi_B})$$

(1.1)

$$V_{T0} = V_{FB} + \phi_B + \gamma \sqrt{\phi_B}$$

(1.2)

$V_{T0}$ is the extrapolated threshold voltage when the source and substrate are at the same potential, and $V_T$ is the threshold voltage due to body effect, which is a potential difference between the source and the substrate, $V_{SB}$ [8]. The terms which are related to the structure of the device are the remaining terms, $\phi_B$, $\gamma$, and $V_{FB}$.

The parameter $\phi_B$ is an approximate value for the maximum value of the surface potential, $\psi_s$, when the device is in strong inversion [8]. In strong inversion it is usually assumed that the surface potential reaches some maximum value, since large changes in $V_{GS}$ produce only very small changes in $\psi_s$ [8]. The maximum surface potential is usually approximated to be $2\phi_F + 6\phi_n$, where $\phi_F$ is the contact potential of
the substrate material and \( \phi_F = \phi_i \ln (N_A/n_i) \), for p-type substrate [8]. \( \phi_i = kT/q \),
where \( k \) is the Boltzmann constant, \( q \) is the magnitude of the electron charge, and \( T \) is
the ambient temperature in Kelvin [8].

The flat-band voltage, \( V_{FB} \), is defined as the external voltage required between
the gate and the substrate material to keep the semiconductor neutral by offsetting the
effects of the contact potentials of the gate and substrate and also to negate the effects
of parasitic charge that exists in the oxide [8]. The parasitic charges in the oxide and
charges at the Si-SiO₂ interface, \( Q'_0 \) (units of fC/um²), are a result of the process of
oxide growth and contamination during oxide growth [8]. The expression for the flat-
band voltage is

\[
V_{FB} = \phi_{MS} - \frac{Q'_0}{C'_{ox}}
\]

(1.3)

\[
\phi_{MS} = \phi_{bulk-mater} - \phi_{gate-mater} \equiv \left( \frac{kT}{q} \right) \ln \left( \frac{N_a N_{d,poly}}{n_i^2} \right)
\]

(1.4)

\[
C'_{ox} = \frac{\varepsilon_{ox}}{TOX}
\]

(1.5)

\( C'_{ox} \) is the capacitance per unit area, \( TOX \) is the oxide thickness in \( \mu m \), and \( \varepsilon_{ox} \) is the
permittivity of silicon dioxide, which is 0.0345 fF/\( \mu m \). The flat-band voltage is
heavily dependent upon the materials used to make the device and the device’s
structure. In (1.4) the approximation is made for a n-type polysilicon gate, used in
NMOS transistor fabrication, with \( N_a \) being the substrate doping and \( N_d \) the doping
of the polysilicon gate. These dependencies carry directly back to the threshold voltage.

Lastly, the body effect coefficient, \( \gamma \), is related to the substrate doping and the oxide capacitance per unit area (see equation 1.6).

\[
\gamma \equiv \frac{\sqrt{2q\varepsilon_s} \sqrt{N_A}}{C_{ox}}
\]  

(1.6)

where \( \varepsilon_s \) is the permittivity of silicon, and \( N_A \) is the doping of the P-type substrate. The value of \( \sqrt{2q\varepsilon_s} \) is 0.00579 fF\( \cdot \)V\(^{1/2}\)\( \cdot \)\( \mu \)m\(^{1/2} \) [8].

From this analysis of just one single parameter, which is involved in the determination of drain current for a given bias, one can see the numerous process dependencies involved. It becomes readily apparent that variations in those process parameters will greatly affect the model parameters and the effectiveness of the model itself. Equations 1.1-1.6 show that there is a strong dependence of the threshold voltage parameter on the substrate doping level.

Additionally, the effective oxide interface charge, \( Q_o' \), affects the flatband voltage, equation (1.3), which in turn affects the threshold voltage. This charge is typically in the \( 10^{11} \) ions/cm\(^2\), or 1000 ions/\( \mu \)m\(^2\), range for modern processes. The oxide interface charge causes the threshold voltage to shift in the negative direction. This non-ideality causes PMOS devices to have a threshold voltage which is too negative, and NMOS devices to become depletion mode devices, where the threshold...
voltage is negative. The solution to this problem is to raise the threshold voltage by implanting the channel region with a shallow ion implantation, called a threshold adjustment implant. This causes the substrate to be nonuniformly doped, and facilitates adjustment of the equations to compensate for the nonuniformity of the substrate doping due to the implanted channel region. A complete analysis can be found in the Tsividis reference.

Mobility is a measure of the ease of carrier motion within a semiconductor crystal [7]. From non-saturation and saturation current equations (eq. 1.7a-b), we can see that mobility directly affects the current in the MOS transistor:

\[
I_{D(Non-Saturation)} = \frac{\mu C_{OX}}{2} W \left[ 2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right]
\]

(1.7a)

and

\[
I_{D(Saturation)} = \frac{\mu C_{OX}}{2} \frac{W}{L} (V_{GS} - V_T)^2,
\]

(1.7b)

where \(C_{OX}\) is the gate oxide capacitance, \(W\) is the width of the device, \(L\) is the length of the device, \(V_{GS}\) is the gate to source voltage, \(V_{DS}\) is the drain to source voltage, and \(V_T\) is the threshold voltage [9].

Carrier scattering is one of the primary factors affecting mobility. Scattering is a condition that occurs when the carrier motion is impeded by collisions with the semiconductor lattice [7]. As the scattering increases mobility decreases. The two factors controlling scattering are temperature and doping concentration [7]. As
temperature increases, the mobility decreases, but the amount of change due to temperature is a function of the doping concentration [7]. Equation 1.8 shows how mobility relates to temperature,

\[ \mu \propto T^{-n}, \quad (1.8) \]

where \( T \) is the temperature, and \( n \) is a positive constant, which varies depending upon material type and the dominant scattering mechanism [5]. In silicon, \( n \) is approximately 5/2 for both holes and electrons [5]. As with temperature, as the doping concentration increases, the mobility decreases, due to increased collisions with the doping ions [7].

Another key factor for mobility is the effective mass of the carrier (eq. 1.9-10). The effective mass is not the actual gravitational mass, but is described by Newton’s force equation and is highly dependent upon the periodic crystal structure, and thus the type of material in which the carrier is traveling [5]. The mobility equations for \( \mu_n \) and \( \mu_p \), the electron and hole mobilities are

\[ \mu_n = \frac{e\tau_n}{m_n^*}, \quad (1.9) \]

\[ \mu_p = \frac{e\tau_p}{m_p^*}, \quad (1.10) \]

where \( e \) is the charge of an electron, \( \tau \) is the weighted average relaxation time for either electrons or holes, and \( m^* \) is the effective mass of either the electrons or the holes [5].
From these equations we can see the importance of doping concentration and temperature and how they relate to mobility. Additionally, the importance of a high quality gate oxide interface becomes apparent. Finally, we can also see how mobility directly affects the drain current in the MOS transistor.

**CMOS Fabrication**

The detailed theory behind the many different processes involved in fabrication of CMOS devices is beyond the scope of this paper, therefore the discussion will be limited to an overview of the layers and mask levels involved in N-well CMOS processing. A more detailed description of the process used is described in the *Procedure* section. Some of the processes used to fabricate the layers will also be described in the following overview.²

CMOS designs require that both NMOS and PMOS transistors be fabricated on the same wafer. This problem may be solved in a number of ways. The use of a P-type wafer and diffusing N-Wells into the P-type wafer allows for PMOS devices to be created in the well regions and NMOS devices to be created in the regions outside the N-Wells. The opposite of this, called P-Well CMOS, or a combination process, called Twin-Well CMOS, in which both N- and P-Wells are diffused in a wafer of either N-type or P-type, may be used. An N-Well process was used for this project.

²For a more thorough discussion consult any of the Processing References listed on pages 91-93.
because it can easily support a vertical NPN transistor for BiCMOS. A layer by layer description of the N-Well process follows.

Beginning with a bare P-type silicon wafer, the first step in fabricating devices is to grow a thin layer of oxide, which is later used to provide a lip for later alignment after the N-Well drive-in step described below. The next step is the creation of the N-Wells. The N-Well mask, mask #1, is used to pattern a layer of resist on the oxidized wafer. The areas of the wafer where the well is to be implanted are clear of resist, while the resist covers the areas where the wafer is to remain P-type. N-type ions (phosphorus ions) are implanted into the wafer using an ion implanter. The implanter is a high-voltage particle accelerator, which produces a high velocity ion beam. The beam, when directed at the target wafer, causes the impurity ions to penetrate the surface of the wafer [10]. After the ions have been implanted, the well is driven in by heating the wafers to very high temperatures (1150°C for example) for a number of hours. This causes the N-type well to extend into the wafer to some depth, usually on the order of a few microns (see figure 2.1).

Figure 2.1: N-Well Layer
The next layer is the active area. The active area is an area in which devices will be formed. The area outside the active area, called the field layer, is an insulation layer, consisting of a thick layer of silicon-dioxide (SiO$_2$). This field oxide layer is created by growing and patterning, using mask #2, a layer of nitride (Si$_3$N$_4$) to cover the active areas. The nitride layer is used later to prevent oxide from forming in the active areas. After the nitride layer has been patterned, mask #3 (which is the inverse of the N-Well mask, mask #1) is used to pattern a layer of resist. A P-field threshold adjustment implant is performed next. This implant adjusts the threshold voltage, $V_T$, in the P-field areas (the areas outside the N-Wells and areas where there is no nitride) to prevent unwanted parasitic device operation in the field areas. After the implant, the resist is removed and the field oxide is grown. As mentioned above, the nitride layer prevents field oxide from forming over the active areas (figure 2.2). After the field oxide has been grown, the nitride is removed, leaving the active areas accessible. One of the problems with this method of isolation, is that a birds beak effect is formed due to a slight lifting of the nitride layer at the edge of the field oxide. The birds beak effect of the LOCOS (Localized Oxidation of Silicon) isolation process is a limiting factor in the reduction of transistor channel lengths.
Once the nitride is removed, a sacrificial oxide is grown over the active regions. The thickness of this oxide is on the order of 500 Å. The entire wafer is implanted with a boron, device threshold adjustment, implant. This threshold adjustment implant increases the threshold voltage of both the NMOS and PMOS devices, thus making it easier to turn on the PMOS devices and more difficult to turn on the NMOS devices. The sacrificial oxide is then removed and the gate oxide is grown to a thickness of 500 Å. Polysilicon is then deposited on top of the gate oxide. Next the polysilicon is doped using a spin on glass dopant. The wafer is heated to allow phosphorus to diffuse into the polysilicon. The glass is then etched off, and the polysilicon is patterned, using the fourth mask level. The unwanted polysilicon is then plasma etched (figure 2.3).
Next the wafers are patterned, using the fifth mask level, and the wafers are implanted with boron (BF$_2$), to produce the P$^+$ source and drain areas of the PMOS devices. The wafers are patterned, using mask level six, the inverse of the fifth mask level. The wafers are again implanted, but this time with phosphorus, to produce the N$^+$ source and drain areas of the NMOS devices (see figure 2.4). Once this is completed, a low temperature oxide (LTO) is deposited using LPCVD (Low Pressure Chemical Vapor Deposition). This oxide is an insulator between the metal and polysilicon layers. The wafers are then placed in the furnace at 900°C for 30 minutes to densify the deposited oxide and drive-in and activate the source and drain areas of the NMOS and PMOS devices.
The wafers are then patterned, using mask level seven. The contact cuts are then etched through the LTO using HF for an appropriate amount of time, depending upon the thickness of the oxide over the source and drain regions and the etch rate of the HF bath. Once the contacts are opened, aluminum is then sputtered on the wafers, after which the aluminum is patterned using mask #8, and etched in a heated aluminum etch (figure 2.5). Finally, the wafers are sintered, that is put in the furnace at 415°C with a forming gas ambient to improve the aluminum contacts to the source, drain, and polysilicon regions.

![Figure 2.5: Aluminum Contacts to Source/Drain](image.png)

**Parameter Extraction Techniques**

Model parameters are extracted by applying mathematical methods to various measured or simulated device characteristic curves, current vs. voltage or capacitance vs. voltage. The required curve or curves are defined by the method for extracting a particular parameter. Two examples of curves used for model parameter extraction include Id vs. Vg (drain current vs. gate voltage, for a small drain bias) and the Id vs.
Vd family of curves (drain current vs. drain voltage, for given gate bias). Additionally, the dimensions of the devices may be varied and the parameter may be extracted from a particular curve based upon the particular sizing of the device and how that curve differs from other curves produced from different device sizes. Examples of such device sizes include large devices (both long and wide channel), short channel devices, and narrow channel devices.

It is not necessary to extract parameters exclusively from measured curves. As mentioned above briefly, simulated curves can be used for parameter extraction. The big advantage with this method is that a particular process may be simulated using a simulation tool, such as TSUPREM 4, and the electrical performance of the devices simulated with a device simulation tool, such as MEDICI. With these tools the curves necessary for parameter extraction may be produced by simulation, and models may be created without fabricating real devices in silicon. Once real devices have been fabricated, the simulations may be calibrated so that the simulated device models match the measured device models accurately. This process can be very important in reducing the time it takes to develop a product using a new process. A simulated model can be provided to circuit designers long before devices have been produced in silicon and models provided from measured devices.

IC-CAP allows the user two methods of parameter extraction: direct and optimized, although it is somewhat misleading to call them two methods as will be described shortly. Direct parameter extraction involves extracting a particular
parameter or set of parameters directly from the appropriate measured curve. Optimization may be used after direct parameter extraction, and is used to optimize the fit between the measured curves and the simulated curves produced from the extracted model parameters. The fit is optimized by varying one or more model parameters from their extracted values and checking the fit. The range over which the parameters may be varied is set by the user, as are the parameters being optimized. Additionally, the order in which parameters are optimized and possibly re-optimized, and the number of possible methods of optimization is infinite.

**Statistical Parameter Extraction**

Statistical parameter extraction requires a "large" amount of data, where 30 or more samples constitutes a large sample size, and statistical procedures for testing the data [4]. The data that was used for statistical parameter extraction was the SPICE model decks for the measured devices. Each measurement has a corresponding SPICE model. The Level 3 SPICE models contain the measured parameters for the "large" device, which mean the transistor channel is both long and wide (32μm x 32μm). The parameters extracted include VTO, U0, NSUB, and THETA (the zero body bias threshold voltage, surface mobility, substrate doping, and the mobility modulation factor, respectively). In this experiment, 73 devices were measured per wafer, with a low of 10 good devices and a high of 72 good devices found on a single wafer.
Once the SPICE models have been collected, the individual parameters are used to generate the average, $+3\sigma$, and $-3\sigma$ model decks. The reason the parameters were used is that it was much easier to collect the parameter data and perform statistics on the parameters than it was to perform statistics on each data point on all the I-V curves. This was also partially due to not fully understanding how to program in the IC-CAP macro language.

The standard deviation for the sample data is defined as a measure of the variability within the sample [4]. The equation for sample standard deviation is shown in eq. 1.7 below [4].

$$s = \sqrt{\frac{1}{n-1} \left[ \sum_{i=1}^{n} X_i^2 - \left( \frac{\sum X_i}{n} \right)^2 \right]} \tag{1.7}$$

Using Iman’s rule of thumb, that 99.7% of all samples will be within 3 standard deviations of the sample mean, the $\pm 3\sigma$ statistical SPICE models are chosen and calculated by adding and subtracting each model parameter’s $3\sigma$ value from the parameter mean [4]. The nominal or average model is created using the parameter averages.

Using the nominal model for a given process to simulate new circuits being designed for that particular process, will give a good indication as to the performance of the circuit. Worst case performance may be examined by using the $+3\sigma$ and $-3\sigma$ models for simulation, but these are not definitive worst case results, and should be
treated with caution. For a particular design, parameters may be correlated with one another, thus a $+3\sigma$ value of one parameter combined with a $-3\sigma$ value of another parameter may be the true worst case scenario and would not be covered by simulation using the average and $\pm 3\sigma$ models. Additionally, a good worst-case designed circuit should operate well beyond the $\pm 3\sigma$ models, and cases such as the one mentioned above should also be simulated by creating a new statistical model, with the worst-case SPICE parameter values included in the model.
Procedure

Test Chip and Device Chip Design

The test chip used for the project was a modification of the N-Well CMOS test chip designed by Bert Berends in August, 1993. Robert Pearson first modified the layout of the test chip, by moving some of the test structures around for better grouping of similar test structures. Further modifications were then made by moving more of the test structures and redesigning the NMOS and PMOS transistors. The new transistor designs included substrate and well contacts for bulk biasing in the parameter extraction process. Additionally, the three transistor sizes required for MOS extraction using IC-CAP (large, short channel, and narrow channel) were designed and placed in a single ten pad configuration, one for NMOS and one for PMOS. This was done because the switch matrix allowed the probe card to be placed on the wafer once. The connections could then be changed for each transistor on the pad set without lifting up the probes.

The device chip contained a number of circuits made up of standard cells routed to output pads. The standard cells ranged from simple devices, such as an inverter, NOR, NAND, and XOR cells, to more complex cells, such as a 4-to-1 multiplexor cell and a 4-bit ripple counter cell. Each of the cells were routed to ten pad groupings for use with the ten pad probe card. The standard cells were laid out with three sizes, the base 2 μm scale, a 2X, and a 4X scale, thus providing...
approximately a 4 µm scale and an 8 µm scale of devices. The three sizes were chosen in an attempt to best ensure working devices (even if only at the largest size), and also to check to see if fabrication of working 2 µm devices could be performed with the N-Well CMOS process at RIT's Cleanroom facilities. The purpose of the device chip is to allow for future comparisons of device simulations using the statistical SPICE models with measured operation of the devices. An example of one of the tests which may be performed is the operation of an inverter. The simulated and measured values of the input voltage, at which the inverter output switches from low-to-high and high-to-low, could be compared. The devices chosen for inclusion in the device chip were taken from the standard cell library provided with the Mentor Graphics\(^3\) v8.2.5 software tools. A second metal layer is required for the operation of the device chip, and the processing of this second metal layer was left for future work.

The standard cells used in the device chip are an inverter, a 2-input NAND, an exclusive-OR, a 2-input OR, a buffer with inverting and non-inverting outputs, a NAND latch, a D-flip flop, a 4-to-1 multiplexor, a 4-bit ripple counter, an input pad cell, and an output pad cell. The input and output pads were included so they could be tested for use with future RIT, N-Well CMOS, circuit designs.

\(^3\)CMOSN Cell Library Revision 3.0A, 10/8/91. Mentor Graphics is a Trademark of Mentor Graphics.
CMOS Processing

The following is a step-by-step description of the N-Well CMOS process steps.

STEP 1: Twenty-five P-type wafers were obtained, and the manufacturer’s data was recorded. One of the wafers was scanned for a particle count. The back of the wafers were scribed, and the wafer was rescanned and the new particle count data was recorded. The wafers were scribed in the following manner: 15 device wafers, 8 control wafers, and 2 alignment wafers. The lot number was also scribed on the wafers. Selected wafers were four-point probed and their resistivity was calculated.

STEP 2: The wafers were then cleaned in an RCA clean, which consisted of a ten minute APM bath, a four cycle rinse, two minutes in a 50:1 HF bath, another four cycle rinse, a ten minute HPM bath, rinsing in the lower and upper cascade rinser, and finally placed in the SRD (Spin Rinse Dry) for additional rinsing and spin drying. Again the wafer measure for a particle count previously was scanned and the new particle count recorded.

STEP 3: The wafers were placed in furnace tube 13 for alignment oxide growth. The following thermal and chemical recipe was used: 1000°C for 10 minutes with 6 slpm dry O₂ and 1 slpm N₂, 1000°C for 55 minutes with 2 slpm dry O₂ and 2 slpm wet O₂, 1000°C for 5 minutes with 7 slpm O₂ and 1 slpm N₂, a 15 minute temperature ramp up to 1150°C with 7 slpm O₂ and 1 slpm N₂, and finally, 1150°C for 600 minutes with 5 slpm N₂. The wafers were inserted and pulled at 900°C in N₂.
The push rate was 12" per minute, and the pull rate was 10" per minute. The load order of the boat was (from load end to source end) C1 - C8, D1 - D15, A1, and A2. The wafers were inserted with the top of wafers facing toward the load end of the furnace. After the wafers cooled down, the oxide thickness was measured on various wafers.

STEP 4: The wafers were then coated with resist using program 3 on the WaferTrac. This program consists of a 250°C prebake for 120 seconds, HMDS prime and photo resist coat, and a 45 second postbake at 100°C. Next the alignment wafers were exposed on the stepper, using mask level 1, the N-Well mask level. The alignment wafers were then developed using program 2 on the WaferTrac. Program 2 consists of a 45 second prebake at 115°C, the developer cycle, and a 120 second postbake at 120°C. The alignment wafers were then examined under a microscope to determine the quality of the exposure and develop. Once it was determined that the exposure and develop was acceptable, the remaining device wafers were exposed and developed. The control wafers were exposed separately from the device wafers. Using a contact aligner, the control wafers were exposed with the top half of the wafer covered (the half with the flat) by a piece of sheet metal. The wafers were etched in HF until they became hydrophobic (pulled dry). This removed the oxide in the areas where the resist had been removed.

STEP 5: Initial formation of the N- Wells was performed when the wafers were then implanted with phosphorus. The implant dose was 6E12 ions/cm² at 130 KeV
of energy. Each wafer was implanted for approximately 16 second, with an arc current of approximately 6 μA.

STEP 6: The wafers were then placed in the plasma asher for 38 minutes, and the resist was removed.

STEP 7: The wafers were RCA cleaned as above, but with a 12 second HF dip.

STEP 8: The wafers were placed in furnace tube 13, for N-Well drive-in and oxide growth. The wafers were pushed in at 900°C at a rate of 8” per minute, with the same boat order as before, and ramped up to 1000°C in 10 minutes in 4 slpm N₂. The recipe is as follows: 1000°C for 10 minutes in 8 slpm dry O₂, 1000°C for 26 minutes in 6 slpm wet O₂, 1000°C for 20 minutes in 8 slpm dry O₂, 15 minute temperature ramp up to 1150°C in 8 slpm dry O₂, 1150°C for 1252 minutes (20 hrs. 52 min.) in 4 slpm N₂, 120 minute ramp down to 800°C in 4 slpm N₂, and 800°C for 360 minutes in 4 slpm N₂. The wafers were pulled at 800°C at a rate of 8” per minute. Oxide thickness measurements were performed on the control wafers on the well and non-well halves of the wafers.

STEP 9: The wafers were then etched in HF until they became hydrophobic, removing any oxide. After the HF etch, wafers were rinsed in the cascade rinses and put in the SRD and rinsed and dried.
STEP 10: The control wafers were then four-point probed on both the well and non-well sides, and resistivity and doping levels were calculated. Control wafers C1 and C2 were grooved and stained on the well side, and well junction depth measurements were made and recorded. The well/non-well step, due to the oxide growth and removal was also measured and recorded.

STEP 11: The wafers were placed in furnace tube 12 at 950°C for 40 minutes in 5.4 slpm dry O₂, to grow a 250 Å pad oxide. The wafers were pushed and pulled at 850°C at a rate of 8” per minute. Temperature ramping was done in 4 slpm of N₂. The oxide thicknesses were measured on the control wafers and recorded.

STEP 12: The wafers were then put in the LPCVD and a 1000 Å target, nitride layer was deposited at a temperature of 800°C. The boat load order was C1 - C2, D1 - D15, C3 - C4, with the wafers facing toward the source end of the tube. The deposition time was 14 minutes. Nitride thicknesses were measured and recorded.

STEP 13: Active layer lithography was performed on the device wafers, using the active layer mask, mask 2. As before, testing was performed on the alignment wafers.

STEP 14: The nitride was etched in the R.I.E. with a 30 sccm SF₆ flow, at 150 Watts and 39.9 mTorr. An etch time was determined using control wafers C1 - C4.

STEP 15: P-Field threshold adjustment lithography was performed next. The resist from the previous lithography remained on the wafers and the new resist was
coated on top of the previous layer. Due to this, the 250°C prebake step was removed from the resist coating program, and replaced with a five second delay. The control wafers were exposed on the contact aligner with the bottom side covered (flat side exposed).

STEP 16: The wafers were then implanted with a boron P-field threshold adjustment implant to prevent transistor turn on in the field regions. Wafers D1 - D7 were implanted with a 2E13 ions/cm² dose of $B_{11}$ at 33 KeV, while D8 - D15 were implanted with a 4E13 ions/cm² dose of $B_{11}$ at 33 KeV.

STEP 17: The 21 wafers were plasma ashed for 40 minutes and the resist was removed.

STEP 18: The wafers were then cleaned in the standard RCA clean process, and spin dried.

STEP 19: The wafers were placed in tube 13 for field oxide growth. The following thermal recipe was used: 800°C in 5.5 slpm $N_2$ and 5.5 sccm dry $O_2$ for 15 minutes, ramp to 1100°C for 20 minutes, 25 minutes at 1100°, ramp down to 950°C for 30 minutes, 15 minutes at 950°C, 300 minutes in 5 slpm wet $O_2$ at 950°C, 30 minutes in 5 slpm $N_2$ at 950°C, ramp down to 800°C in 5 slpm $N_2$ for 30 minutes. A calibrated mass flow controller (MFC) was used to achieve the 5.5 sccm $O_2$ flow. During the last minute before the 5 slpm wet $O_2$ growth cycle, the $O_2$ flow was turned off and the MFC (Mass Flow Controller) was disconnected and the $O_2$ reconnected.
and turned back on. The push-pull rate was 8" per minute. The measured field oxide thicknesses were around 7000 Å, slightly less than the target thickness of 7500 Å.

STEP 20: The oxinitride was etched by dipping the wafers in HF for 3 minutes, 50 seconds. They were then rinsed and spun dry.

STEP 21: The remaining nitride was etched in the R.I.E. for 75 seconds, at 150 watts, 30 sccm SF₆, and a pressure of 40 mTorr.

STEP 22: The pad oxide under the nitride was etched for 35 to 45 seconds in buffered HF until the areas between the chips pulled dry.

STEP 23: A standard RCA clean was performed with out the HF dip. The wafers were then rinsed and dried in the SRD.

STEP 24: A sacrificial oxide was grown in furnace 13, with the following thermal recipe: push in at 900°C at a rate of 8" per minute, 4 slpm N₂ for 25 minutes, 2 slpm dry O₂ and 4 slpm wet O₂ for 25 minutes, 35 minutes in 5 slpm dry O₂, pull at 8" per minute. The target thickness was 600 Å to 700 Å, but the measured thicknesses were 818 Å to 967 Å.

STEP 25: The devices were implanted with boron (B₁₁) for device threshold adjustment. The wafers were implanted with a range of doses, additionally D₄ and D₁₂ were implanted with a punch through prevention implant of 2.5E11 ions/cm² at 160 KeV. The following table shows the 35 KeV threshold adjustment implant doses:
D1 & D9  1E12 ions/cm²,  D2 & D10  1.5E12 ions/cm²,
D3-D5 & D11-D13  2E12 ions/cm²,  D6 & D14  2.5E12 ions/cm²,
D7 & D15  3E12 ions/cm²,  D8  no implant.

STEP 26: The sacrificial oxide was etched in HF.

STEP 27: A standard RCA clean with out the HF step was performed, and the wafers were rinsed and dried in the SRD.

STEP 28: The gate oxide was grown in furnace 12 with the following recipe: push at 8" per minute at 900°C in 4 slpm N₂ and ramp up to 950°C (15 minutes), 90 minutes in 4 slpm dry O₂, followed by 30 minutes in 4 slpm N₂. The gate oxide thickness was approximately 400 Å. The target thickness was 500 Å, but the measured thicknesses were accepted. This thinner gate oxide coupled with a slightly thick sacrificial oxide caused the Vt to shift lower than the target value. The combination of the thin gate oxide and thick sacrificial oxide had multiplicative effects on the threshold voltage; had the sacrificial oxide also been thinner than the target, they may have counter acted each other and the Vt's might have been on target. The load order from load end to source end was C3-C5, D1-D5, N1-N3 (extract wafers which were used for an RTA, rapid thermal anneal, experiment), D6-D10, N4-N6, D11-D15, and C6-C8.

STEP 29: A polysilicon deposition was performed using the LPCVD. The deposition was performed at 600°C for 60 minutes. The target thickness was 5000Å.
STEP 30: Using N-250 Emulsetone (Spin On Glass - SOG), the poly was doped. The N-250 was spun on the wafers at 3000 RPMs for 10 sec, then inserted in an oven at 85°C, while it was still coming up to temperature, for 25 minutes. The step required at 15 minute postbake at 180°C. The wafers were then baked in the furnace for 10 minutes at 950°C in 4 slpm N₂. A push-pull rate of 8” per minute was used, and the wafers were inserted and removed at the 950°C bake temperature.

STEP 31: The polyglass was etched by dipping the wafers in buffered HF for 4 minutes. The wafers were then rinsed and dried using the cascade rinse and the SRD.

STEP 32: The polysilicon was four point probed and the resistivity was measured and recorded for the control wafers.

STEP 33: The polysilicon was patterned using mask 4. The coat step was performed without the 250°C prebake step. In an attempt to achieve a poly bloat, the post bake temperature for the develop step was increased from 120°C to 130°C, but this wasn’t effective, since the 2 µm poly lines were completely etched in the following step. It is suggested that the polysilicon layer be bloated by 1/2 micron on every side if 2 micron poly features are to be attempted. Two micron lines should appear as three microns on the mask, see step 34 below.

STEP 34: The polysilicon was etched in the R.I.E. at 75 watts, 75 mTorr, in 30 sccm SF₆ and 3 sccm O₂, for 105 seconds. When examined under a microscope, it
appeared that the 2 μm poly lines remained intact, but once the resist was removed, the poly had been over etched, and the 2 μm devices had been destroyed.

STEP 35: The resist was removed in a 1:3 solution of H₂O₂:H₂SO₄ for 30 minutes. It is important that the sulfuric acid be added to the peroxide.

STEP 36: Had the gate oxide met the target thickness, a gate oxide etch back would have been necessary, but the 300 Å of oxide over the source and drain regions was acceptable, and the etch back was not performed.

STEP 37: Using mask 5, the P⁺ photolithography step was performed.

STEP 38: A 1E15 ions/cm² dose of BF₂ was implanted at 55 KeV. The source/drain implant times were increased to over 20 minutes per wafer in order to ease the removal of the resist.

STEP 39: The resist was stripped using a 1:3 solution of H₂O₂:H₂SO₄. A total of three fresh chemical baths and over 90 minutes of stripping time was required to remove the resist. After the second bath, a high pressure scrub was used to aid in the resist stripping process. Agitation of the wafers during the chemical bath was very important in this step.

STEP 40: The wafers next had the N⁺ photolithography step performed on them, using mask 6. Due to problems with the track, the wafers were hand developed using the same times and temperatures, but one at a time using a petri dish and a hot plate. The wafers were not prebaked before developing.
STEP 41: The wafers were then implanted with a phosphorus dose of 1E15 ions/cm$^2$ at 35 KeV to create the N-type source and drain regions.

STEP 42: The resist is stripped in the resist strip bath as above. The problems experience after the BF$_2$ implant did not occur this time.

STEP 43: A standard RCA clean was performed followed by a spin dry cycle.

STEP 44: A passivation oxide was grown in furnace tube 13. The wafers were pushed in at 12" per minute in 4 slpm of N$_2$, oxidized at 800°C in 4 slpm wet O$_2$ for 15 minutes, then pulled in 4 slpm of N$_2$ at 12” per minute.

STEP 45: Between 3500 Å and 5000 Å of low temperature oxide (LTO) was deposited using the LPCVD system. Extra dummy wafers were used in an attempt to improve uniformity of the oxide thickness across the device wafers.

STEP 46: The wafers were then put in furnace tube 13 at 900°C in 4 slpm wet O$_2$ for 30 minutes for LTO densification. The oxide thicknesses over the source and drain regions ranged from 3000 Å to 4500 Å. The oxide thickness uniformity was very poor.

STEP 47: The control wafers were rapid thermal annealed (RTA) and four point probed to measure the resistivity of the source and drain regions after implant and RTA. Additionally this was a test of the RTA, to see approximately how long it took to fully activate the regions after implant. It appears that after 30 seconds at 900°C the implanted regions were fully activated. The control wafers should be
immediately undergo RTA and four point probe after an implant step to evaluate the success of the implant step.

STEP 48: The control wafers were grooved and stained, and a source and drain junction depth of approximately 0.4 μm was measured on the same wafers that underwent the RTA step, but not the LTO and LTO densification steps.

STEP 49: The wafers were then patterned using mask 7 for the contact cut lithography.

STEP 50: The contact cuts were etched in HF (BOE - Buffered Oxide Etch) for 8 minutes. This time included some over etch time. An additional 30 seconds of etch time was performed with no change in the oxide thickness of the source and drain areas, thus assuring that the oxide had been completely removed.

STEP 51: The resist was stripped in the peroxide and sulfuric acid bath as above, for 30 minutes.

STEP 52: An RCA clean was performed, but the HF dip was performed last, instead of in the middle. The wafers were then put in the SRD and dried.

STEP 53: Aluminum was then sputtered onto the wafers to a thickness of 8500 Å. The CVC 601 sputtering system was set for 350 volts and 7 amps, with a base pressure of 4e-6 Torr and a sputtering pressure of 5 mTorr. The wafers were preheated at 300°C for 5 minutes and pre-sputtered for 7 minutes. The sputtering time was 24 minutes, and the target thickness was 8000 Å.
STEP 54: The aluminum was patterned using mask 8.

STEP 55: The aluminum was etched in the aluminum etch at 40°C for approximately 1 minute, until the bubbling stopped.

STEP 56: The resist was ashed in the plasma asher for 25 minutes. It is important to note that the resist strip should not be used at this step since the acid in the strip will remove the aluminum.

STEP 57: The wafers were sintered in furnace tube 16 at 415°C for 20 minutes in approximately 5 slpm of forming gas. Once cooled, the processing was completed and testing could begin.

Parameter Extraction & Process Simulation

Once fabrication of the devices through first level metal was completed, parameter extraction began. Using IC-CAP, a macro was written, which utilized the autopробing capabilities of the Semi-Automated Wafer Prober. The macro controlled automated movement of the prober so that each die location on the wafer could be tested. Initial alignment of the wafer and probe placement on a reference position was required before automated probing could begin. At each location measurements were made on each of the three transistor sizes for the type of devices being measured, either NMOS or PMOS. Once the devices were measured, the various current-voltage
plots were displayed and the operator was prompted to extract SPICE parameters, save the results and optionally print the plots.

The parameter extraction process required the operator to make a judgment call of whether or not the current-voltage plots represented a “good” or a “bad” device. A “bad” devices consisted of any curve which represented non-operational devices, and also included curves where the operation of the device was poor enough to cause it to be judged a “bad” device. Future iterations of this procedure should be performed on a process which has been in use longer, so that there is some expected range of measured curves. Additionally, work should be done to further automate the measurement process. The human factor could then be eliminated by performing extractions and comparing one or more parameters to specified limits. The limits would then control the inclusion of a particular measurement in the “good” or “bad” category. One of the reasons that better automation was not done for this experiment was that the parameter extraction tool would fail on curves of non-working devices, thus requiring the restart of the IC-CAP program and a resumption of measurements at the point where the program failed before. Recovery from these crashes was extremely time consuming. The only solution for this problem may be for the software developer to correct it.

Each wafer had a total of seventy-three test die locations, which took approximately forty to fifty minutes to test and perform extractions. The time increased for wafers with a better yield, due to the added time of performing
parameter extractions on only "good" die locations. NMOS devices on wafers D3-D15 were tested, with the exception of D12, where only about half of the die locations were tested. Due to a substantial difference in yield between D3-D7 and D8-D15 (excluding D12), the PMOS devices were only tested on D8-D15, again with the exception of D12. Readers will note that the field Vt adjust implant was a split, with D1-D7 receiving a lower implant dose than D8-D15, also note that D12 was implanted with a punch through prevention implant. From the poor yield in D12 it would seem reasonable to believe that the punch through prevention implant degraded the performance of the devices severely. Additionally, it appears that the higher field Vt adjust implant should be used instead of the lower dose implant, due to the improved yield seen in the D8-D15 wafers. The test macro was modified for increased testing speed, after NMOS testing was performed on D3-D7. The improved macro operated at the testing times mentioned above. Originally the testing took on the order of three to five hours per wafer. Total test time was around forty hours, not including development of the original test macro and the set up of the IC-CAP models and device tests.

The entire process was simulated using TSUPREM4. Simulated I-V curves were generated by MEDICI from the simulated devices. Parameter extraction was performed using IC-CAP on the simulated I-V curves from the simulated devices. The process was simulated using SUPREM IV, a 2-D process simulation tool, and Caesar, a virtual wafer fab simulator, which controls the use of other simulators such
as SUPREM IV and MEDICI, a 2-D device simulator. Process splits for threshold voltage adjustment implants was also simulated. Due to the higher yield of the D8-D15 wafers, only the field threshold adjustment for those wafers was simulated in the process simulation. Processing for devices both in and out of the N-Well region was simulated. Results of the process simulated were compared with measured process data. The results of the process simulation were then used to simulate devices using MEDICI. Gate characteristic curves (Drain current vs. Gate voltage). These curves were imported to IC-CAP, where Level 2 SPICE parameter extractions were performed. The resulting extracted threshold voltages were then compared to the measured threshold voltage ranges from the various wafers.
Results

A substantial amount of information can be gathered through statistical parameter extraction. The use of basic statistics allows this information to be packaged into a more concise view of the overall picture and provide insight into some of the subtleties and interactions of the fabrication process. Additionally, wafer mapping may be used to help explain results. This method consists of plotting data in respect to the location on the wafer, where the data was measured. One example of this is to plot the threshold voltages, of each device measured, at the location of the device on the wafer. This may provide insight into the effects of location on a measured parameter. The use of more advanced statistical methods, not covered here, allow correlation of factors to be performed and provide insight into the process and its effects on the final extracted parameters. The results of this investigation into statistical parameter extraction are described below.

Three basic statistical SPICE model decks are shown in table 1.0. The SPICE model decks consist of an nominal SPICE model, a +3 sigma model and a -3 sigma model. This model deck only contains the models for the devices with the best NMOS and PMOS VT0 values, i.e. the VT0’s are nearest to +1 volt for the NMOS devices and -1 volt for the PMOS devices. The data for the devices from other wafers can be found in Appendix E: Data Analysis.
<table>
<thead>
<tr>
<th>Model Type / SPICE Parameter</th>
<th>VT0</th>
<th>UO</th>
<th>NSUB</th>
<th>THETA</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3 σ NMOS</td>
<td>0.784</td>
<td>361.87</td>
<td>1.98E+16</td>
<td>0.0290</td>
</tr>
<tr>
<td>Nominal NMOS</td>
<td>1.027</td>
<td>510.31</td>
<td>2.34E+16</td>
<td>0.0422</td>
</tr>
<tr>
<td>+3 σ NMOS</td>
<td>1.270</td>
<td>658.75</td>
<td>2.70E+16</td>
<td>0.0554</td>
</tr>
<tr>
<td>-3 σ PMOS</td>
<td>-1.745</td>
<td>178.09</td>
<td>1.46E+16</td>
<td>0.0762</td>
</tr>
<tr>
<td>Nominal PMOS</td>
<td>-1.154</td>
<td>223.45</td>
<td>2.05E+16</td>
<td>0.1209</td>
</tr>
<tr>
<td>+3 σ PMOS</td>
<td>-0.563</td>
<td>268.81</td>
<td>2.64E+16</td>
<td>0.1656</td>
</tr>
</tbody>
</table>

Table 1.0: Statistical SPICE Model Decks

Since a normal distribution was assumed, Gaussian plots were made for each of the SPICE parameters, and are shown in *Appendix E: Data Analysis*. The first two plots are for VT0 for each of the wafers D8 through D15 (D12 was not included since it was not completely tested due to extremely poor yield). These two plots show the variation in threshold voltage for the different device wafers. The vertical scale indicated the yield for the different wafers. The number of test die locations per wafer was 73, and the height of the curves is the number of good die locations divided by 73. The difference from wafer to wafer is due primarily to the different threshold adjustment implants the wafers received during processing (see Procedure section above). The second plot shows the absolute value of the PMOS threshold voltages with the NMOS threshold voltages. This is a more desirable plot, since it shows how well the VT0 curves overlap for a particular device wafer. The goal would be for the NMOS and PMOS curves to completely overlap one another exactly in other words be symmetrical, like +0.9 and -0.9. D10 is the closest to having the NMOS and PMOS curves overlap as desired.

The third plot shows Gaussian plots of U0, the surface mobility of the majority carriers. As would be expected, the U0 curves for the NMOS devices
generally overlap one another, as do the U0 curves for the PMOS devices. This indicates that the threshold adjustment implants have very little effect on the mobility but do determine the threshold voltage.

The remaining two extracted parameters, NSUB and THETA were not examined in any more detail. It should be noted that a lack of good statistics knowledge led to blindly plowing through this particular analysis work, and a more thorough study of the extraction theory and the use of statistics to correlate process parameter variation to extracted parameter variation should be done before repeating this experiment and attempting to look at the resulting data in any more depth. It should also be noted that for the purposes of creating a simple statistical model (mean, and ±3σ model decks), a greater understanding of statistics is not necessary, but would be very helpful, especially in determining the weak points of the statistical model and determining the source or sources of model parameter variations.

The following table (Table 1.1: Comparison of Simulation and Measured Data) shows a comparison of the simulation parameter values vs. the measured values. The parameters include both process parameters such as gate oxide thickness, and SPICE parameters, such as VT0.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation Value</th>
<th>Stat. Match</th>
<th>Average Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Oxide Thickness (Å)</td>
<td>412 Å (NMOS)</td>
<td>-</td>
<td>413 Å (σ=21)</td>
</tr>
<tr>
<td></td>
<td>400 Å (PMOS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Field Oxide Thickness (Å)</td>
<td>7630 Å</td>
<td>-</td>
<td>7142 Å (σ=153)</td>
</tr>
<tr>
<td>D8 VT0 (NMOS)</td>
<td>0.037 volts</td>
<td>N</td>
<td>-0.048 volts (σ=0.019)</td>
</tr>
<tr>
<td>D9 VT0 (NMOS)</td>
<td>0.846 volts</td>
<td>Y</td>
<td>0.869 volts (σ=0.086)</td>
</tr>
<tr>
<td>D10 VT0 (NMOS)</td>
<td>1.114 volts</td>
<td>N</td>
<td>1.027 volts (σ=0.081)</td>
</tr>
<tr>
<td>D11 VT0 (NMOS)</td>
<td>1.312 volts</td>
<td>N</td>
<td>1.297 volts (σ=0.063)</td>
</tr>
<tr>
<td>D13 VT0 (NMOS)</td>
<td>1.312 volts</td>
<td>N</td>
<td>1.228 volts (σ=0.035)</td>
</tr>
<tr>
<td>D14 VT0 (NMOS)</td>
<td>1.466 volts</td>
<td>N</td>
<td>1.406 volts (σ=0.043)</td>
</tr>
<tr>
<td>D15 VT0 (NMOS)</td>
<td>1.605 volts</td>
<td>N</td>
<td>1.523 volts (σ=0.043)</td>
</tr>
<tr>
<td>D8 VT0 (PMOS)</td>
<td>-1.63 volts</td>
<td>N</td>
<td>-2.087 volts (σ=0.201)</td>
</tr>
<tr>
<td>D9 VT0 (PMOS)</td>
<td>-0.83 volts</td>
<td>N</td>
<td>-1.524 volts (σ=0.283)</td>
</tr>
<tr>
<td>D10 VT0 (PMOS)</td>
<td>-0.35 volts</td>
<td>N</td>
<td>-1.154 volts (σ=0.197)</td>
</tr>
<tr>
<td>D11 VT0 (PMOS)</td>
<td>0.16 volts</td>
<td>N</td>
<td>-0.654 volts (σ=0.186)</td>
</tr>
<tr>
<td>D13 VT0 (PMOS)</td>
<td>0.16 volts</td>
<td>N</td>
<td>-0.597 volts (σ=0.225)</td>
</tr>
<tr>
<td>D14 VT0 (PMOS)</td>
<td>0.71 volts</td>
<td>N</td>
<td>-0.057 volts (σ=0.082)</td>
</tr>
<tr>
<td>D15 VT0 (PMOS)</td>
<td>1.25 volts</td>
<td>N</td>
<td>0.825 volts (σ=0.323)</td>
</tr>
<tr>
<td>N-Well Xj (junction depth)</td>
<td>4.8 μm</td>
<td>-</td>
<td>4.8 μm</td>
</tr>
<tr>
<td>Source/Drain Xj (NMOS)</td>
<td>0.22 μm</td>
<td>-</td>
<td>0.40 μm</td>
</tr>
<tr>
<td>Source/Drain Xj (PMOS)</td>
<td>0.24 μm</td>
<td>-</td>
<td>0.37 μm</td>
</tr>
</tbody>
</table>

Table 1.1: Comparison of Simulation and Measured Data

The measured data has sigma values given for the data range where multiple data points were measured. The simulated VT0 values for both NMOS and PMOS were tested statistically against the mean of the measured values to see if they were considered "equal" (see Appendix E: Data Analysis). As can be seen by the nearly zero p-values for the cases where the mean was not considered "equal" to the simulated VT0, they were considered strongly not "equal." Only one of the tests showed the simulated value to be considered "equal" to the measured value. These
results mean that the simulations are currently not very good at predicting the mean VTO’s for the various threshold voltage adjustment implants. Improvements need to be made to get better correlation.
Conclusions

Use of parameter domain statistics to analyze large amounts of extracted SPICE parameters is a simple and illustrative technique, which can be easily adapted to the classroom. With the use of basic statistical methods the correlation between process variations and SPICE parameter variations may be observed. The resulting variations in the circuit and device performance may be observed through the use of the statistical SPICE model decks and circuit simulators.

Additionally, the use of process simulation and the ease of which process variables may be varied, provides a fast and simple method of examining process variations. This is particularly useful for a classroom environment, where it is not practical to fabricate transistors in the lab. An entire three month CMOS process may be completed in less than one hour of simulation, and for the cost of only a few extra hours at most. Different processing parameters may be varied and simulated devices may be examined to observe the effects of the process parameter variations. SPICE parameter extractions may also be performed on the simulated devices. This is also helpful before or during the manufacturing of devices in the lab.

For this particular experiment, the simulated results corresponded to the measured results fairly well for some of the values, such as gate oxide thickness, but very poorly for others, such as VT0. The poor correlation between simulated
threshold voltages and measured threshold voltages for the both NMOS and PMOS devices indicates that the simulated model requires further investigation and refinement to produce better results. One of the parameters, which may be the cause of some of the simulation problems is the oxide charge parameter. The value used in simulation was purely an educated guess, and not a measured quantity. The actual trapped oxide charge in the measured devices may be greater or less than the value used in simulation, and thus a possible cause for differences between the two sets of data. This value can be extracted from the plot of the gate capacitor C-V curves, but this was not known at the time, and is suggested for future test measurement and simulation work.

Parameter domain statistical parameter extraction is a simple tool for illustrating the effects of process variation on individual device and circuit performance. Ideally, it would be used on a stable process, that is relatively consistent from lot to lot, but may also be useful during process development. In the case of the latter, parameter domain statistical parameter extraction could help the process engineers find processing problems, by observing variations in the statistical device models. Trouble spots in the statistical models, such as a large variation in a particular parameter, could then be traced back to problems with either the process itself or problems with one or more processing steps.
Appendix A: Test and Device Chip Designs
Device Chip Layout

Figure A.0: Device Chip Layout
Test Chip Layout

Figure A.1: Test Chip Layout
Appendix B: Process Simulation Files
Process Simulation for D11

$ TMA TSUPREM4 RIT-SCN CMOS NMOS enhancement transistor simulation
$ DATE 3/30/92 - Moved to beavis 3-24-94
COMMENT FILENAME SCN1.IN
$ FILES CREATED SCN1.STR - SUPREM IV
structure file just before
device V1 adjustment implant
COMMENT FILES USED NONE
COMMENT CREATED BY ROB PEARSON
COMMENT EDITED BY SCOTT A. HILDRETH
COMMENT PURPOSE NMOS
device of SCN CMOS
COMMENT
$
$ 3-24-94, I should use LORENZO to read in the mask information
$ MASK LEVELS xxxx - opaque ---- clear
$
$ X axis - um 0---1---2---3---4---5---6---7---8---9---10---11---
12---13---14
$
$ nwell
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
xxxxxxxxxxxx
$ NMOS device is not in the well
$ active
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
xxxxxxxxxxxx
$ field-----------------------------
$ only the nwell is covered, totally clear for NMOS
$ poly xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
-----
$ psselect
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
xxxxxxxxxxxx
$ NMOS devices covered, not implanted, PMOS implanted
$ not psselect -----------------------------
$ NMOS devices implanted
$ contact xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$ metal1 ------------------------
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$ via not simulated
$ metal2 not simulated
$ passivation not simulated
$
$ Define the grid
$
$ Note: The following "DEFINE" statement sets the grid density for the
$ simulation. A larger value of "GDENS" gives a denser grid.
$ A value of 1 is used for setting up the simulation; 2 is
$ used for most of the simulation work, while values of 3 or
$ greater are used to get the final answers.
$ OPTION NORMAL
$ DEFINE GDENS 1
$ Specify the horizontal grid spacings at various x values
LINE X LOCATION=0.0 SPACING=(0.2/GDENS)
LINE X LOCATION=3.0 SPACING=(0.2/GDENS)
LINE X LOCATION=4.0 SPACING=(0.5/GDENS)
LINE X LOCATION=10.0 SPACING=(0.5/GDENS)
LINE X LOCATION=11.0 SPACING=(0.1/GDENS)
LINE X LOCATION=13.0 SPACING=(0.1/GDENS)
LINE X LOCATION=14.0 SPACING=(0.2/GDENS)
$ Specify the vertical grid spacings at various y values
LINE Y LOCATION=0.0 SPACING=(0.1/GDENS)
LINE Y LOCATION=1.0 SPACING=(0.2/GDENS)
LINE Y LOCATION=10.0 SPACING=(2.0/GDENS)
$ Tailor the grid to the device being simulated
$ Eliminate horizontal grid lines below the active device
$ Eliminate vertical grid lines deep in the substrate
ELIMINATE COLUMNS Y.MIN=2.0
ELIMINATE COLUMNS Y.MIN=3.0
ELIMINATE COLUMNS Y.MIN=4.0
$ Initialize the structure
INITIALIZE RATIO=1.5 <100> ROT.SUB=0.0
BORON=0.3E16
OPTION DEVICE=X
SELECT TITLE="RITSCN CMOS - NMOS Initial
Grid"
PLLOT.2D X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0
Y.OFFSET=2.0 T.SIZE=0.4 +
BOUNDARY GRID GRID=I C.GRID=1
$ Initial well masking and alignment oxidation
METHOD VERTICAL
DIFFUSION TIME=10 TEMP=1000 F.O2=6.0
F.N2=1.0
DIFFUSION TIME=55 TEMPERAT=1000 F.O2=2.0
F.H2O=2.0
DIFFUSION TIME=5 TEMP=1000 F.O2=7.0
F.N2=1.0
DIFFUSION TIME=15 TEMPERAT=1000
T.FINAL=1150 F.O2=7.0 F.N2=1.0
DIFFUSION TIME=60 TEMPERAT=1150 F.N2=4.0
$ Do well photolithography (NMOS device completely
covered)
DEPOSIT PHOTORESIST THICKNESS=1.2
SELECT Z=BORON-0.3E16 TITLE="RESIST FROM
WELL LITHOGRAPHY"
PRINT.ID LAYERS X.VALUE=14.0
PLLOT.2D X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0
Y.OFFSET=2.0 T.SIZE=0.4 +
L.BOUND=1 C.BOUND=1
$ Colors: 2-red, 3-green, 4-blue, 5-cyan, 6-magenta, 7-
yellow, 8>=?
$ Always color the layers before drawing the contours, or
colors will fill overlapping
COLOR COLOR=5 OXIDE
COLOR COLOR=2 PHOTORES
LABEL LABEL=OXIDE CM X=4 Y=4 COLOR=1
LEFT SIZE=0.25 RECTANGL C.RECTAN=5+
W.RECTAN=0.3 H.RECTAN=0.5
LABEL LABEL=PHOTORESIST CM X=4 Y=5
COLOR=1 LEFT SIZE=0.25 RECTANGL+
C.RECTAN=2 W.RECTAN=0.5 H.RECTAN=0.5
$ Phosphorus well implant (PH3 source)
IMPLANT PHOSPHOR DOSE=6E12 ENERGY=130
SELECT Z=LOG10(PHOSPHOR)
TITLE="MASKING THE N-WELL IMPLANT"
PLLOT.2D X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0
Y.OFFSET=2.0 T.SIZE=0.4 +
L.BOUND=1 C.BOUND=1
COLOR COLOR=5 OXIDE
COLOR COLOR=2 PHOTORES
LABEL LABEL=OXIDE CM X=4 Y=4 COLOR=1
LEFT SIZE=0.25 RECTANGL C.RECTAN=5+
W.RECTAN=0.3 H.RECTAN=0.5
LABEL LABEL=PHOTORESIST CM X=4 Y=5
COLOR=1 LEFT SIZE=0.25 RECTANGL+
C.RECTAN=2 W.RECTAN=0.5 H.RECTAN=0.5
FOREACH X (12 TO 15 STEP 0.5)
CONTOUR VALUE=X LINE.TYP=3 COLOR=1
END

ETCH PHOTORESIST ALL
$ N well drive-in/oxide growth
DIFFUSION TIME=10 TEMPERAT=1000 F.O2=8
DIFFUSION TIME=26 TEMPERAT=1000 F.H2O=6
DIFFUSION TIME=10 TEMPERAT=1000 F.O2=8
DIFFUSION TIME=15 TEMPERAT=1000
T.FINAL=1150 F.N2=4
DIFFUSION TIME=1250 TEM=1150 F.N2=4.0
DIFFUSION TIME=90 TEMPERATURE=1150
T.FINAL=800 F.N2=4.0
DIFFUSION TIME=360 TEM=800 F.N2=4.0
SELECT Z=LOG10(BORON) TITLE="AFTER N- WELL DRIVE-IN"

PLOT.2D X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0
Y.OFFSET=2.0 T.SIZE=0.4 +
L.BOUND=1 C.BOUND=1
COLOR COLOR=5 OXIDE
LABEL LABEL=OXIDE CM X=4 Y=4 COLOR=1
LEFT SIZE=0.25 RECTANGL C.RECTAN=5 +
W.RECTAN=0.5 H.RECTAN=0.5
FOREACH X (15 TO 20 STEP 0.5)
CONTOUR VALUE=X LINE.TYP=2 COLOR=1
END

PRINT.1D LAYERS X.VALUE=14.0
PRINT.1D LAYERS X.VALUE=0.0
$ Field oxidation
METHOD COMPRESS
$
$ The initial drive-in should be in nitrogen with 0.1-0.2 % oxygen
$

DIFFUSION TIME=15 TEMPERAT=800 F.O2=0.0055
F.N2=5.5
DIFFUSION TIME=18 TEMPERAT=800
T.FINAL=1100 F.O2=0.0055 F.N2=5.5
DIFFUSION TIME=25 TEMPERAT=1100 F.O2=0.0055
F.N2=5.5
DIFFUSION TIME=30 TEMPERAT=1100
T.FINAL=950 F.O2=0.0055 F.N2=5.5
DIFFUSION TIME=15 TEMPERAT=950 F.O2=0.0055
F.N2=5.0
DIFFUSION TIME=30 TEMPERAT=950 F.N2=5.0
DIFFUSION TIME=30 TEMPERAT=950 T.FINAL=800
F.N2=5.0
SELECT Z=LOG10(BORON) TITLE="AFTER LOCOS"

PLOT.2D X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0
Y.OFFSET=2.0 T.SIZE=0.4 +
L.BOUND=1 C.BOUND=1
COLOR COLOR=5 OXIDE
COLOR COLOR=2 PHOTORES
COLOR COLOR=3 NITRIDE
LABEL LABEL=OXIDE CM X=4 Y=4 COLOR=1
LEFT SIZE=0.25 RECTANGL C.RECTAN=5 +
W.RECTAN=0.5 H.RECTAN=0.5
LABEL LABEL=NITRIDE CM X=4 Y=5 COLOR=1
LEFT SIZE=0.25 RECTANGL C.RECTAN=3 +
W.RECTAN=0.5 H.RECTAN=0.5
LABEL LABEL=PHOTORESIST CM X=4 Y=6
COLOR=1 LEFT SIZE=0.25 RECTANGL +
C.RECTAN=2 W.RECTAN=0.5 H.RECTAN=0.5
FOREACH X (15 TO 20 STEP 1.0)
CONTOUR VALUE=X LINE.TYP=3 COLOR=2
END

LABEL LABEL="BORON CONC. 1e15, 1e16 etc."
CM X=4 Y=7 COLOR=1 LEFT +
SIZE=0.25 LINE.TYP=2 C.LINE=1 LENGTH=0.5
PRINT.1D LAYERS X.VALUE=14.0
PRINT.1D LAYERS X.VALUE=0.0
$ Boron field implant
IMPLANT BORON DOSE=4E13 ENERGY=38
PEARSON RP.EFF
SELECT Z=LOG10(BORON) TITLE="JUST AFTER FIELD VT ADJUST IMPLANT"

PLOT.2D X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0
Y.OFFSET=2.0 T.SIZE=0.4 +
L.BOUND=1 C.BOUND=1
COLOR COLOR=5 OXIDE
COLOR COLOR=2 PHOTORES
COLOR COLOR=3 NITRIDE
LABEL LABEL=OXIDE CM X=4 Y=4 COLOR=1
LEFT SIZE=0.25 RECTANGL C.RECTAN=5 +
W.RECTAN=0.5 H.RECTAN=0.5
LABEL LABEL=NITRIDE CM X=4 Y=5 COLOR=1
LEFT SIZE=0.25 RECTANGL C.RECTAN=3 +
W.RECTAN=0.5 H.RECTAN=0.5
LABEL LABEL=PHOTORESIST CM X=4 Y=6
COLOR=1 LEFT SIZE=0.25 RECTANGL +
C.RECTAN=2 W.RECTAN=0.5 H.RECTAN=0.5
FOREACH X (15 TO 20 STEP 1.0)
CONTOUR VALUE=X LINE.TYP=2 COLOR=1
END

LABEL LABEL="BORON CONC. 1e15, 1e16 etc."
CM X=4 Y=7 COLOR=1 LEFT +
SIZE=0.25 LINE.TYP=2 C.LINE=1 LENGTH=0.5
ETCH NITRIDE ALL
ETCH OXIDE THICKNESS=0.11 DRY
SELECT Z=LOG10(BORON) TITLE="AFTER NITRIDE AND PAD OXIDE ETCH"

PLOT.2D X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0
Y.OFFSET=2.0 T.SIZE=0.4 +
L.BOUND=1 C.BOUND=1
$ NMOS devices covered, not implanted, PMOS implanted
$ not pselect ---------------------------------------------
$ $ NMOS devices implanted
$ contact xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$ $ via not simulated
$ $ metal2 not simulated
$ $ passivation not simulated
$ $ Initialize the structure using the structure file created in
$ scnn1.inp
$ INITIALIZE IN.FILE=SCNP1.STR SCALE=1.0
$ $ Unmasked device THRESHOLD voltage adjustment implant
$ IMPLANT BORON DOSE=2.0e12 ENERGY=35
$ PEARSON RP.EFF
$ $ The punchthrough implant is done at this time.
$ $ IMPLANT BORON DOSE=2.0e12 ENERGY=35
$ PEARSON RP.EFF
$ SELECT Z=LOG10(BORON)+
$ TITLE="D11: VT ADJUSTMENT IMPLANT = 2.0E12"
$ PRINT1D X.VALUE=14 LAYERS
$ PRINT1D X.VALUE=0.0 LAYERS
$ PLOT2D SCALE X.SIZE=0.25 Y.SIZE=0.25
$ X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
$ L.BOUND=1 C.BOUND=1
$ COLOR COLOR=5 OXIDE
$ LABEL LABEL="KOOI OXIDE AND FIELD OXIDE" CM X=4 Y=4 COLOR=1 LEFT SIZE=0.25 +
$ RECTANGL C.RECTAN=5 H.RECTAN=0.5
$ $ This structure file can be used for SCN NMOS enh.
$ STRUCTURE OUTFILE=SCNN1.STR
$ STOP
$ $ TMA TSUPREM4 RIT-SCN CMOS PMOS
$ enhancement transistor simulation - Part 2
$ $ DATE 4/9/92 Moved to beavis 3-24-94
$ $ FILENAME SCNP2.IN
$ $ FILES CREATED SCNP_M.STR - MEDICI structure file
$ $ FILES USED SCNP1.STR - SUPREM IV structure file before device VT implant
$ $ CREATED BY ROB PEARSON & Scott Hildreth
$ $ PURPOSE PMOS device of SCN CMOS
$ COMMENT
$ $ Use LORENZO to read in mask information
$ $ $ MASK LEVELS xxxx - opaque ---- clear
$ $ $ x axis - um 0--1--2--3--4--5--6--7--8--9--10--11--12--13--14
$ $ $ sawell
$ $ xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$ $ xxxxxxxxxxx
$ $ NMOS device is not in the well
$ $ active
$ $ xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$ $ xxxxxxx
$ $ fieldv --------------------------
$ $ only the sawell is covered, totally clear for NMOS
$ $ poly xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$ $ $ pselect
$ $ xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$
$ 10 950 - 4.0 - $ Pull in Wet O2 with a flow of 2.0
DIFFUSION TIME=20 TEMPERAT=800 T.FINAL=950
INERT PHOSPHOR=1.0x20
DIFFUSION TIME=10 TEMPERAT=950 INERT
PHOSPHOR=1.0x20
DIFFUSION TIME=30 TEMPERAT=950 T.FINAL=800
WETO2 PHOSPHOR=1.0x20
$ $ Step - Etch spin on dopant or oxide grown during the
anneal from poly $ ETCH OXIDE DRY THICKNESS=.01 $ Do polysilicon photolithography
$ Step - Plasma Etch the Polysilicon $ ETCH POLYSILICON RIGHT P1.X=2.0 P1.Y=0.5
P2.X=1.8 P2.Y=1.0
SELECT Z=doping
PRINT.1D LAYERS X.VALUE=14.0
PRINT.1D X.VALUE=4.0 LAYERS
$ $*************** I may change this step $***************
$Step - Gate Oxide Etch Back (leave about 200-300A of
oxide to implant) $ through - I didn't do this step. $***************
$ ETCH OXIDE OLD.DRY THICKNESS=0.03 $$ ***************
$ Step - Pselect lithography $ DEPOSIT PHOTORESIST THICKNESS=1.2
$ Pattern the resist for the implant $ Step - NMOS D/S Implant $ Species - BF2 (Diborane B2H3 source)
$ IMPLANT BF2 DOSE=1.0E15 ENERGY=55
SELECT Z=doping
PRINT.1D LAYERS X.VALUE=0.0
$ ETCH PHOTORESIST ALL
$ ***************
$ Step - Inverse Pselect (NSElect) lithography, Not for
PMOS devices $ DEPOSIT PHOTORESIST THICKNESS=1.2
$ Pattern the resist for the phosphorus (NMOS) drain
source implant $ Step - NMOS D/S Implant $ Species - P (Phosphine PH3 source)
$ IMPLANT PHOSPHOR DOSE=1.0E15 ENERGY=35
PEARSON RP.EFF
ETCH PHOTORESIST ALL
SELECT Z=doping
PRINT.1D LAYERS X.VALUE=0.0
$ Step - Thermally Grown Passivation Oxide $ time temp. gas flows (standard liters per minute)
$ Start End 02 N2 H2O $ $ 15 900 2.0 - 2.0 $ $ DIFFUSION TIME=15 TEMPERAT=800 F.H2O=4.0
$ $ Step - Spin On Glass (SOG) $ $ Accuglass (Allied Signal) #2995-653 211 lot#8779,
3000pm $ 140C prebake for 30 minutes $ 3000A of Glass after densification $ Densification
$ time temp. gas flows (standard liters per minute)
$ Start End 02 N2 H2O $ $ 30 900 2.0 - 2.0 $ $ DEPOSIT OXIDE THICKNESS=0.3 SPACES=5
DIFFUSION TIME=30 TEMPERAT=900 F.H2O=4.0
$ Step - Contacts cut lithography, Etch Contacts $ ETCH OXIDE START X=5.5 Y=1.0
ETCH CONTINUE X=6.0 Y=1.5
ETCH CONTINUE X=10.0 Y=1.5
ETCH DONE X=10.5 Y=1.0
SELECT Z=doping
PRINT.1D LAYERS X.VALUE=8.0
$ Step - Aluminum Deposition (0.6 microns), Sinter $ DEPOSIT ALUMINUM THICKNESS=0.6
$ Step - Metal lithography, Etch metal $ ETCH ALUMINUM PI.X=4.0 LEFT $ $Step - Strip resist $ $ Plot the final SCN CMOS structure
SELECT Z=LOG10(PHOSPHORUS) TITLE="RITSCN
CMOS - PMOS (final)" PLOT.2D Y.MAX=2.0 X.VALUE=0.25 Y.VALUE=0.25
X.OFFSET=2.0 Y.OFFSET=2.0 +
T.VALUE=0.4 L.BOUND=1 C.BOUND=1
COLOR COLOR=5 OXIDE
COLOR COLOR=4 ALUMINUM
COLOR COLOR=6 POLYSILI
LABEL LABEL=ALUMINUM CM X=14 Y=3
COLOR=1 LEFT SIZE=0.25 RECTANGL +
C.RECTAN=4 W.RECTAN=0.5 H.RECTAN=0.5
LABEL LABEL=POLYSILICON CM X=9 Y=3
COLOR=1 LEFT SIZE=0.25 RECTANGL +
C.RECTAN=6 W.RECTAN=0.3 H.RECTAN=0.3
LABEL LABEL=OXIDE CM X=4 Y=3 COLOR=1
LEFT SIZE=0.25 RECTANGL C.RECTAN=5 +
W.RECTAN=0.5 H.RECTAN=0.5
FOREACH X (15 TO 20 STEP 1.0) CONTOUR VALUE=X LINE.TYP=2 COLOR=2 END
LABEL LABEL="PHOS CONC. 1e15, 1e16, 1e17,
1e18, 1e19, 1e20" CM X=4 Y=4 +
COLOR=1 LEFT SIZE=0.25 LINE.TYP=2 C.LINE=2
LENGTH=0.5
SELECT Z=LOG10(BORON) FOREACH X (15 TO 20 STEP 1.0)
CONTOUR VALUE=X LINE.TYP=1 COLOR=3 END
LABEL LABEL="BORON CONC. 1e15, 1e16, 1e17,
1e18, 1e19, 1e20" CM X=4 Y=5 +
COLOR=1 LEFT SIZE=0.25 LINE.TYP=1 C.LINE=3
LENGTH=0.5 $ $ Now make 1D plots of concentrations in the gate and
D/S regions
SELECT Z=LOG10(BORON) +
TITLE="RITSCN CMOS - PMOS device" PLOT.1D X.VALUE=0.5 LINE.TYP=2 COLOR=2
RIGHT=2.0 BOTTOM=13 TOP=18 +
X.VALUE=0.25 Y.VALUE=0.25 X.OFFSET=2.0
Y.OFFSET=2.0 T.VALUE=0.4
LABEL  LABEL="BORON CONC." CM X=4 Y=4
        COLOR=1 LEFT SIZE=0.25 LINE.TYP=2 +
C.LINE=2 LENGTH=0.5
SELECT  Z=LOG10(PHOSPHORUS)
PLOT.1D  X.VALUE=0.5 LINE.TYP=1 COLOR=3
   ^AXES ^CLEAR
LABEL  LABEL="PHOSPHORUS CONC." CM X=4
        Y=5 COLOR=1 LEFT SIZE=0.25 +
LINE.TYP=1 C.LINE=3 LENGTH=0.5
$
$ This MEDICI structure file can be used for modeling
SCN PMOS enh.
STRUCTURE REFLECT LEFT
STRUCTURE OUT.FILE=SCNP_D11_M.STR
SCALE=1.0 MEDICI POLY.ELE
STOP
Figure B.0: Simulation Plot - Initial NMOS Grid
Figure B.1: Simulation Plot - N-Well Resist Mask
Figure B.2: Simulation Plot - N-Well Implant
Figure B.3: Simulation Plot - Post N-Well Drive-In
Figure B.4: Simulation Plot - Pre Field \( V_T \) Adjust Implant
Figure B.5: Simulation Plot - Post Field $V_T$ Adjust Implant
Figure B.6: Simulation Plot - LOCOS
Figure B.7: Simulation Plot - Nitride and Pad Oxide Etch
Figure B.8: Simulation Plot - Kooi Oxide Growth

NMOS Isolation following Kooi oxide growth

--- BORON CONC. 1e15, 1e16 etc.

OXIDE
Figure B.9: Simulation Plot - $V_T$ Adjustment Implant $2.0E+12$
Figure B.10: Simulation Plot - Final NMOS Device Structure
Figure B.11: Simulation Plot - 1D Cut Plot Under Gate and Drain
Figure B.12: Simulation Plot - $I_d$ vs. $V_g$ for D8 NMOS
Figure B.13: Simulation Plot - Id vs. Vg for D9 NMOS
Figure B.14: Simulation Plot - Id vs. Vg for D10 NMOS
Figure B.15: Simulation Plot - Id vs. Vg for D11 NMOS

$V_{ds} = 0.1\, V$

$12\, \text{amps/micron} \times 10^{16}$

$V_1$ (Volts)
Figure B.16: Simulation Plot - Id vs. Vg for D14 NMOS
Figure B.17: Simulation Plot - Id vs. Vg for D15 NMOS
Appendix C: Sample Parameter Extraction Measurements

The pairs of plots below (Figures C.0 - C.6) show sample I-V curves before (top) and after optimization (bottom). The measured curve is the solid line and the simulated curve is dashed. The optimization generally improves the match between measured and simulated curves.
Figure CO: Sample D8 Id vs. Vg Curves
Figure C.1: Sample D9 $I_D$ vs. $V_g$ Curves
D10 NMOS Location 60: Before/After Optimization

Figure C.2: Sample D10 Id vs. Vg Curves
Figure C.3: Sample D1 I_d vs. V_g Curves
D13 NMOS Location 61: Before/After Optimization

Figure C.4: Sample D13 Id vs. Vg Curves
D14 NMOS Location 35: Before/After Optimization

Figure C.5: Sample D14 Id vs. Vg Curves
D15 NMOS Location 82: Before/After Optimization

Figure C.6: Sample D15 Id vs. Vg Curves
Appendix D: Wafer Maps

The wafer maps show the good test die locations for NMOS, PMOS, and the combination of NMOS and PMOS. For the NMOS and PMOS wafer maps, the good die locations are marked with an X, and the gray areas are non-test die locations. For the composite wafer maps, the areas marked with a P, are where only the PMOS device was good. An N means that only the NMOS device was good, and a # means that both the NMOS and PMOS devices were good.
Figure D.0: NMOS and PMOS Wafer Maps
Appendix E: Data Analysis

Tables E.0 and E.1 summarize the four extracted SPICE parameters, number of good die locations, and yield for each of the wafers, D8-D15. Figure E.0 shows the Gaussian distributions for the VT0 data for each wafer. This shows not only the spread for the individual distributions, but also shows how the distributions shift with the threshold voltage adjustment implants. Figure E.1 shows the ideal threshold adjustment implant based upon NMOS Vt and the negative of the PMOS Vt for both measured and simulated devices. Tables E.2 and E.3 summarize the statistical analysis of the simulated VT0 compared to the mean VT0 for the measured data. The p-value is a gauge of how strongly “equal” or “not equal” the result is. A very low p-value for a result of “not equal” means that the simulated VT0 and the mean VT0 are very “not equal” The single “equal” case (D9 NMOS) can be considered fairly equal from the p-value of 0.419.
<table>
<thead>
<tr>
<th>Wafer</th>
<th>8</th>
<th>8</th>
<th>8</th>
<th>8</th>
<th>8</th>
<th>8</th>
<th>8</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vt Dose</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Parameter</td>
<td>VTO</td>
<td>VTO</td>
<td>UO</td>
<td>UO</td>
<td>NSUB</td>
<td>NSUB</td>
<td>THETA</td>
<td>THETA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count</td>
<td>14</td>
<td>57</td>
<td>14</td>
<td>57</td>
<td>14</td>
<td>57</td>
<td>14</td>
<td>57</td>
</tr>
<tr>
<td>Yield</td>
<td>0.19</td>
<td>0.78</td>
<td>0.19</td>
<td>0.78</td>
<td>0.19</td>
<td>0.78</td>
<td>0.19</td>
<td>0.78</td>
</tr>
<tr>
<td>Mean</td>
<td>-0.05</td>
<td>-2.09</td>
<td>640.41</td>
<td>177.70</td>
<td>3.85E+15</td>
<td>3.56E+16</td>
<td>0.08</td>
<td>0.07</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.02</td>
<td>0.20</td>
<td>27.03</td>
<td>12.68</td>
<td>1.83E+15</td>
<td>1.00E+16</td>
<td>0.00</td>
<td>0.02</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wafer</th>
<th>9</th>
<th>9</th>
<th>9</th>
<th>9</th>
<th>9</th>
<th>9</th>
<th>9</th>
<th>9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vt Dose</td>
<td>1E+12</td>
<td>1E+12</td>
<td>1E+12</td>
<td>1E+12</td>
<td>1E+12</td>
<td>1E+12</td>
<td>1E+12</td>
<td>1E+12</td>
</tr>
<tr>
<td>Parameter</td>
<td>VTO</td>
<td>VTO</td>
<td>UO</td>
<td>UO</td>
<td>NSUB</td>
<td>NSUB</td>
<td>THETA</td>
<td>THETA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count</td>
<td>10</td>
<td>57</td>
<td>10</td>
<td>57</td>
<td>10</td>
<td>57</td>
<td>10</td>
<td>57</td>
</tr>
<tr>
<td>Yield</td>
<td>0.14</td>
<td>0.78</td>
<td>0.14</td>
<td>0.78</td>
<td>0.14</td>
<td>0.78</td>
<td>0.14</td>
<td>0.78</td>
</tr>
<tr>
<td>Mean</td>
<td>0.87</td>
<td>-1.52</td>
<td>463.17</td>
<td>214.76</td>
<td>4.15E+16</td>
<td>2.33E+16</td>
<td>0.01</td>
<td>0.16</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.09</td>
<td>0.28</td>
<td>177.63</td>
<td>135.77</td>
<td>4.72E+16</td>
<td>4.17E+16</td>
<td>0.06</td>
<td>0.48</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wafer</th>
<th>10</th>
<th>10</th>
<th>10</th>
<th>10</th>
<th>10</th>
<th>10</th>
<th>10</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vt Dose</td>
<td>1.5E+12</td>
<td>1.5E+12</td>
<td>1.5E+12</td>
<td>1.5E+12</td>
<td>1.5E+12</td>
<td>1.5E+12</td>
<td>1.5E+12</td>
<td>1.5E+12</td>
</tr>
<tr>
<td>Parameter</td>
<td>VTO</td>
<td>VTO</td>
<td>UO</td>
<td>UO</td>
<td>NSUB</td>
<td>NSUB</td>
<td>THETA</td>
<td>THETA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count</td>
<td>54</td>
<td>61</td>
<td>54</td>
<td>61</td>
<td>54</td>
<td>61</td>
<td>54</td>
<td>61</td>
</tr>
<tr>
<td>Yield</td>
<td>0.74</td>
<td>0.64</td>
<td>0.74</td>
<td>0.64</td>
<td>0.74</td>
<td>0.64</td>
<td>0.74</td>
<td>0.64</td>
</tr>
<tr>
<td>Mean</td>
<td>1.03</td>
<td>-1.15</td>
<td>510.31</td>
<td>223.45</td>
<td>2.34E+16</td>
<td>2.05E+16</td>
<td>0.04</td>
<td>0.12</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.08</td>
<td>0.20</td>
<td>49.48</td>
<td>15.12</td>
<td>1.20E+15</td>
<td>1.98E+15</td>
<td>0.00</td>
<td>0.01</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wafer</th>
<th>11</th>
<th>11</th>
<th>11</th>
<th>11</th>
<th>11</th>
<th>11</th>
<th>11</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vt Dose</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
</tr>
<tr>
<td>Parameter</td>
<td>VTO</td>
<td>VTO</td>
<td>UO</td>
<td>UO</td>
<td>NSUB</td>
<td>NSUB</td>
<td>THETA</td>
<td>THETA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count</td>
<td>63</td>
<td>53</td>
<td>63</td>
<td>53</td>
<td>63</td>
<td>53</td>
<td>63</td>
<td>53</td>
</tr>
<tr>
<td>Yield</td>
<td>0.86</td>
<td>0.73</td>
<td>0.86</td>
<td>0.73</td>
<td>0.86</td>
<td>0.73</td>
<td>0.86</td>
<td>0.73</td>
</tr>
<tr>
<td>Mean</td>
<td>1.30</td>
<td>-0.65</td>
<td>451.63</td>
<td>233.73</td>
<td>4.46E+16</td>
<td>2.37E+16</td>
<td>0.03</td>
<td>0.13</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.06</td>
<td>0.19</td>
<td>38.63</td>
<td>12.20</td>
<td>2.49E+15</td>
<td>1.63E+15</td>
<td>0.01</td>
<td>0.01</td>
</tr>
</tbody>
</table>

Table E.0: D8 - D11 SPICE Parameter Summary
<table>
<thead>
<tr>
<th>Wafer</th>
<th>13</th>
<th>13</th>
<th>13</th>
<th>13</th>
<th>13</th>
<th>13</th>
<th>13</th>
<th>13</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vt Dose</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
<td>2E+12</td>
</tr>
<tr>
<td>Parameter</td>
<td>VTO</td>
<td>VTO</td>
<td>UO</td>
<td>UO</td>
<td>NSUB</td>
<td>NSUB</td>
<td>THETA</td>
<td>THETA</td>
</tr>
<tr>
<td>Type</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>Count</td>
<td>65</td>
<td>60</td>
<td>65</td>
<td>60</td>
<td>65</td>
<td>60</td>
<td>65</td>
<td>60</td>
</tr>
<tr>
<td>Yield</td>
<td>0.89</td>
<td>0.82</td>
<td>0.89</td>
<td>0.82</td>
<td>0.89</td>
<td>0.82</td>
<td>0.89</td>
<td>0.82</td>
</tr>
<tr>
<td>Mean</td>
<td>1.23</td>
<td>0.60</td>
<td>500.85</td>
<td>256.13</td>
<td>3.84E+16</td>
<td>2.08E+16</td>
<td>0.4</td>
<td>0.13</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.04</td>
<td>0.22</td>
<td>50.94</td>
<td>10.80</td>
<td>1.73E+15</td>
<td>1.82E+15</td>
<td>0.01</td>
<td>0.01</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wafer</th>
<th>14</th>
<th>14</th>
<th>14</th>
<th>14</th>
<th>14</th>
<th>14</th>
<th>14</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vt Dose</td>
<td>2.5E+12</td>
<td>2.5E+12</td>
<td>2.5E+12</td>
<td>2.5E+12</td>
<td>2.5E+12</td>
<td>2.5E+12</td>
<td>2.5E+12</td>
<td>2.5E+12</td>
</tr>
<tr>
<td>Parameter</td>
<td>VTO</td>
<td>VTO</td>
<td>UO</td>
<td>UO</td>
<td>NSUB</td>
<td>NSUB</td>
<td>THETA</td>
<td>THETA</td>
</tr>
<tr>
<td>Type</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>Count</td>
<td>38</td>
<td>32</td>
<td>38</td>
<td>32</td>
<td>38</td>
<td>32</td>
<td>38</td>
<td>32</td>
</tr>
<tr>
<td>Yield</td>
<td>0.52</td>
<td>0.44</td>
<td>0.52</td>
<td>0.44</td>
<td>0.52</td>
<td>0.44</td>
<td>0.52</td>
<td>0.44</td>
</tr>
<tr>
<td>Mean</td>
<td>1.41</td>
<td>-0.06</td>
<td>497.98</td>
<td>286.55</td>
<td>5.36E+16</td>
<td>2.57E+16</td>
<td>0.03</td>
<td>0.13</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.04</td>
<td>0.08</td>
<td>47.67</td>
<td>11.59</td>
<td>1.74E+15</td>
<td>1.56E+15</td>
<td>0.01</td>
<td>0.00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wafer</th>
<th>15</th>
<th>15</th>
<th>15</th>
<th>15</th>
<th>15</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vt Dose</td>
<td>3E+12</td>
<td>3E+12</td>
<td>3E+12</td>
<td>3E+12</td>
<td>3E+12</td>
<td>3E+12</td>
</tr>
<tr>
<td>Field Dose</td>
<td>4E+13</td>
<td>4E+13</td>
<td>4E+13</td>
<td>4E+13</td>
<td>4E+13</td>
<td>4E+13</td>
</tr>
<tr>
<td>Parameter</td>
<td>VTO</td>
<td>VTO</td>
<td>UO</td>
<td>UO</td>
<td>NSUB</td>
<td>NSUB</td>
</tr>
<tr>
<td>Type</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>Count</td>
<td>72</td>
<td>53</td>
<td>72</td>
<td>53</td>
<td>72</td>
<td>53</td>
</tr>
<tr>
<td>Yield</td>
<td>0.99</td>
<td>0.73</td>
<td>0.99</td>
<td>0.73</td>
<td>0.99</td>
<td>0.73</td>
</tr>
<tr>
<td>Mean</td>
<td>1.52</td>
<td>0.83</td>
<td>483.88</td>
<td>288.06</td>
<td>6.83E+16</td>
<td>3.62E+16</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.04</td>
<td>0.32</td>
<td>75.75</td>
<td>10.28</td>
<td>3.51E+15</td>
<td>2.05E+15</td>
</tr>
</tbody>
</table>

Table E.1: D13 - D15 SPICE Parameter Summary
Figure E.0: Gaussian VT0 Plots
<table>
<thead>
<tr>
<th></th>
<th>Measured Inv. P-Vt</th>
<th>Measured N-Vt</th>
<th>Difference</th>
<th>Simulated Inv. P-Vt</th>
<th>Simulated N-Vt</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8</td>
<td>2.09</td>
<td>-0.05</td>
<td>2.04</td>
<td>D8</td>
<td>1.63</td>
<td>0.037</td>
</tr>
<tr>
<td>D9</td>
<td>1.52</td>
<td>0.87</td>
<td>2.39</td>
<td>D9</td>
<td>0.83</td>
<td>0.846</td>
</tr>
<tr>
<td>D10</td>
<td>1.15</td>
<td>1.03</td>
<td>2.18</td>
<td>D10</td>
<td>0.35</td>
<td>1.14</td>
</tr>
<tr>
<td>D11</td>
<td>0.65</td>
<td>1.30</td>
<td>1.95</td>
<td>D11</td>
<td>-0.16</td>
<td>1.312</td>
</tr>
<tr>
<td>D13</td>
<td>0.60</td>
<td>1.23</td>
<td>1.83</td>
<td>D13</td>
<td>-0.16</td>
<td>1.312</td>
</tr>
<tr>
<td>D14</td>
<td>0.57</td>
<td>1.41</td>
<td>1.98</td>
<td>D14</td>
<td>-0.71</td>
<td>1.466</td>
</tr>
<tr>
<td>D15</td>
<td>-0.83</td>
<td>1.52</td>
<td>0.70</td>
<td>D15</td>
<td>-1.25</td>
<td>1.605</td>
</tr>
</tbody>
</table>

Measured N & Inverted P Threshold Voltages

Ideal Vt Adjustment Implant is where the two lines cross.
D10 is nearly ideal.

Simulated N & Inverted P Threshold Voltages

Ideal Vt Adjustment Implant is where the two lines cross.
D9 is nearly ideal.

Figure E.1: Ideal Vt Adjustment Implant Plots
### Wafer D8

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Mean</td>
<td>-0.0475</td>
<td>-2.0871</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.0194</td>
<td>0.2013</td>
</tr>
<tr>
<td>Simulated VT0</td>
<td>0.0370</td>
<td>-1.6300</td>
</tr>
<tr>
<td>T2</td>
<td>-16.2984</td>
<td>-17.1462</td>
</tr>
<tr>
<td>DF</td>
<td>13</td>
<td>56</td>
</tr>
<tr>
<td>Significance</td>
<td>0.05</td>
<td>0.05</td>
</tr>
<tr>
<td>T(.975 Quan)</td>
<td>2.1604</td>
<td>2.0032</td>
</tr>
<tr>
<td>Result</td>
<td>Means NOT Equal</td>
<td>Result Means NOT Equal</td>
</tr>
<tr>
<td>P-Value</td>
<td>4.94E-10</td>
<td>6.00E-24</td>
</tr>
</tbody>
</table>

### Wafer D9

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Mean</td>
<td>0.8689</td>
<td>-1.5243</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.0856</td>
<td>0.2828</td>
</tr>
<tr>
<td>Simulated VT0</td>
<td>0.8460</td>
<td>-0.8300</td>
</tr>
<tr>
<td>T2</td>
<td>0.8464</td>
<td>-18.5315</td>
</tr>
<tr>
<td>DF</td>
<td>9</td>
<td>56</td>
</tr>
<tr>
<td>Significance</td>
<td>0.05</td>
<td>0.05</td>
</tr>
<tr>
<td>T(.975 Quan)</td>
<td>2.2622</td>
<td>2.0032</td>
</tr>
<tr>
<td>Result</td>
<td>Means are Equal</td>
<td>Result Means NOT Equal</td>
</tr>
<tr>
<td>P-Value</td>
<td>4.19E-01</td>
<td>1.47E-25</td>
</tr>
</tbody>
</table>

### Wafer D10

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Mean</td>
<td>1.0271</td>
<td>-1.1541</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.0811</td>
<td>0.1973</td>
</tr>
<tr>
<td>Simulated VT0</td>
<td>1.1400</td>
<td>-0.3500</td>
</tr>
<tr>
<td>T2</td>
<td>-10.2248</td>
<td>-31.8222</td>
</tr>
<tr>
<td>DF</td>
<td>53</td>
<td>60</td>
</tr>
<tr>
<td>Significance</td>
<td>0.05</td>
<td>0.05</td>
</tr>
<tr>
<td>T(.975 Quan)</td>
<td>2.0057</td>
<td>2.0003</td>
</tr>
<tr>
<td>Result</td>
<td>Means NOT Equal</td>
<td>Result Means NOT Equal</td>
</tr>
<tr>
<td>P-Value</td>
<td>3.84E-14</td>
<td>2.84E-39</td>
</tr>
</tbody>
</table>

Table E.2: D8-D10 VT0 Analysis Data
<table>
<thead>
<tr>
<th>Wafers D11 &amp; D13</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>Sample Mean</td>
<td>1.2624</td>
<td>Sample Mean</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.0611</td>
<td>Sigma</td>
</tr>
<tr>
<td>Simulated VT0</td>
<td>1.3120</td>
<td>Simulated VT0</td>
</tr>
<tr>
<td>T2</td>
<td>-9.1777</td>
<td>T2</td>
</tr>
<tr>
<td>DF</td>
<td>127</td>
<td>DF</td>
</tr>
<tr>
<td>Significance</td>
<td>0.05</td>
<td>Significance</td>
</tr>
<tr>
<td>T(.975 Quan)</td>
<td>1.9788</td>
<td>T(.975 Quan)</td>
</tr>
<tr>
<td>Result</td>
<td>Means NOT Equal</td>
<td>Result</td>
</tr>
<tr>
<td>P-Value</td>
<td>1.03E-15</td>
<td>P-Value</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wafer D14</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>Sample Mean</td>
<td>1.4064</td>
<td>Sample Mean</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.0433</td>
<td>Sigma</td>
</tr>
<tr>
<td>Simulated VT0</td>
<td>1.4660</td>
<td>Simulated VT0</td>
</tr>
<tr>
<td>T2</td>
<td>-8.4982</td>
<td>T2</td>
</tr>
<tr>
<td>DF</td>
<td>37</td>
<td>DF</td>
</tr>
<tr>
<td>Significance</td>
<td>0.05</td>
<td>Significance</td>
</tr>
<tr>
<td>T(.975 Quan)</td>
<td>2.0262</td>
<td>T(.975 Quan)</td>
</tr>
<tr>
<td>Result</td>
<td>Means NOT Equal</td>
<td>Result</td>
</tr>
<tr>
<td>P-Value</td>
<td>3.18E-10</td>
<td>P-Value</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wafer D15</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>Sample Mean</td>
<td>1.5234</td>
<td>Sample Mean</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.0434</td>
<td>Sigma</td>
</tr>
<tr>
<td>Simulated VT0</td>
<td>1.6050</td>
<td>Simulated VT0</td>
</tr>
<tr>
<td>T2</td>
<td>-15.9518</td>
<td>T2</td>
</tr>
<tr>
<td>DF</td>
<td>71</td>
<td>DF</td>
</tr>
<tr>
<td>Significance</td>
<td>0.05</td>
<td>Significance</td>
</tr>
<tr>
<td>T(.975 Quan)</td>
<td>1.9939</td>
<td>T(.975 Quan)</td>
</tr>
<tr>
<td>Result</td>
<td>Means NOT Equal</td>
<td>Result</td>
</tr>
<tr>
<td>P-Value</td>
<td>3.57E-25</td>
<td>P-Value</td>
</tr>
</tbody>
</table>

Table E.3: D11-D15 VT0 Analysis Data
References

Statistical Modeling References


Statistics References


CMOS Devices and Design References


**Processing References**


Lattice Press, Sunset Beach, California, © 1990.