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A Precise analysis of a class e amplifier

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A Precise Analysis of a Class E Amplifier

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I would like to thank my mother for all of her unyielding support through all that I have endeavored. She has shown me through example in her own life that you can always make a better life for yourself if you aren't scared to take the unknown path. She has gone out of her way to provide me with the opportunities that otherwise may not have been there, and to do her part to ensure I reach the fullest potential that I dare dream.

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Chapter 1: Introduction

1.1- Importance of Class-E Amplifiers

The Class-E amplifier was first introduced by Sokal et al. [1] in 1972. The Class-E amplifier, as shown in Figure 1, was introduced as a narrow-band tuned RF amplifier with a similar topology to that of a standard low noise amplifier (LNA), but with the transistor acting as a switching element instead of as a voltage controlled current source device. Under ideal conditions (infinite loss-less inductors, transistor acts as an ideal switch, and zero fall time of the drain [or collector] current), the Class-E amplifier can be designed to have 100% efficiency [1], making it well suited for portable RF devices such as cell phones and wireless laptop Ethernet connections.

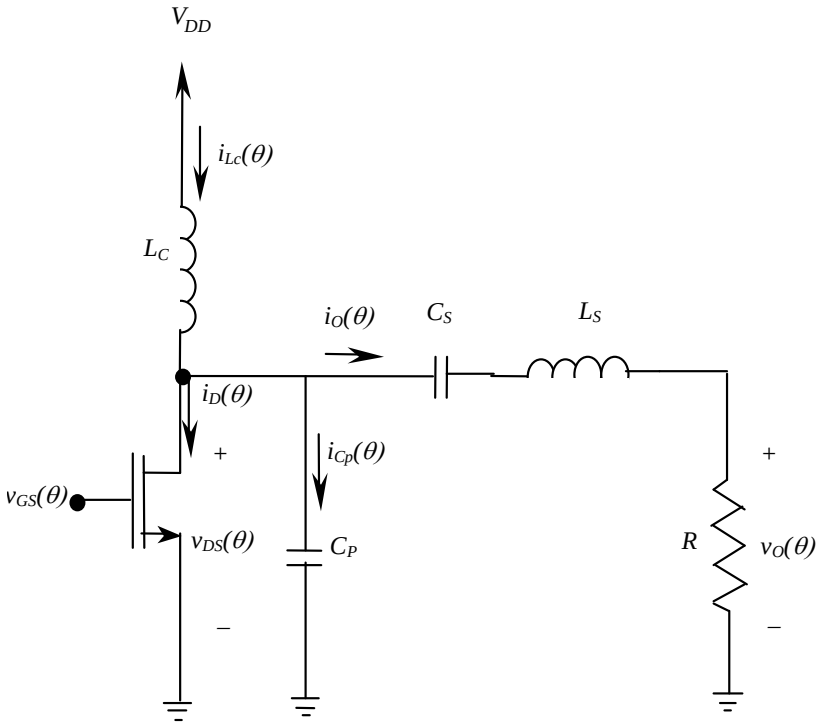


Figure 1.1: The complete schematic for the Class-E power amplifier.

A Class-E amplifier can not be used for wide band amplification, making it well suited for only a select group of applications requiring high frequency narrowband operation. Currently, the most common use of a narrowband high frequency amplifier is to amplify a high frequency carrier signal that is modulated within a narrowband around the carrier signal with a data signal. This type of signal is commonly found in IEEE wireless standards for data transmission such as 802.11N and WiMAX (802.16), and cellular broadcast. These applications, however, in recent years have had an exponentially growing commercial market with the wide adoption of cellular telephone communications and wireless networking. As portable applications continue to become more complex, battery size and lifetime have been a growing concern. For this reason, finding a highly efficient (amount of data throughput per unit of energy) output stage for the transmitter is becoming an increasingly important issue. Since the frequency of operation and data throughput are typically determined by the appliction, the power efficiency will be reported in table 1.1 as the efficiency metric for comparison.

Table 1.1: Comparison of different classes of power amplifiers with respect to RF integrated circuit performance.

Amplifier	Maximum Efficiency	Layout Area	Distortion
Class-A	50%	small	low
Class-B	78.50%	small	high
Class-AB	<78.5%	small	moderate
Class-C	Approaching 100%	moderate	moderate
Class-D	Not Suited for Narrowband RF		
Class-E	Approaching 100%	moderate	low
Class-F (2 Harmonics)	~70%	moderate	low
Class-F (∞ Harmonics)	Approaching 100%	infinite	low

It can be argued that the most important issues considered when deciding on an output stage would be obtainable efficiency, required layout area, and the amount of distortion that would be present at the output. Table 1.1 shows a comparison of the different classes of power amplifiers and their performances with regard to RF communications. As can be observed from Table 1.1, a Class-E amplifier is well suited for narrowband RF systems. It is important to note that the efficiencies presented above are only valid for ideal components under ideal conditions, and will vary greatly with design. Reported efficiencies at different frequencies for Class-E amplifiers are presented in Figure 1.2 as a reference. As can be seen from Figure 1.2, real amplifiers are operating far enough from 100 percent efficiency so as to require an optimized design process that accounts for non-ideal components and non-ideal conditions (such as imperfect gate driving voltage) needs to be implemented. Many of the non-idealities have been accounted for individually previously, but a complete analysis for a Class-E amplifier has not yet been presented, and will be the focus of this thesis.

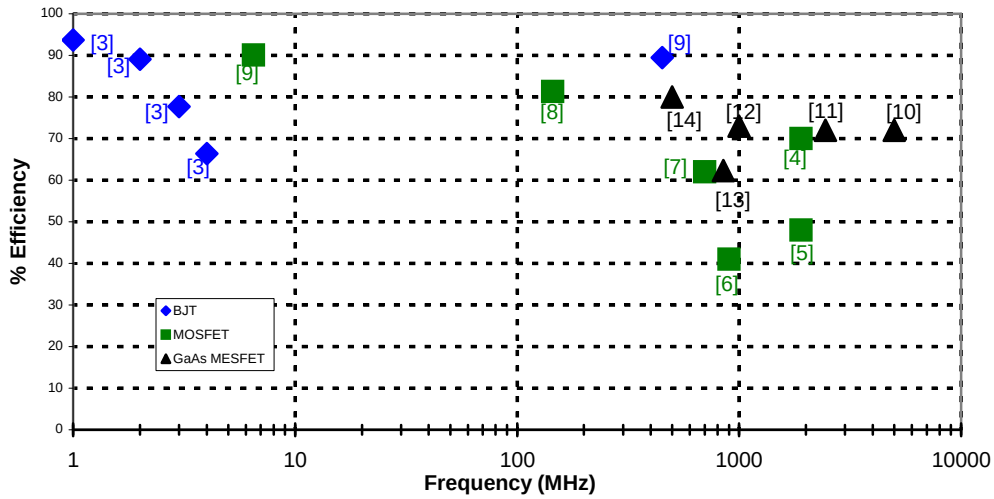


Figure 1.2: Literature reported efficiencies at different frequencies and transistor types for Class-E amplifiers.

1.2 – Original Design by Sokal

Sokal *et al.* [1] performed the original design of the Class-E amplifier assuming ideal passive components and an ideal switching transistor. These approximations lead to the following conditions in the amplifier:

1) Choke inductor current i_{Lc} will be a DC signal,
2) The output current i_O will be a perfect sinusoidal waveform, and
3) The transistor will turn instantly ON and OFF with zero ON resistance and infinite OFF resistance.

Under these conditions, if the drain voltage and the drain current are never both non-zero at the same time, then no power will be consumed by the transistor, and with ideal passives, the amplifier will operate at 100% efficiency. In order for this to occur, Sokal *et al.* stated that the drain voltage and its derivative (the parallel capacitor current i_{Cp} times a scalar as shown in equation 1.3) should both be zero at the instant that the transistor turns ON. The voltage must be zero at the time the transistor turns on to prevent power loss, and the derivative should be zero to allow for slight mistuning of the amplifier [1]. These two conditions have remained as the standard optimal switching conditions for analytical models being developed even today, and will be discussed in greater detail in Chapter 2. From the above assumptions, the choke current and the output current can be defined as

$$\begin{aligned} i_{Lc} &= I_{DC} \\ i_o &= \frac{a}{R}\sin(\omega t + \phi) \end{aligned} \quad , \qquad [1.1]$$

where a is the amplitude of the output voltage, R is the output load resistance and ϕ is the phase shift between the output voltage and the input signal at the transistor gate. Using KCL at the drain of the transistor yields the equation

$$i_{Lc} = i_{Cp} + i_D + i_o . \qquad [1.2]$$

Since the transistor and the parallel capacitor C_P are in parallel, when the transistor is ON, no current flows through C_p. However, when the transistor is OFF, zero can be substituted into eq. 1.2 for i_D with the results of eq. 1.1 yielding

$$\begin{aligned} i_{Cp} &= 0 && \text{[ON]} \\ i_{Cp} &= I_{DC} - \frac{a}{R}\sin(\omega t + \phi) && \text{[OFF]} \end{aligned} \quad . \qquad [1.3]$$

Substituting the results of eq. 1.1 into eq. 1.2 along with the result that $i_{Cp}=0$ in the ON state yields the drain equations of

$$\begin{aligned} i_D &= I_{DC} - \frac{a}{R}\sin(\omega t + \phi) && \text{[ON]} \\ i_D &= 0 && \text{[OFF]} \end{aligned} \quad . \qquad [1.4]$$

Knowing that a current flowing into a capacitor produces a voltage and knowing that the parallel capacitor voltage is the same as the drain voltage yields the following equation for the drain voltage v_{DS}

$$\begin{aligned} v_{DS} &= \frac{1}{Cp}\int_{t=0}^{t} i_{Cp}\,dt = \frac{1}{Cp}\int_{t=0}^{t}\left[I_{DC} - \frac{a}{R}\sin(\omega t + \phi)\right]dt \\ v_{DS} &= \frac{1}{Cp}\left[I_{DC}t + \frac{a}{\omega R}\cos(\omega t + \phi) - \frac{a}{\omega R}\cos(\phi)\right] \end{aligned} \quad . \qquad [1.5]$$

The waveforms for these equations can be seen in Figure 1.3. For Figure 1.3, it was assumed arbitrarily that the transistor is ON for $0 \le \omega t \le \pi$, and OFF for $\pi \le \omega t \le 2\pi$.

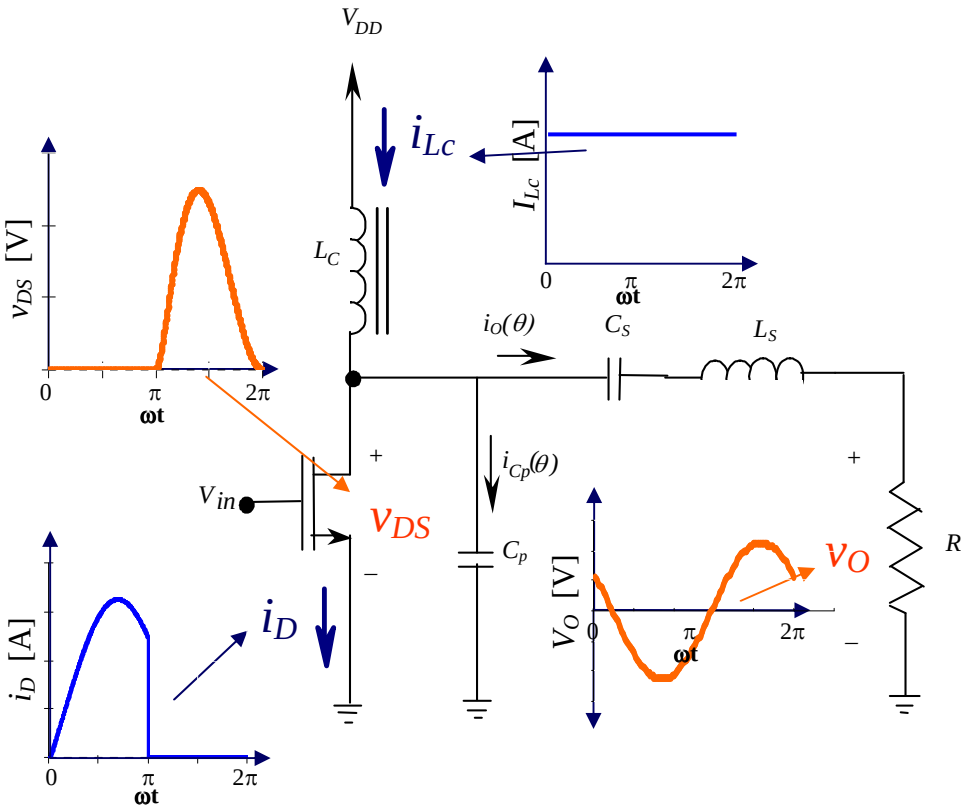


Figure 1.3: Class-E waveforms with ideal components and under optimal switching conditions as described by Sokal *et al.*

1.3 – Recent Advances in Class-E Design

The simplest modification to make to the ideal Class-E analysis is to account for the decay in the transistor at the transition from the ON state to the OFF state. As shown in Figure 1.3, ideally this transition is instantaneous, but in the non-ideal case there is a decay associated with this transition. Kazimierczuk [3] has modeled this as a linearly sloped decreasing line during the OFF state, while Tu *et al.* [15] have more accurately modeled it as an exponential decay in this region which is the approach that will be used

in chapter 3. Neither of these papers however completely account for a non-ideal transistor in the fact that they both assume zero ON resistance. The issue of the ON resistance has been addressed by Choi *et al.* [16], Wang *et al.* [17], Sekiya *et al.* [18], Kessler *et al.* [19], Reynaert *et al.* [20], and Alinikula *et al.* [21], although none of these authors have accounted for the transistor decay time. Kessler *et al.* [19], Alinikula *et al.* [21], and Reynaert *et al.* [20] however, have accounted for the parasitic resistances of the passive components, while Reynaert *et al.* [20] have also accounted for the finite Q of the output along with Tu *et al.* [15] and Sekiya *et al.* [18]. With finite output Q, the load network will not operate as an ideal filter, and additional harmonics besides the fundamental frequency will be present at the output as seen in Figure 1.4. Wang *et al.* [17], Sekiya *et al.* [18] and Reynaert et al. [20] have also accounted for the finite filtering value of the choke inductor L_C. This has the effect of allowing ripple to be introduced onto the i_{Lc} waveform as seen in Figure 1.4. A table summarizing the contributions of these authors is presented in Table 1.2.

Table 1.2: Summary of recent advances in the design and modeling of Class-E amplifiers.

Ref #	Author	Date	R-ON	Q Choke	Q Load	Decay	Inductor Resistance
[3]	Kazimierczuk et al.	1983				X	
[15]	Tu et al.	1999			X	X	
[16]	Choi et al.	1999	X				
[17]	Wang et al.	2002	X	X			
[18]	Sekiya et al.	2001	X	X	X		
[19]	Kessler et al.	2001	X				X
[20]	Reynaert et al.	2003	X	X	X		X
[21]	Alinikula et al.	2003	X				X
[22]	Klehn et al.	2004	X	X	X	X	X

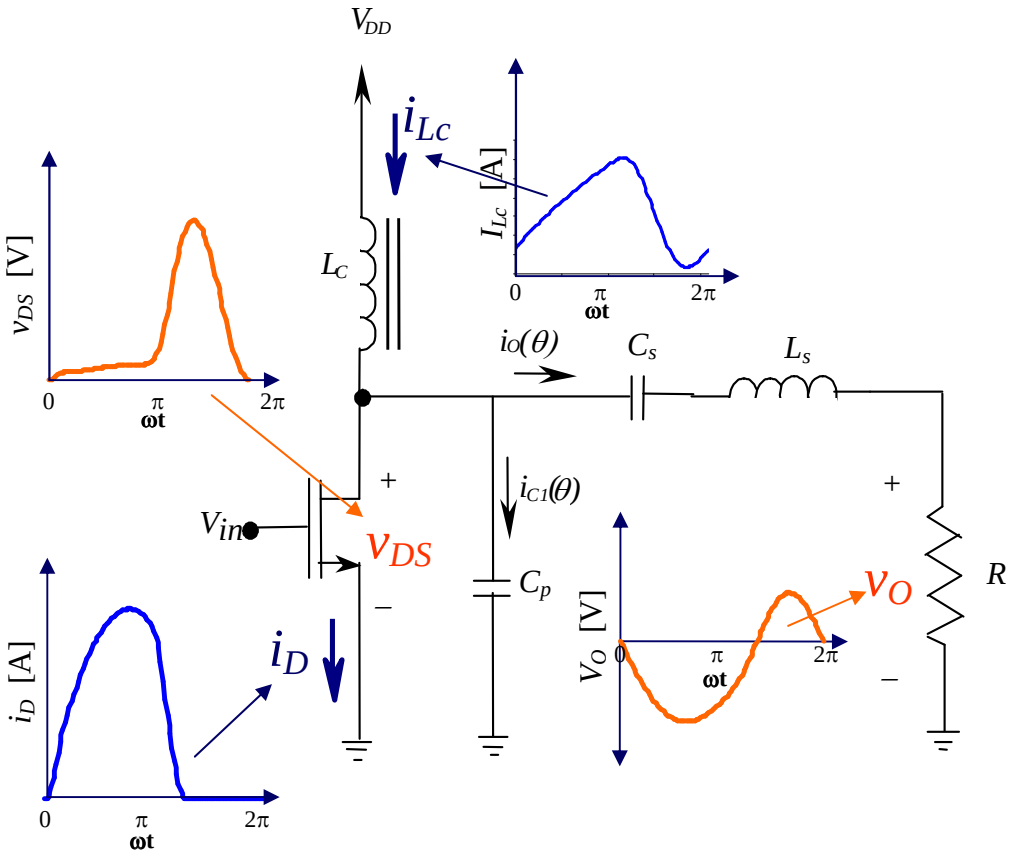


Figure 1.4: Class-E waveforms with non-ideal components and under optimal switching conditions as described by Sokal *et al.* [1].

1.4 – Motivation for this work

These authors have shown that each of these non-idealities has an effect on both the circuit performances such as efficiency and distortion, and the required circuit components needed to meet the optimized switching conditions as defined by Sokal *et al.* [1]. However, up till now, a concise analysis to account for all of these non-idealities at the same time has not been presented. The goal of this thesis is to present an analysis that while accounting for all these non-idealities, also plots the non-ideal waveforms, calculates the required passive components for optimized switching conditions, and

measures the circuit performances through the use of a MATLAB simulation. The analysis, presented in Chapter 2, will account for:

1) Exponential decay angle of the transistor OFF transition dependant on the gate input voltage.
2) A variable ON resistance of the transistor dependant on the instantaneous bias conditions of the transistor (gate and drain voltage).
3) Parasitic resistance of the two circuit inductors.
4) Finite loaded Q for the tuned output network resulting in harmonics being passed to the output waveform.
5) Finite value of the choke inductor L_C resulting in harmonics being present on the choke current i_{Lc}.

Results of varying important design parameters such as transistor aspect ratio and inductor sizes and the effects of such variations on circuit performances and optimized component values is presented in Chapter 3.

1.5 – Thesis Organization

The organization of this thesis will be as follows:

Chapter II will discuss two methods for calculating the circuit parameters and waveforms of the class E amplifier. The first method will be an integral method that will account for finite choke inductances, drain current fall time, and loaded quality factor of the output network inductance. The second method discussed will use a finite difference solution and account for the same non-idealities of the first method, as well as a finite ON

resistance of the switch, rise and fall time of the input signal, and parasitic resistances of both circuit inductors. Chapter III will discuss in greater detail the effects of the non-ideal components accounted for in chapter II as well as the circuit power supply voltage will have on desired circuit parameters such as efficiency, output power, and total harmonic distortion (THD). Chapter IV will demonstrate the accuracy of the equations presented in chapter II by comparing the results of those equations as calculated using MATLAB® vs a commercial circuit simulator (SPECTRE®). An actual class E amplifier is then constructed using discrete components and the output of this circuit is compared to the equations of chapter II as calculated using MATLAB®. Chapter V has conclusions from the presented work as well as discussion on possible future research based on this thesis.

Chapter 2: Analysis

Two methods have been successfully implemented to simulate the class-E amplifier waveforms, optimize the required circuit components, and calculate amplifier performances such as efficiency and total harmonic distortion (THD). The first optimizes the circuit parameters while considering finite choke inductances, drain current fall time, and loaded quality factor of the output network inductance. The second accounts for all these in addition to a finite ON resistance of the switch, rise and fall time of the input signal, and parasitic resistances of both circuit inductors. The first method has been published in the International Symposium on Circuits and Systems (ISCAS) 2004 conference [22], while the second method is more accurate and accounts for more non-idealities presenting a more general solution.

The first method (integral method) utilizes an iterative technique where each waveform is defined symbolically and solved using the integral function in MATLAB. The output current i_O and the choke current i_{Lc} are initially assumed, as well as the size of the two inductors, and the capacitor current i_C and the drain voltage v_{DS} are calculated. From these waveforms, a new output current and choke current are obtained which are considered as inputs to next iteration. During each iteration, the two capacitors C_P and C_S are calculated so that the switching conditions as described by Sokal *et al.* [1] are met. These conditions include the drain voltage and the capacitor current both are zero at the time when the transistor first turns on. This method assumes a constant ON resistance for the switching transistor and an exponential decay on the drain current when the transistor

turns off (the ideal case assumes an infinitely sloped instantaneous turn off [see Figure 1.3]). This methodology also accounts for the effects of the finite choke inductance and its effect on the amount of ripple on the "DC" supply current, and also accounts for the finite *Q* of the load network (See Figure 1.4 to observe the effects of these non-idealities). The load network acts as both a phase shifting element by tuning it slightly below the operating frequency so it appears slightly inductive, and also as a band-pass filter passing the first harmonic, but blocking all others in the ideal case. By taking this as a non-infinite inductor, additional harmonics at the output are accounted for and THD can be accurately calculated.

The second method (finite difference method) expresses the circuit equations using differential equations and solves them simultaneously using finite difference technique. If the waveform starts at the point where the transistor turns ON, then the initial points on the waveforms are known from the aforementioned optimal switching conditions described by Sokal *et al.* [1] as seen in Figure 2.1. From the initial points, the subsequent points can be calculated. This method converges much faster than the integral method while accounting for more non-idealities. The transistor is now modeled more accurately by first defining the gate voltage similar to that of a typical Class-F driving stage (most generic waveforms will also be accepted by the program), and then calculating the region of operation and drain current of the transistor at each time step based on the gate voltage at that time. In this way, the decay of the drain current at the instant when the transistor turns OFF is modeled based on the input signal and the transistor parameters given as

inputs to the program including channel carrier mobility (μ_{eff}), oxide capacitance per unit area (C_{ox}), and threshold voltage (V_T). This enables the program to accurately account for the non-zero ON resistance of the transistor at all time steps based on the bias conditions. The finite inductances are still accounted for, with the addition of a resistance term added in series with the inductors to model low Q conditions similar to those found through the use of silicon fabrication [20].

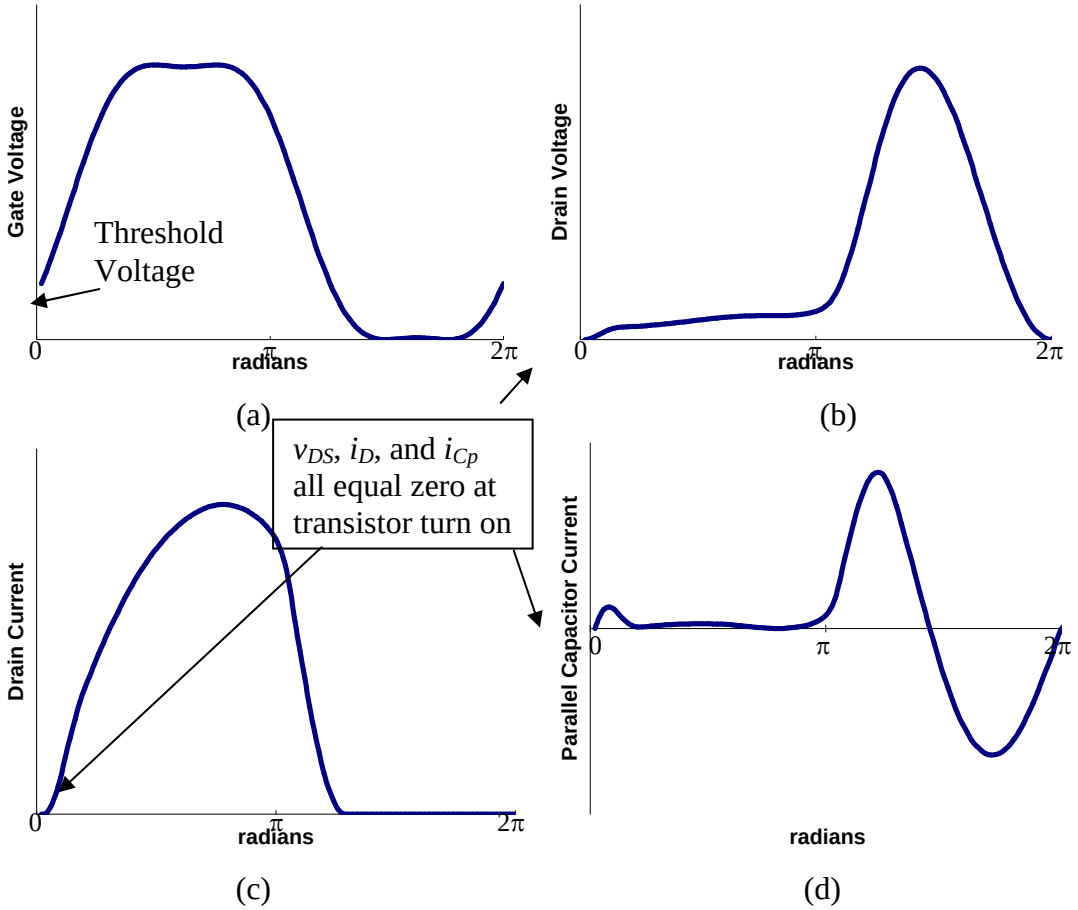


Figure 2.1 – a) Gate voltage, b) drain voltage, c) drain current, and d) parallel capacitor current. Setting t=0 at transistor turn on gives knowledge of initial conditions for these waveforms based on design for optimal switching conditions.

2.1 – Method 1: Integration Method

As mentioned previously, the first iteration of the integration method starts by assuming a symbolic waveform for the output current (i_O) and the choke current (i_{Lc}) from which the drain voltage (v_{DS}), parallel capacitor current (i_{Cp}), drain current (i_D), and new solutions for i_O and i_{Lc} are calculated. The initial waveform for the output current will be assumed to be

$$i_O = \frac{a}{R}\sin(\omega t + \phi) \tag{2.1}$$

where a is the amplitude of the output voltage, R is the output resistance, and ϕ is the initial phase shift of the fundamental frequency at the output. The choke inductor current (i_{Lc}) will be assumed to have no harmonics for the first iteration and will be defined simply as I_{DC1} to represent the DC level of the first iteration.

Using KCL at the drain node of the transistor, we find that

$$i_{Lc} = i_D + i_{Cp} + i_o . \tag{2.2}$$

When the transistor is OFF ($0 \le \omega t \le \pi$), it is assumed that no current is passing through it, therefore, solving for i_{Cp} yields,

$$i_{Cp} = i_{Lc} - i_o \qquad 0 \le \omega t \le \pi . \tag{2.3}$$

When the transistor is ON ($\pi \le \omega t \le 2\pi$), assuming the ON resistance on the transistor is small in comparison to the impedance of the capacitor, the capacitor is essentially shorted out, leaving no current through it allowing the drain current to be defined in this region as

$$i_D = i_{Lc} - i_o \qquad \pi \le \omega t \le 2\pi . \tag{2.4}$$

2.1.1 – Accounting for OFF Transition Drain Current Decay

In order to account for the exponential decay in the drain current when the transistor turns OFF, an additional term must be added to the drain current, and since i_D and i_{Cp} must still add up to i_{Lc}-i_O which are already defined, i_{Cp} must also be modified accordingly giving the final equations

$$\begin{array}{lll} i_D = I_{C0} \cdot e^{-\omega t \cdot \tau} & 0 \le \omega t \le \pi & \text{[OFF]} \\ i_D = i_{Lc} - i_o & \pi \le \omega t \le 2\pi & \text{[ON]} \end{array} \quad \text{and,} \tag{2.5}$$

$$\begin{array}{lll} i_{Cp} = i_{Lc} - i_O - I_{C0} \cdot e^{-\omega t \cdot \tau} & 0 \le \omega t \le \pi & \text{[OFF]} \\ i_{Cp} = 0 & \pi \le \omega t \le 2\pi & \text{[ON]} \end{array} \quad \text{and,} \tag{2.6}$$

where I_{C0} is the magnitude of i_{Cp} at $\omega t = 0$, (also the value of i_D at $\omega t = 2\pi$) in the absence of an exponential. If the transistor were a perfect switch, the drain current would instantaneously go from I_{C0} to 0 at the time that the transistor transitions from the ON state to the OFF state. In addition, the parallel capacitor current would instantaneously go from 0 to I_{C0} as the capacitor becomes the new path for the current. In the presence of a non-ideal switch, the exponential decay of the transistor channel current makes the ON to OFF state transition of both terms more gradual. The magnitude of the exponential is then defined as

$$I_{C0} = i_{Lc} - \frac{a}{R}\sin(\varphi) . \tag{2.7}$$

It is important also to note that τ is a variable used to adjust the angle of the decay of the exponential. The decay angle is defined as the phase when the exponential decays three time constants from its original value. Knowing the decay angle of the transistor will allow an easy calculation of τ for implementation in the model by using

$$\tau = \frac{3}{\psi} \tag{2.8}$$

where ψ is the decay angle of the transistor. For reference, a 30 degree decay angle is represented when τ is set to 5.9 and a 60 degree decay angle is represented with τ set to 2.95.

2.1.2 – Drain Voltage Accounting for Decay and ON Resistance

Knowing the current through the capacitor as a function of time allows for calculation of the voltage introduced across it during the period that the transistor is OFF ($0 \le \omega t \le \pi$), which is also the voltage across the drain of the transistor. When the transistor is ON ($\pi \le \omega t \le 2\pi$), it is assumed that the capacitor current is zero, so the only voltage at the drain will be produced by the current i_D through the ON resistance of the transistor. These waveforms are represented for the period defined as $0 \le \omega t \le \pi$ in the equations

$$\begin{aligned} v_{DS} &= \frac{1}{Cp}\int_0^t i_{Cp} \cdot dt \\ v_{DS} &= \frac{1}{Cp}\left[I_{DC1} \cdot t - \frac{a}{R\omega}\cos(\omega t + \phi) - \frac{1}{\tau} \cdot I_{C0} \cdot e^{-\omega t \cdot \tau} + \frac{a}{R\omega}\cos(\phi) + \frac{I_{C0}}{\tau} \right] \end{aligned} \tag{2.9}$$

and are represented for the period defined as $\pi \le \omega t \le 2\pi$ as

$$\begin{aligned} v_{DS} &= i_D \cdot R_{ON} \\ v_{DS} &= \left[I_{DC1} - \frac{a}{R}\sin(\omega t + \phi) \right] \cdot R_{ON} \end{aligned} \tag{2.10}$$

Note that the equation 2.9 has additional terms when compared to equation 1.5 after accounting for non-ideal components. It is also important to note that the assumption of negligible capacitor current i_{Cp} is only valid for small values of ON resistance R_{ON}. This

is a limitation of the integral method, and will be properly accounted for in the finite difference methodology.

2.1.3 – Applying Optimal Switching Conditions

The unknowns at this point in the analysis are C_p, a, ϕ, and I_{DC1}. Initial values were assigned in the program for each of these parameters. Using these initial values and the equations previously defined, accurate calculation of C_p, a, and ϕ can be performed. It is known through the optimal switching conditions that v_{DS} and i_{Cp} should both be zero at $\omega t=\pi$. The value of ϕ will be set to make v_{DS} equal to zero using the approximate initial values for the other parameters. From equation (2.2), and knowing that i_{Cp} and i_D are both zero at $\omega t=\pi$, we can now say that $i_{Lc}=i_O$, and with ϕ known, a is the only unknown in that equation. It is also known that with no power consumed in the inductor, the average voltage at v_{DS} should be the same as the power supply voltage V_{DD}. The value of C_p will affect the scaling of v_{DS} and can thus be used to make this final condition valid. Note that these values are based on the initial value of I_{DC1}, and will need to be recalculated when a new value of I_{DC1} is determined later on.

2.1.4 – Accounting for Finite *Q* of the Tuned Load Network

Using v_{DS} from above, we can now calculate the new output with harmonics. This is done by tuning the output network just below the operating frequency to accomplish two goals, the first of which is to filter all but the fundamental frequency from the v_{DS} waveform, and the second is to cause a phase shift by tuning the output network slightly

below the operating frequency (setting it slightly inductive at the operating frequency) so that the output has a phase of ϕ. For the analysis, the series network inductor L_S is fixed by the designer. This is because the filtering ability of the network will be improved by larger inductors (see section 3.3), but larger inductors take up much more area on a silicon process. This way, the designer can determine the maximum size inductor allowable within the design constraints. The value of the series output capacitor C_S can than be set to achieve the appropriate phase shift from the equation

$$\angle v_{DS} + \tan^{-1}\left(\frac{\omega L_S - (\omega C_S)^{-1}}{R}\right) = \phi \tag{2.11}$$

where $\angle v_{DS}$ is the angle of the fundamental frequency determined by a Fast Fourier Transform (FFT) of v_{DS}. The nth harmonic of the output can then be calculated using the values obtained for L_S and C_S by

$$i_O = \sum_{n=1}^{\infty} b_n \cdot \sin\left(n\omega t + \angle v_{DSn} + \tan^{-1}\left(\frac{n\omega L_S - (n\omega C_S)^{-1}}{R}\right)\right), \tag{2.12}$$

where $b_n = |FFT_n(v_{DS})| \cdot \left[\sqrt{R^2 + \left(n\omega L_S - (n\omega C_S)^{-1}\right)^2}\right]^{-1}$,

and $|FFT_n(v_{DS})|$ denotes the magnitude of the nth point in the FFT of v_{DS}. This calculation of i_O can be used to obtain the correct value of the *DC* level of i_{Lc}. Since a was already established previously, the magnitude of the first harmonic in this end result (b_1) should equal the magnitude of $\frac{a}{R}$. If it is not, then I_{DC1} will be adjusted accordingly, and the

values of C_p, a, and ϕ will be recalculated, along with a recalculation of i_O, until this condition is satisfied.

2.1.5 – Accounting for Finite *Q* of Choke Inductor L_C

The last calculation left in the first iteration is to account for the ripple introduced by the finite choke inductor L_C. By knowing that the inductor is connected to V_{DD} on one side and v_{DS} on the other, the current through it can be defined as

$$i_{Lc} = \frac{1}{L_C} \int_{t=0}^{t} (V_{DD} - v_{DS}) \cdot dt + I_{DC2} \tag{2.13}$$

where I_{DC2} is the DC level for the second iteration.

2.1.6 – Applying Results of First Iteration to the Second

The first iteration began with an assumption for the output current i_O and the choke current i_{Lc} and ends with a new definition of these two waveforms based on the optimized switching conditions and the given circuit parameters (τ, L_C, L_S, ω, R_{ON}, and R). These two waveforms will be passed as the initial conditions to the next iteration, which will proceed similar to the first with a few modifications. The waveform for i_{Lc} will be held steady except for the I_{DC2} term (i.e., changes in ϕ or a in the second iteration will not affect the first term of eq. 2.13). Secondly, adjustments to the magnitude of the output current $\frac{a}{R}$ in the second iteration will also scale to the harmonics since i_O is now defined as a summation of harmonics instead of a perfect sinusoid. The output phase ϕ however,

will only affect the fundamental frequency. This can be justified since the phase shift at the output is controlled by the excess inductance seen at the nth harmonic frequency and is defined by

$$n\omega L_S - \left(\frac{1}{n\omega C_S}\right). \tag{2.14}$$

When n is equal to one, the magnitudes of $n\omega L_S$ and the inverse of $n\omega C_S$ are roughly similar (the inductive portion is slightly greater), but when n is greater than 1, the inductive portion becomes quite large while the capacitive portion becomes significantly less. This way, a small change in the calculated angle ϕ will result in a small modification of the calculated value of C_S, which will affect the first harmonic, but have little impact on the subsequent harmonics since at higher frequencies the inductive term dominates the reactance of the load network. Figure 2.2 represents the phase shift for different harmonics associated with typical tuned output parameters and the effects of varying the output capacitor by +/- 10%, as would happen in the second and subsequent iterations. It is shown that the fundamental frequency is shifted as desired, and the remainder of the harmonics are virtually unaffected by this variation in capacitance. For this reason, the i_O calculated in the first harmonic will have a and ϕ remain as variables for the first harmonic, the magnitude of the additional harmonics will scale linearly with changes in a, but the phase of the additional harmonics will not be changed by a change in ϕ in the next iteration. This way, the second (and subsequent) iterations still have C_p, a, ϕ, and I_{DCn} as variables, but variations in these variables to meet the optimal switching

conditions and establish convergence on the magnitude of the output current will not adversely alter the two waveforms that are given as the input conditions to each iteration.

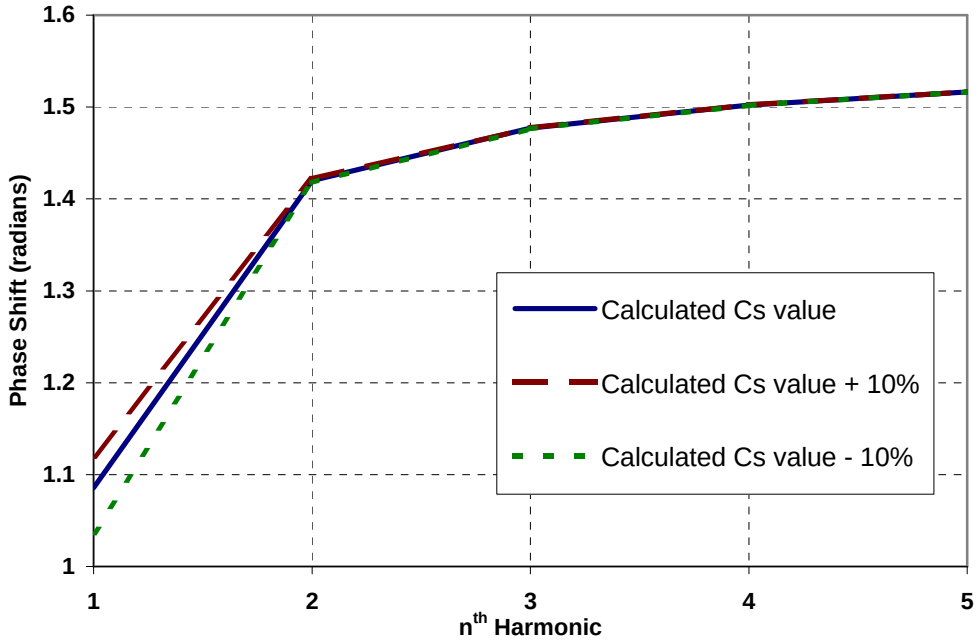


Figure 2.2 - Phase shift associated with the tuned network and load resistor at the first 5 harmonics. Here, L_S = 30nH and C_S = 17.8pF for an output phase ϕ of –0.44 radians at a frequency of 240MHz.

Following this format, the code was written to run for three iterations. It was observed that the waveforms after the third iteration were nearly identical to those of the second, and the calculated parameters also had little variation making three iterations adequate for most situations. In addition to this, the size of the equations grew exponentially as the iterations progressed due to the symbolic completion of two integrals per iteration causing an exponential increase in the amount of time needed to complete each iteration. For this reason, a fourth iteration would not have been practical to implement, causing a

slight error in the accuracy of the program. This error was negligible except when very small inductors were given as inputs to the program. This is not an issue using the finite difference method.

Other limitations of the integral method should also be noted. The transistor is assumed to turn immediately ON and immediately OFF, with the exception of the exponential decay in the current when turning OFF. The resistance of the transistor for the v_{DS} calculation is assumed to go immediately from a constant R_{ON} value to an immediate OFF state without any transition time between the two states. In addition, the resistance of the inductors due to the low quality factor (Q) on silicon processes has not been accounted for. Despite these shortcomings, the integral method when published represented the most concise calculation that the authors had found to date for a Class-E amplifier.

2.2 - Method 2: Finite Difference Method

The finite difference method has many variations and improvements over the integral method. The most important being that the methodology accepts any gate voltage waveform as an input to the program (again MATLAB was used), and using this along with the drain voltage, calculates the resistance of the transistor based on the bias conditions. The drain current is also defined based on the bias conditions, so the exponential decay is no longer added as a mathematical term, but is dependant on transistor parameters given as inputs to the program. The program also accounts for the intrinsic parasitic resistance of the inductors, thus allowing not only improved accuracy, but also presenting a trade off to the designer if a constant Q is assumed for a process

technology. Larger inductors using the integral method always provided better results, but with the finite difference method accounting for the resistance, larger inductors also mean more loss in the system.

2.2.1 – Defining a Gate Voltage

The finite difference methodology begins with a definition of the gate voltage. The only stipulations on this are that the waveform must be a function of time (time defined from zero till the end of one period) and the waveform must be periodic. It is assumed for most of the simulations that the Class-E amplifier would be driven by a Class-F stage prior to it. Typically, the output of a Class-F stage consists of two harmonics (first and third). Although more elaborate tuning networks can be designed, they typically are not used due to the increased complexity and area with very little increase in performance [2]. The equations representing a typical Class-F waveform with flattening [2] is

$$v_{GS} = k_1\left[\sin(\omega t+\theta)+\tfrac{1}{7}\sin\left(3\cdot(\omega t+\theta)\right)\right]+k_2 \tag{2.15}$$

where k_1 is the amplitude of the wave and k_2 is the DC offset. These values are typically set so that the waveform reaches zero volts at its lowest point, and is just under V_{DD} at its highest. The value of θ will be set by the program to start the waveform at the appropriate position of the waveform. Since the finite difference method requires initial conditions, θ will be set so that the waveform begins at a point where conditions of other waveforms in the circuit are known as seen in Figure 2.1.

As mentioned previously, optimal switching is defined by the condition that the drain voltage v_{DS} and the parallel capacitor current i_{Cp} are both zero when the transistor is just turning ON. In order to use both $v_{DS} = 0$ and $i_{Cp} = 0$ as the initial conditions, the v_{GS}

waveform must be set so that it begins increasing from the threshold voltage of the transistor (the point where current just starts to flow) at $t = 0$ as seen in Figure 2.1.

2.2.2 Defining Current Equations from KVL Loop

This technique will still employ an iterative solution to converge on the appropriate values. Again, the initial assumption of the output current will be defined as

$$i_O = \frac{a}{R}\sin(\omega t + \phi) \tag{2.16}$$

where all variables are defined the same as they were in the integral method. As before, a and ϕ are both variables and will be determined by the program, while the load resistance R, and radian frequency ω are user defined. Initial guesses are given for a and ϕ in the beginning of the program, and the first point in the i_{Lc} curve is set equal to the first point in the i_O curve since i_{Cp} and i_D are both zero at this time as described in the integral method. The second point in the choke current i_{Lc} can then be found using mesh analysis around the loop shown in Figure 2.3.

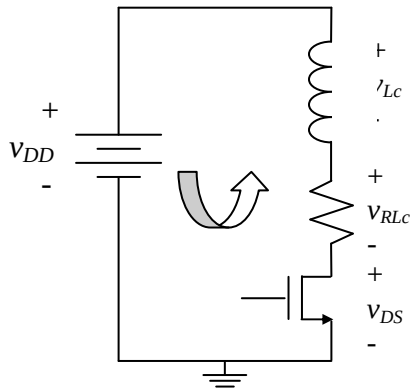


Figure 2.3 - Loop used with kirchoff's voltage law in equations 2.17a-e.

$$v_{DS} + v_{RLc} + v_{Lc} = V_{DD} \tag{2.17a}$$

Substituting current expressions into equation 2.16a yields

$$v_{DS} + i_{Lc} \cdot R_{Lc} + L_C \cdot \frac{di_{Lc}}{dt} = V_{DD}. \tag{2.17b}$$

Applying finite difference to the derivative term and quantising the waveforms gives

$$v_{DS}(n-1) + i_{Lc}(n-1) \cdot R_{Lc} + L_C \cdot \frac{i_{Lc}(n) - i_{Lc}(n-1)}{\Delta t} = V_{DD}. \tag{2.17c}$$

Separating the difference term and rearranging the equation results in

$$L_C \cdot \frac{i_{Lc}(n)}{\Delta t} - L_C \cdot \frac{i_{Lc}(n-1)}{\Delta t} = V_{DD} - v_{DS}(n-1) - i_{Lc}(n-1) \cdot R_{Lc}. \tag{2.17d}$$

And finally, solving for the nth time step from the previous time step yields

$$i_{Lc}(n) = i_{Lc}(n-1) + \frac{\Delta t}{L_C}\left[V_{DD} - v_{DS}(n-1) - i_{Lc}(n-1) \cdot R_{Lc}\right], \tag{2.17e}$$

where Δt is the time step between points and R_{Lc} is the resistance associated with the choke inductor L_C. To obtain the value of i_{Lc} at the second time step of this equation, we need to know the first point in v_{DS} and i_{Lc}. Due to the waveform starting with the transistor just turning on at $t = 0$, it is known that $v_{DS}(1) = 0$ and $i_{Lc}(1)$ is equal to $i_O(1)$.

2.2.3 Defining Remaining Waveforms from KCL

A similar calculation can be performed to find the drain voltage v_{DS}, except instead of using Kirchoff's voltage law to perform mesh analysis, Kirchoff's current law will be used to perform nodal analysis around node "*a*" as seen in Figure 2.4.

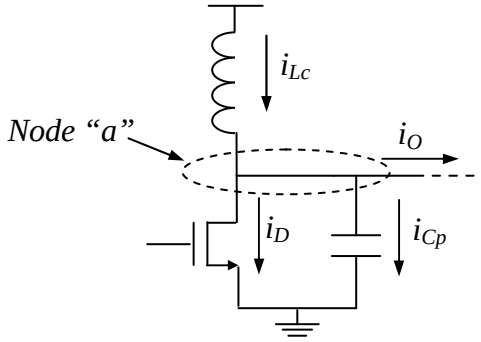


Figure 2.4 - Representation of all currents entering and leaving node "*a*" in the circuit. Equating the arriving currents to the departing currents will be used in equations 2.18a-e to determine the drain voltage v_{DS}.

Equating the currents entering node "*a*" and those leaving yields

$$i_{Lc} = i_{Cp} + i_D + i_O . \tag{2.18a}$$

Substituting a voltage expression for i_{Cp} gives the equation

$$i_{Lc} = C_p \cdot \frac{dv_{DS}}{dt} + i_D + i_O . \tag{2.18b}$$

Applying finite difference to the derivative term and quantising the waveforms gives

$$i_{Lc}(n-1) = C_p \cdot \frac{v_{DS}(n) - v_{DS}(n-1)}{\Delta t} + i_D(n-1) + i_O(n-1). \tag{2.18c}$$

Separating the difference term and rearranging the equation results in

$$C_p \cdot \frac{v_{DS}(n)}{\Delta t} - C_p \cdot \frac{v_{DS}(n-1)}{\Delta t} = i_D(n-1) + i_O(n-1) - i_{Lc}(n-1). \tag{2.18d}$$

And finally, solving for the nth time step from the previous time step yields

$$v_{DS}(n) = v_{DS}(n-1) + \frac{\Delta t}{C_p} \cdot \left[i_D(n-1) + i_O(n-1) - i_{Lc}(n-1) \right], \tag{2.18e}$$

where Δt is defined as the same time step as in 2.17. It is important to note that an exact equation for 2.17 and 2.18 would have taken the n^{th} term of each waveform except for the differential term, which should be split as (n+1/2) and (n-1/2). For ease of calculation, and since only discrete time steps are taken, the above analysis was used and is valid as long as a large number of points are used. If the above equations are solved in the above order, then all required points are available for all time steps except for the drain current i_D, where only the initial condition is know. This waveform must now be defined at each time step using data already calculated.

2.2.4 – Defining ON Current from Transistor Biasing

Knowing the drain to source voltage v_{DS} and the gate to source voltage v_{GS}, along with the transistor parameters given as inputs to the program, the bias conditions for the transistor are known and the current can be calculated. When v_{GS} falls below the threshold voltage of the transistor V_T, the transistor is assumed to be operating in the cut-off region and no current is assumed. When v_{GS} surpasses V_T and v_{DS} is "small" (defined later), the transistor is assumed to be operating in the linear region, with the current defined as

$$i_D(n) = \frac{\frac{1}{2}\cdot \mu_{eff} \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[2 \cdot \left(v_{GS}(n) - \hat{V}_t \right) \cdot v_{DS}(n) - {v_{DS}}^2(n) \right]}{1 + \frac{v_{DS}(n)}{(L \cdot E_c)}}, \qquad (2.19)$$

where μ_{eff} is the electron mobility in the channel, and is given by

$$\mu_{eff} = \frac{\mu_0}{1+\theta\cdot\left(v_{GS}(n)-\hat{V}_t\right)}, \tag{2.20}$$

where θ is defined as β_θ / t_{ox} [23]. Here, t_{ox} is the oxide thickness of the transistor and β_θ is given as a typical range of values, and is empirically derived to match the Cadence I-V curves. C_{ox} in equation 2.18 is the oxide capacitance per unit area, W is the gate width and L is the gate length of the transistor, and E_c is the critical electric field used to account for short channel effects present in small gate length transistors [23]. The critical electric field is approximated as

$$E_c = 1.7\times10^4\left(V/cm\right) \tag{2.21}$$

for Si devices [24]. Tsividis however, points out that this parameter is not very easily modeled, and typically requires fitting from experimental data (Tsividis does not even present an equation, simply a range of values that should be reasonable) [pp 280-282]. $\hat{V}_t$ is used in equation 2.18 as a modification to the standard threshold voltage. It is known that through Drain Induced Barrier Lowering (DIBL), that the threshold voltage starts falling below its zero body effect threshold voltage V_{T0} value in short channel devices and decreases linearly with v_{DS} [23]. For this case, $\hat{V}_t$ will be modeled as

$$\hat{V}_t = V_t - \alpha\cdot v_{DS}(n) \tag{2.22}$$

with α and V_t determined empirically from extracted IV curves.

The transistor is assumed to remain in the linear region until v_{DS} surpasses the saturation drain to source voltage V_{DS}', with V_{DS}' defined as

$$V_{DS}' = \frac{2 \cdot \left(v_{GS}(n) - \hat{V}_t \right)}{1 + \sqrt{1 + \left(v_{GS}(n) - \hat{V}_t \right) \cdot \frac{2}{L \cdot E_c}}}. \tag{2.23}$$

When v_{DS} is greater than V_{DS}', the transistor is assumed to be in the saturation region, where the current is assumed to be

$$i_D(n) = \frac{\mu_{eff} \cdot C_{ox} \cdot \frac{W}{L} \left[\left(v_{GS}(n) - \hat{V}_t \right) \cdot V_{DS}' - 0.5 \cdot V_{DS}'^2 \right]}{1 + \frac{V_{DS}'}{L \cdot E_c}} \times \left[1 + \frac{v_{DS}(n) - V_{DS}'}{V_A + V_{DS}'} \right], \tag{2.24}$$

where V_A is the Early voltage of the transistor. The first part of equation 2.24 accounts for the critical electric field and velocity saturation in short channel MOSFETs while the second part of the equation is used to account for channel length modulation effects [23]. As seen in Figure 2.5, the transistor characteristics much more closely matched the Cadence simulation when short channel effects were accounted for.

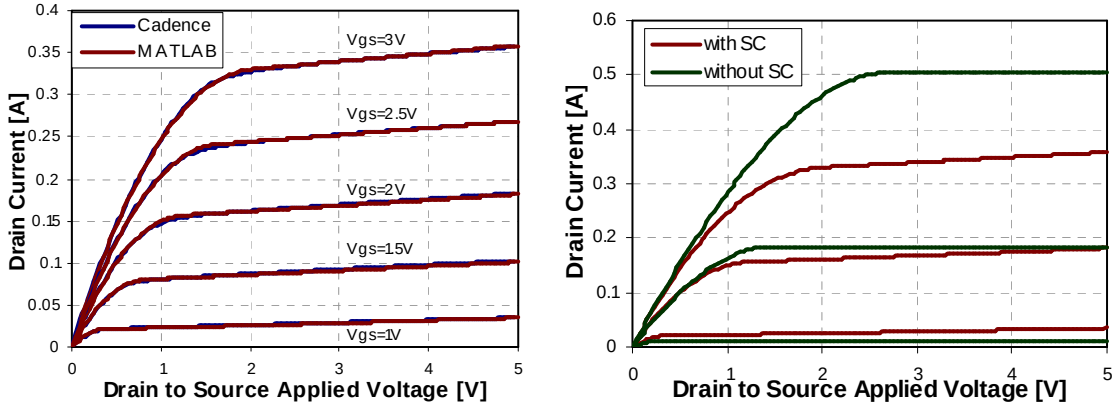


Figure 2.5 – a) Comparison of MATLAB and Cadence I-V curves for a device with a W/L ratio of 1500/0.6 μm. b) Comparison of I-V curves with and without accounting for short channel effects for the same 1500/0.6 μm transistor. Contact resistance was accounted for in the long channel case.

2.2.5 – Applying Optimal Switching Conditions

At this point in the calculation, all of the waveforms are defined, but the variables C_p, ϕ, and a are still unknown. For this methodology, C_p and ϕ will be adjusted to set v_{DS} and i_{Cp} equal to zero at transistor turn ON, and a will be readjusted based on a comparison of its assumed value and its calculated value from the Fast Fourier Transform (FFT) of v_{DS}. The calculation for i_O will be the same as it was in the integral method shown in equation 2.12. One modification was made to the i_O calculation from the integral method in order to account for the resistance (R_{Ls}) of inductor L_S. The new equation accounting for this is

$$i_O = \sum_{n=1}^{\infty} b_n \cdot \sin\left(n\omega t + \angle v_{DS} + \tan^{-1}\left(\frac{n\omega L_S - \left(n\omega C_S\right)^{-1}}{R + R_{Ls}} \right) \right), \qquad (2.25)$$

where $b_n = \left| FFT_n\left(v_{DS}\right) \right| \cdot \left[\sqrt{\left(R + R_{Ls}\right)^2 + \left(n\omega L_S - \left(n\omega C_S\right)^{-1}\right)^2} \right]^{-1}$.

It was observed that an increase in *Cp* had the effect of increasing the value of the final point in the v_{DS} curve while decreasing the value of the final point in i_{Cp}. An increase in the value of ϕ had the effect of decreasing the end point of both curves. A loop was established so that the waveforms would be calculated with the initial guesses, the variables would be adjusted, and the waveforms recalculated. This will continue until the last point of v_{DS} has a magnitude less than 0.001, i_{Cp} is less than 0.0002, and the difference between *a* going into the loop and *a* coming out is less than 0.001. Once this convergence is set, the output current with five harmonics is calculated and is passed to the next iteration in the loop. The same criteria was set as in the integral method; the adjustment of the phase ϕ will only adjust the phase of the first harmonic, while changes in the magnitude of *a* will scale across all harmonics. This method reaches a solution much faster than the integral method, and 10 or more iterations can be run without taking too much CPU time. As can be seen in Figure 2.6, the solution typically converges on a solution after a few iterations.

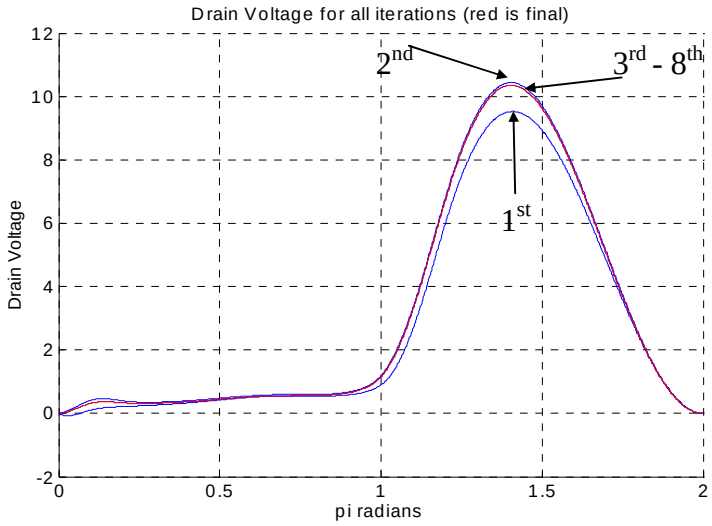


Figure 2.6 – Plot of eight iterations of the drain voltage. As was the case with the integral method, the solution has excellent convergence after three iterations.

2.2.6 – Quantifying Amplifier Performances

At this point, the only thing left to be calculated is the relevant specifications of the designed amplifier. The output parameters to be considered are THD, efficiency, and input and output power, as well as the power consumed in the different parts of the circuit. Since the amplitude of the output current *a* is known, the output power can be calculated as

$$P_{out} = \frac{(I_{RMS})^2}{R} = \frac{\left(a/\sqrt{2}\right)^2}{R}. \qquad (2.26)$$

Knowing the power supply voltage and the waveform for the power supply current (i_{Lc}), the input power can be defined as the average current times the voltage,

$$P_{in} = \sum_{n=1}^{N} \frac{i_{Lc}(n) \cdot V_{DD}}{N}. \tag{2.27}$$

The difference between P_{in} and P_{out} represents the power lost in the system, which is a combination of the power lost in the transistor,

$$P_{trans} = \sum_{n=1}^{N} \frac{v_{DS}(n) \cdot i_{D}(n)}{N},$$

(2.28)

the power consumed in the inductors,

$$\begin{aligned} P_{R_{Lc}} &= \sum_{n=1}^{N} \frac{i_{Lc} \cdot R_{Lc}}{N} \\ P_{R_{Ls}} &= \sum_{n=1}^{N} \frac{i_{O} \cdot R_{Ls}}{N} \end{aligned}, \tag{2.29}$$

and the power lost in the unwanted harmonics at the output,

$$P_{harm} = \sum_{n=1}^{N} \frac{(i_O)^2 \cdot R}{N} - P_{out}\ . \tag{2.30}$$

From this, the THD can be calculated as the ratio of the power consumed in the harmonics to the power at the output.

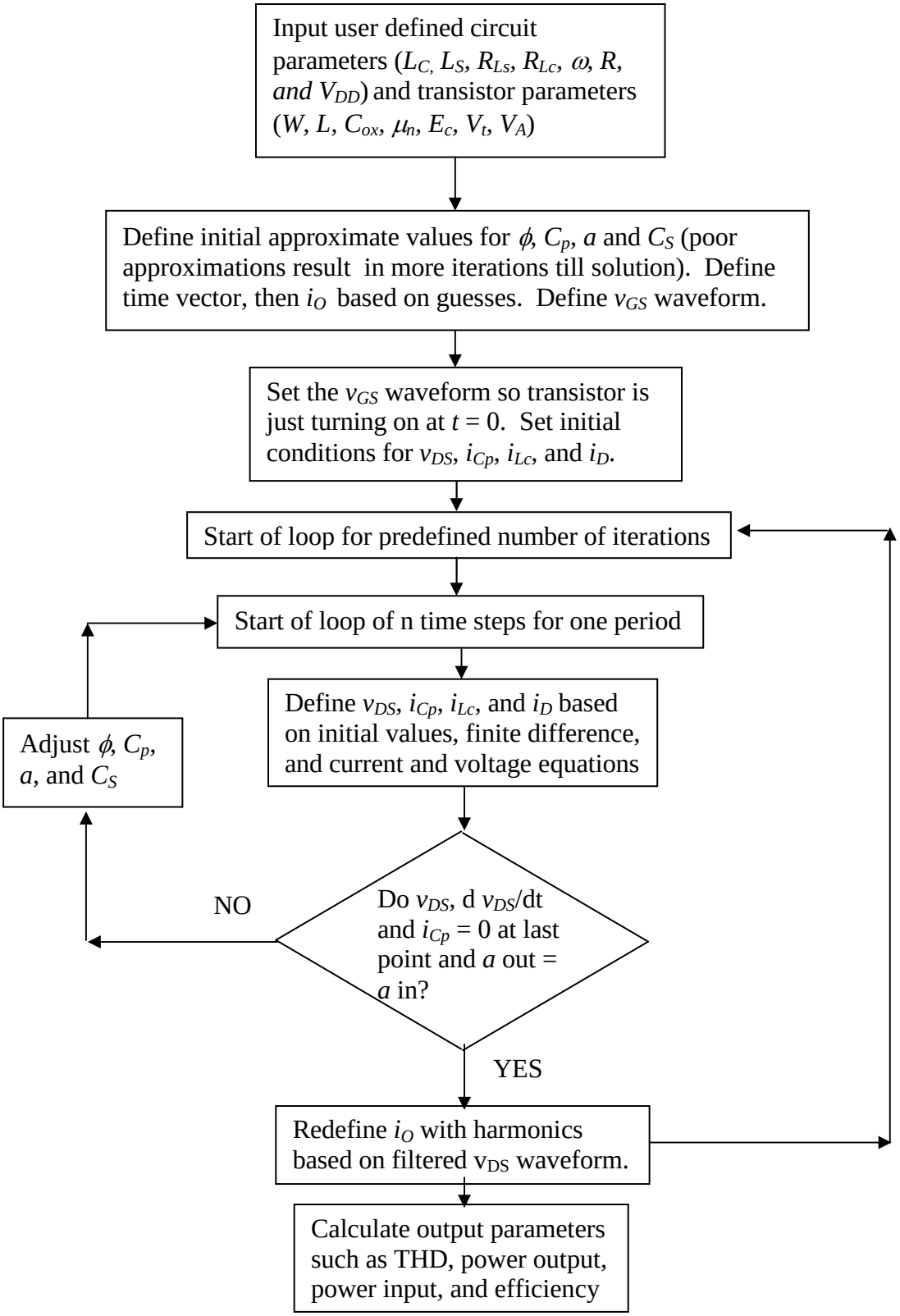


Figure 2.7 – Flow chart for finite difference program.

Chapter 3: Results and Discussion

As can be seen from Chapter 2, the modeling of the Class-E amplifier through the use of MATLAB takes into account a large number of variables and outputs all voltage and current waveforms, design specifications, and optimized circuit parameters. Due to the large number of inputs and outputs of the program, the results presented will take into account the most relevant variables from a design standpoint (inductor sizes, load resistance, *W/L* ratio of the transistor, and power supply voltage) and will be limited to the most pertinent output specifications (output power, efficiency, and Total Harmonic Distortion [THD]) as well as the optimized circuit components (C_P and C_S). For example, the output voltage amplitude *a* can be obtained from output power for a given load resistance, and since plots of output power are presented in this chapter, *a* will not be. Similarly, the offset phase of the output ϕ is not as useful of a figure as the capacitor value (C_S) required to produce this phase (only the most pertinent specification will be presented when much correlation exists between two variables). For all simulations presented in this chapter, the default parameters will be those of Table 3.1 unless otherwise stated.

Table 3.1 – List of default parameters used in results presented in Chapter 3.

Parameter	Symbol	Value
Choke Inductor	L_C	5nH
Series Inductor	L_S	5nH
Q of Inductors	Q	15
Load Resistor	R	50Ω
Transistor Width	W	1500μm
Transistor Length	L	0.6μm
Power Supply	V_{DD}	3.3V
Frequency	ω	2π×2.4GHz

3.1 – Effects of Load Resistance and Transistor Aspect Ratio Variation

Working on a fixed supply system, the biggest influence that the designer has on the output power would be the load resistance. Considering that the average of the voltage observed at the drain needs to equal the power supply voltage (minus voltage drop from the Choke inductor resistance), the v_{DS} waveform will not have much variation in magnitude with variation in the load resistance. Since the output voltage is simply a filtered waveform of the drain voltage, the output voltage will not have significant variation to the changes in load resistance (except for losses in the series inductor L_S and attenuation from the reactance of the slight inductive tuning of the load network). As can be seen in Figure 3.1, as the load resistor decreases from 100Ω to 20Ω, the power tends to increase since the voltage is relatively fixed because of an increase in the load current. However, once the load resistance approaches the ON resistance of the transistor shown in Figure 3.2 (and that of the resistances of the inductors), the output power drops off quickly due to the fact that the amplifier is no longer operating near ideal conditions. Figure 3.2 shows that the ON resistance decreases as the width of the transistor increases. Note that a total drain and source contact resistance of 1.5Ω was included in the model. It is interesting to point out that the transistor does not turn immediately ON or OFF as would happen in the ideal case. This is mostly from the fact that the gate voltage does not switch instantly, but is modeled as the typical output of a Class-F gate driving stage. The instantaneous drain voltage of the circuit is also considered in The ON resistance model is defined as the ratio of the instantaneous drain voltage to the instantaneous drain current from Ohm's law.

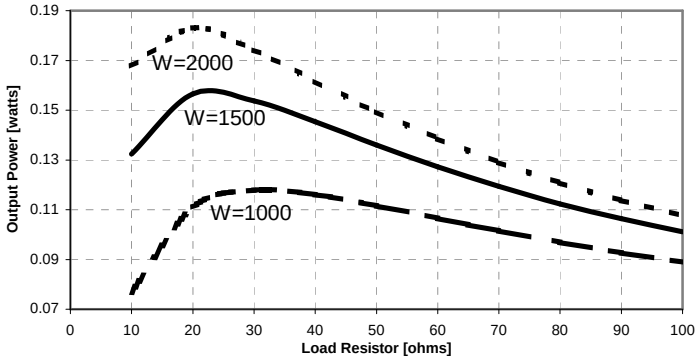
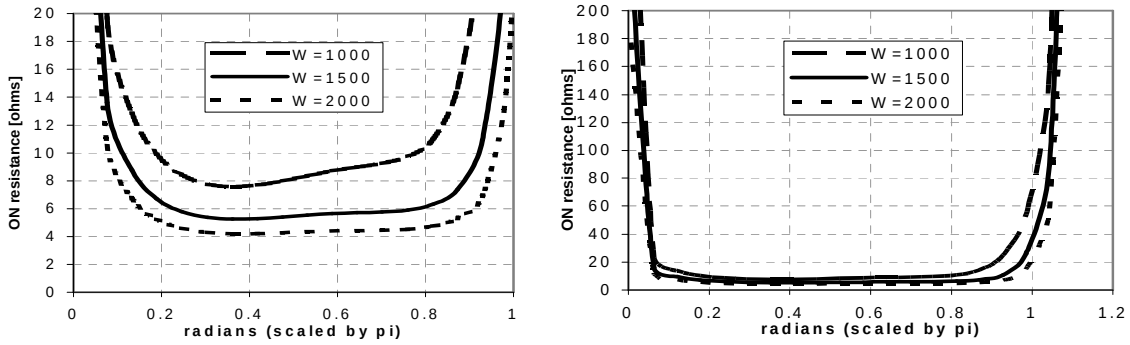


Figure 3.1 – Variations of output power with load resistance with the transistor width as a parameter. For these plots, R_{Lc}=R_{Ls}=3Ω.

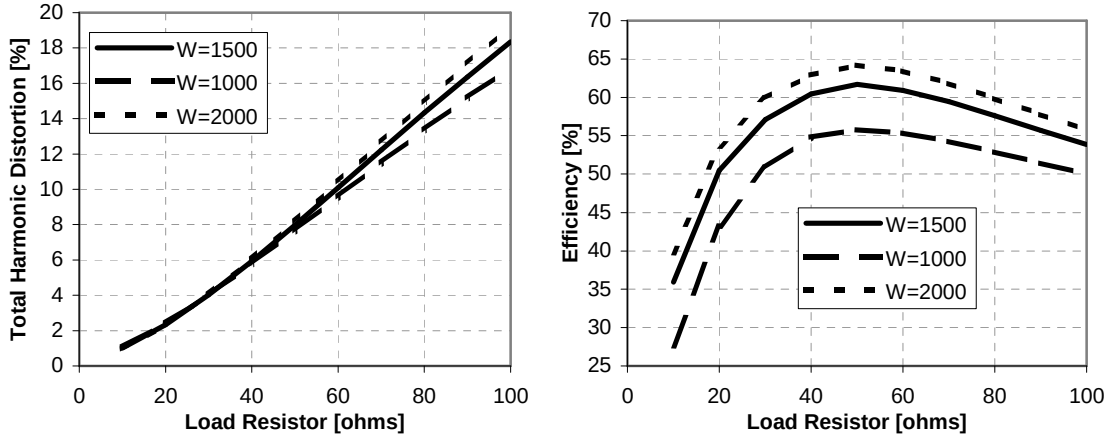


(a) (b)

Figure 3.2 – (a) ON resistance of the transistors modeled for Figure 3.1 (same parameters used). (b) Same as (a) except with larger scales on the axis.

Plots of THD and efficiency are presented as functions of the load resistor in Figures 3.3 (a) and (b), respectively. It is worth noting that the larger transistor proved to have the best performance in terms of power output and efficiency, but it has slightly lower performance in harmonic noise. These results are attributed to the lower ON resistance of the larger transistor. Reynaert et al. [20] however, have shown that although larger transistors increase the efficiency of the Class-E stage; they are harder to drive due to a larger gate capacitance. This will result in a decrease in the efficiency of the driving

stage, and after a certain size, will eventually result in a decrease in overall Power Added Efficiency (PAE).



(a) (b)

Figure 3.3 – a) THD and b) efficiency as functions of load resistance and transistor width.

To complete the analysis, the impact on the optimized load network parameters with respect to variations in the load resistance will be considered. As can be seen in Figure 3.4, the extra area taken up by larger transistors will be somewhat offset by the decrease in the optimized capacitor sizes. It is also important to note that the capacitance modeled here is the total capacitance seen from drain to ground, so a larger transistor will also decrease the value of C_P (drain to source capacitance is part of C_P). This puts a theoretical limit on the maximum size of the switching transistor. Fortunately, one would most likely use a larger transistor for higher power applications that would require a smaller load resistor, and as shown in Figure 3.4, would require a larger C_P, thus accommodating the larger transistor. One important note about Figure 3.4 is that the capacitor values scale inversely proportional with frequency (e.g., if the operating

frequency is one tenth of the frequency specified, the capacitor values required would be ten times larger if inductors ten times larger are also used).

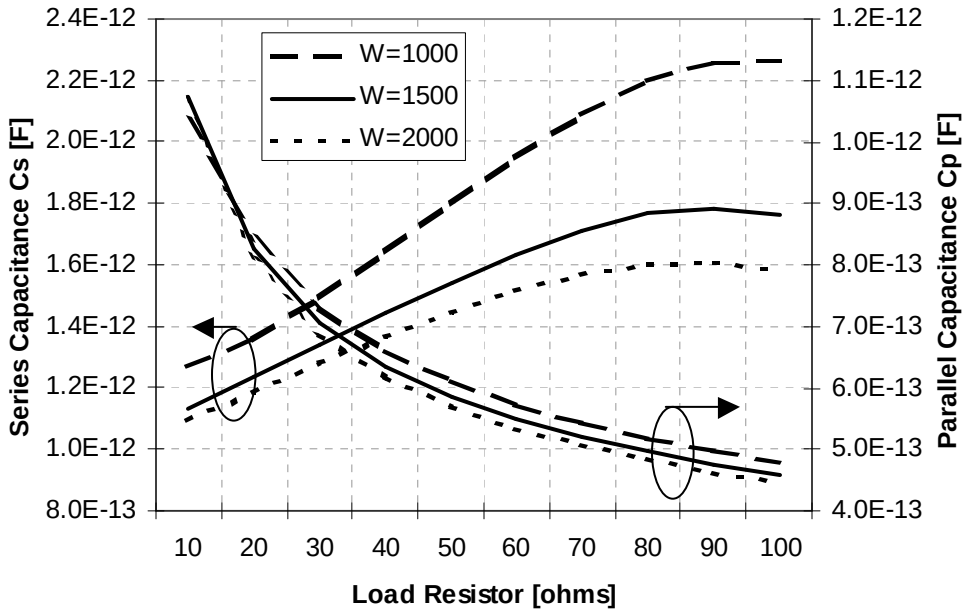


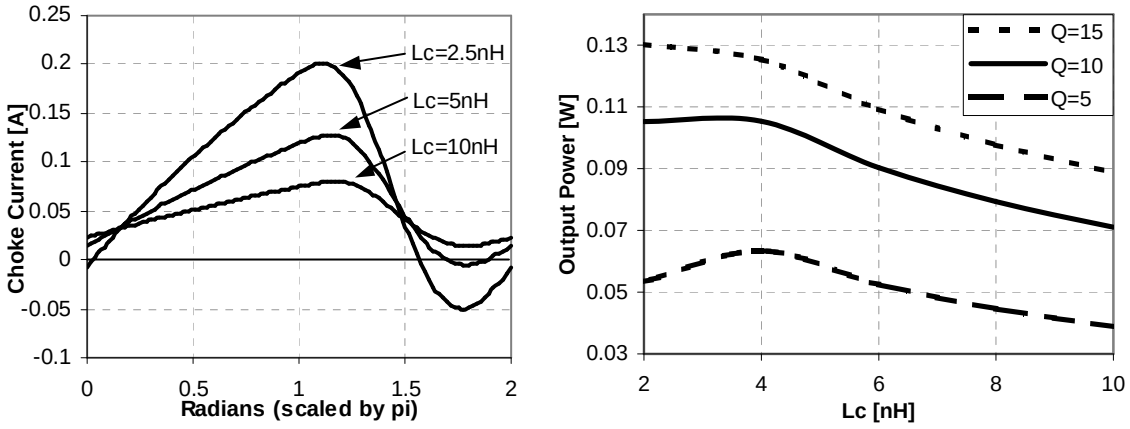
Figure 3.4 – Circuit capacitors C_S and C_P as functions of the load resistance with the transistor width as a parameter. Other circuit values used are equivalent to those of Figure 3.1.

3.2 – Varying Choke Inductor Size and *Q*

As mentioned in Section 2.1, the sizes of the two circuit inductors will be set by the designer, thus requiring a detailed discussion on the advantages and consequences of variations in these parameters. The choke inductor L_C has the effect of attenuating the harmonics present in the choke current i_{LC}, and will be the topic of discussion for this section. The ideal case, modeled in most conventional analysis with exceptions of Chan and Toumazou [25] and Li and Yam [26], assumes an infinitely large inductor, thus blocking all harmonics and only passing a pure DC current. Both references however,

assumed an ideal switch of a transistor (zero ON resistance, infinite OFF resistance, instantaneous turn ON and turn OFF) and lossless inductors, thus not accounting for most of the non-idealities presented in this analysis.

As shown in Figure 3.5a, as the choke inductor L_C is increased representing a more ideal case, the amount of ripple present on the waveform is also decreased. The average current is also noticeably decreased as L_C is increased, resulting in less input power. The effects of the decreasing input power with larger L_C values are offset above 4 to 5nH by a subsequent decrease in output power as shown in Figure 3.5b. This drop in output power is mostly due to an increase in the intrinsic resistive losses inside the inductor.



(a) (b)

Figure 3.5 – a) Variations of the choke current waveform i_{Lc} with different choke inductors. b) Variations of output power with choke inductance with Q as a parameter. The Q of L_S was assumed the same as that of L_C.

Since one would typically assume the output power to increase with an increase in choke inductance (more ideal operation from more ideal conditions), and this does not occur as

explained below. It is observed that the power consumed in the harmonics remains almost perfectly constant throughout the entire range of choke inductors for a given value of Q, even though the power of the first harmonic decreases with larger choke inductors. This is most likely due to the change in phase at the output. It was discussed in Section 2.1.6 that if the phase ϕ were to change, the excess inductance seen by the fundamental would change significantly, but that seen by the harmonics would see virtually no effect. It is shown in eq. 2.12 that the excess inductance is taken into account in attenuating and filtering the v_{DS} waveform. Therefore, if the optimal phase were to change with larger L_C values in such a way as to increase the required excess inductance, then the output power decrease with larger choke inductors can be attributed to the voltage attenuation of the output due to the impedance of the larger excess inductance seen by the fundamental frequency at the optimized load network. The only thing left to prove then to support this explanation would be that the excess inductance is indeed increasing as L_C increases. For the simulations shown, L_S was held constant at 5nH, but as shown in Figure 3.6, the series capacitance C_S increased when L_C increased. This would cause a greater excess inductance at the fundamental frequency as less of the inductance would be canceled out, and thus supports the explanation that the additional harmonics introduced by small inductors actually have an effect of shifting the desired output phase in a desirable way so as to increase the output power without increasing the harmonic power. This leads to the result shown in Figure 3.7a where the THD is shown to increase with increasing values of L_C. This would imply then that for certain applications, smaller L_C values are desirable within limitations. We can see from Figure 3.7b that the efficiency is much lower for

very small values of L_C, leveling off around 4 to 5nH. This then implies that an optimal value of L_C is found around 4 to 5nH depending on the desired specifications (5nH will have slightly higher efficiency, but 4nH will have slightly more output power and lower THD).

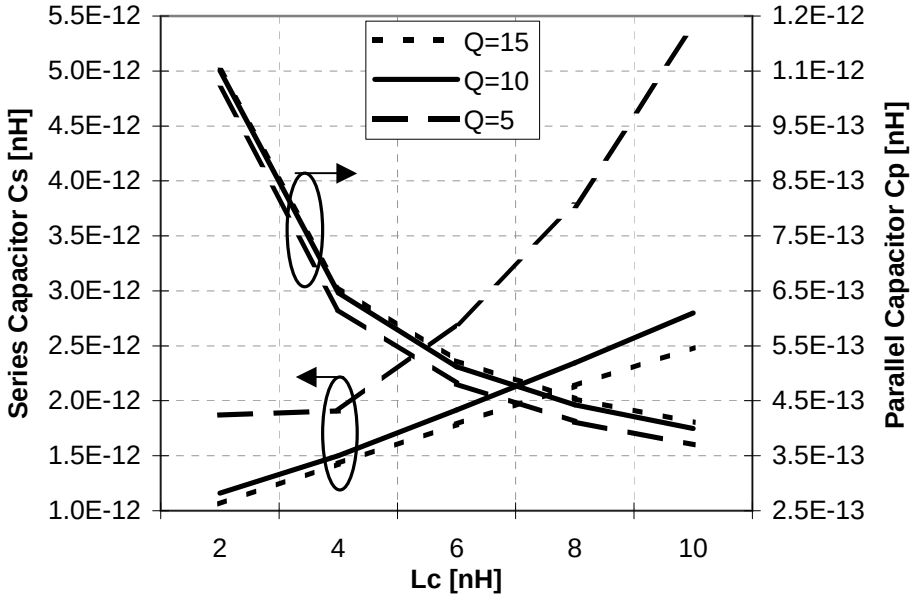
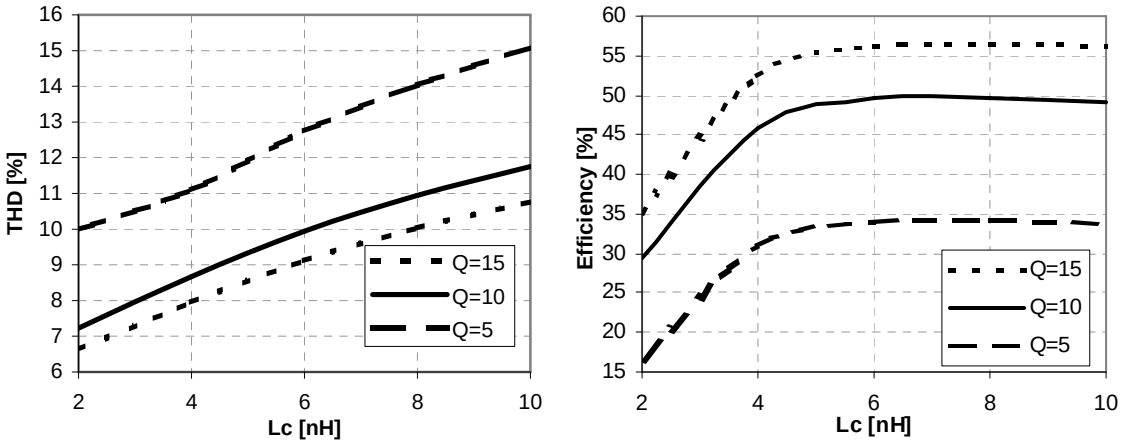


Figure 3.6 – Optimized circuit capacitors as a function of L_C and inductor Q.



(a) (b)

Figure 3.7 – a) Total Harmonic Distortion as a function of the choke inductance with Q as a parameter. The Q of L_S was assumed to vary along wit the Q of L_C. b) Efficiency as a function of the choke inductance with Q as a parameter.

It is important to note that this condition is not a set optimization, but is also dependant on other variables in the design. The most notable of these is the load resistance. It is worth noting that 4nH to 5nH is about the value of L_C where the impedance of the choke equals the value of the impedance of the load network (tuned network and load resistance). If the value of the load resistance were to decrease (to meet the output power requirements), the efficiency would level off at a lower value of the choke inductor L_C.

3.3 - Varying Series Inductance Size and *Q*

The size of the series inductor mostly affects the loaded *Q* of the tuned load network and thus determines the amount of harmonics that will be passed to the output. By increasing the value of L_S, a smaller value of C_S will be used in order to ensure that the same value of excess inductance is seen by the fundamental frequency (resulting in no net change in the phase shift produced by the load network). Then, an appreciably larger value of inductive reactance will be seen by the harmonics, making them more greatly attenuated. However, the larger inductors will also have lager internal resistances associated with them, and will result in significant power loss in the inductor itself. This is offset by the fact that less undesired power is consumed by the load at harmonic frequencies, causing a very little variation in the efficiency of the amplifier with variation in the series inductance L_S. Since the output power at the fundamental frequency is virtually unaffected by variations in L_S because the same excess inductance is used, the output power also has very little variation with L_S. For this reason, efficiency and output power will be shown in tabulated form in Table 3.2, and only a variation of 1 to 2 percent from

the given values will be seen for values of L_S from 4nH to 10nH (inductors below 4nH cannot be used since the excess inductance required would be greater than inductor itself for load resistances of 50Ω). The THD however, will be greatly affected by changes in L_S, and is presented in Figure 3.8.

Table 3.2 – Output power and percent efficiency as functions of inductor *Q*.

Q	Po	%E
5	0.31	31
10	0.95	47.5
15	0.116	55

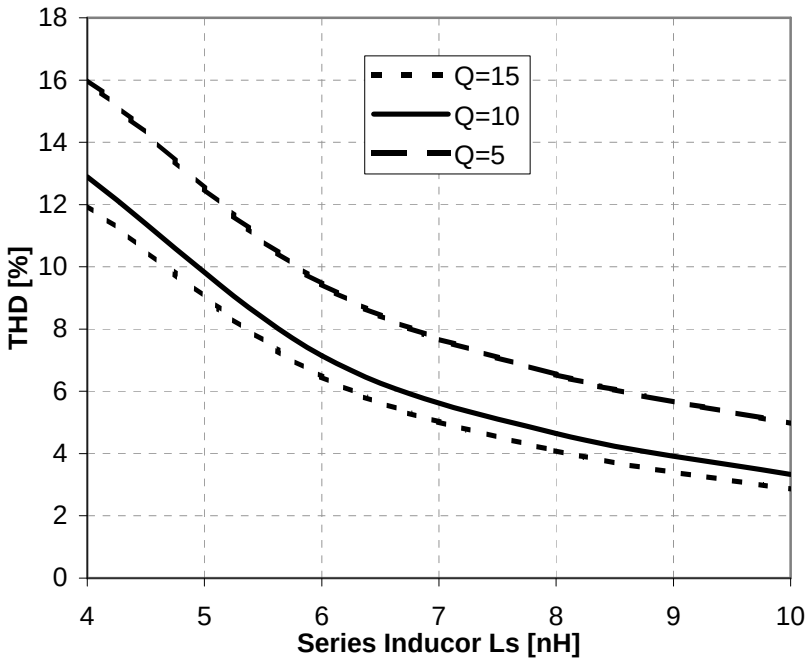


Figure 3.8 – THD as a function of L_S with inductor *Q* as a parameter.

The last point to consider with respect to the size of the series inductor L_S is the size of other components in the system. It has been shown that the overall performance improves as the size of L_S increases, and Figure 3.9 shows that both C_S and C_P decrease

with increasing L_S, thus the total chip area may not suffer greatly by increasing the size of L_S due to a decrease in the size of other components.

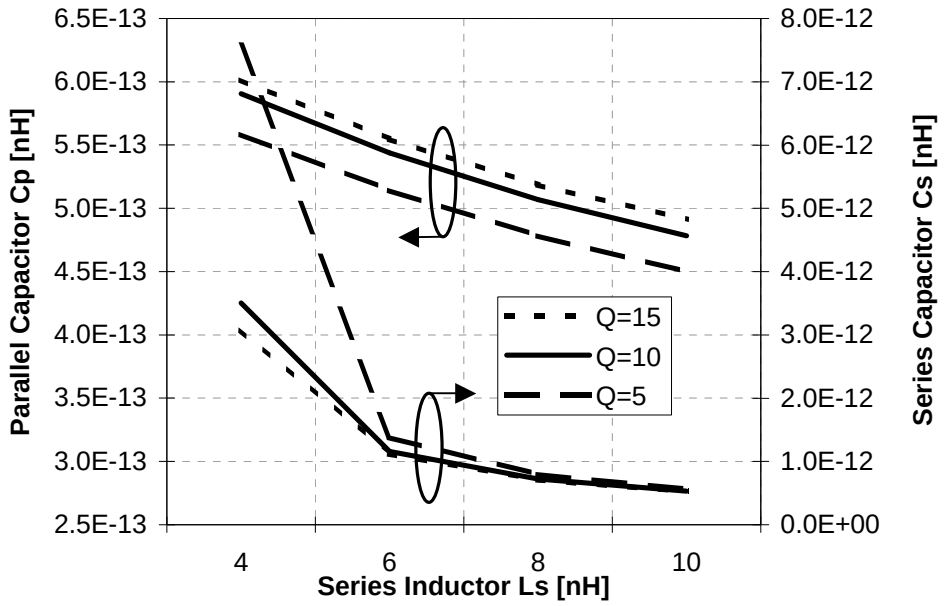


Figure 3.9 – Circuit capacitor values as a function of series inductor L_S with inductor Q as a parameter. Here, the Q of L_C was assumed to vary with the Q of L_S.

3.4 – Varying V_{DD}

The two most significant factors in setting a desired output power are the load resistor as discussed in Section 3.1, and the power supply voltage V_{DD}, which will be the topic of discussion for this section. Figure 3.10 shows the plot of output power, efficiency, THD and series and parallel capacitances as a function of power supply voltage V_{DD}. Figure 3.10a shows an exponential relationship between supply voltage and output power (this is due to the squared relationship between power and voltage [$P = \frac{V^2}{R}$]). However, as the supply voltage increases, the THD also increases and the efficiency levels off around 4V and then starts declining rapidly. This is due to the correlation between increased power

supply voltage and increased output current. As the output current is increased, the effectiveness of the series inductor L_s is decreased, and more harmonic noise is present at the output. An even bigger consideration to increasing the supply voltage should be the drain to source voltage of the transistor. It is shown in Figure 4.3c in section 4.1 that the drain voltage can go over three times as high as the supply voltage, possibly pushing the transistor past breakdown.

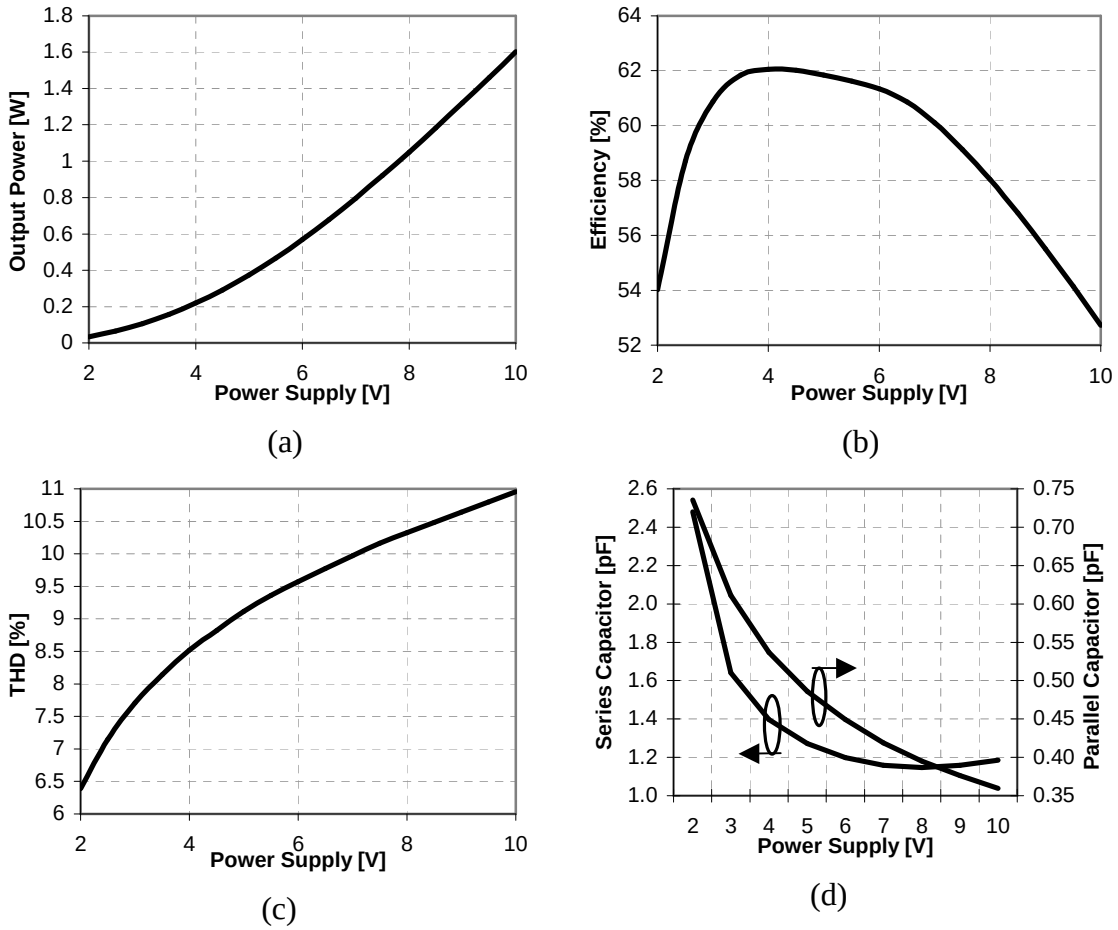


Figure 3.10 – Class-E amplifier a) output power, b) efficiency, c) THD, and d) circuit capacitors with variation of the power supply voltage V_{DD}.

Chapter 4: Verification of Results

4.1 – Verification with SPECTRE®

Results of the MATLAB simulation waveforms were verified using SPECTRE® circuit simulator with BSIM3 MOSFET model of the 0.5μm AMI technology. The first step in the verification process was to ensure that the I-V curves of the transistor match, as seen in Figure 2.5. The circuits will then be simulated using the same parameters, with the exception that the parallel capacitance will be split amongst the dedicated capacitor C_P and the transistor. The parameters as mentioned in Table 3.1 were used except that a load resistance of 20Ω was used for both simulators. The series capacitor calculated by MATLAB to be used in SPECTRE® was 1.2587pF, while the parallel capacitor was calculated to be 0.7907pF. The parallel capacitance was split as 0.3225pF for the stand-alone capacitor, and 0.4682pF from the capacitance of the transistor. These numbers were chosen by decreasing the physical capacitor until the correct switching conditions were observed. The calculated capacitance minus the parallel capacitor was assumed to be the transistor capacitance, and was then verified as seen in Figures 4.1 and 4.2. The MATLAB code only gives a plot for the current through the total capacitance seen from drain to ground when producing the waveform for i_{Cp} (it assumes C_P is one lump capacitance), and only gives the drain current i_D as the channel current. SPECTRE, however, gives the drain current as a combination of the drain current and current passing through the drain to ground capacitance of the transistor, and the capacitor current is given as only the current passing through the dedicated capacitor. For this reason, the

MATLAB plots have been modified so that the drain current curve (Figure 4.1) shows $i_D + \frac{0.4682}{0.7907} \cdot i_{Cp}$ and the capacitor current (Figure 4.2) is modified to show $\frac{0.3225}{0.7907} \cdot i_{Cp}$.

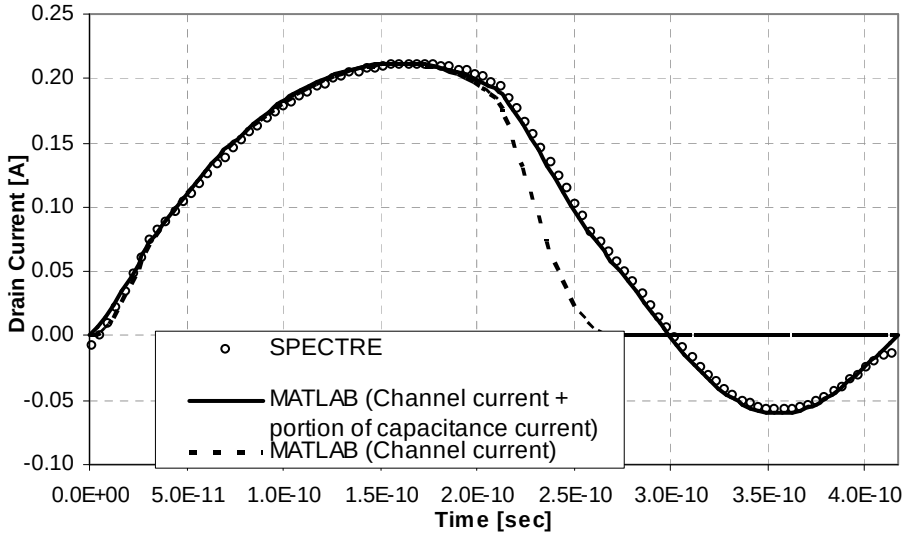


Figure 4.1 – Drain current plotted for one period of the waveform. The channel current is represented by the dashed line, while the solid line accounts for the current through the transistor capacitance.

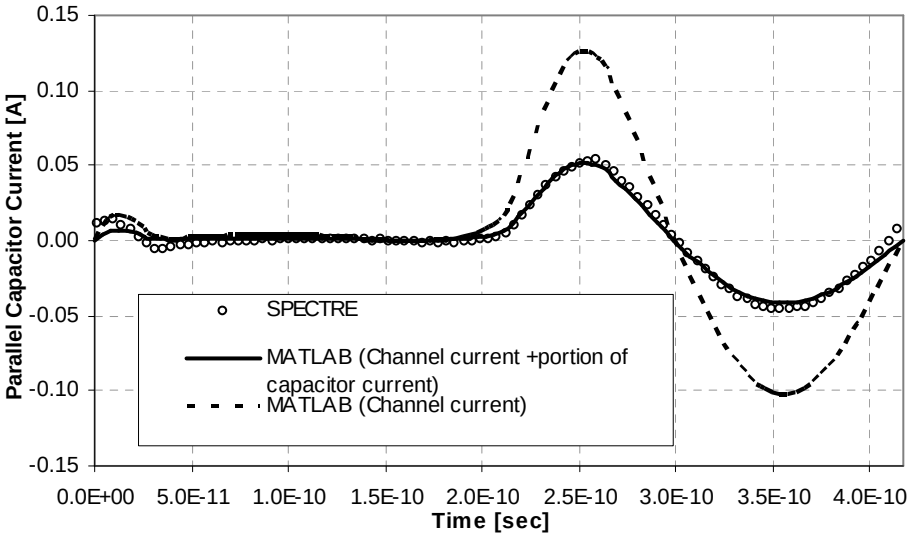


Figure 4.2 – Parallel capacitor current plotted for one period of the waveform. The dotted line is the current due to the total capacitance seen from the drain of the transistor to ground, while the solid line is the current through the portion of the parallel capacitance excluding the transistor drain to ground capacitance.

The standard Class-E waveforms are presented in Figure 3.13. Note that the transistor is assumed ON for roughly the first half of the period and OFF for the second half. The transition point from ON to OFF being somewhat subjective based on the transistor resistance shown in Figure 3.2. It was assumed for this simulation that the Class-E circuit would be driven by a Class-F stage preceding it, and a typical Class-F output voltage waveform [2] is presented as the gate voltage input as seen in Figure 3.13a. It is observed in Figure 3.13b that the ripple present on the choke current i_{Lc} is quite significant; despite using a relatively large 5nH choke inductor. This waveform obviously cannot be approximated as a DC signal as would be the case in the conventional analysis. The drain to source voltage is shown in Figure 3.13c. It is observed that even with a transistor size of 1500/0.6μm that an appreciable voltage still exists across the transistor in the ON state. The most simplified conventional analysis of this circuit assumes that the ON resistance is zero making the ON state voltage zero, which clearly is not the case. More accurate analysis (Choi et al. [16], Wang et al. [17], Sekiya et al. [18], Kessler et al. [19], Reynart et al. [20], Alinikula et al. [21], Raab et al. [27], and Mandojana et al. [28]) assume a constant ON resistance, making the drain voltage perfectly follow the drain current. Although similarity exists between the waveforms, there is an appreciable difference between the drain current and the drain voltage due to the variable resistance as modeled in Figure 3.2, thus requiring the more thorough model of the transistor as presented in this analysis. Figure 3.13d shows the distorted output waveform due to the finite output inductor L_S. The waveform shown has only 2.7% THD, yet the waveform is quite noticeably distorted from an ideal sinusoidal

wave as presented in the conventional analysis. The harmonics presented here do not just affect the output, but will affect the accuracy of the rest of the current waveforms (and subsequently the voltage waveforms) in the circuit since the output current i_O, the capacitor current i_{Cp}, and the drain current i_D must sum up to the choke current i_{LC}.

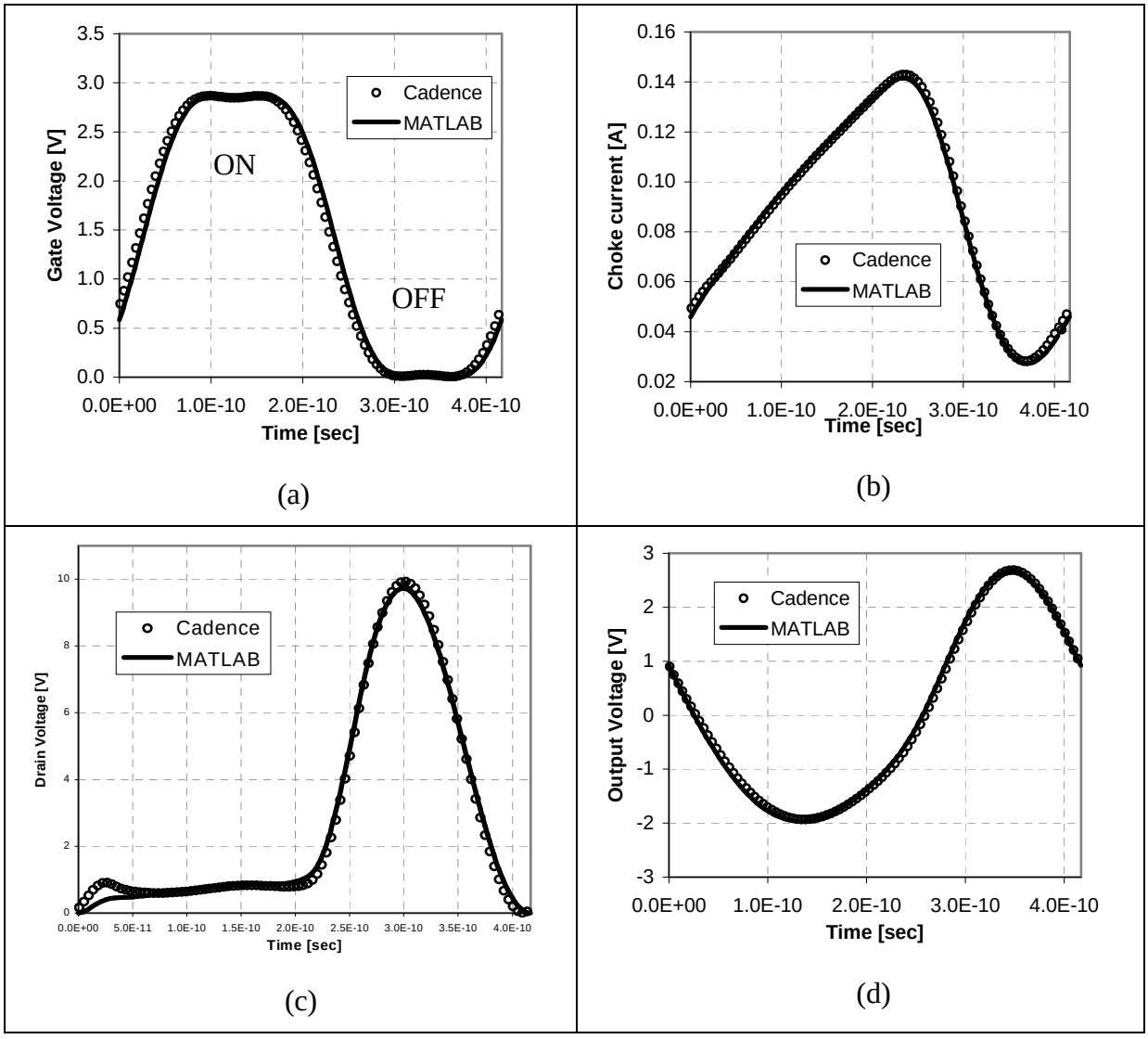


Figure 4.3 – Comparison of MATLAB and Cadence Class-E amplifier waveforms. a) Input voltage v_{GS} at the gate of the transistor, b) Choke current $i_{Lc,}$ c) Drain voltage $v_{DS,}$ and d) Output voltage v_O waveform.

4.2 – Partial Verification with Hardware

Verification was also done on the theoretical calculations using discrete components on a prototype board. It was discussed in Chapter 3 that if the frequency is scaled by a given factor, the reactive components in the circuit can be inversely scaled by the same factor to maintain the same impedance in the circuit. For this reason, the hardware was implemented at 120kHz with inductor sizes of 100μH, representing an equivalent impedance of running the circuit at 2.4GHz with 5nH inductors as would be typically seen on a silicon fabricated IC. Since the *Q* of passive inductors is typically much higher than that of silicon fabricated ones (the ones used had less than 0.2Ω of resistance), a 5Ω resistor was added in series with the inductors to represent the intrinsic losses that would otherwise be present. Placing the resistor for the choke inductor between inductor and power instead of inductor to drain also aided in the measurement of the choke current. Having a fixed reference voltage on one side of the resistor allowed for easy measurement of the voltage across the resistor with the oscilloscope, and subsequently the current through it by dividing by the value of the resistor. The transistor used is a Radio Shack® IRF-510 n-channel power MOS power MOSFET. In order to accurately model the circuit, accurate representation of the transistor must first be obtained. This was done using the Techtronix® 571 curve tracer to obtain the desired I-V characteristic curves for the transistor. Once the curves could be modeled using the transistor parameters discussed in Chapter 2, the parameters could be used in the simulation to represent the transistor. The parameters used to model the transistor are given in table

4.1, and the results of the hardware experiment and their comparison to the MATLAB simulation are shown in Figure 4.5.

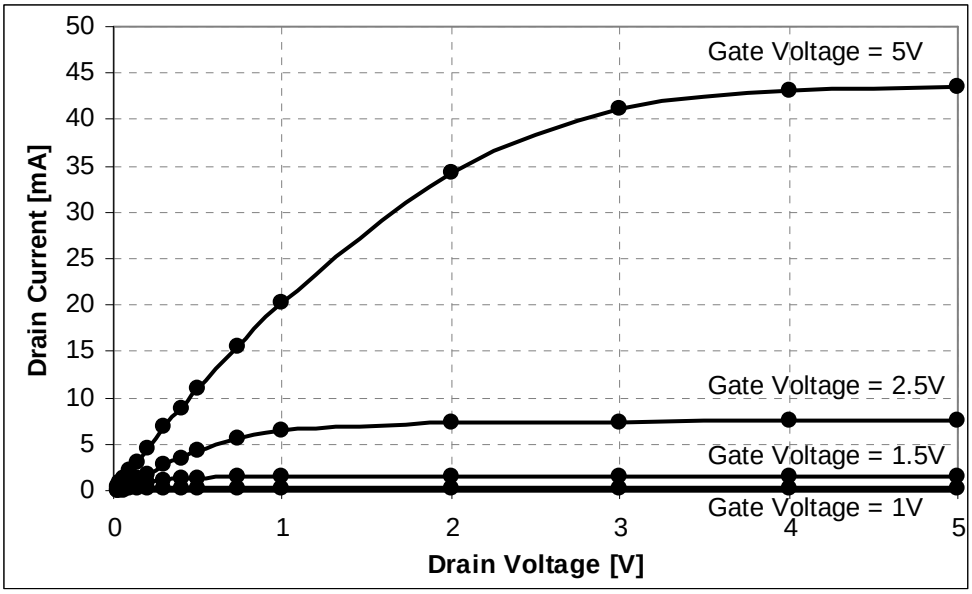
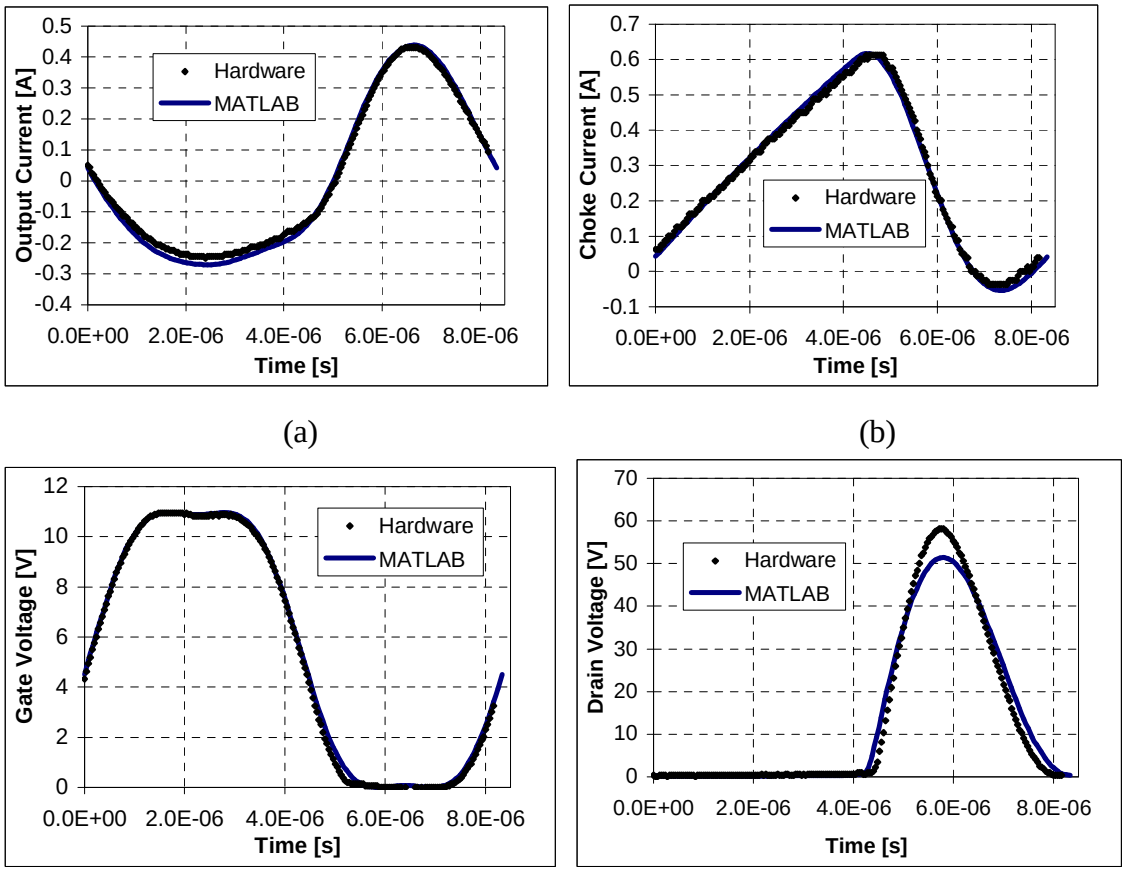


Figure 4.4 – I-V curves extracted form the Radio Shack® IRF-510 n-channel power MOS using a Techtronix® 571 curve tracer.

Table 4.1 – Parameters used for modeling the Radio Shack® IRF-510 n-channel power MOS. A constant mobility model is used for this analysis.

Parameter	Symbol	Value
Threshold Voltage	V_t	4.5V
Drain/Source Contact Resistance	R_{drain}, R_{source}	0.015Ω
Transistor Width	W	6500μm
Transistor Length	L	1μm
Early Voltage	V_A	155V
Critical Electric Field	E_C	6.7e6 V/cm
DIBL Parameter	α	0.00025



(a) (b)

(b) (d)

Figure 4.5 – Hardware versus simulated results for a) output current, b) choke current, c) gate voltage, and d) drain voltage for a Class-E amplifier.

The hardware results show excellent agreement with the simulation, with the exception of the drain voltage. This is most likely due to sub-threshold currents. It was observed on the curve tracer that there was a reasonable current present at voltages quite far below the threshold voltage, where as the model assumes zero current in this state. Typically the threshold voltage is found by plotting drain current versus gate voltage and extrapolating a line to the gate voltage axis. The model then assumes an abrupt point junction at this threshold, whereas the real component had a transition that was much slower. This

caused the current to be underestimated below threshold, and over estimated just above threshold as the transistor turned on more slowly.

This hardware simulation was done using discrete components and does have limitations when compared against a high frequency integrated circuit. A high frequency power amplifier may have issues with inductive coupling of the inductors as well as temperature effects associated with inductors and transistor. Also, do to the large scale of the components used, the parasitic effects of the interconnects are negligible, where this may not be the case on an integrated circuit depending on the design and layout.

Chapter 5: Conclusions and Future Work

The model for a Class-E amplifier presented in this thesis proved to be successful through verification in the SPECTRE® circuit simulator and in hardware. The circuit combined all the major non-idealities previously discussed in literature into a single model, and also incorporates the driving gate waveform as a parameter. The excellent agreement shown in Chapter 4 verifies the use of this model for the design of a Class-E amplifier without the need to purchase expensive circuit simulators such as SPECTRE. Any improvements to the model would have a small enough impact on the final result that they would be completely be absorbed by the large tolerances inherent in silicon processing.

One deficiency of this model that was ignored due to its insignificance was the non-linearity of the capacitance seen in the transistor from drain to ground. It is known that both the drain to source and drain to gate capacitances are variable with applied voltage, but the amount of variation was shown to be insignificant in Figures 4.1 and 4.2. The capacitance associated with the large inductors was also assumed insignificant compared to the much larger discrete capacitors. If the process technologies in future years were to change so that these assumptions were no longer valid, the model would need to be modified to account for these.

Future work associated with this project could be done in the area of the optimal switching conditions. Sokal *et al.* [1] assumed that the drain voltage should return all the way to zero volts at the switching points since that was the assumed ON state drain

voltage of the transistor. This switching condition has been the standard used in literature, but when the drain ON voltage is not assumed to be zero, it may be able to be shown that better performance could be obtained if the drain voltage returned to the ON voltage from the OFF state instead of to zero. Initial experiments performed by modifying the MATLAB code have supported this theory, but the drain ON voltage is not a constant value, so the value of the drain voltage to be set for the OFF to ON transition currently is approximated by the programmer. Deriving an expression to obtain the correct optimal switching condition would require significant calculation in order to prove this theory correct, and will be left for future work.

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