Development of a deep submicron fabrication process for tunneling field effect transistors

Michael Barth

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Development of a Deep Submicron Fabrication Process for Tunneling Field Effect Transistors

By

Michael J. Barth

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in Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in Microelectronic Engineering

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ROCHESTER, NEW YORK
Development of a Deep Submicron Fabrication Process for Tunneling Field Effect Transistors

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Michael J. Barth

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I dedicate this thesis to my family: my mother Adrienne, my father Bernard, my sister Megan, and my Grandmother Victoria. Without your support and encouragement this work would not have been possible.
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Abstract

The requirements placed upon next-generation devices include high on-state current, low power supply voltages, and low subthreshold swing. Tunneling Field Effect Transistors (TFETs) have been of recent interest because they have the potential to fulfill these requirements. The TFET is a gated tunnel junction. The TFET operates by modulating the probability of band-to-band tunneling between the source and the channel of the device. When the tunnel transistor is off, there is a potential barrier between the source and the channel. The width of this potential barrier is large enough to prevent electrons tunneling from the valence to conduction bands, the result of which is a lower leakage current and improved power efficiency. The potential barrier narrows as bias is applied to the gate. When the applied gate voltage exceeds the threshold voltage this potential barrier becomes thin enough to allow for tunneling from the valence band to the conduction band. The tunneling mechanism allows the device to have a high on-state current and low subthreshold swing at low power supplies.

To date the majority of the work involving TFETs has been simulation-based. Unfortunately the models used in these simulations are deficient. The models require physical data for proper calibration [1]. The few experimental demonstrations of TFETs have not yielded a body of empirical data sufficient for calibration. This work intends to help provide that body of experimental data on gated and non-gated tunneling junctions in InGaAs. This work focuses on the development of a process to gate p-i-n junctions and extract the contribution of the gate on junction performance.
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List of Symbols

\begin{itemize}
  \item[$D$] Overlap Integral
  \item[$\hbar$] Planck’s Constant
  \item[$\xi$] Electric Field
  \item[$E_g$] Band Gap
  \item[$m^*$] Effective Mass
  \item[$k$] Relative Permittivity
  \item[$V_p$] Peak Voltage
  \item[$V_v$] Valley Voltage
  \item[$J_p$] Peak Current Density
  \item[$J_v$] Valley Current Density
\end{itemize}
## List of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>TFET</td>
<td>Tunneling Field Effect Transistor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>PVCR</td>
<td>Peak to Valley Current Ratio</td>
</tr>
<tr>
<td>EBL</td>
<td>Electron Beam Lithography</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic Layer Deposition</td>
</tr>
<tr>
<td>PE4400</td>
<td>Perkin Elmer 4400 Sputtering System</td>
</tr>
<tr>
<td>TiN</td>
<td>Titanium Nitride</td>
</tr>
<tr>
<td>TaN</td>
<td>Tantalum Nitride</td>
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Chapter 1
Introduction

The desire for improved performance drives the search for next-generation devices. While in the past this improved performance was quantified in terms of speed, the new benchmark is performance with high efficiency. Causing this shift is the rise of consumer demand for ultra-mobile devices and the push for efficient “green” technology. The scaling of the power supplies for TFETs can be greater than that of Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs). TFETs require less power to operate and thus are more efficient.

A high-order approximation of a TFET would be a gated Esaki tunnel diode. Esaki diodes have a very abrupt and degenerately doped $pn$ or $p-i-n$ junction. This abrupt junction causes the conduction bands of the two highly doped regions to overlap. This overlap allows for tunneling between the two regions when a small bias is applied. A reverse bias on the Esaki diode results in Zener tunneling, while a forward bias results in a tunneling component where the current increases with forward bias. TFETs are typically operated in the Zener regime. The addition of a gate along the junction allows for control of the conduction band overlap. With a small bias applied to the gate the conduction bands will shift, allowing the gate to control the probability of tunneling.

Theoretically this gate control should allow for a device with a high on current, low leakage current and a sub 60-mV/dec subthreshold slope. TFETs demonstrating all of these properties have only been in realized in simulation. These simulated TFETs utilize complex quantum and band-to-band tunneling models with discrete meshing to predict their behavior. The few experimentally demonstrated TFETs have only demonstrated the
low leakage currents and sub-60 mV/dec subthreshold slope [2]. Non-gated tunnel diodes have shown tunnel junctions with high on currents of 975 kA/cm$^2$ [3]. The models themselves have also been reported to underestimate the current density of devices by up to two orders of magnitude [1]. The disparity between simulation and experimental results and the admitted errors with the models necessitate more experimental research on tunneling junction, gated tunneling junctions, and TFETs.

This work introduces a mesa-first process for fabricating TFETs. The process utilizes electron beam lithography to define a series of mesas in a $p$-$i$-$n$ junction. A high-$k$ dielectric and a refractory metal are used to gate the sidewall of an individual mesa. This process utilizes a spin-on dielectric to isolate the individual devices and enable a second level contact. The dielectric layer and second level contact enables the fabrication of deep submicron devices while allowing for large contact pads. Deep submicron scaling is essential to studying tunneling devices as it allows for the perimeter to be a greater fraction of the device.
Chapter 2
Background

2.1. TFET Device Physics and Simulation:

A TFET like the device shown in Figure 2-1 is a gated $p$-$i$-$n$ diode. This TFET is a vertical structure with a polysilicon gate along the junction and sidewall of the device. Top and bottom contacts are used to contact the $n+$ and $p+$ regions. The $n+$ and $p+$ regions can act as either the source or drain depending on bias conditions.

![TFET Diagram](image)

*Figure 2-1: TFET shown operating in p-channel mode [4]*

Applying a reverse bias to the gate of the TFET in Figure 2-1 creates a hole channel in the insulator region ($i$-zone) leading to a tunnel junction at the $n+$ Si source. With reverse bias applied to the gate, the device is in the $p$-channel operation mode. Conversely applying a forward bias on the gate causes an electron channel to be induced in the insulating region, the device is in $n$-channel operating mode. With a forward bias on the gate, the $n+$ region acts as the drain while the $p+$ region acts as the source. The electron channel induced by the forward biased gate creates a tunnel junction at the $p+$
source. In both operating regimes the channel length is determined by the thickness of the insulating region.

![Figure 2-2: Simulated band diagram for a 100 nm n-channel silicon TFET [5]](image)

As seen in Figure 2-2, when the applied gate voltage $V_{GS}$ is zero the separation between the conduction band in the insulating region and the valence band in the p+ region results in a very low probability that tunneling will occur. Thus the device is considered to be off as no current will flow. As voltage applied to the gate is increased the separation between the conduction and valence band narrows. Applying a voltage on the gate of $V_{GS}=1.5$ V lowers the barrier height thus increasing the probability of tunneling to occur. With a high probability of tunneling, the transistor is on.

Modeling the behavior of the TFET begins with Kane’s model for band-to-band tunneling as seen in Eq 2-1 [6].

$$J = \frac{q^2 \xi}{36\pi^2} \sqrt{\frac{2m^*}{E_g}} \cdot D \cdot \exp \left( -\frac{\pi \sqrt{m^* E_g^{3/2}}}{2\sqrt{2h\xi}} \right)$$  

(2-1)
This model is a function of the electric field $\xi$, the bandgap across the tunnel junction $E_g$, Planck’s constant $\hbar$ and the effective carrier mass $m^*$. The tunneling current effective mass is often assumed to be the conduction band effective mass. The $D$ term in the expression for tunneling current refers to an overlap integral.

![Figure 2-3: Band Diagram Tunneling Probability][6]

The band-to-band tunneling model developed by Kane assumes a triangular barrier similar to the one shown in Figure 2-3 above. The model further assumes direct tunneling, tunneling in which momentum is conserved. The overlap integral $D$ shown in Eq. 2-2 [7] describes how the bands overlap as the electric field is varied.

\[
D = \int \left( F_c(E) - F_v(E) \right) \left( 1 - \exp \left( \frac{-E_g}{E} \right) \right) dE
\]

(2-2)
The overlap integral is dependent on $F_c$ and $F_v$ as well as two terms $E_s$ and $\bar{E}$. $\bar{E}$ as seen in Eq. 2-3 [7] is a ratio of constants dependent on the applied electric field, the band gap, and the effective mass.

$$\bar{E} = \frac{\sqrt{2qh\xi}}{\pi \sqrt{m^*E_g}}$$

(2-3)

The overlap integral describes how the energy bands overlap as the electric field is varied. $F_c$ and $F_v$ are the Fermi-Dirac distribution functions for the valence and conduction bands. The term $E_s$ refers to the smallest value of $E_1$ and $E_2$. As seen in Figure 2-3 $E_1$ refers to the difference in energy between a given energy level and the conduction band of the n-region. $E_2$ is similarly the difference in energy between the same given energy level and the valence band of the p-region. The limits of integration for $D$ are from $E_{cn}$ to $E_{cp}$. The overlap integral has no closed-form solution. In order to calculate the integral, two methods are commonly employed. The first method involves using a numerical solver to approximate the overlap integral. This method is best used in a TCAD simulation platform. The second method of calculating the overlap integral relies on approximating the overlap integral as a linear constant that is a function of charge and voltage.

A standard treatment of the Kane model assumes an average electric field throughout the structure Eq. 2-4 [7].
The average electric field approximation is not accurate. The electric field throughout the TFET will vary as a function of doping. Further the average electric field approximation fails to take into account the influence of the gate. A better approach to applying Kane’s model is to use an electrostatics-based electric field meshed across a device structure, using an advanced device simulation suite such as Silvaco Atlas or Sentaurus.

It should be noted that the Kane model is often quoted from the S.M. Sze text as seen in Eq. 2-5 [7]. This quotation has a discrepancy with that of Kane’s original model described in Eq. 2-1.

\[
J = \frac{q^2 \xi}{36 \pi \hbar^2} \sqrt{\frac{2m^*}{E_g}} \cdot D \cdot \exp \left( \frac{4 \sqrt{2m^* E_g^{3/2}}}{3 \hbar \xi} \right)
\]

(2-5)

The discrepancy is with argument of the exponential. The result of this discrepancy is that the current density given by the Sze version is 1-2 orders of magnitude less then Kane’s original formula. The origin of this discrepancy is due to the different approximation of the potential barrier. Sze uses the triangular approximation for the potential barrier while as shown in Figure 2-3, while Kane originally used a parabolic approximation for the potential barrier. This is important as theoretical work on TFET
based upon the Sze formula may under-predict the actual current density of their device [8, 9].

\[
S_{\text{Tunnel}} = \frac{V_{GS}^2}{\pi m^* E_g^{3/2}} \frac{\pi m^* E_g^{3/2}}{2V_{GS} + \frac{2e\hbar}{D}}
\]  

(2-6)

The subthreshold swing \( S \) for a TFET is given by Eq. 2-6 [4, 5]. As seen in Eq. 2-6 the subthreshold swing has a strong dependency on \( V_{GS} \). The \( E_g \) has weak influence on the subthreshold swing. Assuming a constant \( V_{GS} \), an increase in the \( E_g \) of the TFET would lead to a decrease in subthreshold swing. The strong proportional relationship between \( V_{GS} \) and subthreshold swing indicates that an applied \( V_{GS} \) equal to zero could lead to a subthreshold swing of zero; however this is not so. With \( V_{GS} \) equal to zero and the assumptions of an “infinite channel length under flat band conditions” [5] the TFET acts as a \( p-i-n \) diode. As a \( p-i-n \) diode there is no probability of tunneling, thus only a small amount of leakage current is present. Adding a small \( V_{GS} \) to the TFET leads to a small finite probability of tunneling[5]. As this small \( V_{GS} \) is applied the diode transitions to a TFET device. During this transition the subthreshold swing mathematically becomes infinitely large [5].

The subthreshold swing’s weak dependence on \( E_g \) means that a reduction in the band gap of the tunnel junction can result in an increase of the subthreshold swing. Adding a \( p^+ \) \( \delta \)-doped SiGe layer between the \( p^+ \) source and insulating region in an n-channel TFET can lead to an improved (lower) subthreshold swing [5].
As seen in Figure 2-4 adding the $p^+$ SiGe layer causes the conduction band to be lowered while the valence band is raised. This change in band positions results in a decrease of the tunnel width and an improved probability of tunneling. With a $p^+$ SiGe layer added into the n-channel TFET a subthreshold swing of below 60 mV/dec is theoretically possible [5]. The performance increase in p-channel operation mode that results by adding an $n^+$ SiGe layer between the $n^+$ source and insulating region is very small. This is due to the fact that by adding the $n^+$ SiGe layer only the valence band is raised [5]. The conduction band is not affected by the $n^+$ SiGe layer. The tunnel width is determined by the conduction band edge in the $n^+$ source and the valence band in the silicon channel [5]. As the conduction band is not lowered, the tunneling width is not reduced.

As seen in Eq. 2-6 there is no direct temperature dependence in the expression for subthreshold swing. The only temperature dependence that exists is the small temperature dependence associated with $E_g$. The temperature dependence of the $E_g$ is seen in Eq. 2-7 [4].
\[ E_g(T) = E_g(T) - \frac{\alpha T^2}{T + \beta} \] (2-7)

where \( \alpha \) and \( \beta \) are fitting constants and \( T \) is temperature. The effect of temperature on the \( E_g \) is negligible. This very weak temperature dependence on subthreshold swing distinguishes the TFET from the conventional MOSFET. The subthreshold swing of a MOSFET device cannot be scaled below 60 mV/dec, due in part to the MOSFET subthreshold swing’s strong dependence on temperature. The subthreshold swing of a MOSFET is given by Eq. 2-8 [4].

\[ S_{MOSFET} = \ln(10) \cdot \left( \frac{nkT}{q} \right) \] (2-8)

The subthreshold swing of a MOSFET is a function of temperature. The \( n \) term is a “geometry parameter” generally assumed to be at least equal to one and may range up to 1.5 [4].

The threshold voltage of the TFET can be defined several ways. The constant current method assumes that the TFET is on at a certain current value of \( I_{DS} = 10^{-7} \text{ A}. \) The gate voltage to this defined current value is the threshold voltage. However this current value is an arbitrary value with “no physical meaning” [11]. Another definition of threshold voltage is the gate threshold voltage \( V_{TG} \). The gate threshold voltage is based upon the transconductance change method. The transconductance change method defines the threshold voltage as the voltage which corresponds to the maximum of the
transconductance derivative, \( \frac{d g_m}{d V_{GS}} \) [11]. Another threshold voltage definition is the drain current threshold voltage. The drain current threshold voltage \( V_{TD} \) is also based on the transconductance change method, where the \( V_{TD} \) corresponds to the maximum of the transconductance derivative, \( \frac{d g_m}{d V_{DS}} \) [11]. The drain current threshold voltage method uses the fact that there needs to be a small voltage on the drain for the device to be on. This minimum drain voltage comes from the fact that the barrier width of the TFET is a function of both \( V_{GS} \) and \( V_{DS} \) [11].

Figure 2-5 shows \( V_{TG} \) and \( V_{TD} \) extracted from the \( I_{DS}–V_{GS} \) and \( I_{DS}–V_{DS} \) curves using the transconductance method. Plots A and C show \( I_{DS}–V_{GS} \) and \( I_{DS}–V_{DS} \) curves for a simulated TFET. Plots B and D shows the corresponding transconductance and transconductance derivatives. Using the transconductance method for the same device, the
$V_{TD}$ was found to be 0.5 V, which was less than the $V_{TG}$ of 1.1 V. This relationship indicates that the TFET is more sensitive to the changes in the drain voltage than the gate voltage.

One of the main limitations associated with a TFET is a low on-state current $I_{on}$. This low $I_{on}$ is due to the band-to-band tunneling carrier injection mechanism. As the potential between the source and channel increases the band-to-band tunneling current is less sensitive to the electric field [2]. Past the subthreshold region it is difficult to achieve high $I_{on}$. There are several TFET device parameters that can be optimized to increase $I_{on}$. These parameters include lowering the bandgap of the material, adjusting the source doping profile to be more abrupt, lowering the equivalent oxide thickness (EOT), and the use of a double gate. The use of a lower bandgap material will improve the $I_{on}$ since the tunneling current density is exponentially dependent on the bandgap as seen in Eq. 2-1. For a Si-based device, adding a SiGe layer in the source region will increase the band-to-band tunneling. Adding a SiGe layer to the entire active region will also increase $I_{on}$. However adding a SiGe layer to the entire active region will also increase the $I_{off}$. This increase in off-state current will lower the $I_{on}/I_{off}$ current ratio[2]. The effect of a lower bandgap makes III-V materials an attractive option for TFETs.

For a TFET, an abrupt junction profile helps to increase $I_{on}$ by decreasing the tunnel barrier width. This decrease in tunnel barrier width results in an increase in tunneling probability. The addition of another gate on the TFET can lead to a doubling of the $I_{on}$ [12]. A lower EOT leads to higher on-state current by increasing the coupling between the gate voltage and the channel potential [2]. The use of high-κ dielectrics for
the gate oxide allows for the reduction of the EOT. Simulations of the TFET and different dielectrics show the improvement in $I_{on}$ with the introduction of high-$\kappa$ dielectrics [2].

A majority of the published research on TFETs has been in the realm of simulations [1, 5, 10, 12-14]. The conclusions of these simulations have to be viewed with a certain degree of suspicion. The models that these simulations utilize have not been calibrated with experimental data. Dr. Boucart in her thesis summed up the issue with the current simulation tools.

“After the experience of using Silvaco Atlas for five years, I believe that the non-local BTBT model gives good relative results when parameters are varied. For example, when the gate dielectric constant is changed, we can get an idea of how much the on-current will change relative to some reference device. On the other hand, the absolute values of on-current, subthreshold swing, and threshold voltage, are not calibrated. The on-current could be mis-estimated by two or more orders of magnitude. This is an understandable situation when simulating emerging devices, that for the moment still lack the adequate experimental data necessary to calibrate these tools.” [1]

Experiential studies are needed in order to provide the data necessary for TFET model calibration.

2.2 Experimentally Demonstrated TFETs:

A few groups have experimentally demonstrated TFETs. One of the earliest reported TFETs was a gated $p-i-n$ structure from Uemura et al. [15]. Uemura et al. referred to their device as a Channel Doped Surface Tunnel Transistor (CD-STT). Their
device as shown in Figure 2-6 was a GaAs \( p-i-n \) mesa with a GaAs/AlGaAs regrown gate along the mesa edge. The structure layers were grown via Molecular Beam Epitaxy (MBE). The channel region of the device was directly doped with donors to improve the peak tunneling current density to 3.7 \( \mu A/\mu m \) and enable a Peak-to-Valley Current Ratio (PVCR) of 1.5 [15].

![Figure 2-6: Channel Doped Surface Tunnel Transistor (CD-STT) Electrical Performance and Structure][1]

The CD-STT exhibited Negative Differential Resistance (NDR) and gate modulation of the tunneling current. The NDR is indicative that tunneling is the current transport mechanism. The shift in the I-V curves as the gate voltage is varied is indicative of gate control.

Mookerjea \textit{et al.} demonstrated a similar sidewall gated mesa approach to a TFET [16]. The Mookerjea device was an InGaAs based device with an Al\(_2\)O\(_3\) and Pt/Au gate stack along the edge of the mesa.
As seen in Figure 2-7 the Mookerjea et al. structure also demonstrated NDR and gate control of the tunneling current. The Mookerjea et al. device had a peak $I_{on}$ of 20 $\mu$A/$\mu$m and an off current at $V_{DS} = 50$ mV of 40 pA/$\mu$m [16]. The subthreshold swing was found to be 150 mV/dec.

Choi et al. fabricated a 70 nm n-channel silicon TFET on silicon-on-insulator (SOI) substrate [2] at room temperature. Their device used the SOI layer as the insulating region between the $p^+$ source and the $n^+$ drain. The channel length of the device was determined by the length of the SOI region. Figure 2-8 shows a SEM cross-section of the device.
The Choi TFET showed a sub-60 mV/dec subthreshold swing; however, the $I_{on}$ of the device was low. The electrical performance of the Choi TFET can be seen in Figure 2-9.

The $I_{on}$ of the device was measured at 12.1 µA/µm while the $I_{off}$ was measured at 5.4 nA/µm. The value of $I_{on}$ was found to be low compared to a conventional MOSFET.
The value of $I_{off}$ for the device was found to be larger than expected for a TFET. The larger $I_{off}$ is attributed to drain-to-gate leakage current [2].

The similarity between these devices is a gated mesa sidewall approach. The vertical mesas are a result of the MBE to grow highly doped and ultra sharp junctions. All of the mesas are formed during an isolation etch. The isolation etch is often a crystallographic wet etch. The etch results in a sloped profile along the mesa. While this structure allows for the alignment of the gate along the junction it also results in a large overlap of the gate to the drain of the device. This gate overlap as seen in Figures 2-6 and 2-8 result in a gate-to-drain leakage current. This leakage current results in a lower $I_{off}$. Further adding to the drain-to-gate leakage current is the thin gate oxide. Since the gate oxide is also used to separate the gate and drain, as the gate oxide is thinned down to improve gate control the overlap between the gate and drain becomes more serious. A solution to this problem is the addition of a barrier layer on top of the drain [15]. This barrier layer helps further isolate the gate from the drain. The barrier layer can be selectively etched to allow for contact to the drain. The barrier layer is one of several design considerations that need to be made for a TFET.

2.3 Esaki Diode

Esaki diodes are tunnel diodes with a very abrupt and degenerately doped pn or p-i-n junction. The general difference between an Esaki diode and a TFET is that the Esaki diode lacks a gate across the junction and a thinner i-region. This thin abrupt junction causes the conduction bands of the two doped regions to overlap. This overlap allows for tunneling between the two regions when a small biased is applied. An applied reverse
bias on the Esaki diode results in Zener tunneling. When a forward bias is applied there is a forward tunneling component where the current increases with forward bias. At a certain point the current drops as forward bias is increased. The maximum current value before the current begins to decrease is referred to as the peak tunneling current. The current continues to degrade as the voltage is increased until the forward applied bias reaches a certain value where the current will begin to increase again. The minimum current before the current begins to increase again is referred to as the valley current. The region where forward bias is increased yet the current decreases is referred to as negative differential resistance. Negative differential resistance is a key characteristic of an Esaki diode. In this region of negative differential resistance, tunneling is the main current transport mechanism. The current decreases as forward bias is applied due to the conduction bands passing each other as the forward bias is increased. As the conduction bands separate from each other the degree of tunneling decreases. Following the valley point diffusion current is the current transport mechanism. Figure 2-10 shows these different regions of operation for an Esaki diode as current is plotted against voltage.
Esaki diode performance is evaluated utilizing the Peak-to-Valley Current Ratio (PVCR). A high PVCR is desirable for logic applications and noise margin performance. The higher the PVCR the more robust a device is against noise in the input signal. In general for logic applications a PVCR of 2.0 is needed. The PVCR is the ratio of the peak tunneling current to the lowest tunneling current when forward bias is applied to an Esaki diode. Eq. 2-9 shows the equation used to calculate PVCR.

\[
PVCR = \frac{J_p}{J_v}
\]  

(2-9)

As seen in Figure 2-10, the peak tunneling current is the max current at the onset of negative differential resistance; the valley current is the current level when diffusion currents begin to be responsible for carrier transport. Where \(J_p\) is the peak current density and \(J_v\) is the valley current density.
Chapter 3
Process Details

This work utilizes two different process approaches to study tunneling devices. The mesa-first process has been developed to fabricate TFETs and gated tunneling devices. The metal-first process has been used to fabricate sub-micron Esaki diodes [3], the result of the metal-first process will be used as a baseline to compare with the mesa-first process. Both approaches rely on creating a mesa out of a heavily doped p-i-n layer. These mesas become the individual tunneling devices. The metal-first process defines the mesa by first depositing a metal contact and then using this contact as the etch mask for the mesa. The mesa-first process differs in that a removable etch mask is used to define the mesa. The removable mask allows for the sidewalls of the mesa to be easily gated. The sidewall gate runs across the vertical p-i-n junction, thus adding control to a tunnel junction. Section 3.1 will detail every step of the mesa-first process flow. Section 3.2 will detail the metal-first Esaki diode process used to calibrate the tunneling structures. Section 3.3 will review the TFET layout developed for this process.
3.1 **Mesa-First Process Flow**

The mesa-first process was designed to be flexible across multiple material systems: InGaAs, SiGe, GaSb, and InAs. These different material systems have individual requirements for example; compatible contact materials and temperature limits. Therefore individual process steps may differ for different material systems. This process was originally developed for InGaAs. The process steps listed below correspond to InGaAs based devices. The modular nature of this process means that it can be easily adapted to multiple material systems. All that is needed is a check of material compatibility, etch chemistry, and thermal budget constraints.

3.1.1 **Surface Preparation**

A clean surface is critical for the mesa-first process flow. The individual samples that the devices are fabricated on average 0.6 x 0.7 cm in dimension. These samples are cleaved from a wafer with a $p$-$i$-$n$ junction epitaxially grown on top of an InP substrate. Cleaving a sample results in particles on top of the device surface. These may cause defects in subsequent lithography and etch steps. A post-cleave IPA rinse is used to clean the top of the sample. If there is no sacrificial layer to be stripped from the top of the sample, it is ready for the first lithography step.

A $p$-$i$-$n$ layer structure may be grown with an undoped etch cap. This undoped cap serves as a sacrificial layer to protect the top of the $p$-$i$-$n$ junction. Typically an InP etch cap is used for an InGaAs-based device. The InP etch cap allows it to be selectively etched away from the InGaAs device. This etch cap may also be used as an isolation layer
between the gate and the drain of the device. The InP etch cap etch is removed in an HCL:H₂O (1:1) solution. The HCL:H₂O (1:1) is selective to the InGaAs [17]. To verify that the etch cap is completely removed a simple ohmmeter may be used. The undoped etch cap typical measures in the MΩ range while the top of the device structure is in the tens of Ω range.

3.1.2 Mesa Definition Lithography

The first lithography step is the most critical as it defines the TFET mesas. The lithography is performed on a LEO EVO 50 Scanning Electron Microscope (SEM) with the Nanometer Pattern Generation System (NPGS). This direct write Electron Beam Lithography (EBL) system was used to define the mesas in MaN 2401. MaN 2401 is an electron-beam-sensitive negative resist which, when exposed, developed, and cured, is resistant to etch chemistry and is removable by an O₂ plasma.

Mesa lithography begins with the sample being first submerged in SurPass 3000 for 30 seconds. The sample is then rinsed in deionized water for 30 seconds. The samples are then spun dry at 1500 RPM for 30 seconds. The MaN 2401 resist is then applied and spun coat at 1500 RPM for 60 seconds. The sample is then baked at 90°C for 60 seconds. The sample is then mounted to the SEM’s sample holder. Special attention must be given to the cleanliness of the sample holder and the back of the sample. As the sample is secured to the mount, any macroscopic particle on the back of the sample or piece holder may cause the sample to break. The first level EBL defines a series of mesas ranging from mask-defined widths of 150 nm to 2μm. Table 3-1 contains the magnification, spacing, and dose information for resolving 150 nm features in MaN 2401 resist.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnification</td>
<td>150X</td>
</tr>
<tr>
<td>Center-to-Center Spacing</td>
<td>56.20 nm</td>
</tr>
<tr>
<td>Line Spacing</td>
<td>56.20 nm</td>
</tr>
<tr>
<td>Dose</td>
<td>210 µC/cm²</td>
</tr>
<tr>
<td>Mask Level</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 3-1: Level 1 Electron Beam Lithography Job Parameters

Following exposure the sample is developed in a bath of CD-26 developer for 60 seconds. A subsequent develop step in a new bath of CD-26 is performed for 15 seconds. The sample is rinsed and dried. Following a microscope inspection the piece is baked at 100°C for 60 seconds. Figure 3-1 shows a cross section of the device after mesa definition lithography.

### 3.1.3 Mesa Etch

The mesa etch for InGaAs is a wet etch utilizing citric acid (C₆H₈O₇). The etch chemistry is C₆H₈O₇:H₂O:H₂O₂ (20:20:1). The etch rate is dependent on the layer structure of the device and the doping of the individual layers. Undoped layers will etch at a slower rate than doped regions. Profilometry measurement before, during and after the etch are taken to calculate etch rates and a final etch depth. Figure 3-2 shows the cross section of the device after the mesa etch.
3.1.4 MaN Resist Strip

Following the mesa etch the MaN 2401 resist mask is removed. The mask is removed via oxygen plasma etch. The Lam 490 AutoEtch was utilized to remove the MaN 2401 resist. The plasma recipe developed for this etch uses 100 sccm of O₂ at a power of 100 W. Table 3-2 contains the full etch recipe details. Figure 3-3 shows the cross section of the device after the resist etch. SEM inspection is utilized to verify that the MaN resist has cleared.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure</td>
<td>300 mtorr</td>
</tr>
<tr>
<td>Gap Spacing</td>
<td>1.65 cm</td>
</tr>
<tr>
<td>O₂ Flow</td>
<td>100 sccm</td>
</tr>
<tr>
<td>RF Power</td>
<td>100 W</td>
</tr>
<tr>
<td>Time</td>
<td>2 minutes</td>
</tr>
</tbody>
</table>

*Table 3-2: MaN 2401 Strip Etch Recipe - LAM 490 AutoEtch*
The resist strip was found to fully clear most of the resist. However it was found that the MaN resist was susceptible to contamination. For example if the MaN resist is not fully cured and exposed to chlorine-based chemistry such as HCl, the resist forms a residue that is difficult to remove. Figure 3-4 shows the residue remaining after a plasma treatment.

To fully remove this resist residue, fluorine was added to the plasma etch chemistry. A plasma etch of O$_2$:SF$_6$ (5:1) at 100 W was found to fully clear the resist.
3.1.5 Gate Stack Deposition

The TFET gate stack is deposited through Atomic Layer Deposition (ALD) and reactive sputtering. The gate stack consists of a high-k dielectric and a refractory gate metal. The main limitation in this body of work was the lack of ALD onsite at Rochester Institute of Technology. The ALD deposition performed in this work was done at The Pennsylvania State University and at SEMATECH. Al₂O₃ is deposited as the gate oxide through the ALD. The gate oxide thickness is targeted at 6-10 nm.

The refractory gate metal was deposited either by ALD deposition or via a reactive sputtering. TaN and TiN are used as the gate metal. An ALD gate metal such as TiN has an advantage in that it is deposited after the gate oxide without having to break vacuum. This helps ensure a high quality metal dielectric interface. However, the TiN that is deposited via ALD is limited in thickness to between 10 nm and 100 nm. ALD-deposited TiN requires a subsequent deposition of a much thicker material for a gate contact. For this role TaN can be reactively sputtered. Further, if ALD gate metal is unavailable TaN can serve as the gate metal. These two methods for gating are shown in Figure 3-5.
Gate process flow one calls for the deposition of Al₂O₃ followed by deposition of TiN using ALD. An EBL lift-off process is used to define where TaN will be reactively sputtered to add more gate material. This second level EBL step defines the shape and location of the gate. For the EBL lift-off process a LOR5A PMMA resist stack is coated using the spin recipe listed in Table 3-3.
<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Spin Speed [RPM]</th>
<th>Time [Seconds]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><strong>Apply LOR5A</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2a)</td>
<td>Spin Coat LOR5A – Ramp</td>
<td>0-500</td>
<td>2</td>
</tr>
<tr>
<td>2b)</td>
<td>Spin Coat LOR5A – Steady State</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>2c)</td>
<td>Spin Coat LOR5A – Ramp</td>
<td>500-4000</td>
<td>2</td>
</tr>
<tr>
<td>2d)</td>
<td>Spin Coat LOR5A – Steady State</td>
<td>4000</td>
<td>45</td>
</tr>
<tr>
<td>3</td>
<td><strong>Apply PMMA</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4a)</td>
<td>Spin Coat PMMA – Ramp</td>
<td>0-500</td>
<td>2</td>
</tr>
<tr>
<td>4b)</td>
<td>Spin Coat PMMA – Steady State</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>4c)</td>
<td>Spin Coat PMMA – Ramp</td>
<td>500-4000</td>
<td>2</td>
</tr>
<tr>
<td>4d)</td>
<td>Spin Coat PMMA – Steady State</td>
<td>4000</td>
<td>45</td>
</tr>
</tbody>
</table>

Table 3-3: Gate Level EBL LOR5A/PMMA Resist Coat Recipe

The PMMA/LOR5A resist stack is then baked at 180°C for 10 minutes. The sample is then mounted on a piece holder and loaded into the SEM. The second level alignment and electron beam lithography is performed using the NPGS system. Table 3-4 contains the magnification spacing information and dose information.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnification</td>
<td>150X</td>
</tr>
<tr>
<td>Center-to-Center Spacing</td>
<td>56.20 nm</td>
</tr>
<tr>
<td>Line Spacing</td>
<td>56.20 nm</td>
</tr>
<tr>
<td>Dose</td>
<td>300 µC/cm²</td>
</tr>
<tr>
<td>Mask Level</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 3-4: Gate Level Electron Beam Lithography Job Parameters

The TaN reactive sputter is performed using the PE4400 using the deposition recipe as outlined in Table 3-5, with a deposition time of 20 minutes. Submerging the sample in a heated bath of Remover PG then lifts off the excess TaN. Following the lift off the exposed TiN is etched using a CF₄ plasma. The exposed Al₂O₃ is etched away in a 50:1 HF bath for 1 minute.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target Material</td>
<td>Tantalum</td>
</tr>
<tr>
<td>Base Pressure</td>
<td>$1.0 \times 10^{-7}$ Torr</td>
</tr>
<tr>
<td>Deposition Pressure</td>
<td>2 mTorr</td>
</tr>
<tr>
<td>$N_2$</td>
<td>1.85 sccm</td>
</tr>
<tr>
<td>Ar</td>
<td>35 sccm</td>
</tr>
<tr>
<td>Rotation Speed</td>
<td>2.4 RPM</td>
</tr>
<tr>
<td>RF Power</td>
<td>400 W</td>
</tr>
</tbody>
</table>

Table 3-5: PE4400 TaN Sputter Deposition Recipe

The alternative gate process flow or gate process flow two does not incorporate the TiN deposition or etch. The TaN is used directly as the gate metal and is defined and deposited using the same procedure.

3.1.6 Benzocyclobutene (BCB) Deposition

BCB is utilized as an Inter Layer Dielectric (ILD) to support the top contact. This process was developed using BCB from Dow Chemical, CYCLOTENE 3022-35. The BCB was deposited through a spin coat process. For adequate adhesion of the BCB a clean surface is required. The sample surface is first cleaned with an isopropyl alcohol followed by a rinse in deionized $H_2O$ and a dehydration bake. The sample is then treated with the adhesion promoter AP3000. The BCB is then spin coated, followed by a soft bake at 140$^\circ$C for 10 minutes. Table 3-6 contains the spin coat recipe for the BCB.

![Figure 3-6: BCB Deposition](image)
<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Spin Speed [RPM]</th>
<th>Time [Seconds]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><em>Apply AP3000</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Spin Coat AP3000</td>
<td>1000</td>
<td>60</td>
</tr>
<tr>
<td>3</td>
<td><em>Apply BCB</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4a)</td>
<td>Spin Coat BCB – Ramp</td>
<td>0-500</td>
<td>2</td>
</tr>
<tr>
<td>4b)</td>
<td>Spin Coat BCB – Steady State</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>4c)</td>
<td>Spin Coat BCB – Ramp</td>
<td>500-4000</td>
<td>2</td>
</tr>
<tr>
<td>4d)</td>
<td>Spin Coat BCB – Steady State</td>
<td>4000</td>
<td>2</td>
</tr>
<tr>
<td>4e)</td>
<td>Spin Coat BCB – Ramp</td>
<td>4000-5000</td>
<td>2</td>
</tr>
<tr>
<td>4f)</td>
<td>Spin Coat BCB – Steady State</td>
<td>5000</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 3-6: BCB Spin Coat Recipe

Following the spin coat, the BCB is cured in a two-part bake procedure. During the cure it is critical that the BCB is not heated above 150°C in an oxygen ambient. At temperatures above 150°C, the BCB in the presence of oxygen can oxidize. The sample is first baked on a hot plate for 10 minutes at 140°C to help set the BCB. The BCB is then cured at 250°C for 1 hour in the Blue M box oven with a nitrogen ambient. The sample is loaded into the oven at a temperature of 140°C. The piece is held at a soak of 140°C for 10 minutes with nitrogen flowing. The temperature is then ramped to 250°C and then held at 250°C for 1 hour. Following the 1-hour cure the temperature is ramped down to 140°C before the piece is removed. Figure 3-6 shows the cross section of the device following the BCB coat.

A blank silicon piece of similar size should be co-processed during this step. This silicon piece is coated with BCB and baked with the device sample. This piece is used to calibrate BCB etch rates for subsequent steps.
3.1.7 BCB Etch Back

The BCB process results in a significant amount of overburden. This overburden inhibits contacting the top of the mesas. The BCB is thus etched back to clear the top of the mesa. The BCB is etched back in an O\textsubscript{2}: SF\textsubscript{6} (4:1) plasma. The etch rate is dependent on the power used and the BCB cure cycle. Slight variations in the BCB cure cycle can cause the etch rate to vary by 20\%. The BCB etch is performed in the Lam 490 AutoEtch using the etch recipe describe in Table 3-7.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure [mtorr]</td>
<td>300</td>
</tr>
<tr>
<td>Gap Spacing [cm]</td>
<td>1.65</td>
</tr>
<tr>
<td>O\textsubscript{2} Flow [sccm]</td>
<td>80</td>
</tr>
<tr>
<td>SF\textsubscript{6} Flow [sccm]</td>
<td>20</td>
</tr>
<tr>
<td>RF Power [W]</td>
<td>25-50</td>
</tr>
<tr>
<td>Time [minutes]</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 3-7: BCB Etch Back Lam 490 AutoEtch Recipe

The BCB etch back begins with a calibration of etch rates using the BCB coated silicon test piece. The BCB thickness on the silicon piece is measured with a Nanospec, by setting the Index of Refraction (n) to 1.54. The BCB silicon test piece is then etched for 1 minute at 50 W. The remaining BCB thickness is measured and the etch rate for 50 W is calculated. The BCB is then etched for a minute at 25 W. The remaining BCB thickness is measured and the etch rate for 25 W is calculated. These two etch rates will be used to calculate the BCB etch time for the device sample.

The BCB thickness on the device sample is measured using a point between different die. With the BCB thickness data, the measured mesa height, and the previously calculated etch rates, the time needed to etch the BCB to just above the top of the mesa is calculated. Generally a 50 W etch is used for this first etch step. Nanospec measurements
are then taken to verify the thickness of remaining BCB. A second etch at 25 W is used to place the final BCB thickness a few nm below the top of the mesa. The calibrated 25 W etch rate along with the remaining BCB thickness and the mesa height is taken into account to calculate the second etch time. Figure 3-7 shows the cross section of the device after the BCB etch back.

![Figure 3-7: BCB Etch Back](image)

Following the second etch measurements are taken with the Nanospec to verify the final BCB thickness. To insure that the BCB has cleared the top of the mesas, the samples are placed in the SEM. The criterion for a successful etch back is a final BCB thickness less than the top of the mesa but 10 nm above the top of the $i$-region. This insures that the BCB is sufficiently isolating the junction. If the BCB was over-etched a plasma etch is performed to completely remove the BCB and the sample is reworked.

### 3.1.8 BCB Via Etch Lithography

The BCB is now isolating the top of the device from the $i$-region, the gate contact and the substrate. Vias through the BCB are needed to contact gate and the substrate. The vias are etched using the similar plasma etch as the BCB etch back. This via etch uses a
LOR5A/PMMA resist mask as etch mask. The LOR5A and PMMA are spin coated using the recipe listed in Table 3-8.

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Spin Speed [RPM]</th>
<th>Time [Seconds]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><em>Apply LOR5A</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2a)</td>
<td>Spin Coat LOR5A – Ramp</td>
<td>0-500</td>
<td>2</td>
</tr>
<tr>
<td>2b)</td>
<td>Spin Coat LOR5A – Steady State</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>2c)</td>
<td>Spin Coat LOR5A – Ramp</td>
<td>500-4000</td>
<td>2</td>
</tr>
<tr>
<td>2d)</td>
<td>Spin Coat LOR5A – Steady State</td>
<td>4000</td>
<td>45</td>
</tr>
<tr>
<td>3</td>
<td><em>Apply PMMA</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4a)</td>
<td>Spin Coat PMMA – Ramp</td>
<td>0-500</td>
<td>2</td>
</tr>
<tr>
<td>4b)</td>
<td>Spin Coat PMMA – Steady State</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>4c)</td>
<td>Spin Coat PMMA – Ramp</td>
<td>500-4000</td>
<td>2</td>
</tr>
<tr>
<td>4d)</td>
<td>Spin Coat PMMA – Steady State</td>
<td>4000</td>
<td>45</td>
</tr>
</tbody>
</table>

Table 3-8: BCB Via Etch LOR5A/PMMA Resist Coat Recipe

The PMMA/LOR5A resist stack is then baked at 180°C for 10 minutes. The sample is then mounted on a piece holder and loaded into the SEM. The via etch level alignment and electron beam lithography is performed using the NPGS system. Table 3-9 contains the magnification spacing information and dose information.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnification</td>
<td>150X</td>
</tr>
<tr>
<td>Center-to-Center Spacing</td>
<td>56.20 nm</td>
</tr>
<tr>
<td>Line Spacing</td>
<td>56.20 nm</td>
</tr>
<tr>
<td>Dose</td>
<td>300 μC/cm²</td>
</tr>
<tr>
<td>Mask Level</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 3-9: Level 3 Electron Beam Lithography Job Parameters

Following exposure the piece is developed in MIBK:IPA 1:3 for 2 minutes. A subsequent develop step in a new bath of CD-26:H₂O (1:1) is performed for 2 minutes. A final develop in CD-26 for 10 seconds is performed. The sample is rinsed and dried. Figure 3-8 shows the cross-section of the device after via etch lithography.
3.1.9 BCB Via Etch

The BCB via etch is performed using the Lam 490. The via plasma etch chemistry is the same etch as that which is used for the etch back. The etch recipe for the via etch can be found in Table 3-7, with the etch being performed at 50 W. The etch time is determined by the remaining BCB thickness and the previously calculated etch rates. In general this etch is on the order of a few seconds. Following the etch Nanospec measurements are taken within the via etch to verify that the remaining BCB is gone. Dark-field microscope inspection is also useful in verifying that the remaining BCB is removed from the vias. Once it is verified that the vias are clear, the sample is placed in a bath of Remover PG for 5 minutes. The Remover PG removes the remaining resist etch mask. Figure 3-9 shows the cross section of the device following this procedure.
3.1.10 Contact Metal Lithography and Deposition

Gold (Au) is utilized as the contact metal for the InGaAs based device. The first step is to define the regions where the contact metal will be deposited through an EBL lift-off process. This process uses a LOR5A/PMMA resist stack. The LOR5A is spin coated twice followed PMMA. The spin coat the recipe is listed in Table 3-10.

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Spin Speed [RPM]</th>
<th>Time [Seconds]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Apply LOR5A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2a)</td>
<td>Spin Coat LOR5A – Ramp</td>
<td>0-500</td>
<td>2</td>
</tr>
<tr>
<td>2b)</td>
<td>Spin Coat LOR5A – Steady State</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>2c)</td>
<td>Spin Coat LOR5A – Ramp</td>
<td>500-4000</td>
<td>2</td>
</tr>
<tr>
<td>2d)</td>
<td>Spin Coat LOR5A – Steady State</td>
<td>4000</td>
<td>45</td>
</tr>
<tr>
<td>3</td>
<td>Apply LOR5A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4a)</td>
<td>Spin Coat LOR5A – Ramp</td>
<td>0-500</td>
<td>2</td>
</tr>
<tr>
<td>4b)</td>
<td>Spin Coat LOR5A – Steady State</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>4c)</td>
<td>Spin Coat LOR5A – Ramp</td>
<td>500-4000</td>
<td>2</td>
</tr>
<tr>
<td>4d)</td>
<td>Spin Coat LOR5A – Steady State</td>
<td>4000</td>
<td>45</td>
</tr>
<tr>
<td>5</td>
<td>Apply PMMA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6a)</td>
<td>Spin Coat PMMA – Ramp</td>
<td>0-500</td>
<td>2</td>
</tr>
<tr>
<td>6b)</td>
<td>Spin Coat PMMA – Steady State</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>6c)</td>
<td>Spin Coat PMMA – Ramp</td>
<td>500-4000</td>
<td>2</td>
</tr>
<tr>
<td>6d)</td>
<td>Spin Coat PMMA – Steady State</td>
<td>4000</td>
<td>45</td>
</tr>
</tbody>
</table>

Table 3-10: Contact Metal Lithography LOR5A/PMMA Resist Coat Recipe

The PMMA/LOR5A resist stack is then baked at 180°C for 10 minutes. The sample is then mounted on a piece holder and loaded into the SEM. The contact level EBL is
performed using the NPGS system. Table 3-11 contains the magnification spacing information and dose information.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnification</td>
<td>150X</td>
</tr>
<tr>
<td>Center-to-Center Spacing</td>
<td>56.20 nm</td>
</tr>
<tr>
<td>Line Spacing</td>
<td>56.20 nm</td>
</tr>
<tr>
<td>Dose</td>
<td>300 µC/cm²</td>
</tr>
<tr>
<td>Mask Level</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 3-11: Level 4 Electron Beam Lithography Job Parameters

Following exposure the piece is developed in MIBK:IPA 1:3 for 2 minutes. A subsequent develop step in a new bath of CD-26:H₂O (1:1) is performed for 2 minutes. A final develop in CD-26 for 10 seconds is performed. The sample is rinsed and dried.

The sample is then loaded into the Nano 38 thermal evaporator. For the contact metal 2000 Å of Au is deposited. The sample is then placed into a heated bath of Remover PG. After the Au is lifted off the piece is placed into another bath of Remover PG. This second bath is utilized to remove any lift-off resist residue. Figure 3-10 shows the cross section of the device after Level 3 lithography and Au deposition. The device after this point is ready for test.
3.2 Metal-First Esaki Diode Process Flow

The metal-first Esaki diode process utilizes EBL to fabricate a series of small diameter devices between 100 nm and 40 micron. This approach can be seen in Figure 3-11. The process utilizes an (a) E-beam lift-off lithography process to define the initial gold contacts. This is followed by (b) wet isolation etch utilizing the gold contact as an etch mask. (c) Bisbenzocyclobutene (BCB) is coated to isolate the tunnel diodes and support the gold contacts. (d) The BCB is plasma-etched back to remove the overburden. (e) The sample is then coated with LOR5A and PMMA. (f) The sample is aligned and second level lithography is performed to define larger probe contacts. Following a gold contact deposition the remaining gold is lifted off.
The metal-first process shares many features with the mesa-first process. While using different mask designs, the process modules are the same. Table 3-12 highlights the corresponding process modules and changes between the two processes.
<table>
<thead>
<tr>
<th>Metal-first Process</th>
<th>Corresponding Mesa-first Process</th>
<th>Amendments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level 1 Metal Definition</td>
<td>Coat &amp; Write conditions from 3.1.8</td>
<td>New Mask File</td>
</tr>
<tr>
<td>Mesa Etch</td>
<td>3.1.3</td>
<td></td>
</tr>
<tr>
<td>BCB</td>
<td>3.1.6</td>
<td></td>
</tr>
<tr>
<td>BCB Etch Back</td>
<td>3.1.7</td>
<td></td>
</tr>
<tr>
<td>Level 2 Metal Definition</td>
<td>3.1.10</td>
<td>New Mask File</td>
</tr>
</tbody>
</table>

Table 3-12: Metal-first Process Details

To extract the electrical performance of the Esaki diodes, a methodical testing approach has been developed. Following the initial wet isolation etch, SEM cross-sections are taken to assess the undercut for each of the different diode sizes. The cross-sections are taken in both etch planes. Top-down SEM measurements are taken across the sample to measure the area of the gold contact. The measurements across the sample allow for e-beam variations to be corrected for in the effective area calculations. The top-down SEM micrographs are put through image-processing routines to calculate the area of the gold contacts. Using the area and undercut profile information, effective device areas are calculated. This corrected area is used in the current density calculations. Following fabrications the devices undergo extensive electrical testing. Data analysis is performed on the IV curves to extract series resistance, contact resistance, $PVCR$, $V_{peak}$, $J_{peak}$ and $V_{valley}$.

### 3.3 Mesa-first TFET Layout

EBL is used to define deep submicron mesas in the $p$-$i$-$n$ structure, the wrap-around gates, via and top contacts. The mask design used for the EBL processes, is defined using Design CAD LT. The mask design is a single file containing all of the layout information for one die. The layout consists of numerous devices, including gated and non-gated devices.
The basic layout for all gated devices is the same. The layout for a single TFET calls for a rectangular mesa. A wrap-around gate is applied across the rectangular mesa. A contact is used to contact the top of the device. For the TFET size of the mesa, the number and area of the gates and contacts is varied. Figure 3-12 shows the masked defined view of a TFET and a cross section of the device corresponding to a cutline through the middle device. This design is based upon four layers, which correspond to the different lithography steps.

![Figure 3-12: Individual TFET Layout](image)

The layout contains four layers. Level 1 defines the mesa and alignment marks used for subsequent lithography steps. Level 2 defines the gate across the mesa. Level 3 defines vias in the BCB to contact the gate and the substrate layers. Layer 4 defines the top contact metal. The whole layout with multiple gated devices, non-gated diodes, and test structures can be seen in Figure 3-13.
As seen in Figure 3-13 each die is centered around alignment “L’s”. These are alignment marks defined during the first level lithography. The NPGS system scans for these alignment marks during later levels to align each individual die. Also situated on the mask design is a series of non-gated diodes. These mesa-first tunnel diodes are used to compare the fabrication process with that of tunnel diodes fabricated using a metal-first scheme. The gated test structure is used to verify that the gate is conformal over the sidewall of the device.
Chapter 4
Process Module Development

This chapter will focus on development of selected process modules needed to fabricate a mesa-first TFET. The following process modules are essential to the mesa-first process and provide additional details beyond what was described in Chapter 3. Section 4.1 will discuss electron beam lithography and alignment. Section 4.2 will cover BCB deposition and curing. Section 4.3 will discuss plasma etch of BCB. Section 4.4 will cover TaN reactive sputtering.
4.1 Electron Beam Lithography

Electron Beam Lithography (EBL) enables the fabrication of nanometer-scale devices without the need for expensive Excimer laser based systems. EBL’s advantages lay in its resolution and flexibility. EBL has resolution limit between 10-20 nm. EBL, unlike optical lithography, does not require a mask to define a pattern. Instead EBL is a direct write process. EBL systems direct an electron beam point by point to define a pattern in an electron-sensitive resist. The lack of a physical mask enables quick prototyping of devices by allowing for easy design changes. However this quick prototyping comes at the cost of EBL’s low throughput. Thus EBL is limited to research and development applications and low-volume production.

The mesa-first process uses EBL for its versatility and its ability to easily write small pieces. Due to the limited supply of III-V semiconductor samples, the individual piece size is limited to 0.6 x 0.7 cm. This small size limits the options for lithography. Optical projection-based steppers require special piece chucks to secure such small samples. The NPGS EBL system at RIT where this work was performed already has the capability to write on small pieces. NPGS is a standalone system, which modifies the LEO EVO 50 SEM and transforms it into an EBL system. NPGS works by controlling the stage movements and the blanking of the electron beam to write the specified patterns.

Overlay precision is critical for the mesas first process. At the second level and beyond, EBL is dependent on proper alignment. NPGS has the capability to perform automatic and assisted manual alignment. To do so NPGS requires the DesignCad mask file, alignment spacing information, and clear alignment marks. NPGS reads the Design Cad file for the alignment marks’ shape and locations. The alignment marks that NPGS
looks for are those which were transferred into the sample by previous EBL steps. Using the alignment spacing information, NPGS can automatically search for alignment marks, identify the marks with the mask file, and align the die for the write.

There are two sets of alignment marks utilized for alignment, the global alignment marks and die alignment marks. The global alignment marks are a 3x3 array of crosses used to correct for global rotational errors. The die alignment marks are the four “L” shaped alignment marks that are on the corner of each device die. Figure 4-1 shows how NPGS writes the die and global alignment marks on the sample.

Figure 4-1: Electron Beam Lithography Process
The location of the global alignment marks is determined by the size of the device array. As seen in Figure 4-1 the 3x3 global alignment mark array is aligned to the center of the sample. The device array is offset to be inside the global alignment array. The numbers of columns and rows of the device array are constrained by the size of the die, the spacing between die, and the active area of the sample. These constraints are taken into account per sample to determine the size of the array that will fit within the active area. Eq. 4-1 and Eq. 4-2 show how the global alignment mark spacing is calculated as a function of the device array and the die spacing.

\[
Y_{\text{Global Alignment Spacing}} \ [\mu m] = \frac{\text{Number of Rows} \times Y_{\text{Die Spacing}} [\mu m]}{2} + 300 [\mu m] \tag{4-1}
\]

\[
X_{\text{Global Alignment Spacing}} \ [\mu m] = \frac{\text{Number of Columns} \times X_{\text{Die Spacing}} [\mu m]}{2} + 300 [\mu m] \tag{4-2}
\]

Recording the device array size, die spacing, and corresponding global alignment spacing is critical for second level alignment. The NPGS requires this information to search for the die level alignment marks.

The alignment procedure is two-fold. Using the SEM control, an outer corner global alignment mark is found. A SEM stage move corresponding to the \( Y_{\text{Global Alignment Spacing}} \) is used to bring a center edge global alignment mark into focus. The alignment cross is then centered in the SEM field of view. A stage shift of \( -Y_{\text{Global Alignment Spacing}} \) in the y-axis is performed. The lower alignment mark is centered in the SEM field of view by only adjusting rotation. A stage shift \( +Y_{\text{Global Alignment Spacing}} \) in the y-axis is performed. The
center edge alignment mark is centered in the SEM field of view by using only $x$ and $y$ translational adjustments. The procedure is repeated until a stage shift in either direction results in the global alignment marks being centered in the SEM field of view. The stage is then shifted to the center global alignment cross. The SEM is then handed over to the NPGS system. When the EBL job is started NPGS begins the individual die alignment.

There is an issue with NPGS system at RIT. Since the NPGS is a stand alone system, it requires a separate computer, digital-to-analog converter, and cabling to interface with the SEM. Somewhere in the connection between the SEM and the NPGS controller there is an RC time constant delay with the image capture. The origin of the RC time constant is suspected to be an issue relating to the digital-to-analog converter card on the NPGS system. Figure 4-2 shows the difference between images of an alignment mark from what the SEM natively captures and what the NPGS captures.

![Figure 4-2: Comparison of PMMA LOR5A Coated III-V Mesa Alignment Mark Capture Between SEM and NPGS. 1. LEO EVO 50 Rough Scan. 2. LEO EVO 50 Fine Scan. 3. NPGS Fine Scan.](image-url)
As seen in Figure 4-2 the alignment mark that was imaged was an III-V mesa alignment mark coated with LOR5A and PMMA. Figure 4-2 (1) shows the rough scan of the alignment mark captured just by the SEM. This rough scan is at the fastest scan speed with no image enhancement performed. Figure 4-2 (2) shows the fine scan of the alignment mark. This fine scan was performed at a slower scan speed with a line integration image enhancement routine. Figure 4-2 (3) shows the fine scan that the NPGS system reads from the SEM. The RC time constant causes the edge of the feature to bleed in one direction. Further the contrast between the top of the mesa and the field is lost as the image is transferred from the SEM to the NPGS system. The image deformation and loss of contrast inhibits the ability to align to the feature. The alignment process uses level 1 mask-defined outline of the alignment mark to compare with the image alignment mark. Using the information from the level-one mask, NPGS compares the shape, rotation, and location of the alignment marks to the mask defined. The NPGS system then attempts to correct for translational shift and slight rotational errors to align the individual die. NPGS’s image recognition begins with a scan of the image. The NPGS software will take that scan data and automatically adjust the display contrast. The NPGS system then performs spatial averaging of the pixels and the edge enhancement to detect the alignment mark. The image distortion and poor contrast that is a result of the image transfer from the SEM to the NPGS software inhibits automated alignment. Manual correction is thus needed, making the alignment process very tedious.

To help improve the contrast and alignment mark detection a high contrast material such Gold (Au) can be used. In electron beam imaging the contrast of a material is related to the atomic number. The higher the atomic number or Z number the higher the
number of backscattered electrons. The lower the atomic number of the material the deeper an incident electron can penetrate the sample without scattering. Eventually the electrons will slow down and scatter, however the likelihood of the electrons backscattering into the detector is low. As the atomic number increases the depth of penetration of incident electron is less, increasing the probability of scattering. The higher probability of scattering increases the number of electrons that are backscattered into the detector [18], thus the contrast of the material increases. Au has a high atomic number material of 79. Using Au as an alignment mark as seen in Figure 4-3 can improve the contrast of the alignment mark as seen by the NPGS system.

![Au Alignment Mark](image1.png) ![III-V Mesa Alignment Mark](image2.png)

Figure 4-3: Comparison of PMMA LOR5A Coated Au and III-V Mesa Alignment Marks As Detected By NPGS Utilizing the Secondary Electron Detector

While the Au alignment marks help improve the contrast for alignment there are some issues concerning process compatibility. If Au is used for the initial alignment marks there is a contamination concern during the ALD step. Many ALD systems will not allow Au contaminated samples in for fear of contaminating the process chamber. These ALD systems are also used for silicon-based devices. As Au is a mobile contaminant in silicon there is a fear that the contaminated process chamber will affect succeeding silicon
samples. This contamination fear needs to be considered in the process flow. If Au contamination is not an issue for the ALD, Au could be used for zero-level alignment marks. If Au contamination is a concern it should be completely left out until after the ALD. Following the ALD a second set of alignment marks may be deposited. Another solution involves depositing a more stable metal, such as a refractory metal, as a zero-level alignment mark.

The micrographs taken by the NPGS system in Figure 4-3 were taken using the secondary electron detector on the SEM. Another solution to improve alignment mark recognition without the use of Au is the use of the backscattered electron detector, instead of the secular electron. The backscattered electron detector is mounted direct above the sample. The backscattered electron detector is able to collect the backscatter electrons and determine the sample composition or surface topography. Using the backscattered detector in sample composition mode NPGS is better able to resolve the III-V mesa alignment marks.

![Figure 4-4: Comparison of NPGS III-V Mesa Alignment Marks Recognition, Secondary Electron Detector versus Backscattered Electron Detector](image)

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Figure 4-4 shows the same III-V mesa alignment as captured by the secondary electron detector and the backscattered electron detector. The alignment mark was a III-V mesa with BCB etched backed just below the top of the mesa. No resist was present. The Backscattered electron detector provides better contrast than the secondary electron detector. The same RC delay is present in both images; however with the higher contrast probability of alignment mark recognition is greater. The use of a higher Z number material such as Au as the alignment mark with backscattered electron detector would further improve the contrast.

Without proper alignment the gates and contact fingers can touch each other and short the device.

![Image of misaligned top contact shorting to the gate](image)

*Figure 4-5: Misaligned Top Contact Shorting to the Gate*
Figure 4-5 above shows the result of misalignment during the top contact EBL. The alignment was off by half a micron. The result of this was that the top contact shorts to the gate. Increasing the spacing between the gate and the top contact could have prevented this problem. However the NPGS system is capable of precise submicron overlay. The root cause of this misalignment was alignment mark recognition failure.

4.2 BCB Deposition and Cure

Benzocyclobutene (BCB) is a common material used in III-V semiconductor fabrication to provide a planarization layer and passivate the sidewalls of III-V devices [19]. BCB is used for its low dielectric constant and ability to be easily deposited with low tool contamination risk. BCB has a dielectric constant \(k\) of 2.5 [20], which is lower than the \(k = 3.9\) for silicon dioxide. The use of silicon dioxide with III-V semiconductors requires a Chemical Vapor Deposition (CVD) step. With III-V devices there is a concern that the III-V semiconductor material and Au-based contacts might contaminate the CVD chambers. BCB uses a spin coat process with a relatively low temperature thermal cure process. This reduces the risk of contamination.

BCB layers are generally applied through a spin coating process followed by a curing step. Varying the spin speed affects the thickness of the polyimide coating. The higher the spin speed, the lower the thickness of the polyimide. The ability of the polyimide layer to reduce the surface topography and planarize a surface is given by the Degree of Planarization (DOP) as seen in Eq. 4-1 [21].

\[
\text{DOP\%} = \left(1 - \frac{H_2}{H_1}\right) \times 100
\]

\hspace{1cm} (4-1)
Where $H_2$ is the final step height of the topography features following planarization while $H_1$ is the initial step height of the feature. The degree of planarization is affected by spin speed [22] and the variable factors including molecular weight, cure mechanisms, solvent volatility, solution viscosity, solids content, feature dimensions, processing and cure conditions [23]. A single coat of BCB offers an average degree of planarization of 84% [23]. A two-coat application increases the degree of planarization to an average of 96% [23].

The BCB thermal cure must be carefully performed. For the soft bake which is performed on a hotplate it is critical that the BCB is not heated above 150°C in an oxygen ambient. At temperatures above 150°C in the presence of oxygen the BCB can oxidize. The result of this oxidation is a possible increase in the dielectric constant of the film [24]. The hard bake to fully cure the BCB is done in nitrogen ambient. The concentration of oxygen needs to be below 100 ppm [20]. The BCB cure is dependent on time and temperature; Figure 4-6 contains the manufacturer’s extent of cure versus time and temperature plot. An increase in temperature can result in a decrease in the cure time. Decreasing the temperature results in an increase in the needed cure time. The effect of temperature and thermal budget is important to consider.
It is important to take into effect the temperature of the bake and the material present. With InGaAs-based samples, a bake at 250°C for 1 hour is not an issue. However, for materials like silicon with metals such as Au present, temperature needs to be considered. At these high temperatures the migration of metal could lead to shorting of devices and degraded device performance.

4.3 BCB Plasma Etching – Overburden Etch and Via Etch

The BCB planarization process results in a significant amount of BCB overburden. This overburden is a thick layer that is on top of the isolated device mesa. To make contact to the TFET the overburden needs to be removed. A Reactive Ion Etch (RIE) process is utilized to etch back the BCB and expose the top of the isolated device. The chemistry used for this RIE process is typically fluorine-based. A common BCB etch
process utilizes 5:1 O$_2$/SF$_6$ [22]. Another etch that can be used is an 80% O$_2$ 20% CF$_4$ plasma etch [23]. Fluorine helps to attack the silicon-based BCB and increase the etch rate. Using oxygen plasma without a fluorine component for the etch can result in undesirable amorphous silicon oxide forming on the surface of the BCB. As a result of this the etching process becomes self-passivating, and the etch rate slows down and eventually stops. The resulting SiO$_2$ layer is brittle and can lead to cracking of the BCB film [20].

For this process an O$_2$: SF$_6$ (4:1) plasma etch was utilized to remove the BCB overburden. A heavier fluorine concentration was chosen to reduce the risk of amorphous silicon oxide formation. The plasma etch rate is dependent on the power supplied to the plasma. Screening experiments were performed to get a general etch rate as a function of RF power. As seen in Figures 4-7 and 4-8 the 50 W plasma etch offers the highest average etch rate.

![Figure 4-7: BCB O$_2$: SF$_6$ (4:1) Plasma Etch](image-url)
As seen in Figure 4-7 the individual etch rates for each RF power level are relatively uniform. The average BCB etch rate generally scales evenly with RF power. The average 50 W plasma etch rate is 434 nm/minute. However this etch rate can vary by up to 20% depending on the cure cycle. These variations in etch rate are the result of variations in the cure soak time and temperature. The temperature controller used on the Blue M oven is not precise, resulting in uneven ramp rates and soak temperatures up to 10 degrees above target. The data reflected in Figure 4-7 and 4-8 was obtained from on pieces that were cured at the same time. To overcome the etch rate variations a calibration etch is performed on a co-processed test piece. This allows for an accurate etch rate when planning to etch a particular sample.

Any ILD scheme requires vias to connect second-level metal to the level-1 metal. The BCB via etch was developed by using the same 50 W O₂: SF₆ (4:1) plasma etch used
for the overburden etch back. To enable the via etch a removable etch mask is needed. This etch mask must be able to withstand the plasma etch and then be removable. Many process options were considered however the simplest solution was to use a PMMA/LOR5a resist stack as the etch mask. The PMMA/LOR5A allows for the vias to be defined by EBL, yet the plasma etch will also attack the resist stack. The mask can be used for pattern transfer, due to the differences in thickness and etch rate between the BCB and the PMMA/LOR5A resist stack.

![Figure 4-9: BCB Via Etch Rate](image)

The BCB via etch features as shown in Figure 4-9 were masked-defined as 1000 nm in diameter. After 300 seconds in the plasma etch the BCB via had fully cleared. While the BCB via had been completely cleared there was significant pattern deformation and loss.
of BCB in the masked regions. The resulting via was 2.5 times larger than defined in the mask. Further, the portion of BCB that was masked had been etched. The BCB thickness loss was approximately 1450 nm. This thickness loss is easily attributed to the resist etch mask not holding up to the plasma etch. For very thick BCB thicknesses the PMMA/LOR5A resist stack is not an ideal etch mask. However, for the fabrication of the TFET, 1600 nm of BCB is not needed. After etch back the BCB thickness is only about 100 nm. The plasma etch required to clear 100 nm is approximately 20 seconds. The PMMA/LOR5A resist mask can easily withstand this short time in the plasma etch.

### 4.4 TaN Gating Development

Gating the TFET is a challenge, especially with III-V based devices. Silicon has an advantage in its ability to grow a thermal oxide. III-V materials do not have this ability; thus, an ALD high-k dielectric is needed. For the gate metal, material compatibility is a concern. Refractory metals are often used with III-V semiconductors for their low resistivity and low diffusivity. The low diffusivity enables refractory metals to avoid gate sinking effects [25]. In III-V Metal Semiconductor Field Effect transistors (MESFET) and High Electron Mobility Transistors (HEMT) sinking gates are the result of gate metal diffusion into the channel of the device. [26] The metal diffusion results in reduced effective channel length, increased channel resistance, and a higher pinch-off voltage [26]. TaN and TiN are refractory alloys that have been demonstrated as gate metals in InGaAs based MOSFETs [27]. For this work a TaN lift-off process was developed. A lift-off process was used in preference to a blanket deposition and dry etch of TaN as a gate metal.
due to the risk of the dry etch potentially deteriorating the insulating high-k dielectric and the high-k/InGaAs interface [27].

The TaN gate metal is deposited via RF reactive sputtering. The reactive sputter involves sputtering from a Ta target in a N₂/Ar RF plasma. The N₂ reacts with Ta, forming TaN. The composition of the TaN is determined by the pressure in the process chamber and the flow of Ar and N₂. The stoichiometry of the TaN is controlled by varying the flow of the N₂ relative to Ar. Figure 4-10 shows how the relative gas flows affect the composition of the TaN film.

![Figure 4-10: TaN Composition, Resistivity, and Sputter Rate as Function of Gas Mixture][28]

The TaN film developed for this process was chosen to be a low resistivity film; therefore the ratio of N₂ to Ar+N₂ was selected to be 0.05. The reactive sputter was performed in a
PE4400, as it had an average base pressure of $1.5 \times 10^{-7}$ Torr. The deposition pressure was set at 2 mTorr with 1.85 scm of N$_2$ and 35 scm of Ar flowing. The reactive sputter was performed at a power of 400 W. A series of runs were performed with these process conditions at varied times. The resulting film thickness versus time is shown in Figure 4-11.

![Figure 4-11: PE4400 TaN Deposition Thickness at 400 W](image)

As seen in Figure 4-11 the average deposition rate for 400 W was about 2.25 nm per minute. There is some variation in the deposition rate for the multiple treatment combinations performed at 3.5 minutes. This variation in deposition rate corresponds to additional revolution though the plasma. The PE4400 is set up such that the exposed target and plasma only form a portion of the process chamber. The sample platen rotates though the plasma at a given speed to insure a uniform coat across the samples. Every time a given sample rotates through the plasma, target material is sputtered onto the sample.
Depending on how the sample is loaded into the PE4400 the number of rotations through the plasma can vary by up to one rotation for the same given time.
Chapter 5  
Results and Analysis

This chapter will focus on the processing and electrical results from samples fabricated using the mesa-first and metal-first processes. Two different layer structures were studied as part of this work. The first, denoted by the prefix “RT,” was an InGaAs p-i-n Esaki diode layer. The i-region for this Esaki diode was only 3 nm in width. The second layer structure that was investigated was a p-i-n layer design to be a TFET. This layer, denoted by the prefix “DRT” had an i-region of 100 nm in width.
5.1 RT-1

The first gated sample was fabricated on an InGaAs tunnel diode structure grown at the Technion-Israel Institute of Technology. The layer structure of RT-1 can be seen in Figure 5-1. Secondary Ion Mass Spectrometry (SIMS) of the layer structure can be seen in Figure 5-2. The layer structure was originally grown as a $p$-$i$-$n$ Esaki diode.

<table>
<thead>
<tr>
<th>Layer Thickness</th>
<th>Layer Composition</th>
<th>doping</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 Å</td>
<td>InP</td>
<td>undoped</td>
</tr>
<tr>
<td>500Å In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>$p = 1 \times 10^{19}$ cm$^{-3}$</td>
<td></td>
</tr>
<tr>
<td>100Å In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>$p = 1 \times 10^{20}$ cm$^{-3}$</td>
<td></td>
</tr>
<tr>
<td>30Å In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>undoped</td>
<td></td>
</tr>
<tr>
<td>1000Å In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>$n = 5 \times 10^{19}$ cm$^{-3}$</td>
<td></td>
</tr>
<tr>
<td>3000Å In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>$n = 1 \times 10^{19}$ cm$^{-3}$</td>
<td></td>
</tr>
</tbody>
</table>

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Figure 5-1: Layer Structure RT-1
5.1.1 RT-1 Process History

RT-1 was processed using the mesa-first process outlined in Chapter 3. There were a few deviations from the specified process flow. These deviations were followed to make use of the InP etch cap as an isolation layer between the gate and the drain. The original intent of this layer was for it to be removed immediately before contact metal deposition, insuring a clean metal semiconductor interface. The InP etch cap lends itself to being used as an extra isolation layer due to the wet etch being selective between InP and InGaAs.

After mesa definition lithography a two-part etch is performed. The first etch is a blanket etch using the HCL:H$_2$O (1:1) to remove the InP cap from the field. The second etch is the C$_6$H$_8$O$_7$:H$_2$O:H$_2$O$_2$ (20:20:1) mesa etch. Following these two wet etches the MaN 2401 resist was removed via plasma etch. However, the interaction between the HCL and the MaN 2401 resulted in resist residue that could not be removed by the initial O$_2$ plasma etch. Figure 3-4 shows the extent of resist remaining after the first resist removal plasma etch. Additional O$_2$ plasma etches were performed for a total etch time of 10 minutes, however these extra plasma treatments had little effect. To fully remove the remaining resist, SF$_6$ was added to the plasma chemistry for an additional etch time of 4 minutes. The fluorine component was able remove the resist; however, the mesa had been exposed to a plasma for 16 minutes. This prolonged exposure to plasma could have resulted in degraded device performance.

The ALD high-k dielectric was deposited at The Pennsylvania State University. The gate dielectric consisting of 10 nm of Al$_2$O$_3$ was deposited. Following the gate level
EBL a TaN gate was deposited. The gate metal was targeted at 15 nm; however, due to the variations associated with the PE4400 only 7.9 nm of TaN was deposited. After the lift off of the excess TaN, the Al₂O₃ was etched using the gate as the etch mask. The remaining InP on top of the mesa was then removed with the gate again serving as an etch mask. The remaining processing went according to the procedure specified in Chapter 3. During the contact level EBL there was an issue with identifying all of the die level alignment marks. The result of this was that several die were missaligned. The result of this was that only 25 percent of the die yielded functional devices. Figures 5-3 and 5-4 show micrographs of the completed devices.

Figure 5-3: Fabricated TFET Side Profile Micrograph
As seen in Figure 5-4 the processing left a rough surface on top of the mesa. The source of this damage is unknown but could be attributed to the difficulty in removing the MaN 2401 resist.

### 5.1.2 RT-1 Electrical Results.

To evaluate the performance of the mesa-first process, the Esaki diodes from sample RT-1 were compared with metal-first Esaki diodes fabricated on a sample with the same layer structure. Figure 5-3 shows the comparison of forward tunneling performance between the two processes.
As seen in Figure 5-5 the mesa-first process was able to produce diodes that exhibited Negative Differential Resistance (NDR). NDR is indicative of band-to-band tunneling. The mesa-first device exhibited a current density similar to that seen by the metal-first process. The layer structure that RT-1 was fabricated on has demonstrated a peak current density of 220 kA/cm². Figure 5-3 also shows that the RT-1 Esaki diodes had a greater series resistance than the metal-first diodes. This higher series resistance is indicated by the shift in the peak voltage. The valley current of the metal-first diode is higher then that of the metal-first diode. This shift could possibly be caused by an additional leakage current. The source of this leakage current and increase in series resistance is most likely a result of the resist removal issues and subsequent long plasma treatment.
Figure 5-6 shows the electrical results of a gated device. A mesa with a length of 15 microns and width of 1 micron was tested. It was gated with three gates with a width of 2 microns each.

![Figure 5-6: RT-1 Gated Mesa IV Results (W=1\mu m L=15\mu m with 12\% Perimeter Gate Coverage)](image)

As seen in Figure 5-6 the gate current is orders of magnitude less than the drain current of the device, indicating that the gate was isolated from the contacts. As the gate voltage is increased there is a slight increase in the Zener current. It is inconclusive whether if the increase is a result of gate modulation or leakage. The large size of the device along with the high series resistance on the sample and the small width of the $i$-region confound these
results. It is possible that the $i$-region is too small for the gate to have any meaningful effect on the tunneling current. Further, it is possible that with the gate covering only 12% of the sidewall of the device, the gate contribution was minuscule. The large size of the device and the poor surface quality could be masking any changes in the device.

5.2 DRT Series TFETs

The DRT series are a set of samples fabricated on a layer structure specifically designed as a TFET. This InGaAs TFET structure was grown at the Technion-Israel Institute of Technology Israel. The layer structure of the DRT series can be seen in Figure 5-7. The change in this layer structure was a decrease in the designed p-type doping and an increase in the thickness of the undoped region.

<table>
<thead>
<tr>
<th>Thickness</th>
<th>Layer</th>
<th>Doping</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 Å</td>
<td>InP</td>
<td>undoped</td>
</tr>
<tr>
<td>600 Å</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As}$</td>
<td>$p = 5 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>1000 Å</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As}$</td>
<td>undoped</td>
</tr>
<tr>
<td>600 Å</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As}$</td>
<td>$n = 5 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>100 Å</td>
<td>InP</td>
<td>$n = 1 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>2000 Å</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As}$</td>
<td>$n = 3 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>500 Å</td>
<td>InP</td>
<td>$n = 1 \times 10^{19}$ cm$^{-3}$</td>
</tr>
</tbody>
</table>

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Figure 5-7: Layer Structure DRT-2
5.2.1 DRT-1 Processing Summary and Electrical Results

DRT-1 was processed utilizing the metal-first tunnel diode process. The metal-first process was utilized to establish a baseline on the layer structure’s electrical performance. This baseline will be used to evaluate the potential performance of the TFET structure and serve as a way to evaluate samples fabricated using the mesa-first process. Figure 5-8 shows the IV curve for tunnel diodes tested immediately following the mesa etch.

As seen in Figure 5-8 the DRT-1 had a very low Zener current density. At -0.25V the current density was approximately 170 µA/cm². This lower Zener current density
translates to a low off-state voltage in a gated device. Figure 5-9, shows electrical results for DRT-1 following the BCB process and second level contact.

As seen in Figure 5-9 the diodes are sensitive to light. Further, there was degradation in device performance between devices tested after the mesa etch and devices tested after second level metal. The Zener current density is much greater following BCB and second level metal. This increase in current density suggests that there is a shunt current, the origin of which is possibly caused by a gap between the BCB and the sidewall of the device.
5.3 Modeling of Tunneling Currents

Many of the published TFET simulations should be evaluated with a degree of uncertainty. These tunneling simulations have been reported to underestimate the current density of devices by up to two orders of magnitude [1]. TFET simulations may use a variety of models to calculate tunneling current. These models include the Kane model, [29] the Hurkx band-to-band tunneling model [30] and the Schenk tunneling model [31]. Further complicating the simulations are variables such as potential barrier approximations, effective mass, and accounting for Shockley-Read-Hall recombination. The variety and complexity of the quantum tunneling models, the disparity between simulation and experimental and the lack of experimental data results in debate over the efficacy of individual models. One model with certain variables may match a selected set of experimental results while another model may agree with a separate set. No physical model has yet been demonstrated with the universality necessary to work across different material systems, junction profiles, and doping.

A question then arises, is a physical model needed? For the purposes of complete understanding of tunneling the answer is yes. For purpose of circuit modeling and the rapid realization of tunneling-based devices, the answer is no. An empirical model a model sufficient enough to predict TFET and tunneling behavior and allow for circuit design built upon experimental data could be realized. They key to realizing this empirical model is a large volume of experimental data of both gated and non-gated devices. Part of
this work looked at the development of an initial low-level tunneling model based upon experimental observations.

Figure 5-10 shows a series of curves of IV curves for 150 nm radius circular Esaki diodes. The curves shown in Figure 5-8 are from a sample with the same layer structure as RT-1. The spread between the curves is related to uncertainty in measuring the actual junction areas.

Analysis of the experimental data showed a correlation between the forward tunneling current and the Zener current. Figure 5-11 shows the ratio of the Zener current to the forward current with respect to voltage.
As seen in Figure 5-11 the ratio of Zener current to forward tunneling current is exponential in nature, in the form of $J_Z/J_F = Ae^{BV}$. Using this relationship the Zener current can be plotted in terms of the forward tunneling current and the exponential relationship. By multiplying the empirical equation for forward tunneling current found in Sze with this exponential relationship a new empirical formula for the Zener current is derived as seen in Eq. 5-1

$$J_{Zener} = AJ_p \frac{V}{V_p} \exp\left(1 - \frac{-V}{V_p} - BV\right)$$

(5-1)
This empirical Zener model is a function of the peak current density, the peak voltage, the applied voltage and the two fitting constants (A&B) from the empirical relationship. Figure 5-12 shows the model plotted against measured data.

Figure 5-12: Zener Empirical Model A=0.94 B=7.2 Vp=0.165 V Jp=183kA/cm²

As seen in Figure 5-12 the empirical Zener model has a good correlation with the measured data. The question then arises how will this model stand up to changes in temperature? Esaki diodes from an RT series sample were heated from 313 K to 433 K. The measured data as well as the accompanying model for each temperature is plotted in Figure 5-13. Table 5-1 contains the fitting parameters for each temperature step. It was found that as the temperature increased there was an increase in current density. The “A” fitting constant also increased with temperature.
Figure 5-13: Zener Empirical Model Function of Temperature

Table 5-1: Zener Empirical Model Fitting Constants as a Function of Temperature

<table>
<thead>
<tr>
<th>Temperature [K]</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>313.15</td>
<td>0.933</td>
<td>6.392</td>
</tr>
<tr>
<td>329.15</td>
<td>0.944</td>
<td>6.328</td>
</tr>
<tr>
<td>348.15</td>
<td>0.947</td>
<td>6.437</td>
</tr>
<tr>
<td>371.15</td>
<td>0.963</td>
<td>6.825</td>
</tr>
<tr>
<td>433.15</td>
<td>0.981</td>
<td>6.425</td>
</tr>
</tbody>
</table>

Figure 5-14: Fitting Constants as a Function of Temperature
As seen in Figure 5-14 the “A” fitting constant increase linearly with temperature. The variation of the “B” makes the effect of temperature on it inconclusive.

By adding an additional term to Eq. 5-1 the empirical model can be extended to gated devices. As seen in Eq. 5-2 this additional term is a fitting constant “C” multiplied with applied gate voltage $V_g$.

$$I = AI_p \frac{-V}{V_p} \exp \left(1 - \frac{-V}{V_p} - BV + CV_g\right)$$  \hspace{1cm} (5-2)

The model in Eq. 5-2 was applied to the results from Uemura et al. [15], the result of which is plotted in Figure 5-15.

Figure 5-15: Zener Empirical Model with Gate Control
As seen in Figure 5-15 the empirical model was able to match the measured data in the Zener regime with $V_g$ between 0 V and 0.6 V. When $V_g = -0.2$V the model predicts a lower current than the measured data. Further experimental data is necessary to refine the empirical model and explore the meaning of the fitting constants.
Chapter 6
Conclusions and Future Work

6.1 Conclusions

A mesa-first process was developed for the fabrication of submicron tunnel devices. This process enables the fabrication of both gated and non-gated devices. Samples that were fabricated with the mesa-first process showed NDR but little if any notable gate control. For devices on RT-1 the lack of gate control can attributed to either the small fraction of the device perimeter that was gated or the small \( i \)-region. RT-1 showed that there are several highly critical components of the process that must be monitored to ensure functional devices. These components are the tunneling device structure, alignment, and gate material compatibility, as well as surface cleanliness.

EBL was the key enabler of this process; however, there are several alignment challenges associated with it. These alignment challenges stemmed from alignment mark recognition. If the NPGS system is unable to recognize the alignment marks due to low contrast materials or similar contrasting materials, alignment will be very difficult. There are several techniques and process options that can be incorporated to improve alignment mark recognition. The alignment can be improved by using high-contrast material such as Ta or Au as an alignment mark. While metal contamination may be an issue before ALD, following the high-\( k \) gate dielectric deposition a second set of alignment marks may be deposited either as an individual layer or incorporated with the gate level lithography. The use of a backscatter detector in conjunction with a secondary electron detector can further improve the contrast. The two detectors collect different signals from the samples.
These different signals can be mixed and overlaid with each other. The result is an improvement in image contrast and alignment mark recognition.

The mesa-first process showed that surface preparation and cleanliness is critical. Issues with surface contamination can lead to difficulty with removing layers. The result of the resist removal issues in RT-1 was excessively long plasma etch to fully remove the resist. It is not conclusive that this long plasma treatment resulted in the rough top surface but it certainly could have caused interface damage along the sidewall of the device. A smooth top surface would result in lower contact resistance and overall reduced series resistance.

It was found that a high quality gate interface is needed. The deposition of the high-$k$ dielectric via ALD followed by a reactive sputter of TaN is not ideal as it can lead to issues with gate to dielectric interface quality. To improve the interface quality an in-situ gate metal should be used to improve the gate to dielectric interface. The gate and gate bolster materials need to be thermal stable and low in resistivity, with the ability to be patterned. Refractory alloys such as TiN and TaN fit these requirements. They are lower resistivity materials and are resilient against gate skinning effects. TaN has the ability to be patterned via lift off lithography while TiN can be etched in a CF$_4$ plasma. TaN is an ideal gate or gate bolster material as it has a high Z number. The high Z number enables a second set of alignment marks to be incorporated into the layer design for the gate definition lithography.
6.2 Future Work

Two components of the TFET are in need of further study. The first is structure of the device. To the knowledge of the author no study has yet shown an approach where the doping, layer structure and $i$–region thickness of a TFET have been varied. This type of study is needed as a result of the current uncertainty with simulation models. One detailed study in a given material system would provide a set of data for model calibration. Such a study would allow for new empirical relationships and models to be developed. The process developed as a part of this work provides a basic flow to help analyze these different samples. The second component of the TFET that is in need of further study is the gate. The gate materials, gate dielectric thickness, and gate metal thickness are in need of refinement.

For the mesa-first process the gate is an essential component. This process utilizes ALD to deposit the gate dielectric and the gate metal. The lack of onsite ALD at RIT restricted the development of the mesa-first process by limiting number of samples that could be fabricated. Therefore a very conservative approach to fabrication had to be adopted. A majority of the development work was preformed on a highly resistive InGaAs layer structure with similar etch properties to the tunnel structures studied with this work. This analogue served as a great development tool for EBL, planarization, and contact procedures. However the InGaAs analogue offered no insight into the challenges associated with the gate stack. Many of the alignment issues arose when the gate material was introduced into the process. The lack of repeatability with gated samples limited the
ability to fully develop the gate process. More samples with ALD high-$k$ dielectric are needed to fully characterize and develop the gating portion of the whole process.

Another area for future development is the use of an optically based system to enable the gate, via level and contact level lithography. The critical dimensions on these layers are often no smaller than a micron, lending to the use of an optical system. The advantages of an optical system would be the improvement in alignment mark recognition by being able to use information in the visible wavelength spectrum. Further, the higher throughput of the optical projection stepper would reduce the process cycle time significantly. The challenges involved with this are in creating an alignment scheme that can be transferred between the EBL and optical lithography systems.
References