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Three-terminal Si-based negative differential resistance circuit element with adjustable peak-to-valley current ratios using a monolithic vertical integration

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Si-based resonant bipolar transistors are demonstrated by the monolithic vertical integration of Si-based resonant interband tunnel diodes atop the emitter of Si/SiGe heterojunction bipolar transistors (HBTs) on a silicon substrate. In the common emitter configuration, I_C versus V_{CE} shows negative differential resistance characteristics. The resulting characteristics are adjustable peak-to-valley current ratios, including infinite and negative values, and tailorable peak current densities by the control of the HBT base current under room temperature operation. With the integrated RITD-HBT combination, latching properties which are the key operating principle for high-speed mixed-signal, memory, and logic circuitry, are experimentally demonstrated.

Circuitry using negative differential resistance (NDR) devices is of a great interest for future memory and logic circuit applications.[1,2] The inherent folded $I-V$ characteristic of NDR devices can provide multiple stable states that reduce device count and circuit complexity with increased functionality per device and lower power consumption for switching and multistate memory circuit applications. Furthermore, since the tunneling phenomenon is a majority carrier effect, the speed of circuits using NDR devices can be much faster. In particular, the integration of a tunnel diode with heterojunction bipolar transistors (HBTs) enables the NDR device to be used for high-speed highly functional monolithic microwave integrated circuits, such as voltage controlled oscillators and analog-to-digital converters.[3,4]

These types of hybrid circuits have already been demonstrated in many III-V compound semiconductor material systems mostly by the integration of unipolar resonant tunnel diodes with HBT[2,5] or high electron mobility transistors.[1,2] However, despite the better performance of III-V-based NDR devices stemming from the different material properties, such technology will never reach mainstream complementary metal-oxide-semiconductor (CMOS) or SiGe HBT technology, unless a suitable Si-based NDR device and integration technology compatible with existing Si-based CMOS or HBT devices is available. Successful demonstration on a Si platform could reduce device count and augment the goals articulated on the International Technology Roadmap for Semiconductors (ITRS).

This Si integration was made possible by the advent of Si-based resonant interband tunnel diodes (RITDs).[6–8] In this letter, we report a three-terminal Si-based NDR device by epitaxially growing an RITD atop the emitter (E) of a Si/SiGe HBT on a silicon substrate. The integrated RITD-HBT combination enables the peak-to-valley current ratio (PVCR) to be continuously adjusted from infinite to zero or even to negative values. The peak current density (PCD) can also be scaled by the base (B) current. The exact control of PVCR and PCD are very important to overcome current mismatches in bistable logic functioning circuitry.

The integration of the Si-based RITD-HBT consists of an n-on-p RITD, a p-on-n backward diode and an $n-p-n$ SiGe HBT. The structure, as shown in Fig. 1(a), is designed such that the RITD is placed atop the emitter of the HBT.

The growth of the RITD-HBT composite structure was carried out by two successive epitaxial growth techniques. For the $n-p-n$ HBT,[9] the sub-collector and collector (C) were grown by metalorganic chemical vapor deposition (CVD) on a 4 in. p-type silicon substrate with a resistivity over 2000 Ω cm. Phosphorus was used as the dopant for the 450 nm n^+ subcollector (2.5×10^{19} cm^{-3}) and 1.85 μm n^- collector (1.5×10^{17} cm^{-3}) growth.

The remaining HBT base, emitter, connecting backward diode, and RITD were grown by a molecular-beam epitaxy (MBE) system using elemental Si and Ge sources heated by electron beams. In the SiGe base region, pseudomorphically grown atop the CVD-grown collector, the Ge profile was

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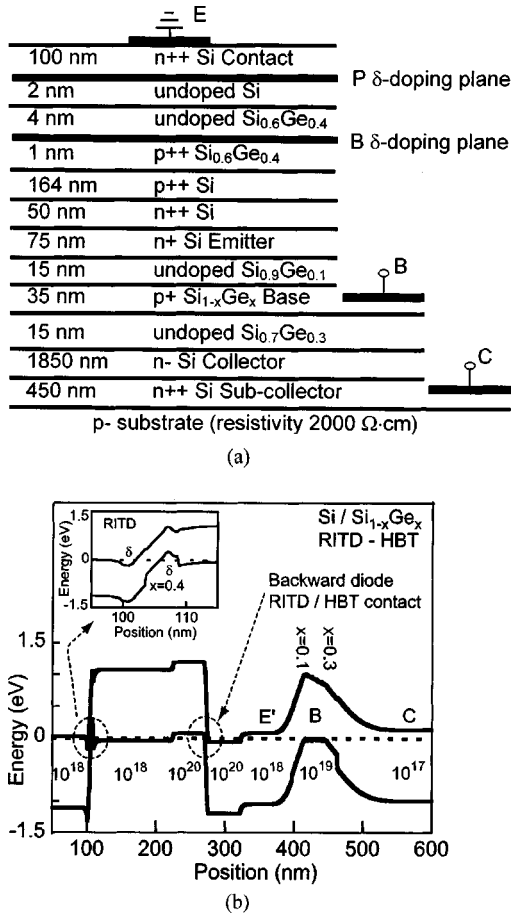

FIG. 1. Schematic diagram of the SiGe RITD with SiGe HBT composite RBT structure and its calculated band diagram.

graded to have 30% Ge at the base/collector junction and 10% at the emitter/base junction. In order to minimize boron dopant outdiffusion due to the high doping concentration in the base region, the 35 nm boron-doped p^+ SiGe base layer (1.0×10^{19} cm^{-3}) was sandwiched between two 15 nm undoped SiGe layers. Finally, a 75 nm n^+ Si emitter layer (1.0×10^{18} cm^{-3}) was grown on top to complete the HBT structure.

Following the $n-p-n$ HBT growth, a p-on-n backward diode consisting of a 50 nm phosphorus-doped n^+ Si layer (5.0×10^{19} cm^{-3}) and a 48 nm boron-doped p^+ Si layer (5.0×10^{19} cm^{-3}) was inserted as transition layers to overcome a polarity mismatch between the RITD and HBT.

Next, a SiGe RITD was grown atop the p-on-n backward diode. The basic structure of this RITD consisted of two δ-doped layers (1.0×10^{14} cm^{-2}) to create defined quantum wells and spacer layers (2 nm of undoped Si and 4 nm of undoped $Si_{0.6}Ge_{0.4}$) for the intrinsic tunnel barrier. Details on RITD growth and discrete results are reported elsewhere.[6,8,10] Finally, a post-growth rapid thermal annealing treatment at 800 °C for 1 min was performed *ex situ* after the completion of the RITD-HBT growth to reduce point defects created during the low-temperature MBE process.[11] The processed RITD-HBTs have a double-mesa structure obtained using conventional photolithography and a self-aligned process.

The corresponding energy band diagram of the RITD-HBT structure is shown in Fig. 1(b) generated from a semi-

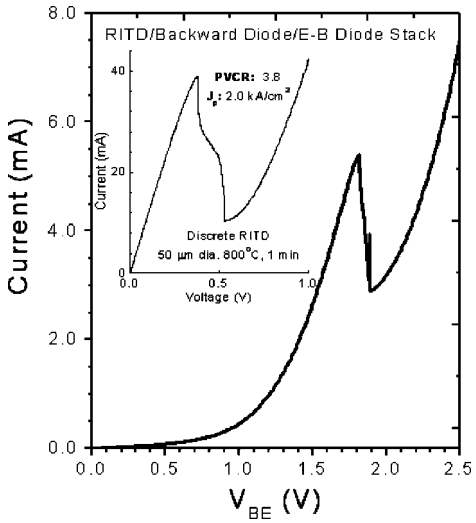

FIG. 2. Measured base/emitter $I-V$ characteristics of the RITD-HBT with the collector open at room temperature. Inset shows $I-V$ characteristics of a representative discrete RITD.

classical Thomas–Fermi charge calculation with the inset showing the RITD portion.

Figure 2 shows the base/emitter $I-V$ characteristics of an RITD-HBT measured at room temperature with the collector open. Shown in the inset of Fig. 2 are the $I-V$ characteristics of a representative discrete RITD having the same structure as utilized in this RITD-HBT tandem. Unlike the discrete RITD showing an NDR region at around 0.4 V, the base/emitter $I-V$ curves shows an NDR region at around 1.9 V. This shift is due to the voltage drop across the base-emitter junction of the HBT and the backward diode.

Figure 3 shows the common emitter $I-V$ characteristics of the three-terminal NDR device with 0.5 mA base current steps, measured at room temperature. Under the common emitter configuration, for the forward active region operation through the saturation region, the RITD is forward biased. With a small base bias current, the amount of emitter/base forward bias is also small, and it is well below the critical peak voltage point for tunneling to occur in the RITD. As the base bias current initially increases, the emitter/base forward

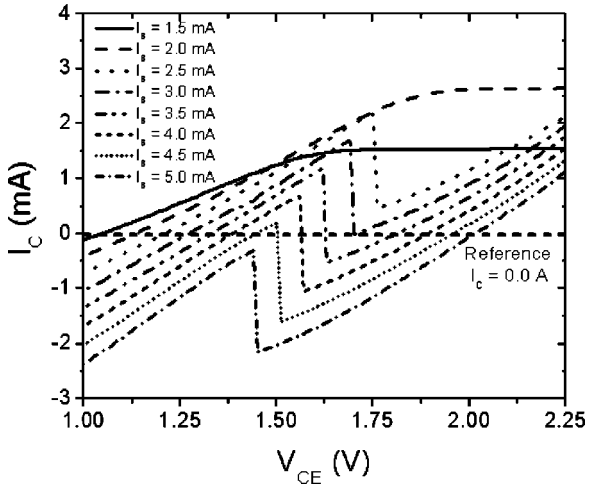

FIG. 3. Measured common emitter $I-V$ characteristics showing the NDR region demonstrate PVCR and PCD can be controlled by the base current. These curves also indicate infinite or even negative PVCR can be realized.

bias, including the RITD and backward diode, also increases, but the HBT operates conventionally. However, at a critical amount of base bias current, the forward bias forces the serial connection of the RITD, backward diode, and emitter/base forward bias into the tunneling region of the RITD as the energy states in the RITD cross to satisfy the condition for tunneling, as shown in Fig. 3. As the bias increases further, the bands uncross and NDR behavior is observed.

The observed behavior occurs since electron injection into the base becomes suppressed from the emitter/base junction because the forward-biased RITD is operating in the NDR region and effectively blocks electron flow. At this moment, unlike a normal bipolar transistor, the number of electrons injected from the emitter is reduced due to the NDR characteristic of the RITD acting as a current limiter. Consequently, the collector current traces out the NDR characteristics of an RITD as the NDR behavior modulates the emitter current.

Figure 3 illustrates that negative values for the collector current can be obtained. This is expected when the injected emitter current drops below the base current, because $I_C = I_E - I_B$. Physically, what occurs internally in the HBT is that the net buildup of positive charge in the base region stemming from the sudden decrease of electron injection by the RITD current limiter results in a sudden forward bias increase across both the emitter/base and base/collector junctions. When this occurs, the surplus holes from the base bias current no longer participate in recombination with electrons because the number of electrons is deficient in the base, but some surplus holes flow instead into the collector region. When these surplus holes transit the forward-biased base/collector junction, the net collector current is effectively reduced. Negative collector current is observed when the number of holes flowing in the collector is larger than the number of electrons flowing into the collector. It is the injected base holes which transit the forward biased base/collector junction that results in a large or even infinite PVCR, shown in Fig. 3. Clearly, not only the PVCR, but also the PCD, is adjustable by the base bias current, as shown in Fig. 3.

The fabricated RITD-HBT can readily function as a latching circuit element. For small I_B values between the peak and valley current positions of the RITD, the integrated RITD-HBT acts as a latch with two stable operating points B′ and C′ for a fixed V_{CE}, as shown in the inset of Fig. 4. The voltage V_{BE} can then be used as a logic level since $V_{BE} = V_{\mathrm{RITD}} + V'_{BE}$, where V'_{BE} is the voltage across the base/emitter diode which is fixed. Starting with a low I_B level, at point A of the inset of Fig. 4, switching is performed by increasing I_B until I_E is equal to the RITD peak current (point B of the inset of Fig. 4). The operating point then jumps to C, and the return path goes through point D and back to A. Switching operation is experimentally demonstrated in Fig. 4 for a fixed V_{CE}. It should be noted that the $I-V$ characteristics shown in this study were all measured at room temperature and they were repeatable and stable.

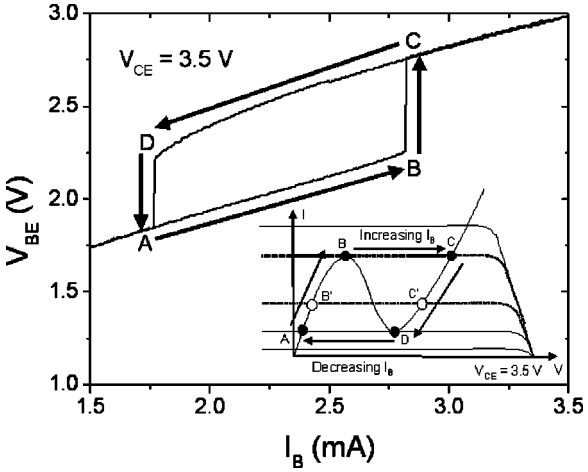

FIG. 4. Measured $I_B - V_{BE}$ characteristics demonstrating switching operation in which V_{CE} is fixed at 3.5 V and I_B is swept in dual mode. Inset is a load line analysis for V_{BE} switching.

In conclusion, a vertical monolithic integration of a Si-based RITD atop a SiGe HBT was demonstrated in this study. The resulting devices have the distinguishing characteristics of infinite, negative, and adjustable PVCR with adjustable PCD by the control of the HBT base current. This study has also analyzed its operation as a latching element and demonstrated its switching operation experimentally.

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