Fabrication of Sub-300nm Fins at RIT by SADP

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Outline

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Project Goals

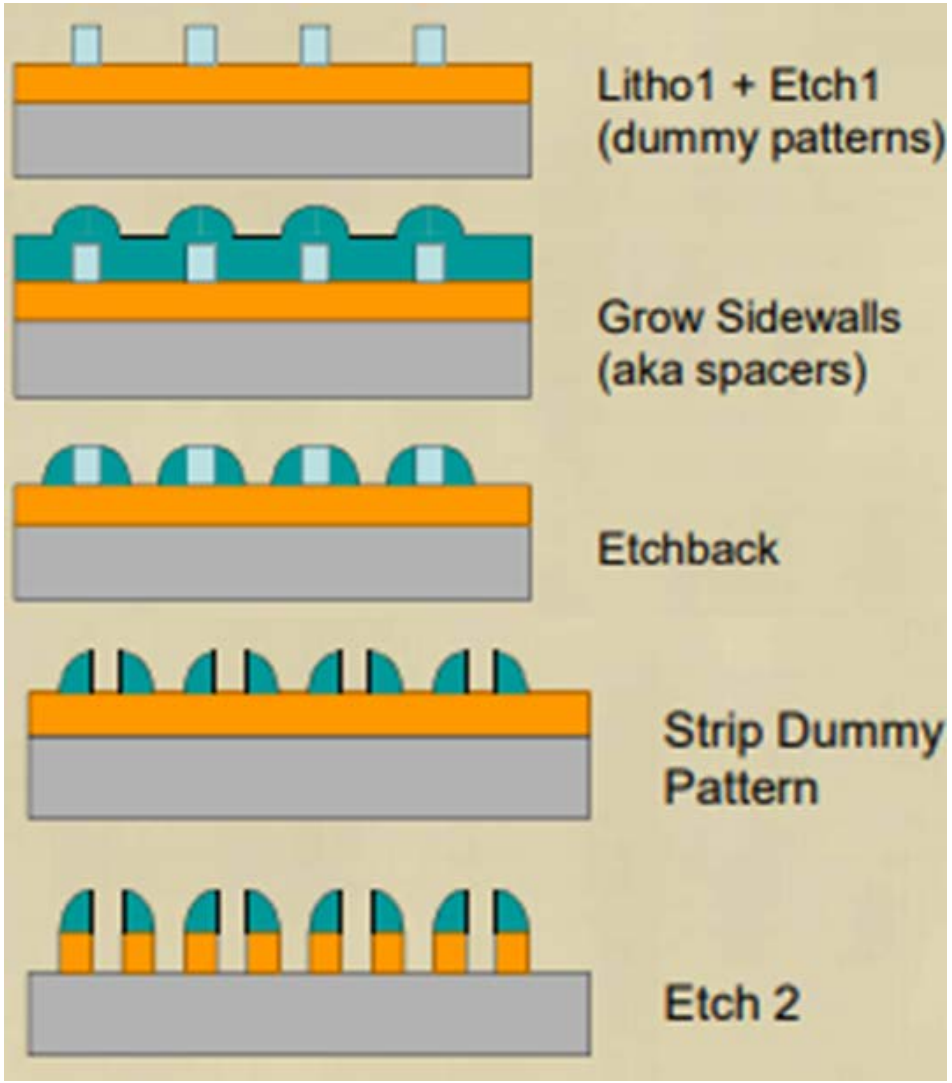
Goal: Fabricate sub-300nm silicon fins at RIT's SFML by self-aligned double patterning (SADP).

Motivation:

- Patterning advancements necessary to uphold Moore's Law
- SADP → FinFETs
- RIT currently implements a planar CMOS process

SADP Overview

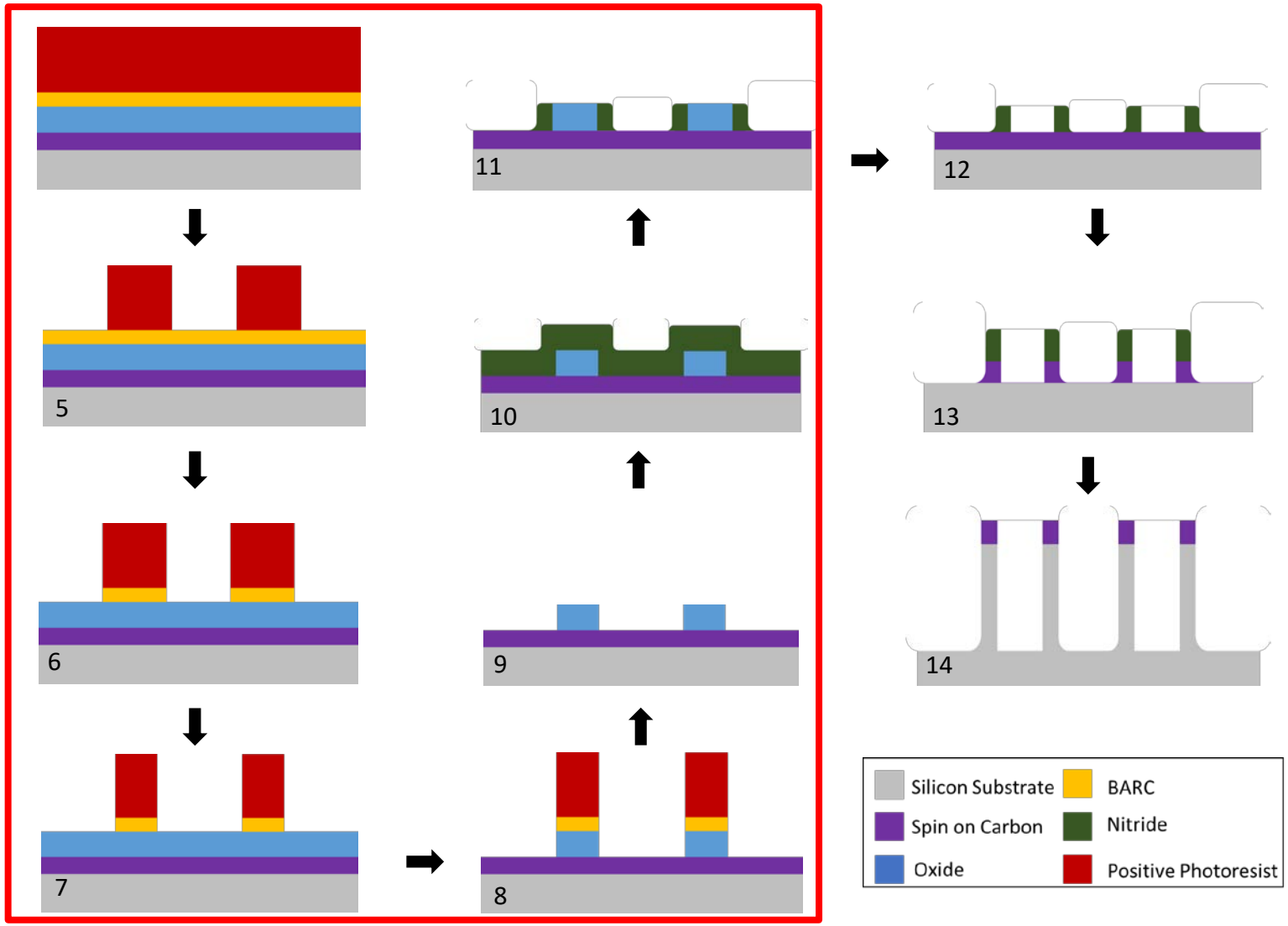
- Allows for the lithography pattern to be transferred to a mandrel, which in turn is used as an etch mask.
- Smaller features may be realized without the implementation of more expensive lithography equipment.



[1]

Process Flow [2]

1. RCA Clean
2. SOC Hardmask Deposition
3. Oxide Mandrel Deposition
4. BARC Deposition
5. Photolithography
6. Etch BARC
7. Trim Etch for Mandrel
8. Mandrel Etch
9. Solvent Strip
10. Silicon Nitride Deposition
11. Silicon Nitride Spacer Etch
12. Strip Oxide Mandrel
13. Etch SOC
14. Etch Silicon Fins



Results

- Determined spin speeds and times for SOC, BARC, and PR depositions
- Deposition rates determined:
  - Nitride = ~64 Å/s with 20 min. deposition in LPCVD
  - Oxide = ~88 Å/s in Applied Materials P5000 TEOS chamber
- Produced the following standard deviations in film uniformity:
  - SOC: 1.56%
  - Oxide: 3.45%
  - BARC: 0.47%
  - Photoresist: 1.27%
  - Nitride: 1.49%
- Etch rates determined:
  - Oxide: ~32 Å/s
  - BARC: ~8 Å/s
  - Nitride: ~3 Å/s

- Lithography:
  - Qualified AZ MiR 701 PR for use with process
  - Thinned resist 2:1, 701 PR:PGMEA for 300nm coat
  - FEM performed → Conventional illumination, NA = 0.48, Sigma = 0.625 → dose = 148 $^{mJ}/_{cm^2}$

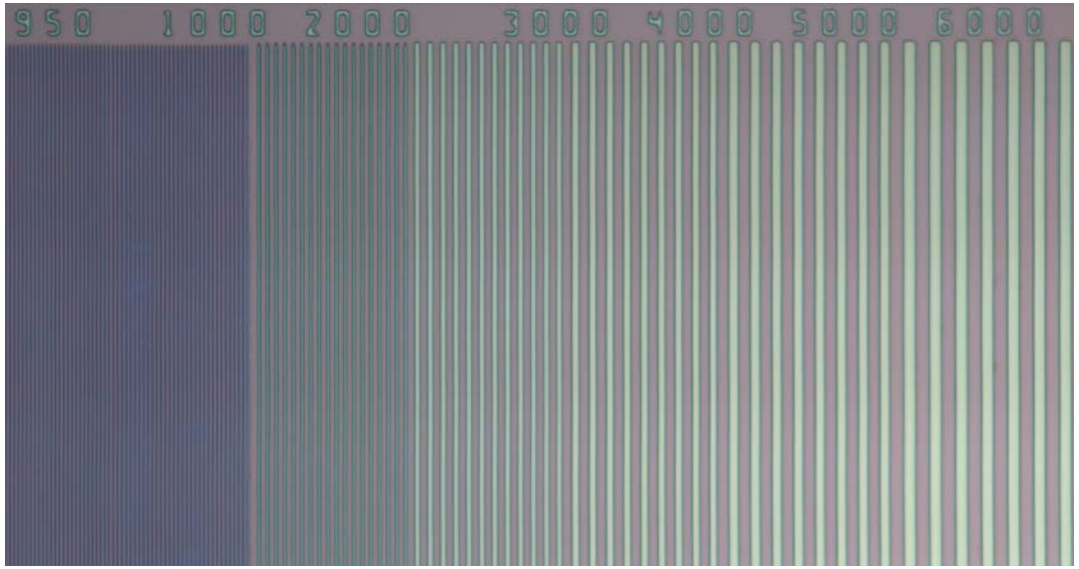


Figure 1: Patterned lines and spaces.

Results – Oxide Mandrels

- Applied Materials P5000
  - 60 second etch
  - 30 scc CHF3
  - 60 scc CF4
  - 100 scc Ar

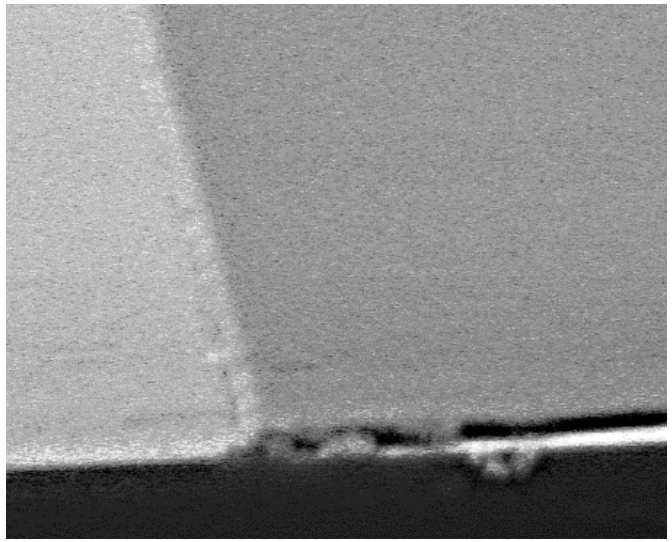


Figure 2: Zoomed-in view of oxide mandrel sidewall.

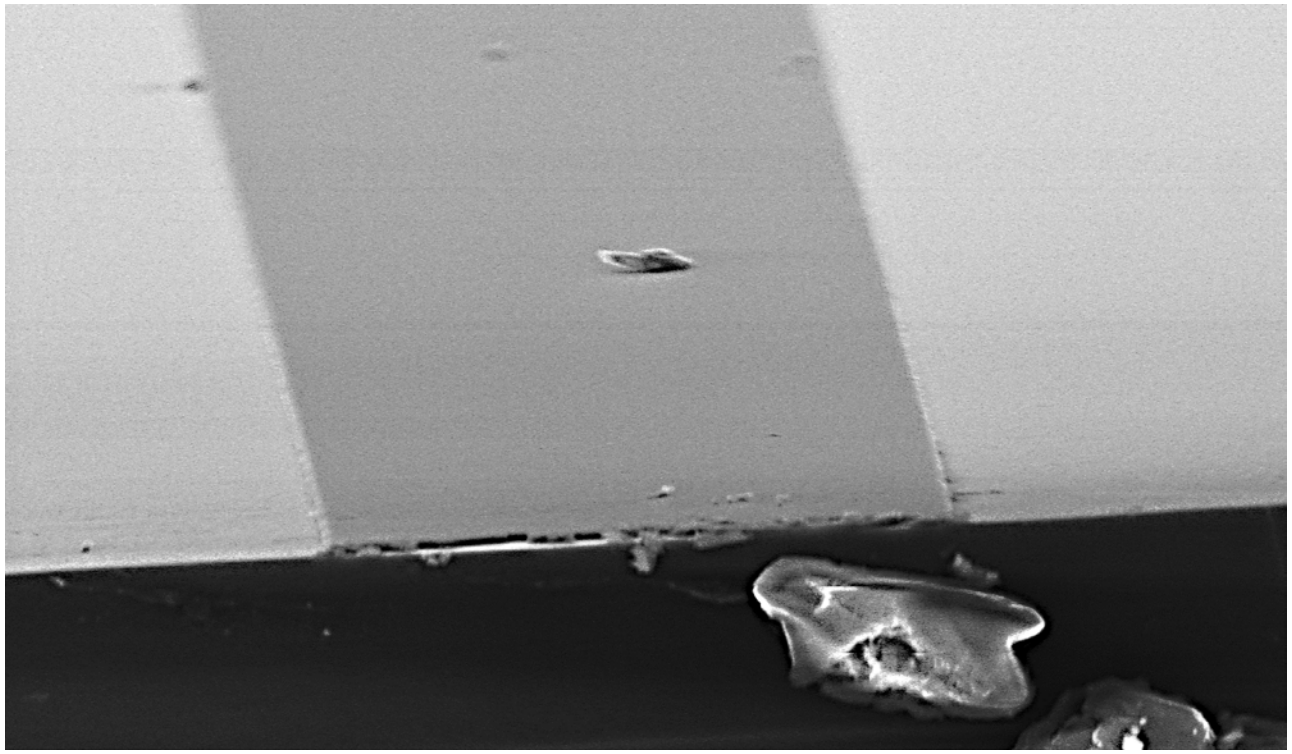


Figure 2: Wide oxide mandrel on silicon substrate.

Results – Nitride Spacer Etch

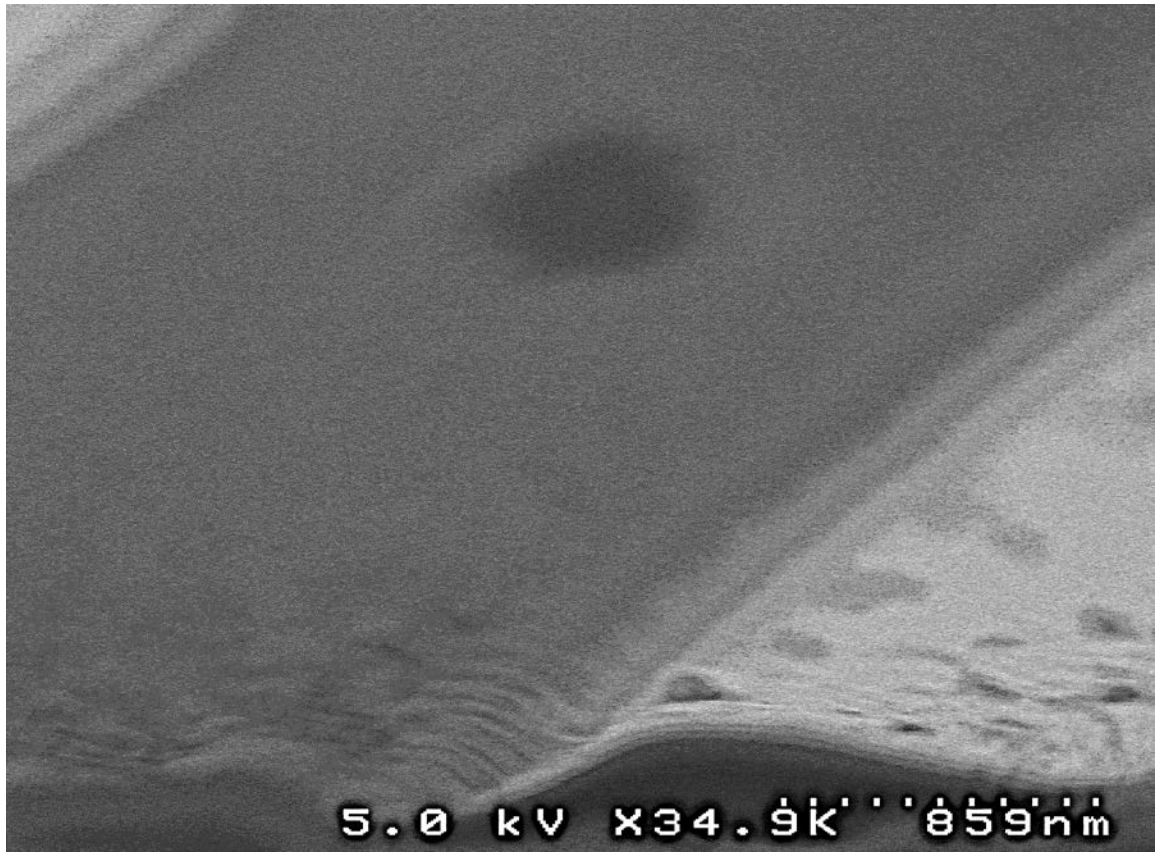
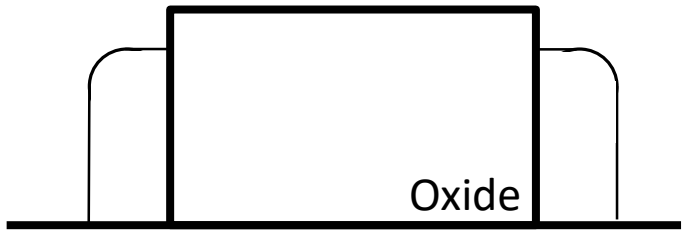


Figure 4: Post nitride etch.

Results – What Went Wrong

Achieved:

Desired:



Conclusions

- Hard mask layer needed on top of oxide mandrel layer
- In addition, oxide mandrel etch may not be anisotropic enough, resulting in undesired removal of silicon nitride spacers
- Further testing and development necessary

Future Work:

- Development of RIE/hardmask plasma etch process improvements
- Develop complete implementation of P5000 tool cluster
- Undergraduate course – implementation of fin fabrication in labs
- PhD candidate – development of FinFET process

Acknowledgements

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References

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