

# FeFET Process Integration and Characterization

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**Abstract**—A process for fabricating n-channel ferroelectric field-effect transistors (FeFETs) in-house at RIT has been developed, incorporating atomic layer deposition (ALD) of Al:HfO<sub>2</sub> and CMOS processing techniques. Test results of the first lot show signs of improper source/drain formation, evidenced in part by high off-state leakage and a poor on- to off-state current ratio; the root cause of improper formation is still being investigated. Nevertheless, ferroelectric behavior has been observed, and a memory window of approximately 150mV has been extracted for FeFETs with 20nm Al:HfO<sub>2</sub> films. The impact of threshold adjustment implantation on the transfer characteristics and memory window of the devices was also examined, and ultimately found to shift both transfer curves of a given device without degrading its memory window. To revive the current devices, monolayer doping (MLD) techniques will be employed to recreate source and drain regions, and devices will be retested.

**Index Terms**—FeFETs, Ferroelectric Memory, Al:HfO<sub>2</sub>

## I. INTRODUCTION

FERROELECTRIC materials are continuing to gain popularity in solid-state electronics for a variety of applications. The inherent nature of ferroelectric materials, namely their ability to become polarized in the presence of an electric field, and their ability to retain said polarization when unbiased, has made them an attractive candidate for non-volatile memory applications in particular. Ferroelectrics are also known to exhibit what is referred to as negative capacitance in certain operating regimes, which has been exploited to achieve subthreshold slopes less than the theoretical Boltzmann limit of 60mV/dec in silicon-based MOS technologies. When biased appropriately, these films would allow for the realization of ultra-low power operation in devices incorporating them.

Despite ferroelectrics in solid-state electronics being a research topic of interest since the 1950s, these materials have not been widely adopted due to their processing limitations (low temperature), and incompatibility with modern CMOS technology. However, with the advancements in atomic layer deposition technology and the discovery of ferroelectricity in popular, high-k gate dielectric materials like hafnium oxide and hafnium zirconium oxide, integration of these materials into current, state-of-the-art CMOS manufacturing facilities has become a possibility. One critical advantage of ferroelectric hafnium oxide and hafnium zirconium oxide over ceramic-based ferroelectric materials is their lower coercive fields,

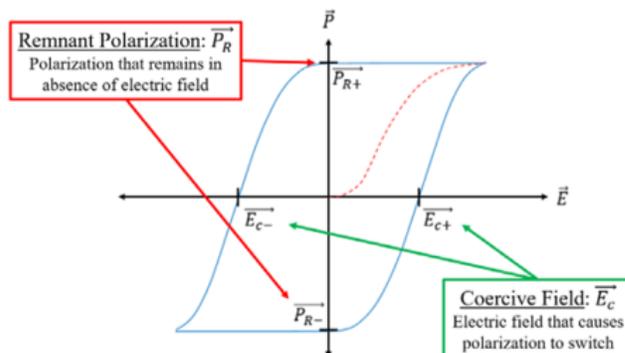


Fig 1. Typical polarization v. voltage characteristic curve for ferroelectric materials with labeled remnant polarization charges and coercive fields.

which, when coupled with ALD, allows for aggressive device scaling to nodes comparable to those in modern CMOS technology. Furthermore, ALD techniques allow for well-controlled, conformal deposition of materials, even on newer three-dimensional architectures like the FinFET. It is because of this that novel ferroelectric devices like ferroelectric field effect transistors, negative capacitance field effect transistors (NC-FETs) and even ferroelectric tunnel

## II. THEORY

### A. Ferroelectric Materials

Ferroelectric materials, by definition, are materials that can become spontaneously polarized in the presence of an electric field. The polarization v. voltage (P-V) characteristics of these materials exhibit hysteretic behavior and bistability, even when bias is removed from the material, justifying its popularity in the field of non-volatile memory. Figure 1 shows the hysteretic P-V characteristics of a ferroelectric material with some points of interest labeled.

In Figure 1, the remnant polarization charges ( $P_{R+}$  and  $P_{R-}$ ) along with the coercive fields ( $E_{c+}$  and  $E_{c-}$ ) are denoted on the y- and x-axes, respectively. Remnant polarization charge is the charge remaining within the material, positive or negative, after external bias has been removed. The coercive field associated with these loops is the electric field the material must “see” to induce switching from positive polarization charge to negative polarization charge, or vice versa. If the thickness of the ferroelectric film is known, one can multiply the coercive field values by the film thickness to obtain coercive voltage values ( $V_c$ ) instead.

Hafnium oxides doped with aluminum, silicon and even

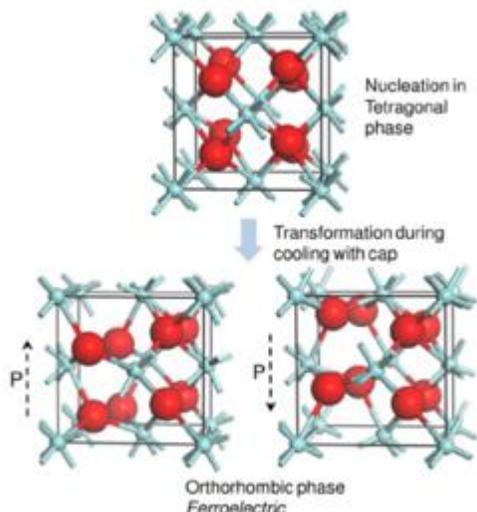


Fig 2. Transition of doped hafnium oxide to orthorhombic crystalline phase during cooling

yttrium, which are popularly used today as ferroelectric materials, do not possess ferroelectric properties as deposited. For spontaneous polarization to occur, the doped hafnium oxide must be in a particular non-centrosymmetric crystalline phase, known as the orthorhombic phase. Forcing the material into this phase is often achieved through rapid thermal processing with a TiN capping layer, which provides physical stress to the underlying hafnium oxide during cooling. This transformation to the desired crystalline phase in hafnium oxide is illustrated in Figure 2.

Once the hafnium oxide is deposited and forced into this crystalline phase, the thermal budget of future processing steps should be reduced to maintain the integrity of the now ferroelectric film.

### B. FeFET Devices and Operation

Ferroelectric FETs are quite similar to MOSFETs, with the main differences residing in the gate stack of the device. Unlike a MOSFET, which incorporates an insulating dielectric layer, traditionally  $\text{SiO}_2$ , in between the gate and the channel, FeFETs incorporate ferroelectric materials instead. Inserting a material with bistable charging states in between the gate and channel of a transistor results in bistable transfer characteristics. Consequently, there are two operating states of a FeFET, denoted as the on- and off-states. A representative plot of the transfer characteristics of an n-channel FeFET with labeled operation states is shown in Figure 3.

To achieve “on-state” transfer characteristics from the device, the source and drain of the device are grounded while the gate is pulsed with a high, positive voltage that exceeds the coercive voltage of the ferroelectric film. This presents positive polarization charge to the surface of the transistor channel, partially depleting it and causing an apparent decrease in threshold voltage (Fig. 3). For off-state operation, the gate is now pulsed with a high magnitude, negative voltage that is less than (or, greater in magnitude than) the negative coercive voltage of the ferroelectric film. Now, negative polarization charge is presented to the surface of the transistor channel,

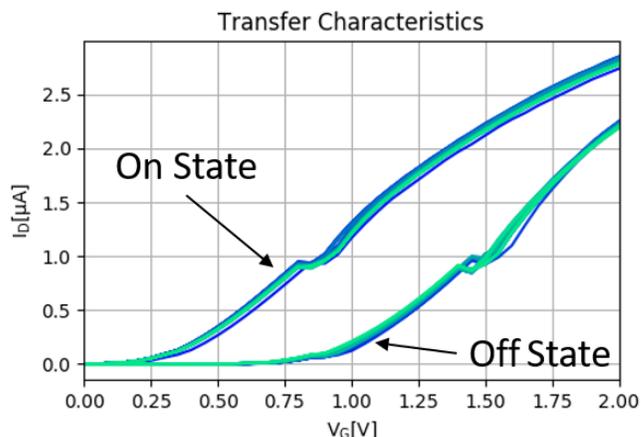


Fig 3. Bistable transfer characteristics of an n-channel FeFET with labeled operating states

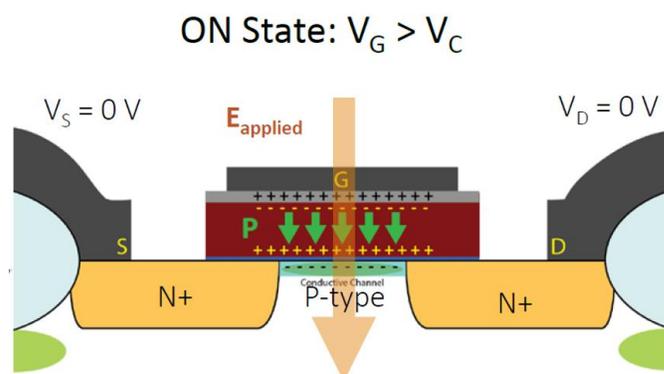


Fig 4. Depiction of on-state FeFET charging effects

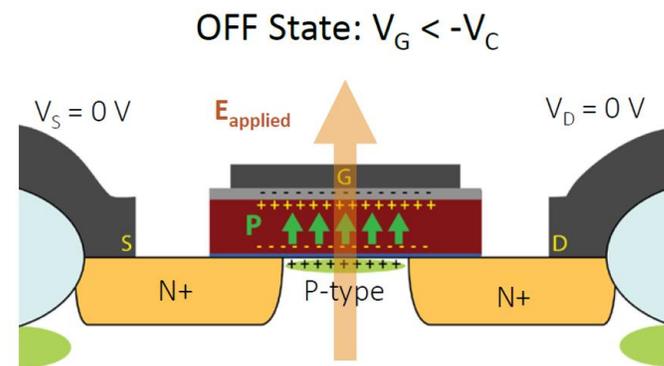


Fig 5. Depiction of off-state FeFET charging effects

causing majority carriers from the substrate to accumulate at the surface during equilibrium. The net effect is an increase in the threshold voltage of the off-state transfer characteristics when compared to those of the on-state. These charging phenomena in regard to the n-channel FeFET are depicted in Figures 4 and 5 for on-state and off-state operation, respectively.

When it comes to memory applications and FeFETs, the storage element and the access element are combined in the same architecture, providing for the simplicity of a 1T1C memory cell. The quality of this memory cell is quantified by a FeFET-based memory figure of merit, memory window (MW). The

memory window of a FeFET is simply the difference in threshold voltage between the off- and on-state transfer characteristics. However, the theoretical maximum of this quantity can also be determined from the ferroelectric material's P-V characteristics, as it is linked to the coercive voltage/field of the film. Equations 1 and 2 show how to compute the MW for a FeFET from its transfer characteristics and P-V characteristics, respectively.

$$MW = V_{t,off} - V_{t,on} \quad (1)$$

$$MW_{max} = 2 \cdot E_c \cdot t_{FE} \quad (2)$$

In Equation 2,  $t_{FE}$  denotes the thickness of the ferroelectric film. It is desirable for a FeFET to have a large memory window, as this is essentially a measure of how easily one can differentiate between storage values within the cell.

### III. EXPERIMENTAL DETAILS

An n-channel FeFET process flow has previously been developed at RIT to fabricate the transistor surrounding the ferroelectric material, as ferroelectric deposition has not always been possible at RIT [1], [4]. Once an ALD system was acquired by the institution, work was done to characterize the deposition of ferroelectric Al:HfO<sub>2</sub> with the tool and determine the necessary annealing/capping layer conditions [2], [3]. Integrating the work of [1]-[4] to develop an in-house n-channel FeFET process flow at RIT, comparing the electrical results of FeFETs fabricated solely at RIT to those fabricated with NaMLab deposited gate stacks and studying the impact of threshold adjustment on fabricated devices and their corresponding memory windows were of primary interest in this particular study. In order to achieve this, several processing splits were established. A tree diagram illustrating all processing splits of interest is shown in Figure 6.

The “gate stack” splits highlighted in orange were deposited at RIT while those highlighted in blue were deposited at NaMLab in Dresden, Germany. The red “V<sub>t</sub> adjustment” splits are indicative of negative threshold adjustment, while those in green imply positive adjustment. The respective species and implant doses for each of these splits is shown in the diagram. Threshold splits that are not color-coded did not receive a threshold adjustment implant. “FE” and “AFE” in Figure 6 are short for “ferroelectric” and “anti-ferroelectric,” respectively. Anti-ferroelectric films were also targeted to gain a better understanding of the influence of aluminum doping on the properties of the ALD Al:HfO<sub>2</sub> films. The lone wafer on the left of the diagram with un-doped HfO<sub>2</sub> is a reference wafer that

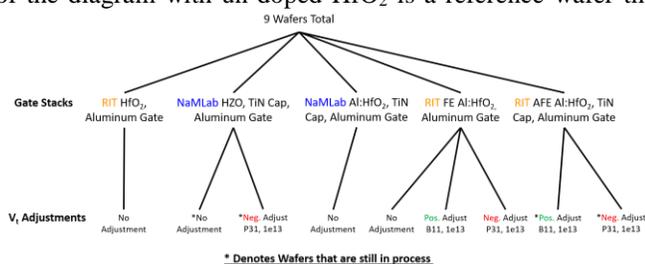


Fig 6. Tree diagram showing processing splits of interest

can be used for C-V analysis, so oxide charges within the deposited films can be studied/ modeled. Due to time constraints, only five of the nine splits were completed, leaving the other four in process to be completed at a later date.

## IV. RESULTS AND DISCUSSION

### A. Initial Results

Prior to polarizing the ferroelectric material within the gate stack, the transfer characteristics of the fabricated FETs were obtained using an HP 4145 parameter analyzer. In an effort to reduce the amount of ferroelectric domain switching, the gate was swept from -2.5V to 2.5V, much less than the -5V and 5V used to induce remnant polarization charge. The resulting transfer characteristics (linear scale) for a representative device from the non-threshold adjusted wafer are found in Figure 7.

As indicated by Figure 7, there appears to be modulation in current with increasing gate voltage, suggesting gate control has been established. However, the difference between what appears to be the on- and off-state drain currents is only a factor of ~10. In addition, the off-state leakage current is in the microamp range, which is fairly high. The mechanism/cause for this off-state leakage current was examined further and is discussed in more detail later in this section.

Despite the highly resistive response observed in the initial transfer characteristics of the devices, the impact of the threshold adjustment implant splits, as well as the ferroelectric behavior of the ALD deposited films, was still of interest. To test for ferroelectricity, the on- and off-state transfer characteristics of the FeFETs were obtained using the same parameter analyzer used to obtain the data in Figure 7. Starting with the on-state characteristics, the device under test (DUT) had its source and drain grounded before having its gate pulsed with 5V for 10ms. Following this pulse, the drain voltage was brought up to 0.1V and the gate was swept from 0.5V to 2V, or 1.5V to 3.5V, depending on the threshold voltage adjustment that the DUT experienced during processing. Immediately after this first sweep, the drain and source were again grounded and the gate was pulse with -5V for 10ms to obtain off-state transfer characteristics. After the pulse, the same sweep conditions were applied to the DUT and the two transfer curves were plotted on the same set of axes. The threshold voltages of each of the curves were obtained using the maximum slope method, and the memory window was computed using Equation 1. Ultimately, two of the three ferroelectric films deposited at RIT exhibited

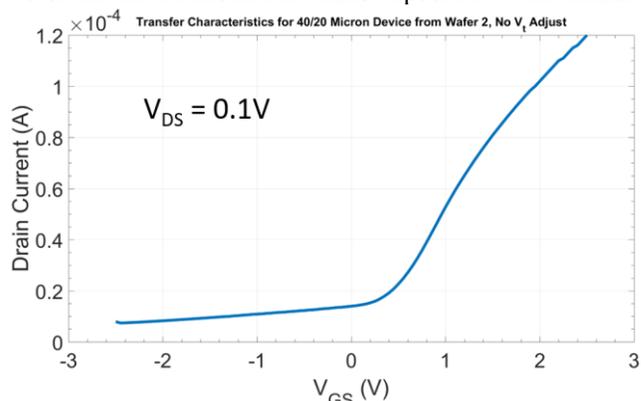


Fig 7. Transfer characteristics of a representative FeFET from non-threshold adjusted wafer

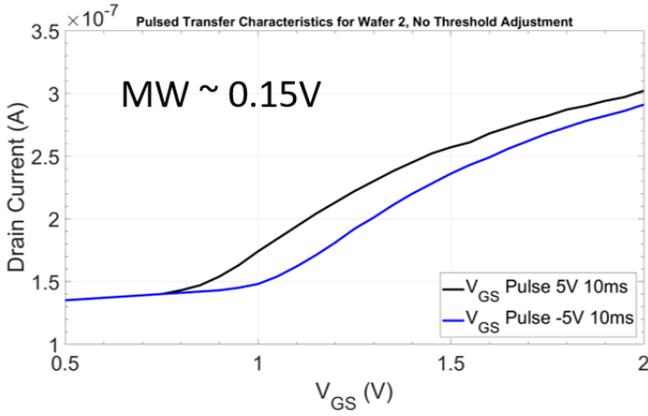


Fig 8. Transfer characteristics of a representative FeFET from non- $v_t$  adjusted sample shows a MW of  $\sim 0.15V$

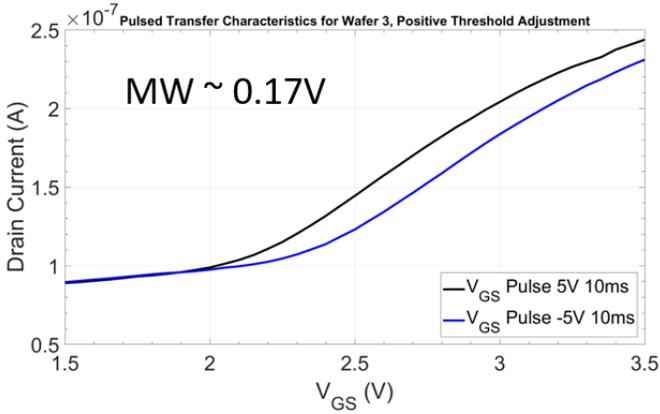


Fig 9. Transfer characteristics of a representative FeFET from positive  $v_t$  adjusted sample shows a MW of  $\sim 0.17V$

ferroelectric characteristics, and the threshold adjustment implants were found to shift both bistable transfer characteristics without degrading memory window. Ferroelectric transfer characteristics of representative FeFETs from the non-threshold adjusted sample and the positively adjusted sample are in Figures 8 and 9, respectively.

The memory windows measured on the RIT samples were found to be comparable to the memory window obtained for FeFETs on a wafer with Al:HfO<sub>2</sub> deposited by NaMLab, whose characteristics are displayed in Figure 10.

One interesting thing to note about the sample from NaMLab is that the blue and black curves, corresponding to the negative

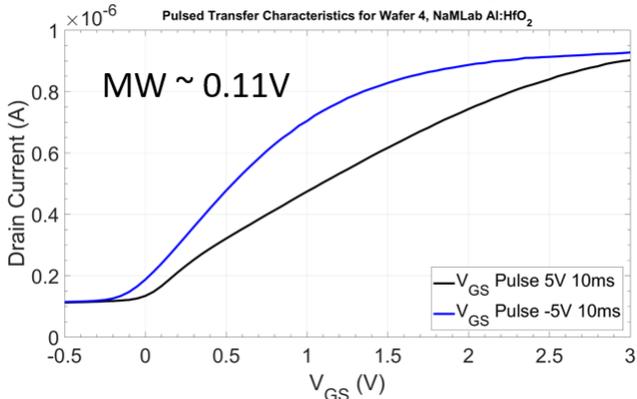


Fig 10. Transfer characteristics of a representative FeFET from NaMLab Al:HfO<sub>2</sub> sample shows a MW of  $\sim 0.11V$

and positive gate pulses, respectively, are oppositely oriented compared to the RIT samples. This suggests that the film from NaMLab may in fact be anti-ferroelectric, which could be further justified with polarization v. voltage measurements of capacitors incorporating the same material stack.

To check the effectiveness of the threshold adjustment implants, the transfer characteristics of similarly sized FeFETs on the negative threshold adjustment wafer, positive threshold adjustment wafer and non-threshold adjusted wafer were measured and compared. Figure 11 shows sample transfer characteristics for all three varieties appended on the same set of axes.

To estimate the expected threshold adjustment shift for both the positive and negative adjustment implants, the following equation was used:

$$\Delta V_t = \frac{q \cdot Dose}{C_{ox}} \quad (3)$$

In the Equation 3,  $q$  represents the elementary charge of an electron and “Dose” is the implanted dose in ions/cm<sup>2</sup>. To compute the oxide capacitance for the ferroelectric films, the relative permittivity reported for Al:HfO<sub>2</sub> in [2], and the actual film thickness of the deposited films, as measured through VASE, were used. Table 1 summarizes the theoretically calculated threshold shifts and those obtained through linear extrapolation as shown in Figure 11.

TABLE I. THEORETICAL AND EXPERIMENTALLY EXTRACTED THRESHOLD VOLTAGE SHIFTS FOR VARIOUS THRESHOLD ADJUSTMENT IMPLANTS

$V_t$ Adjustment Conditions	Extracted $V_t$ (V)	Shift from Control (V)	Theoretical Shift (V)
B11, $10^{13}$	1.65	+1.20	+0.78
P31, $10^{13}$	-0.70	-1.15	-0.78

The threshold voltage extracted for the control sample was 0.45V, which was used to compute the “shift from control” value in column three of the table. From Table 1, it is evident that the identical implant doses for both boron and phosphorous resulted in near symmetric shifts about the control sample, which is expected. However, the theoretically calculated threshold shifts and those extracted from the device wafers differ by about 50%. These discrepancies could be explained by the relative permittivity used for computing  $C_{ox}$  in Equation 3, which may not have been entirely accurate for the films deposited in this study; the films in this study have slightly

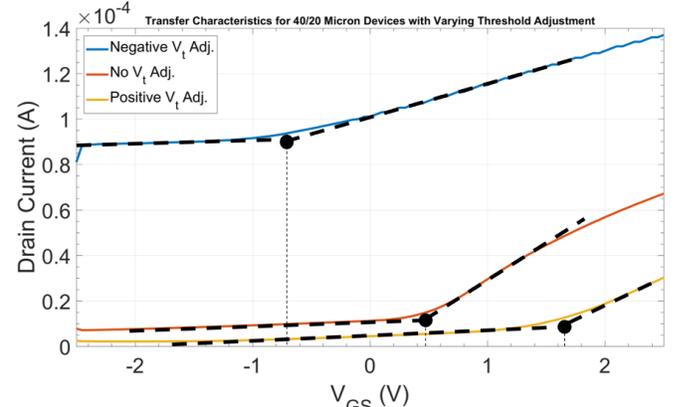


Fig 11. Transfer characteristics of FeFETs with each  $v_t$  adjustment treatment

different aluminum concentrations, and were deposited at different temperatures than those in [2]. Further differences could be explained by oxide charges present within the ferroelectric films, which could be extracted and modeled through C-V analysis.

### B. Off-state Leakage Investigation

Following initial characterization of the devices, various troubleshooting tests for causes of the off-state leakage current were conducted. Firstly, the starting wafer type was verified using “hot-probe” methodology. The highly resistive behavior seen in Figure 7 suggested that the starting substrate could have been n-type, which would have resulted in a resistive, n-type channel capped off on either end with higher doped n-type regions. After testing, however, the starting wafer was confirmed to be p-type, as desired for proper n-channel MOS fabrication. Next, the transfer characteristics were mapped across the wafer vertically and horizontally to determine whether or not this was a localized effect. Transfer characteristics for various columns of one wafer are appended onto the same set of axes for comparison in Figure 12. A similar plot for the rows of the same wafer was constructed in Figure 13.

From Figures 12 and 13, it can be concluded that the observed off-state leakage current was not a localized effect. Finally, two different parasitic I-V characteristics were measured to determine channel conductance with a floating gate and examine the leakage current between what were supposed to be “isolated” devices. To perform the former of the two tests, two probes were placed on the source and drain pads of one device and the drain current was measured while the voltage at the drain was swept between -5V and 5V; the gate was kept floating. Following this, two probes were placed at the source/drain pads of two adjacent devices, and the same sweep and measurement scheme employed for the first test was applied. The results from the first of the two tests can be seen in Figure 14 while the results of the second can be viewed in Figure 15.

The significant amount of current flow between the terminals of interest in these two tests suggests improper source/drain formation in the fabricated FeFETs. If there truly were n-type junctions present at the source and drain, current flow would have been blocked between adjacent devices. In addition, there would not have been current flow between the source and drain of a device with a floating gate. Instead, measurements indicate hundreds of microamps of current flow between source and drain within the channel of a device with a floating gate and tens of microamps of current flow between isolated devices. Perhaps the actual implanted dose was not what it was programmed to be on the tool, preventing the implanted species from overcoming the background doping concentration of the wafer after annealing. Alternatively, the species implanted may not have been the targeted P31, which could have been the result of tuning the analyzer magnet incorrectly.

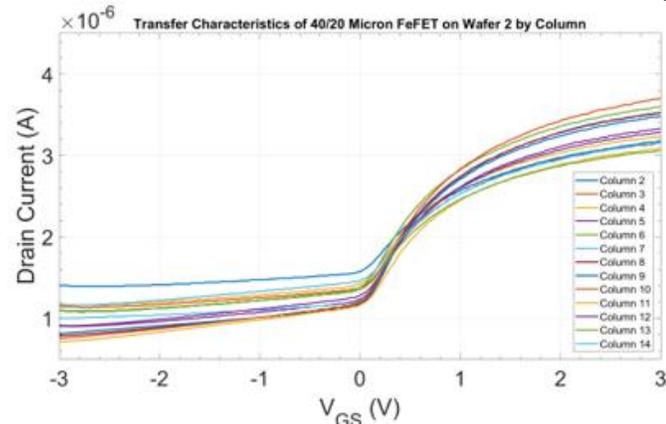


Fig 12. Transfer characteristics of FeFETs by column on non-threshold adjusted wafer

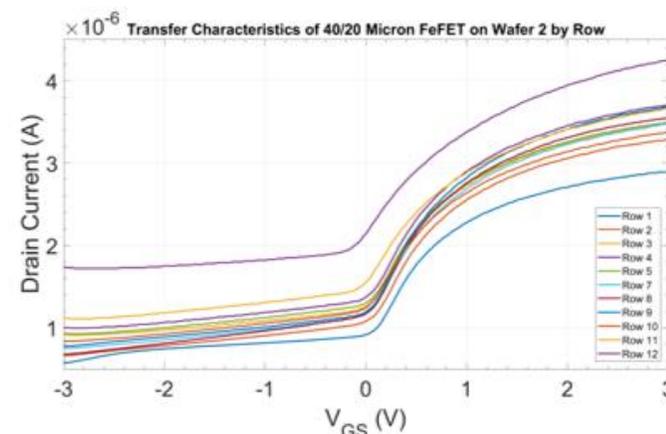


Fig 13. Transfer characteristics of FeFETs by row on non-threshold adjusted wafer

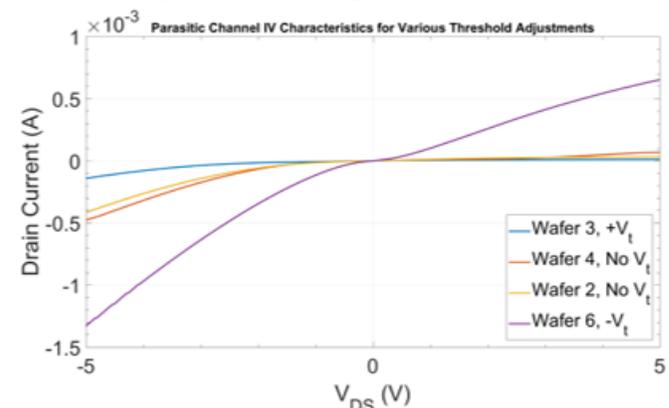


Fig 14. Measured drain current v. swept drain voltage for FeFET with floating gate.

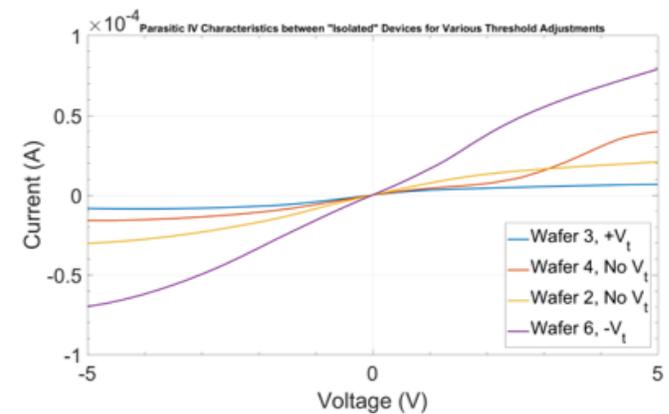


Fig 15. Measured leakage current between source/drain pads of adjacent FeFETs.

In an attempt to revive the source and drain regions of the current devices, it is of interest to remove the metal from a wafer, expose said wafer to a monolayer doping source, anneal it once doped, redeposit/pattern a new metal layer and retest the devices. In addition to potentially reducing the off-state leakage current observed in the current devices, this may provide for a new self-aligned source/drain doping process.

## V. CONCLUSIONS

Overall, improper source/drain formation is a likely candidate for the observed off-state leakage in fabricated devices. Incorrect dose processing and/or implantation of an inappropriate species, stemming from inadequate tuning of the analyzer magnet, would corroborate this theory. Nonetheless, two of the three RIT FeFET wafers demonstrated ferroelectric behavior in their transfer characteristics. In addition, all threshold adjustment implants investigated appear to have been successful, shifting both transfer characteristics of the FeFETs without degrading memory window. Further examination of the types of oxide charges present within the deposited films and/or the modeling of the relative permittivity of the deposited films is needed to explain the discrepancies between calculated and experimentally extracted threshold voltage shifts.

In the future, it may be advantageous to implement more advanced CMOS processing techniques into this process flow, such as monolayer doping and low-temperature silicide formation, both of which have been demonstrated at RIT. The former of the two processes also poses a potential method for reviving the sources and drains of the devices presented in this work. The deposition of ferroelectric films at RIT also paves the way for more advanced device architectures utilizing these materials, such as negative-capacitance FETs and ferroelectric tunnel junctions.

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