Biristor Array Investigation

By Jeremiah Leit

A device that can be used for hardware based encryption and neural network computing
What is a Biristor?

• A biristor is a two terminal device with two different modes of operation.
  1) Silicon Controlled Rectifier Latch
  2) Neuron Fire mode

• It is essentially a floating base Bipolar Junction Transistor.

• The device can be either NPN or PNP however, in this project I am fabricating NPN devices.

• It observes an avalanche effect which changes the internal resistance of the device.

• This makes it essentially a type of resistor with volatile memory or memristor.
What do the I-V characteristics look like?

Silicon Controlled Rectifier Latch
module of operation

Leaky Latch/Un-latch or
Neuron-Fire
module of operation


Jin-Woo Han; M. Meyyappan
Biristor applications?

- A latching change in the resistance value of the device which would allow it to be used as a memory element.

- The neural spiking method can be used to create neural networks that are designed to compute information more in manner more like a human brain than a microprocessor and possibly use less energy.

- If scaled properly the diode isolation from both directions as well as that caused by the dielectric TEOS around the device could create quantum dots.
What are my project goals?

- Fabrication of Biristors
  1. Mask Design
  2. Process Design
  3. Fabrication
  4. Electrical Testing
- Compare Measured Results to Published Results
- Determine Relation Between Scaling and I-V Characteristics
The Ion Implant Steps

• Replicate the device fabricated by Jin-Woo Han.
  Consulted for ion implantation details and other processes.

• Three Implant steps
  Shallow arsenic implant
    \(3 \times 10^{15} \text{ cm}^{-3} \text{ 80keV}\)
  Boron implant
    \(8 \times 10^{13} \text{ cm}^{-3} \text{ 100keV}\)
  Deep phosphorous implant
    \(1 \times 10^{14} \text{ cm}^{-3} \text{ 500keV}\)

Implant done by Innovion
Mask Design For Individual Biristor
Biristor layout with probe pad

100x100 micron metal probe pad

Biristor
Mask Layout of Biristor Array

- Pillar Dimensions range from 1.1um to 2.7um
- Contact Dimensions are 0.5um
- Main Array Area

Resistor testing area
Ion Implantation Profiles and Etching

Monolayer Doping was done on two wafers whose fabrication was not completed.

Negative photoresist

n emitter

p base

n collector

P-Si

Etch silicon just to reach n type collector ~ 500nm

n emitter is Arsenic doped

p base is boron doped

n collector is phosphorus doped

Etch 500nm Si

Monolayer Doping was done on two wafers whose fabrication was not completed.
Pillar Structure Formed After Etching

1.1um, 1.7um, 2.2um and 2.7um

Boron doped wafer

Phosphorus

Arsenic

Boron

silicon
Oxide Deposition Over Pillar
Contact Cuts

0.5um Contact

Arsenic
Boron
Phosphorus
SiO₂

Boron doped wafer
silicon
Final Device

- Silicon
- Phosphorus
- Boron
- Arsenic
- SiO₂
- Metal
- Boron doped wafer

Phosphorus layer above silicon.

Boron doped wafer is present under the layers.
Completed Biristor Device

Mask Layout

Contacts

Metal

Arsenic and Boron

Phosphorus

2.7umX2.7um Pillar

Biristor after the Metal Etch
SEM Micrographs of the Device

1.1μm X 1.1μm Device

Tool used JEOL JSM-IT100 LA

Courtesy of Bruce E. Kahn, AMPrint Center
Rochester Institute of Technology
Measured I-V Characteristic

Hysteresis of Bistator (2.7μm × 2.7μm)

Current [pA]

-10.0  -7.5  -5.0  -2.5  0.0  2.5  5.0  7.5  10.0

voltage [V]

10^{-1}  10^{0}  10^{1}  10^{2}  10^{3}  10^{4}  10^{5}

Abs. of current [pA]

-10.0  -7.5  -5.0  -2.5  0.0  2.5  5.0  7.5  10.0

voltage [V]

Forward pass
Backward pass
Conclusions

- During the process of fabricating the device several obstacles were overcome. Primarily the determination of how to etch the silicon pillars, how to get proper contact cut selectivity when using a dry etch tool and most importantly how to resolve .5um aluminum traces for wires. Additionally the mask design was difficult because design rules had to be determined. Proper probe spacing was achieved without the use of a template.

- Overall, these efforts resulted in a device that exhibited a biristor like I-V curve that displayed path dependent resistance. The reason for this discrepancy is yet to be determined.

- This was the first Biristor made at RIT.
Acknowledgements

• Dr. Kurinec, Dr. Pearson, Dr. Ewbank
• Dr. Bruce Kahn of AMPrint Center RIT (SEM images)
• Patricia Meller, SMFL
• Sean O’Brien, SMFL
• John Nash, SMFL
• Jordan Merkel
• I would also like to thank the Class of 2019 for all their support and encouragement!