Biristor Array Investigation

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Project Objectives

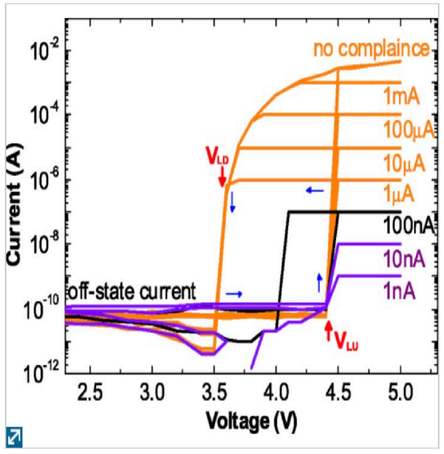
The goal of this project was to fabricate and test a working Biristor device to compare I-V characteristics during scaling with a reference paper. Additionally there was the goal of simulating the devices and comparing actual with simulated results.

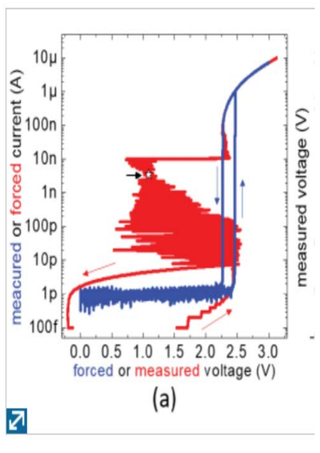
Motivation

The importance of this project stems from the possible usage of the biristor for hardware based encryption due to its hysteresis effects when voltage driven. It can also be used for neural network computing when current driven. Neural network based devices increase the efficiency of computation due to non-standard logic.

Biristor Operation

The Biristor works off the principle of the “Avalanche effect” in which charge carriers build up and at a certain breakdown voltage reduce the resistance through the device. These characteristics are shown below in data that was created by the reference paper.



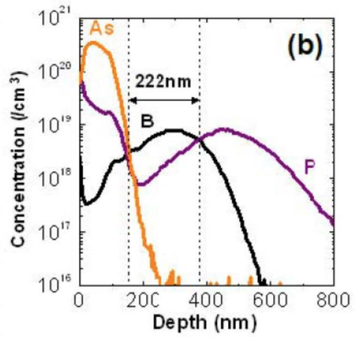


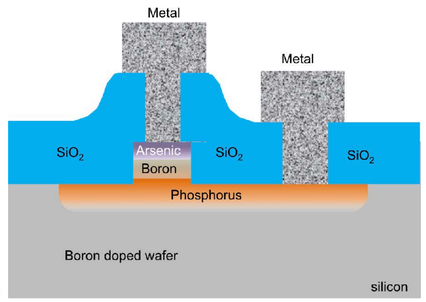
Device Layout

Biristor Schematic:

The pillar dimensions were as follows: 1.1μm^2, 1.7μm^2, 2.2μm^2 and 2.7 μm^2

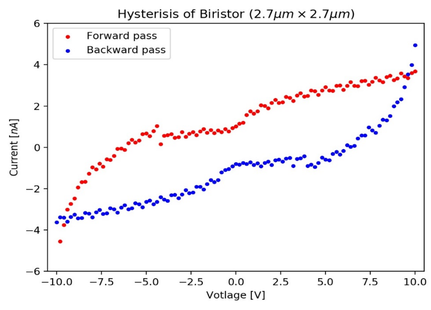
The implant profile was obtained from Dr. Han whose paper was referenced for this project.





Etch 500nm Si

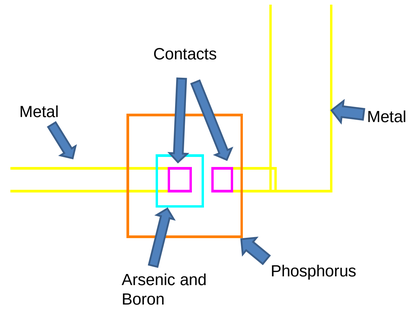
I-V Characteristics

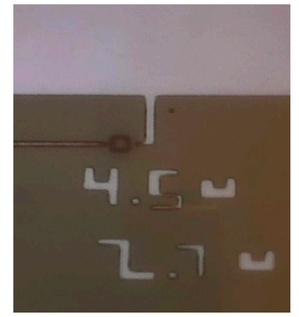


The top curve is the sweep from -10V to 10V and the bottom curve is sweep from 10V to -10V. It can be seen from the curves that the different directions in sweeps will yield current pathways. This is useful because, the device will operate in a different way based on the method through which it is biased.

Device Image

Below is a functioning device that has a pillar size of 2.7um.





Conclusions

Overall, during the course of this project only one device was successfully tested. It resulted in an IV characteristic that was interesting in the sense that it had non-linear path dependent resistance.

Future Work

Dr. Kurinec plans to continue the fabrication of the Birisitors however, she will use monolayer doping on them to decrease the R value of the contacts. Two wafers have been brought to MLD contact cuts in this way but the biristor fabrication has yet to be finished. The mask will be modified in order to increase the ease of fabrication.

References

J. Han and M. Meyyappan, "Trigger and Self-Latch Mechanisms of n-p-n Bistable Resistor," in *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 387-389, March 2014.

Acknowledgements

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