

CAPPING LAYERS FOR INCREASED THERMAL STABILITY OF IGZO THIN-FILM TRANSISTORS

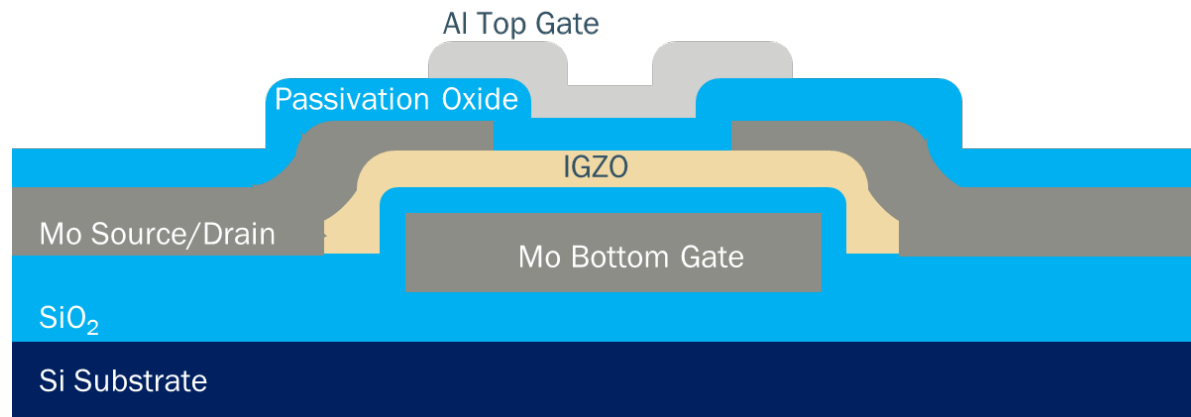
Jason Konowitch

Indium-Gallium-Zinc Oxide

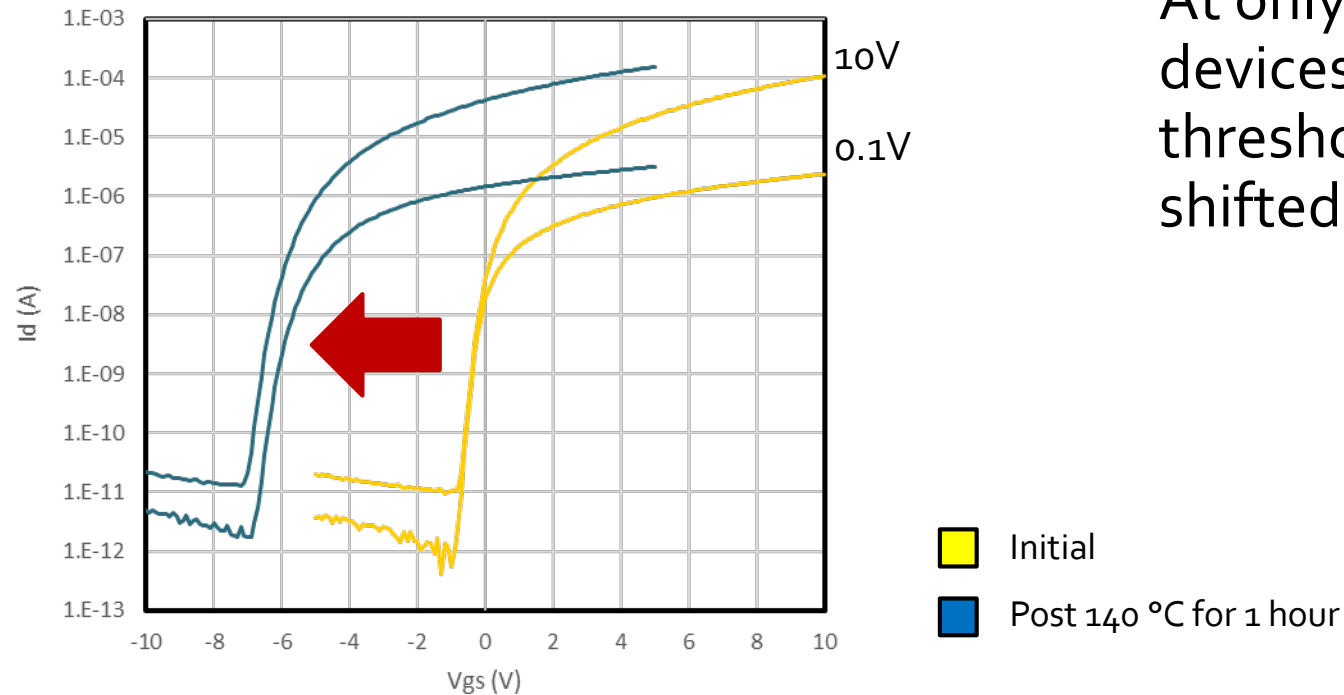
- Research being done is to show performance capabilities of IGZO devices
 - Theoretically have higher mobility than thin-film-transistors made with amorphous Silicon at a price much lower than the cost of devices using crystalline Silicon
- These devices have been fabricated in the past at RIT but, over time, devices were no longer performing well, so a baseline process had to be re-established
- There are device stability issues that must be worked out which commonly attributed to the absorption of water into the passivation layer
- Adding different capping layers might yield more stable devices due to behaving as a better water barrier, inclusion of the capping layer has shown promise in the past

Why Do the Devices Need to be Thermally Stable?

- After fabrication of the TFTs, further processing must be done to make functional flat panel displays
- Processing requires devices to have their temperature raised without compromising the devices



Thermal Stability Issue



At only 140 °C,
devices can have their
threshold voltage
shifted by ~6V

Process Flow

■ Point of Split

- Label Wafers
- RCA Clean
- Oxide Growth
- Mo Sputter
- Measure film thickness
- Measure sheet resistance
- Measure bow
- Gate lithography
- Gate Etch
- Resist Strip
- TEOS deposition
- Densify TEOS
- IGZO deposition (at Corning)
- MESA lithography
- IGZO Etch
- Resist strip
- S/D, gate pad lift-off lithography
- S/D, gate pad metal deposition
- Lift-off
- Passivation/top gate dielectric TEOS
- **Anneal**
- **Capping layer deposition**
- Contact Lithography
- Contact Etch
- Resist strip
- Top gate lift-off lithography
- Top gate metal deposition
- Metal lift-off

Key Processing Points and Splits

- IGZO Film
Thickness
50nm
- Anneal
Times between 3-8hr
- Capping Layer
Deposition temperature (Also effects thickness)
100, 150, 200, 250°C
Material
Aluminum Oxide

Starting Wafer

Si Substrate

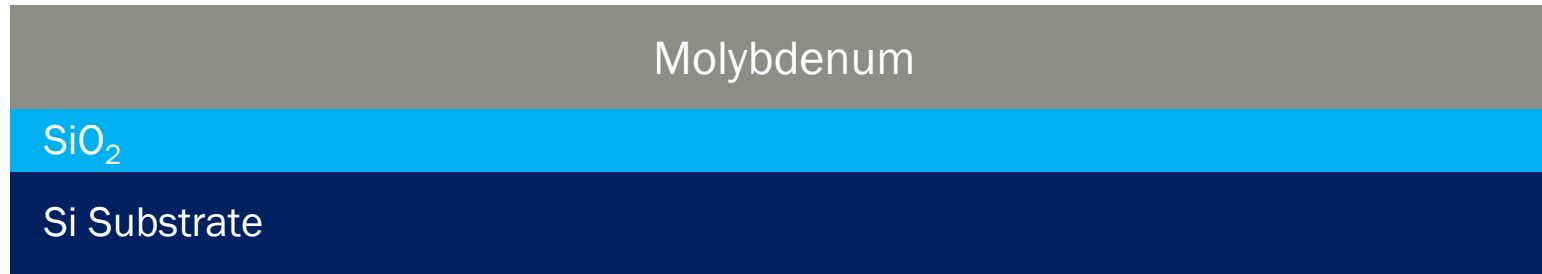
Oxide Growth

650nm Oxide

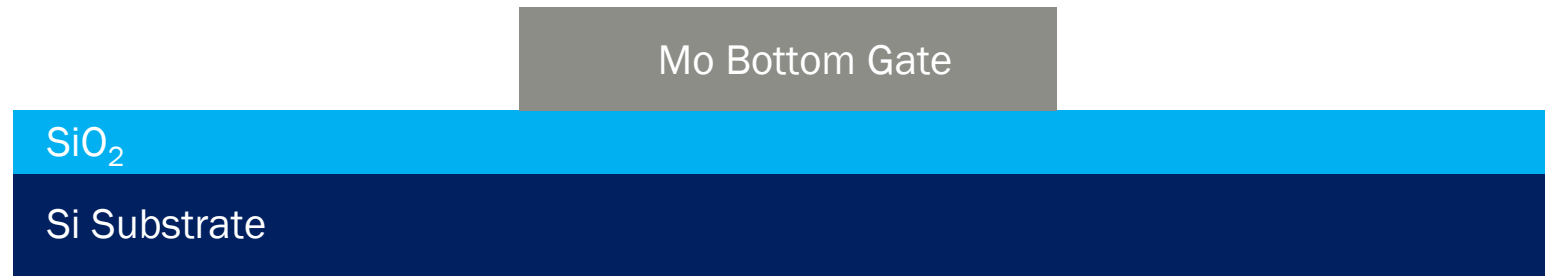


Molybdenum Sputter

50nm Moly



Bottom Gate Lithography and Etch

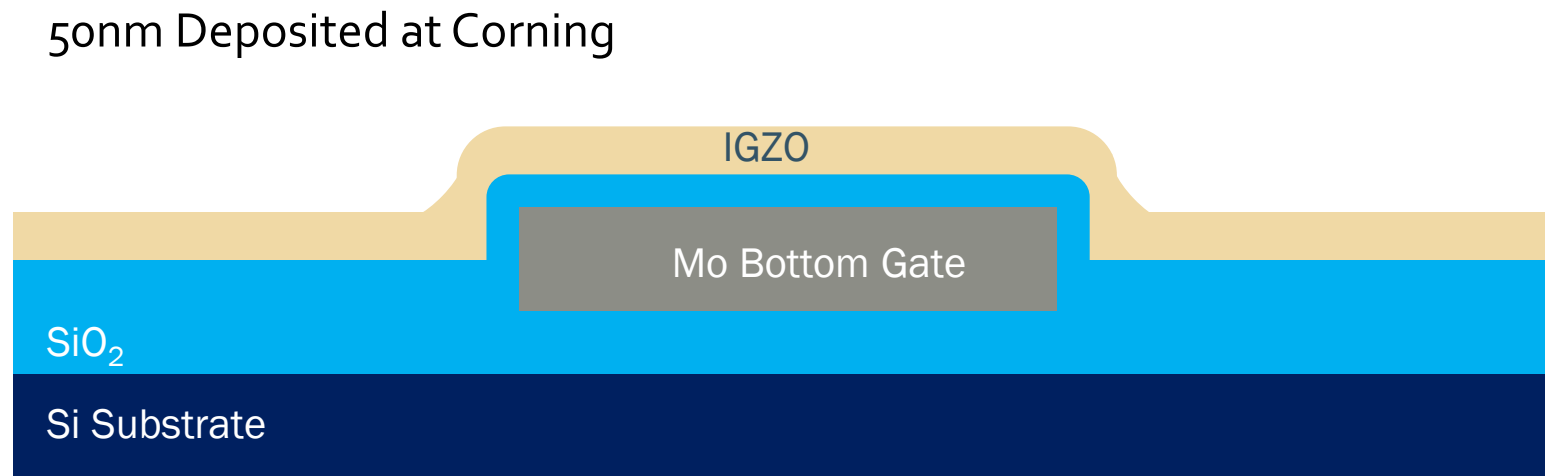


TEOS Oxide Deposition

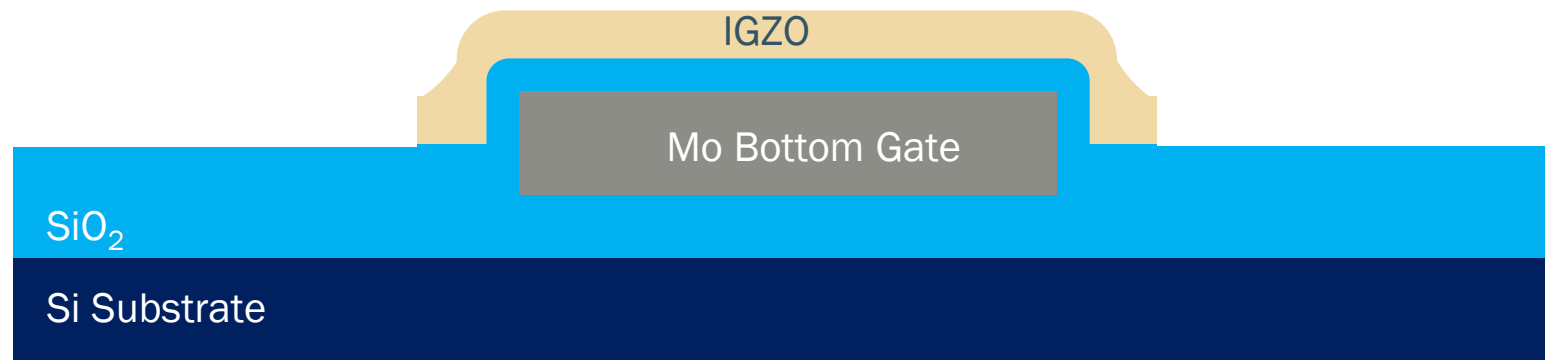
50nm Bottom Gate Dielectric



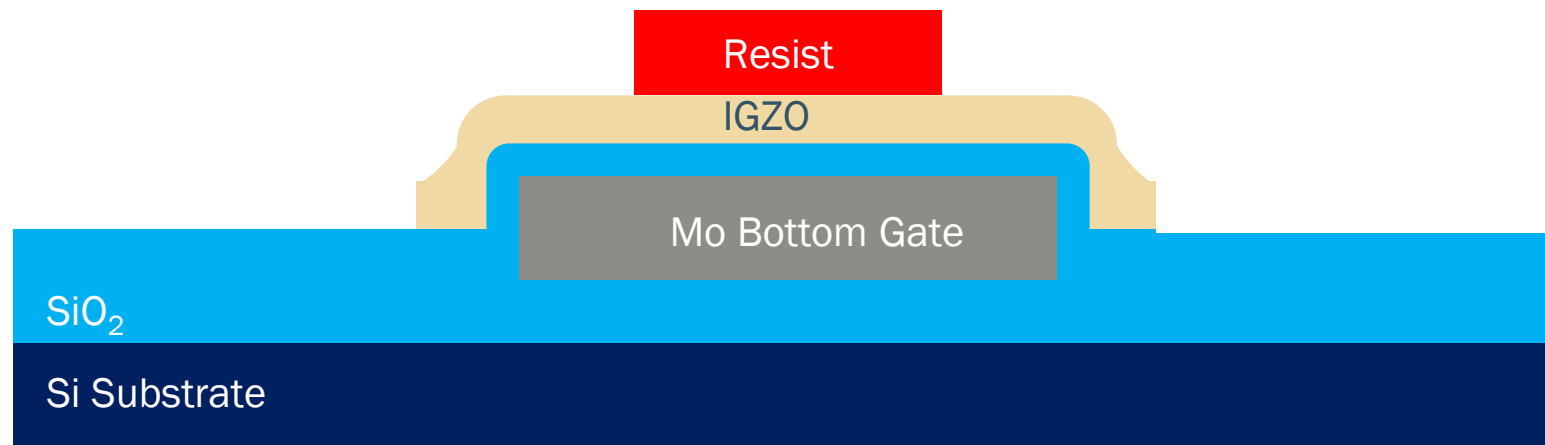
IGZO Deposition



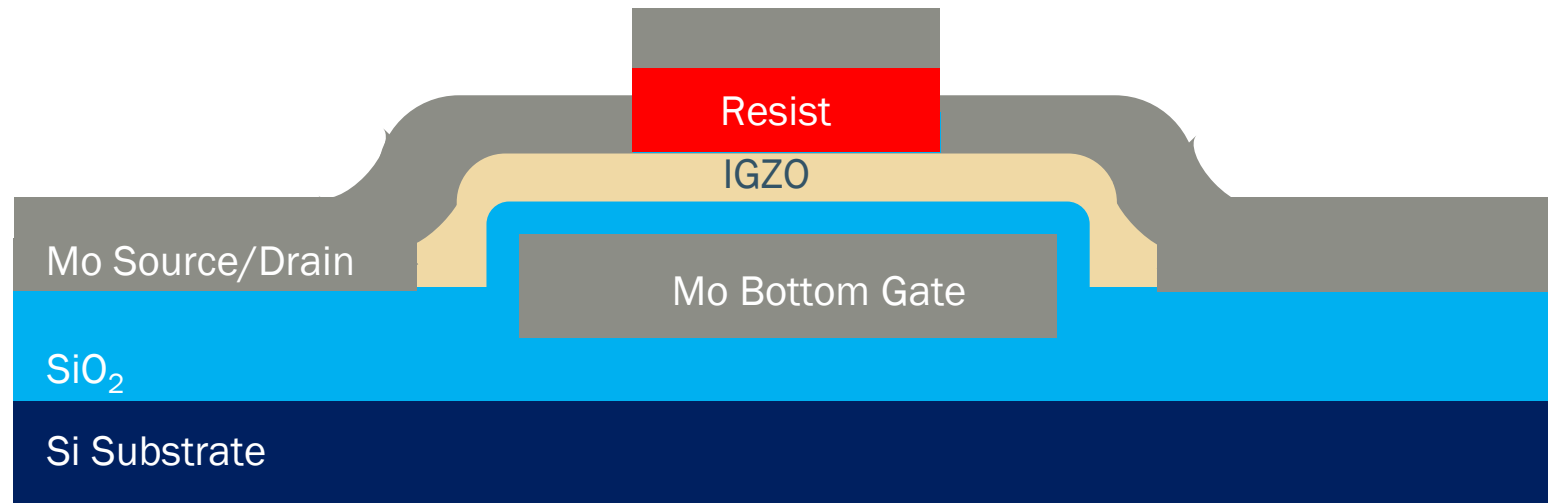
IGZO MESA Lithography and Etch



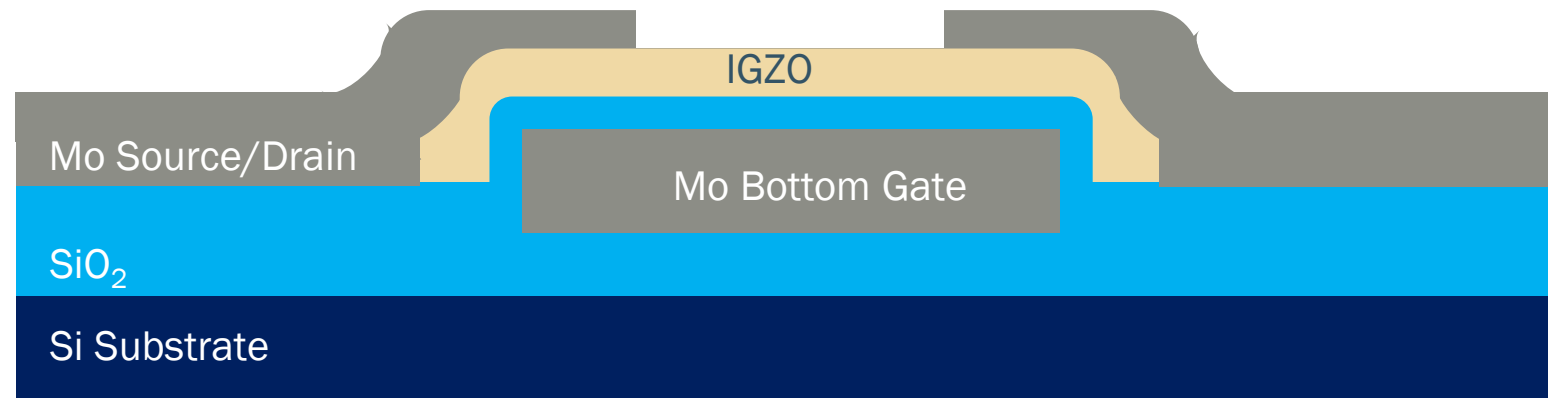
Source/Drain Lift-off Lithography



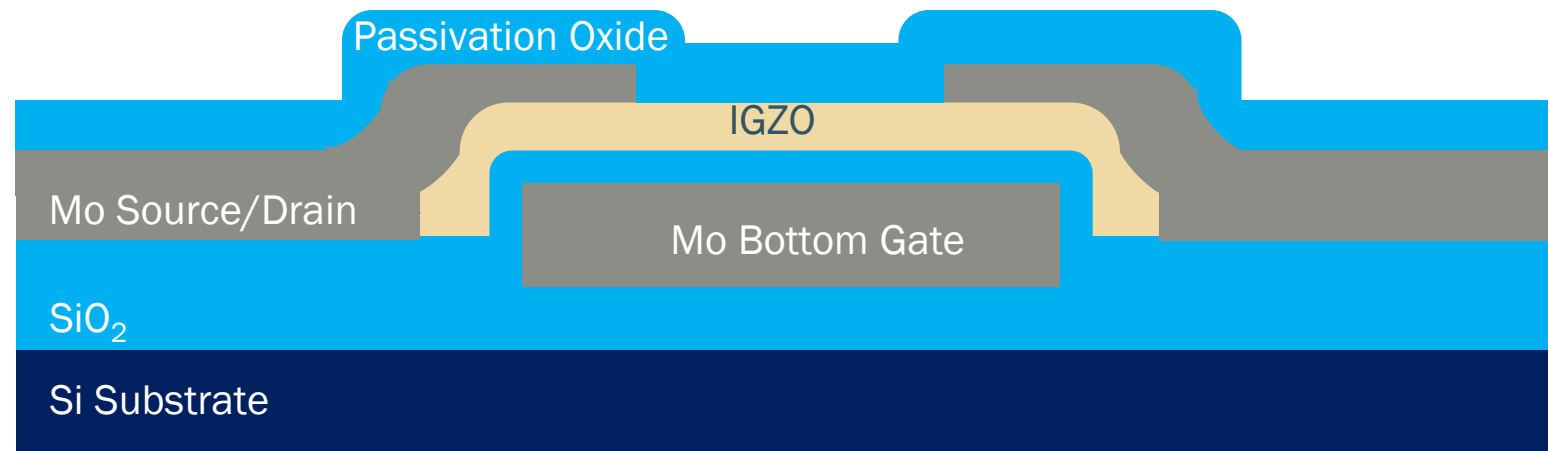
Source/Drain Deposition



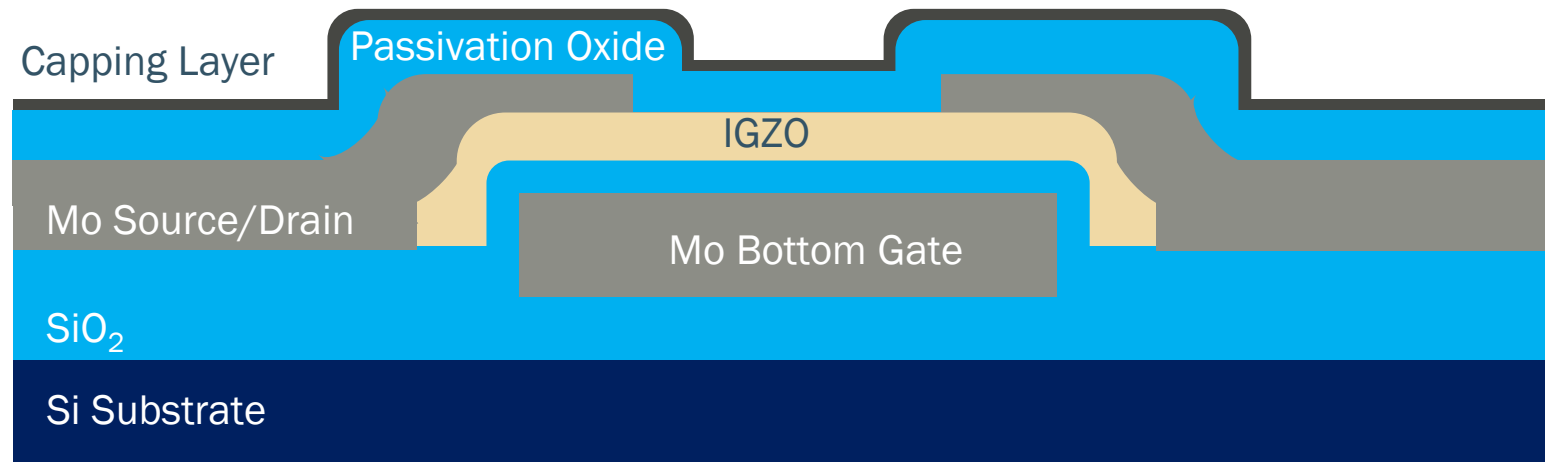
Source/Drain Lift-off



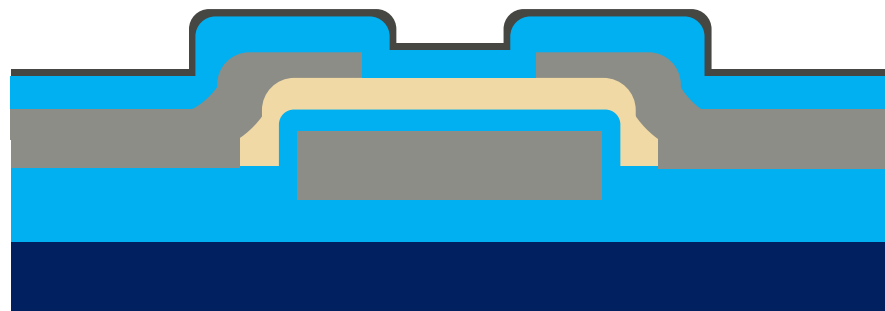
TEOS Oxide Deposition



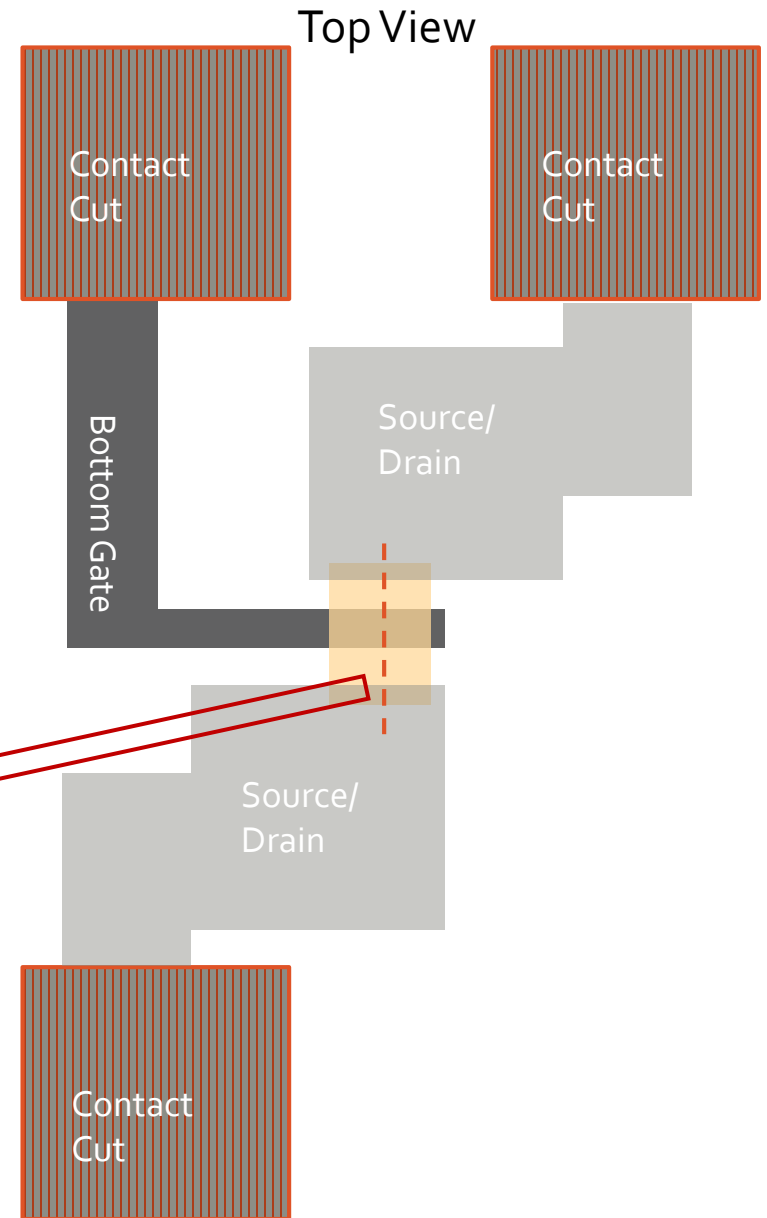
Capping Layer Deposition



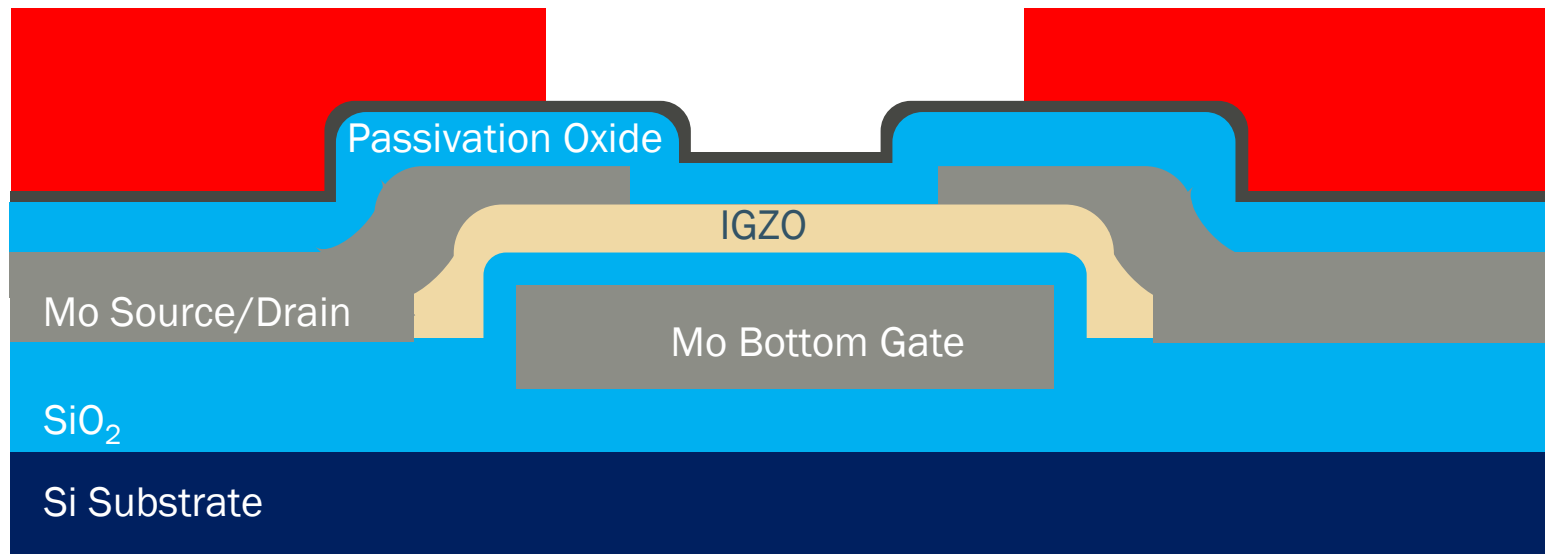
Contact Cut Etch



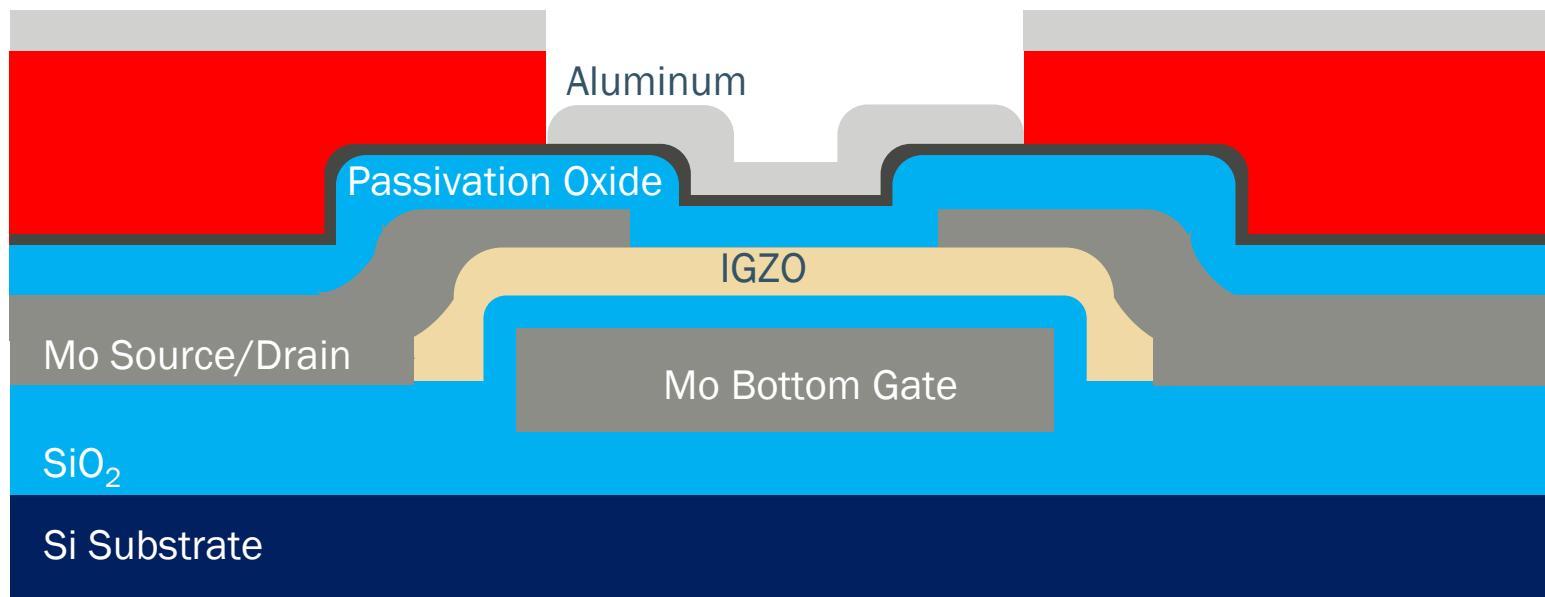
Cross Section



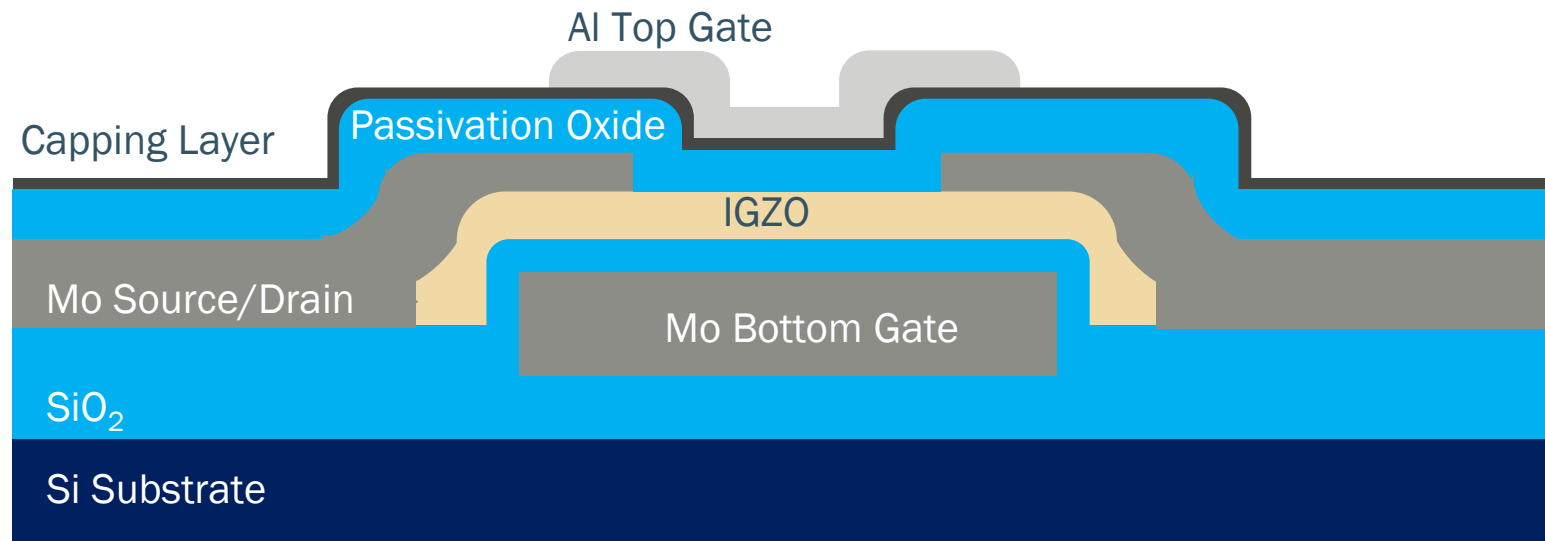
Top Gate Lift-off Lithography



Top Gate Deposition



Top Gate Lift-off



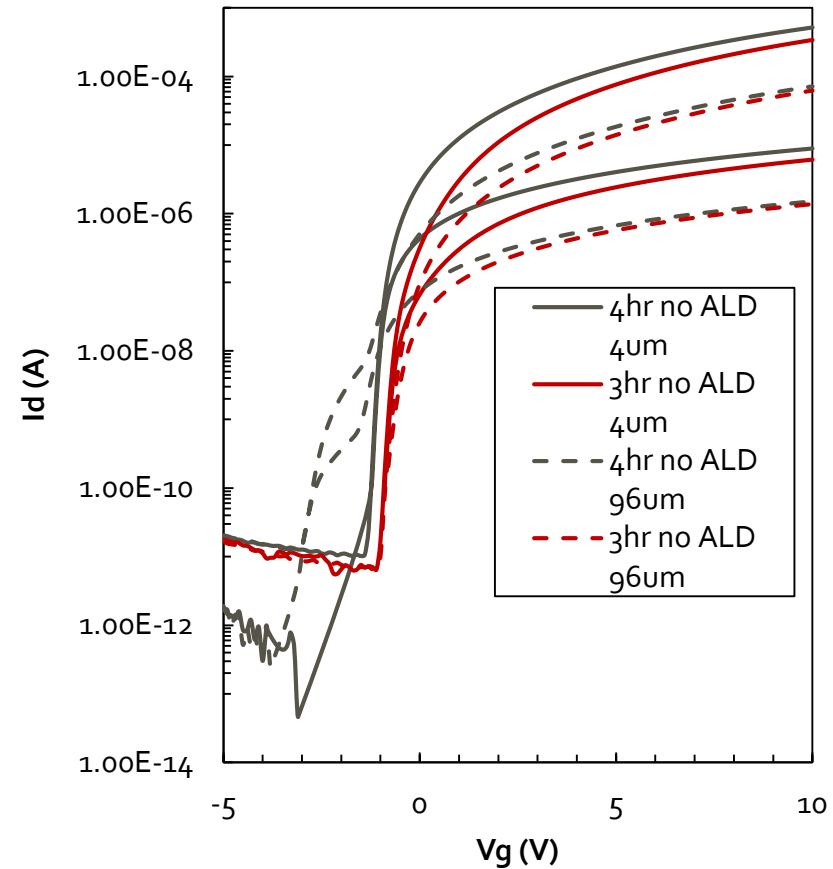
Testing Thermal Stability

- Completed wafers have initial testing done
- The wafers are then placed on a hotplate for an hour at a given temperature (normally 140-200°C)
- The same devices are tested and overlaid onto the initial plots for comparison

Results

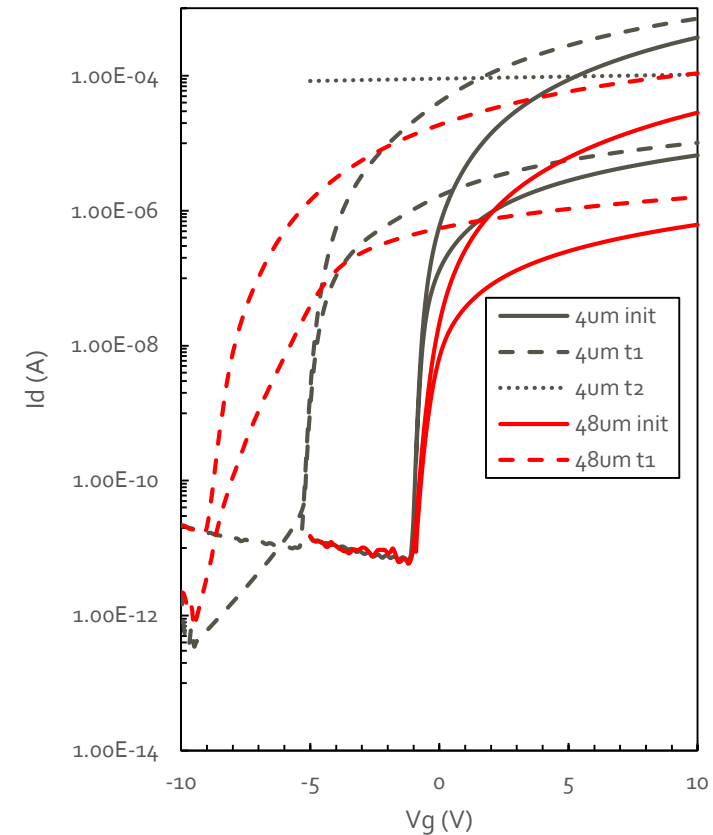
Response to anneal time (3&4 hours)
without ALD capping layer

- Short channel devices show similar results
- Large devices show distortion only on the wafer with the 4 hour anneal
- Performance trends were noticed based on location on the wafer



Results- Length Dependency

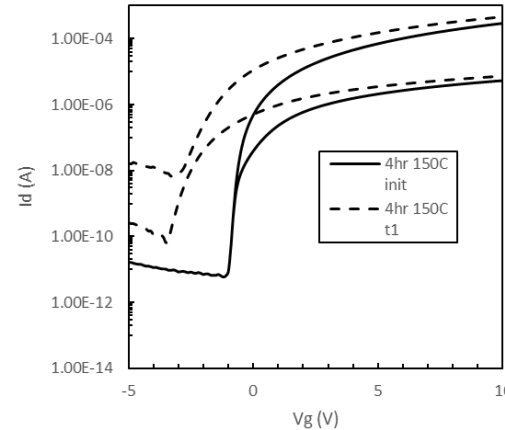
- Short channel devices were more resistant to shifting during thermal stress
- Long channel devices show greater shift and are show separation between low and high drain bias



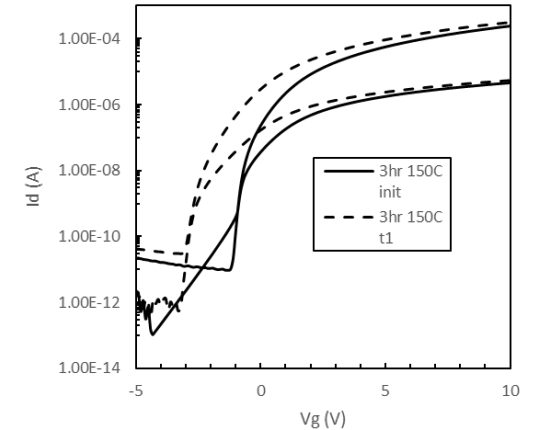
Results- ALD Treatments

- Different anneal and process treatments showed different responses to thermal stress

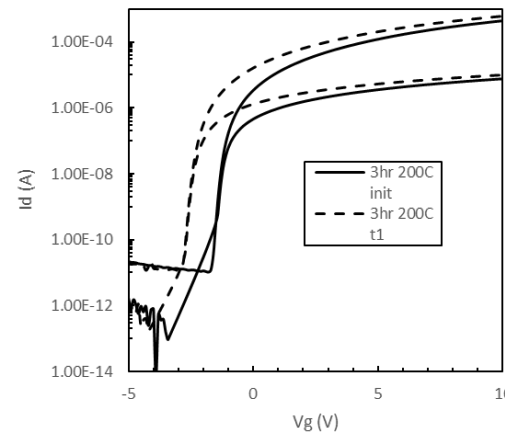
4 hour anneal with 150°C ALD



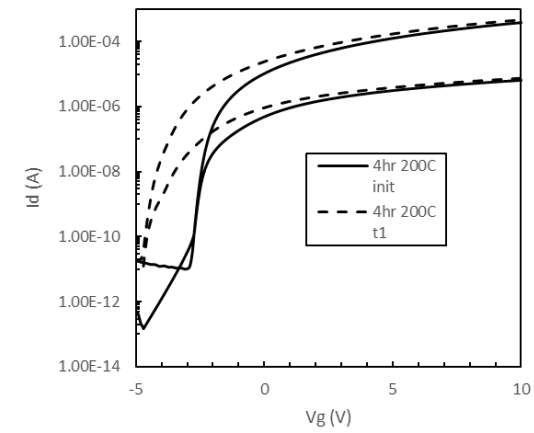
3 hour anneal with 150°C ALD



3 hour anneal with 200°C ALD



4 hour anneal with 200°C ALD



Results- ALD Treatments

- Voltage shift extracted from I-V curves where drain current was 1nA
- The treatment of 3 hour anneal with 200°C ALD deposition showed greatest resistance

	4μm	12μm	24μm	48μm
3hr 150°C	-1.7V	-1.4V	-1.5V	-2V
3hr 200°C	-1.2V	-1V	-1.85V	-2V
4hr 150°C	-2.4V	-1.4V	-1.5V	-1.8V
4hr 200°C	-3.2V	-2V	-2V	> -5V

Conclusions

- Channel length was found to influence thermal stability; shorter devices were shown to be more thermally stable with a smaller voltage shift.
- This length dependence was less pronounced in devices fabricated with an ALD Al₂O₃ capping layer.
- The 3 hour anneal with the 200°C ALD capping layer showed greatest promise in yielding thermally stable devices.
- Despite improvement, further investigation is required to remove this residual shift and permit higher temperature exposure (e.g. 200 °C).

Future Work

- Increased device sampling to identify dependence on wafer location
- Increase passivation oxide thickness
 - Challenge: coupled with anneal process
- Investigate other capping layer material options

Acknowledgements

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