CAPPING LAYERS FOR INCREASED THERMAL STABILITY OF IGZO THIN-FILM TRANSISTORS

Jason Konowitch
Indium-Gallium-Zinc Oxide

- Research being done is to show performance capabilities of IGZO devices
  - Theoretically have higher mobility than thin-film-transistors made with amorphous Silicon at a price much lower than the cost of devices using crystalline Silicon

- These devices have been fabricated in the past at RIT but, over time, devices were no longer performing well, so a baseline process had to be re-established

- There are device stability issues that must be worked out which commonly attributed to the absorption of water into the passivation layer

- Adding different capping layers might yield more stable devices due to behaving as a better water barrier, inclusion of the capping layer has shown promise in the past
Why Do the Devices Need to be Thermally Stable?

• After fabrication of the TFTs, further processing must be done to make functional flat panel displays

• Processing requires devices to have their temperature raised without compromising the devices
Thermal Stability Issue

At only 140 °C, devices can have their threshold voltage shifted by ~6V.
Process Flow

- Label Wafers
- RCA Clean
- Oxide Growth
- Mo Sputter
- Measure film thickness
- Measure sheet resistance
- Measure bow
- Gate lithography
- Gate Etch
- Resist Strip

- TEOS deposition
- Densify TEOS
- IGZO deposition (at Corning)
- MESA lithography
- IGZO Etch
- Resist strip
- S/D, gate pad lift-off lithography
- S/D, gate pad metal deposition
- Lift-off

- Passivation/top gate dielectric TEOS
- Anneal
- Capping layer deposition
- Contact Lithography
- Contact Etch
- Resist strip
- Top gate lift-off lithography
- Top gate metal deposition
- Metal lift-off

Point of Split
Key Processing Points and Splits

- IGZO Film
  Thickness
  50nm

- Anneal
  Times between 3-8hr

- Capping Layer
  Deposition temperature (Also effects thickness)
  100, 150, 200, 250°C

Material
  Aluminum Oxide
Starting Wafer

Si Substrate
Oxide Growth

650nm Oxide

$\text{SiO}_2$

Si Substrate
Molybdenum Sputter

50nm Moly

- Molybdenum
- SiO₂
- Si Substrate
Bottom Gate Lithography and Etch

Si Substrate

Mo Bottom Gate

SiO₂

Si Substrate
TEOS Oxide Deposition

50nm Bottom Gate Dielectric

SiO₂

Mo Bottom Gate

Si Substrate
IGZO Deposition

50nm Deposited at Corning

`Si Substrate`

`Mo Bottom Gate`

`SiO₂`

`IGZO`
IGZO MESA Lithography and Etch

Si Substrate

Mo Bottom Gate

SiO₂

IGZO
Source/Drain Lift-off Lithography

Si Substrate
Mo Bottom Gate
SiO₂
IGZO
Resist
Source/Drain Deposition
Source/Drain Lift-off
TEOS Oxide Deposition
Capping Layer Deposition

- Capping Layer
- Passivation Oxide
- IGZO
- Mo Bottom Gate
- Mo Source/Drain
- SiO₂
- Si Substrate

5/10/2019
Contact Cut Etch
Top Gate Lift-off Lithography
Top Gate Deposition

37th Annual Microelectronic Engineering Conference – Rochester Institute of Technology-Jason Konowitch

5/10/2019
Top Gate Lift-off

- Si Substrate
- Capping Layer
- Passivation Oxide
- Mo Bottom Gate
- Mo Source/Drain
- IGZO
- Al Top Gate
- SiO₂
Testing Thermal Stability

• Completed wafers have initial testing done

• The wafers are then placed on a hotplate for an hour at a given temperature (normally 140-200°C)

• The same devices are tested and overlaid onto the initial plots for comparison
Results

Response to anneal time (3&4 hours) without ALD capping layer

- Short channel devices show similar results
- Large devices show distortion only on the wafer with the 4 hour anneal
- Performance trends were noticed based on location on the wafer
Results - Length Dependency

• Short channel devices were more resistant to shifting during thermal stress

• Long channel devices show greater shift and are show separation between low and high drain bias
Results - ALD Treatments

• Different anneal and process treatments showed different responses to thermal stress.
Results- ALD Treatments

• Voltage shift extracted from I-V curves where drain current was 1nA

• The treatment of 3 hour anneal with 200°C ALD deposition showed greatest resistance

<table>
<thead>
<tr>
<th>Time</th>
<th>Temperature</th>
<th>4µm</th>
<th>12µm</th>
<th>24µm</th>
<th>48µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>3hr</td>
<td>150°C</td>
<td>-1.7V</td>
<td>-1.4V</td>
<td>-1.5V</td>
<td>-2V</td>
</tr>
<tr>
<td>3hr</td>
<td>200°C</td>
<td>-1.2V</td>
<td>-1V</td>
<td>-1.85V</td>
<td>-2V</td>
</tr>
<tr>
<td>4hr</td>
<td>150°C</td>
<td>-2.4V</td>
<td>-1.4V</td>
<td>-1.5V</td>
<td>-1.8V</td>
</tr>
<tr>
<td>4hr</td>
<td>200°C</td>
<td>-3.2V</td>
<td>-2V</td>
<td>-2V</td>
<td>&gt;</td>
</tr>
</tbody>
</table>
Conclusions

- Channel length was found to influence thermal stability; shorter devices were shown to be more thermally stable with a smaller voltage shift.

- This length dependence was less pronounced in devices fabricated with an ALD Al$_2$O$_3$ capping layer.

- The 3 hour anneal with the 200°C ALD capping layer showed greatest promise in yielding thermally stable devices.

- Despite improvement, further investigation is required to remove this residual shift and permit higher temperature exposure (e.g. 200 °C).
Future Work

- Increased device sampling to identify dependence on wafer location
- Increase passivation oxide thickness
  - Challenge: coupled with anneal process
- Investigate other capping layer material options
Acknowledgements

• Dr. Karl Hirschman
• Muhammad Salahuddin Kabir, Rahnuma Rifat Chowdhury
• Corning Inc.
• Dr. Robert Pearson, Dr. Dale Ewbank
• SMFL Staff
• Class of 2019