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Capping Layers for Increased Thermal Stability of IGZO Thin-Film Transistors

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Project Objectives

Goal: To investigate the effects of encapsulation layers on the performance and stability of Indium-Gallium-Zinc-Oxide thin film transistors and to re-establish the baseline process of the TFT fabrication.

An ideal encapsulation layer will not negatively impact the I-V characteristics of the device while also providing resistance to thermal stress.

Motivation

IGZO TFTs are proving to be a viable alternative for TFTs that utilize amorphous silicon (a-Si) or polycrystalline silicon (poly-Si) in high performance display applications. IGZO is a happy medium between the two silicon type devices because it is less expensive than the high mobility poly-Si, but still has a higher mobility than the low-cost a-Si.

Despite its advantages, IGZO has downsides; one of which is its susceptibility to change when the device is put under thermal stress. The electrical characteristics can be greatly shifted or distorted at temperatures above 100 °C, which is bad for industrial applications which require further processing of fabricated TFTs at elevated temperatures.

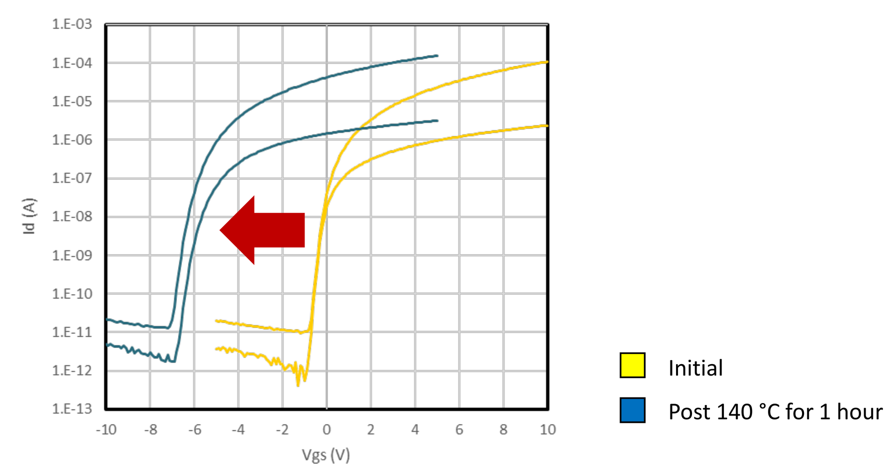

Fig. 1: A 24um device which shows a left shift and some distortion after being subjected to 140 °C for one hour.

Hypothesis for Thermal Instability

IGZO is negatively effected by any exposure to water, therefore the presence of any water within the SiO_2 layer of a TFT will cause the device to be more sensitive to stress conditions.

The Passivation Oxide will absorb water molecules, allowing them to reach the IGZO that it is ideally protecting, resulting in enhanced electron concentration due to donor-like behavior. Reaction of H_2O with the top-gate electrode may also result in the liberation of monatomic hydrogen which has also been characterized as a donor in IGZO.

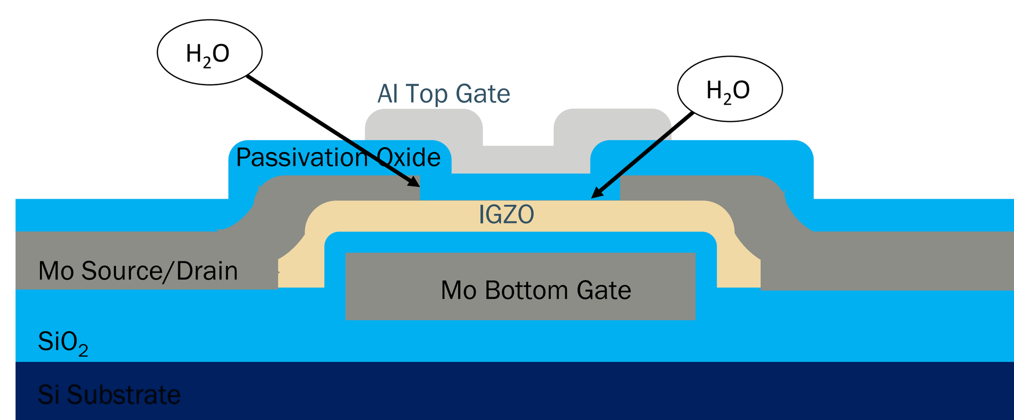

Fig. 2: H_2O entering the passivation oxide which interacts with the IGZO channel

Proposed Solution

Due to the SiO_2 tendency to absorb water, an encapsulation layer deposited on top can block the water molecules from entering the SiO_2. The encapsulation layers in this investigation is atomic-layer deposited (ALD) on the surface of the SiO_2 before formation of the top Aluminum gate.

There are several potential capping layers that are possible solutions to this issue. Aluminum Oxide (Al_2O_3), Hafnium dioxide (HfO_2), Titanium Oxide or even an alternating combination of the layers are proposed solutions to improve IGZO TFTs.

In this experiment, the PECVD SiO_2 passivation anneal time and Al_2O_3 ALD deposition temperature were parameters investigated for their influence on the thermal stability of IGZO TFTs.

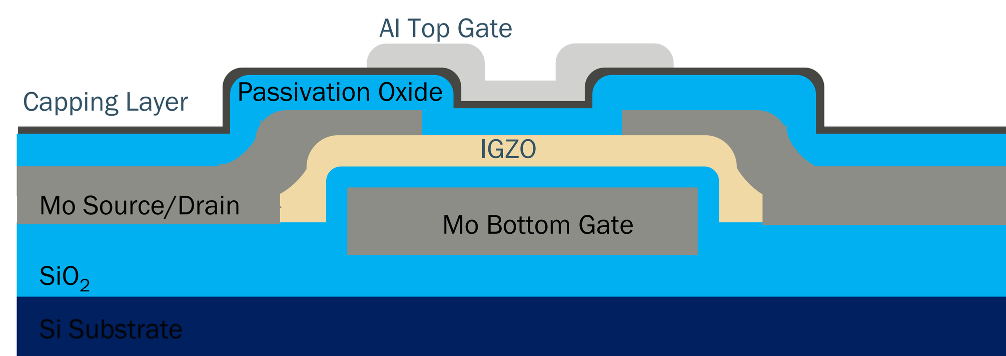

Fig. 3: A TFT with an ALD capping layer to act as a water barrier

I-V Characteristics

Figure 4 shows differences between the 400°C anneal time (3hr & 4hr) on devices fabricated without an ALD capping layer. The shorter devices (L=4μm), show similar performance, but for larger devices, such as the 96μm transistors, the 4hr anneal treatment exhibits distortion not observed using the 3hr anneal treatment.

Measurements also showed performance trends associated with the location on the wafer, which gave evidence of devices showing better transfer characteristics when closer to the edge of the wafer

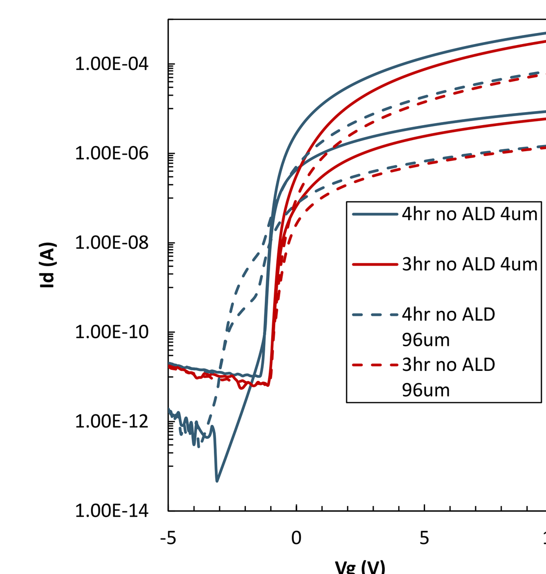

Fig 4: Anneal time comparison of devices without an ALD capping layer.

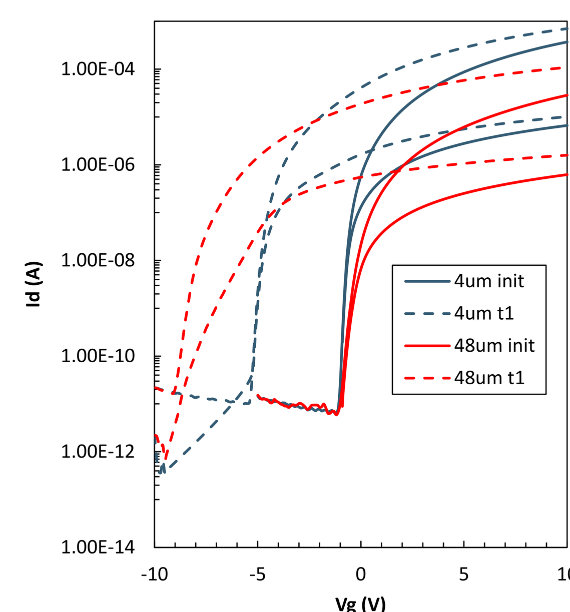

Fig 5: Channel length dependence on thermal stress

Figure 5 shows a comparison of the influence of thermal stress on short-channel (L=4μm) and long-channel (L=48μm) devices fabricated with a 3hr anneal time, without an ALD capping layer. The "t1" treatment is a hotplate bake for 1hr at 140°C. While both devices experience a left-shift from the initial position, the longer device demonstrates a larger magnitude shift as well as distortion and separation that is not shown by the short device.

I-V Characteristics (con't)

Figures 6-9 show the different anneal and ALD process splits and representative I-V curves of the devices before and after being stressed at 140°C for one hour. All devices shown have a channel length L=4μm.

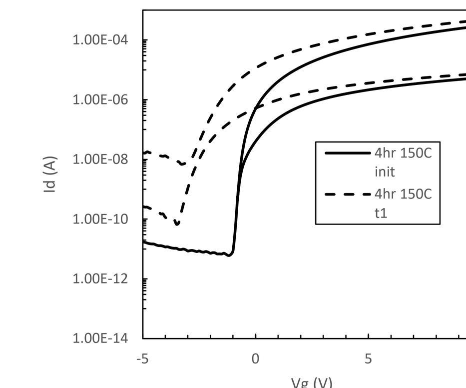

Fig 6: 4 hour anneal with 150°C ALD

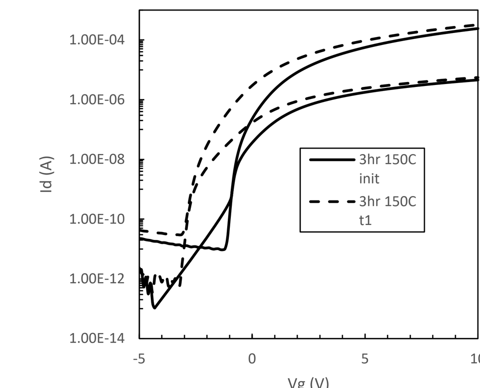

Fig 7: 3 hour anneal with 150°C ALD

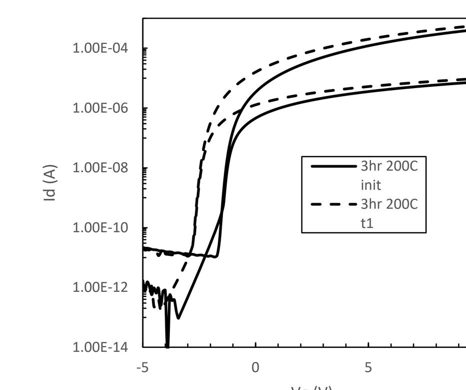

Fig 8: 3 hour anneal with 200°C ALD

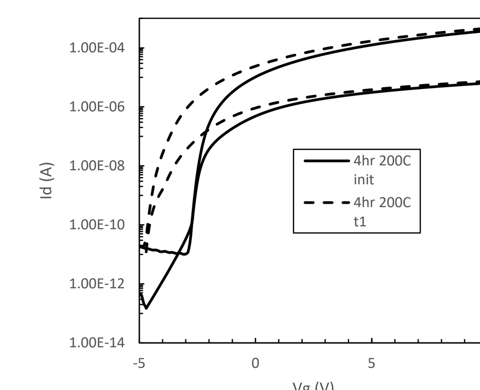

Fig 9: 4 hour anneal with 200°C ALD

Table 1 shows the voltage shift induced by thermal stress, extracted at I=1nA.

	4μm	12μm	24μm	48μm
3hr 150°C	-1.7V	-1.4V	-1.5V	-2V
3hr 200°C	-1.2V	-1V	-1.85V	-2V
4hr 150°C	-2.4V	-1.4V	-1.5V	-1.8V
4hr 200°C	-3.2V	-2V	-2V	>|-5V|

Table 1: Voltage shifts shown by different treatments

Conclusions

- Channel length was found to influence thermal stability; shorter devices were shown to be more thermally stable with a smaller voltage shift.
- This length dependence was less pronounced in devices fabricated with an ALD Al_2O_3 capping layer.
- The 3 hour anneal with the 200°C ALD capping layer showed greatest promise in yielding thermally stable devices.
- Despite improvement, further investigation is required to remove this residual shift and permit higher temperature exposure (e.g. 200 °C).

Areas for further study:

- Increased device sampling to identify dependence on wafer location
- Increase passivation oxide thickness
  - Challenge: coupled with anneal process
- Investigate other capping layer material options

References

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[2] J. K. Um et al., "High-Performance Homojunction a-IGZO TFTs With Selectively Defined Low-Resistive a-IGZO Source/Drain Electrodes," IEEE Transactions on Electron Devices, vol. 62, no. 7, pp. 2212-2218, 2015.
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Acknowledgements

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