Capping Layers for Increased Thermal Stability of IGZO Thin-Film Transistors

Jason Konowitch
Department of Electrical and Microelectronic Engineering
Rochester Institute of Technology
Rochester NY, USA
jgk7706@rit.edu

***Abstract* ---The goal of this project was to initially re-establish a baseline process for the fabrication of Indium-Gallium-Zinc Oxide thin-film transistors, shown in Figure 1, that have been a part of ongoing research here at RIT. After bringing the fabricated devices back into a reliable process, capping layer differences were investigated to determine their effects on device thermal stability. The time of the passivation layer anneal was varied between 3 and 4 hours for the primary lot and the temperature of the ALD capping layer was varied between 150°C and 200°C. The devices were tested and then thermally stressed on a hot plate for an hour at 140°C and 200°C. From the initial testing, it was shown that devices with 200°C ALD and with a 3 hour anneal had the best performance were the most thermally stable. After testing I-V characteristics, a length dependency was also found from the thermal stability in which the shorter devices remained operational after stress, whereas, longer devices became short circuits.**

I. Introduction

The research being done is to show performance capabilities of IGZO devices which theoretically have higher mobility than thin-film-transistors made with amorphous Silicon at a price much lower than the cost of devices using crystalline Silicon. There are device stability issues that must be worked out which are commonly attributed to the absorption of water into the passivation layer. Inclusion of a capping layer acts as a barrier to keep out water but must not interfere with device quality.

Inclusion of the capping layer has shown promise in the past, but different capping layers might yield more stable devices due to behaving as a better water barrier than the current Alumina capping layer used. This project is an investigation into correcting the current process followed by implementation of the alternative capping layers and their effects on device performance.

II. Theory

IGZO TFTs are proving to be a viable alternative for TFTs that utilize amorphous silicon (a-Si) or polycrystalline silicon (poly-Si) in high performance display applications. IGZO is a happy medium between the two silicon type devices because it is less expensive than the high mobility poly-Si, but still has a higher mobility than the low-cost a-Si.

Despite its advantages, IGZO has downsides; one of which is its susceptibility to change when the device is put under thermal stress. The electrical characteristics can be greatly shifted or distorted at temperatures above 100°C, which is bad for industrial applications which require further processing of fabricated TFTs at elevated temperatures up to at least 200°C.

IGZO is negatively affected by any exposure to water, therefore the presence of any water within the SiO_2 layer of a TFT will cause the device to be more sensitive to stress conditions. Shown in Figure 1 is the effect of thermal stress on a 24µ device fabricated without a capping layer present. As seen in the figure, the I-V characteristics can shift up to -5V and a separation between low and high drain is present.

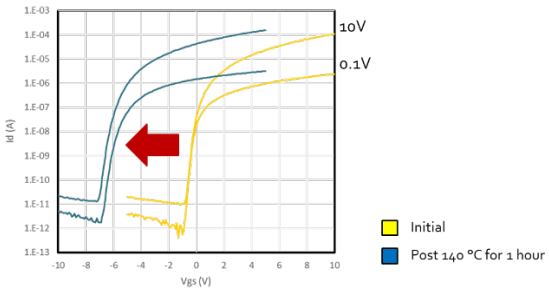

Figure 1: The voltage shift of a thermally stressed device

The passivation oxide will absorb water molecules, allowing them to reach the IGZO that it is ideally

protecting, resulting in enhanced electron concentration due to donor-like behavior. Reaction of H_2O with the top-gate electrode may also result in the liberation of monatomic hydrogen which has also been characterized as a donor in IGZO.

The first goal of this project is to reestablish a baseline process that has reproducible and meaningful results that can then be used for further study. Understanding the effects of IGZO thickness and back-channel surface condition, passivation oxide thickness and O_2 annealing time is important for device fabrication.

The second goal, after reestablishing a baseline process, is to fabricate designed experiments of IGZO TFTs using different anneals and capping layers to determine which process results in the best transistor characteristics that is also resistant to thermal stress.

Standard electrical characterization as well as thermal and bias stress testing will be used to determine how effective the capping layer prevents water from interacting with the back-channel region.

III. Experiment

IGZO TFT's have been fabricated for several years at RIT, with constant process changes and improvements due to ongoing research. The focus of this project was the adjustment of the passivation anneal and capping layer deposition. The process steps done for the devices fabricated in this project are detailed in the following steps.

1. *RCA Clean*
   After obtaining the silicon wafers to be used that were supplied by Corning Inc., the blank wafers had to be cleaned using the standard RCA clean.
2. *Oxide Growth*
   The wafers were loaded into the Bruce furnace and underwent a thermal Oxide growth with a target thickness of 650nm. This oxide growth is done to simulate a glass substrate that functional devices would be fabricated on. This way the fabrication can be done with the silicon wafers rather than the more fragile glass wafers.
3. *Bottom Gate Definition*
   A molybdenum sputter was done in the CVC 601 with a target thickness of 50nm. The sputter was done with Argon and a molybdenum target and a presputter was done to ensure film quality. This sputter is done to provide the metal layer for the bottom gate of the devices. The Molybdenum film was then patterned using the SVG track and GCA stepper and etched in a wet etch. The remaining photoresist was then stripped off using solvent.
4. *TEOS Oxide Deposition*
   Using the ASM P5000, 50nm oxide was deposited from a TEOS precursor. The deposited Oxide was then densified in the furnace at 600°C for 2 hours. This oxide layer serves as the bottom gate dielectric for the TFTs.

Figure 2: Cross section following TEOS Oxide deposition

5. *IGZO Deposition*
   The wafers were then sent to Corning for the IGZO to be deposited. 50nm were deposited using a sputter system that includes an Indium-Gallium-Zinc alloy target. The wafers had to be sent to Corning since the RIT SMFL does not have the capabilities to deposit the necessary film. This IGZO acts as the channel in the completed devices.
6. *MESA Definition*
   Using the SVG track and GCA stepper, the IGZO MESA was patterned. The IGZO was then etched in a bath of 6:1 DI + HCL, defining the MESA. The remaining photoresist was once again stripped using a wet bath with solvent.
7. *Source/Drain and Pad Definition*
   The source and drain, as well as the testing pads are defined using a lift-off process. Photoresist was deposited and then patterned on the GCA stepper. Molybdenum was then sputtered onto the patterned photoresist using the CVC 601. The target thickness of the Molybdenum sputter was 50nm and a presputter was done to ensure film quality. Using the Ultrasonic Bench, the wafers were placed in a solvent bath, removing the photoresist and the Molybdenum on top of it, leaving behind metal as the source and drain regions.

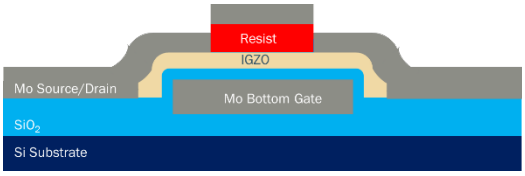

Figure 3: Cross section before metal lift-off for source/drain definition

8. *Passivation Oxide Deposition*

Next, using the ASM P5000, another 50nm of Oxide was deposited on the wafers. This layer serves to passivate the IGZO, as well as to serve as the gate dielectric for the top gate.

9. *Passivation Layer Anneal*
   The following step is one of the variables for the experiment. The wafers were annealed at 400°C in O2. The time of the Anneal was the factor, with wafers being annealed from 3 to 5 hours. Previously the process used an 8 hour anneal, but the devices being fabricated started to have a worse performance, prompting this change in anneal time.
10. *Capping Layer Deposition*
    The other factor in the experiment was the differing capping layers. Some wafers were omitted from this step to be used as controls, and the remaining wafers had a 15nm capping layer of Al2O3 deposited using the Ultratech S200 ALD using different deposition temperatures.

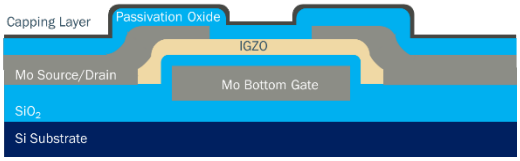

Figure 4: Cross section of device with added capping layer

11. *Contact Cuts*
    The next step was to use the GCA stepper to pattern the contact cuts down to the source, drain and bottom gate. The contacts were then etched in a bath of 10:1 HF. The remaining photoresist was then stripped in solvent.

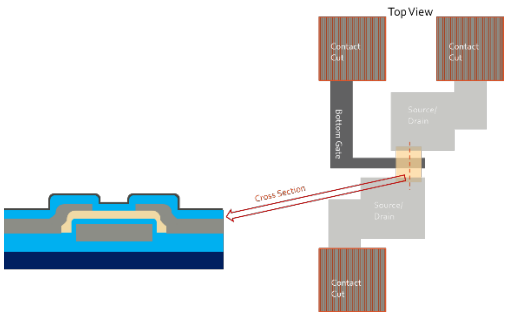

Figure 5: Contact cut placement

12. *Top Gate Definition*
    Next, the Top gate was defined using a lift-off process. Like the Source/drain definition process, photoresist was deposited and then patterned on the wafer using the GCA stepper. Using the AL Flash evaporator, 250nm of Aluminum was deposited on the wafers. Lift-off was then done in a solvent bath in the Ultrasonic Bench.

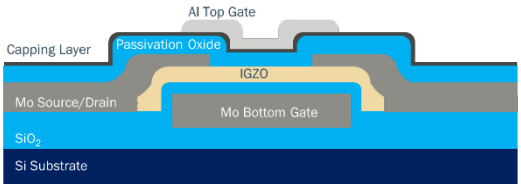

Figure 6: Completed device with capping layer

Following these steps, the devices were then complete and ready to be tested.

13. *Device Testing*
    Initial I_D-V_{GS} sweeps were done on devices of varying sizes across the wafers. Wafers were then thermally stressed on a hot plate at 140°C for an hour. The same devices were then retested to see the effects of the thermal stress. The stress was then repeated to see if the devices further deteriorated under continued stress.

IV. Data and Results

To help reestablish the baseline process, it needed to be determined which anneal time yielded the best results. The initial lot that was tested had devices which showed poor performance. The wafers with 3 and 4 hour anneals showed promise and wafers of the following lot were fabricated with the same conditions to see if they would yield good devices. Figure 7 shows the differences between the two wafers with a 3 and 4 hour anneal time that do not include a capping layer. Smaller devices (L=4µm) show a similar performance, but larger devices (L=96µm) from the 4 hour anneal treatment showed distortion.

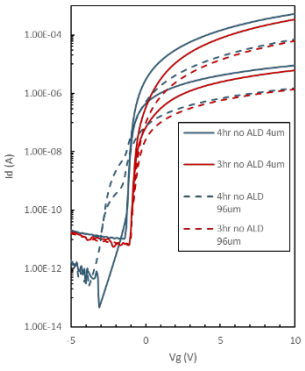

Figure 7: Anneal comparison of devices without an ALD capping layer

An issue that arose from testing was that a correlation was seen between device performance and its place on the wafer. Devices close to the edge of the wafer were more likely to show optimal transfer characteristics while devices near the center of the wafer were showing distortion.

After thermally stressing the two wafers without an ALD capping layer that were to be used as controls, a length dependency was discovered. Shorter length devices showed a smaller voltage shift after being thermally stressed. The shorter devices also showed no distortion or separation between the low and high drain. Figure 8 shows the difference in voltage shift between a 4µm device and a 48µm device (the "t1" treatment is 1 hour at 140°C). Both the short and long channel devices show an undesirable voltage shift, but the short channel device is more thermally stable.

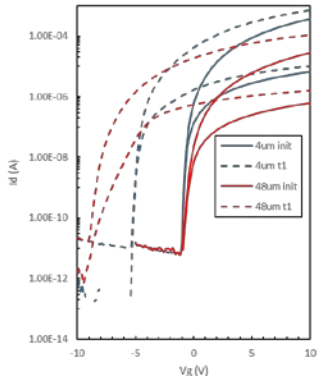

Figure 8: Length dependency of thermal stress

The two different anneal times were also split into different ALD deposition temperatures to determine the effect of the deposition on thermal stability. The ALD Alumina deposition was done at both 150°C and 200°C. The thermal stress testing was done on each treatment combination to determine the optimal processing. Figures 9-12 show the voltage shifts of representative devices of each treatment.

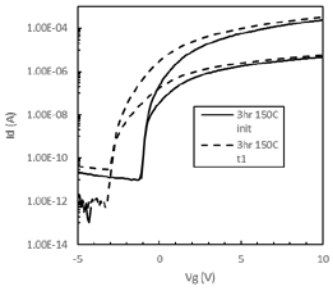

Figure 9: 3 hour anneal with 150°C ALD

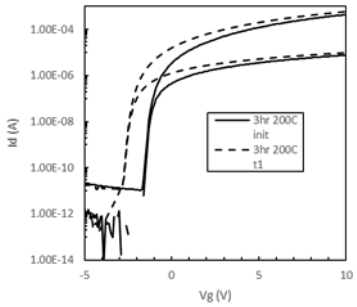

Figure 10: 3 hour anneal with 200°C ALD

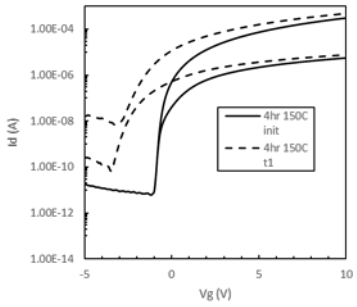

Figure 11: 4 hour anneal with 150°C ALD

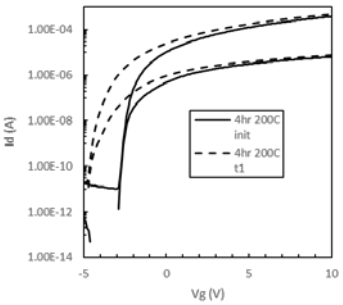

Figure 12: 4 hour anneal with 200°C ALD

Voltage shifts for devices were extracted by taking measurements at I=1nA and the data is displayed in Table 1. Based on the extracted voltage shifts, the treatment of a 3 hour anneal with Alumina deposited at 200°C showed the greatest thermal stability.

	4µm	12µm	24µm	48µm
3hr 150°C	-1.7V	-1.4V	-1.5V	-2V
3hr 200°C	-1.2V	-1V	-1.85V	-2V
4hr 150°C	-2.4V	-1.4V	-1.5V	-1.8V
4hr 200°C	-3.2V	-2V	-2V	>|-5V|

Table 1: Voltage shifts shown by different treatments

Despite the increased thermal stability seen by inclusion of the capping layer, the devices were not capable of being stressed up to 200°C, and nearly every device was reduced to a short from the high temperature.

V. Conclusions

The IGZO TFT process was reestablished, with the devices fabricated with a 3 hour anneal showing the best performance and the addition of the ALD capping layer deposited at 200°C to be the most thermally stable.

In the experiment, a channel length dependency was found from the results of the thermal stress tests. Shorter devices were shown to be more thermally stable with a smaller voltage shift. The length dependency was less pronounced in devices fabricated with the Alumina capping layer. Despite improvement, further investigation is required to completely remove the shift due to thermal stress and permit higher temperature exposure (e.g. 200°C). Further research with increased device sampling is also necessary to determine the performance dependency based on device location on the wafer.

Further exploration should also be done into other materials as options for the capping layer to determine which material yields the devices with the best performance.

Acknowledgements

My advisor, Dr. Karl Hirschman for guidance and help with data interpretation. Muhammad Salahuddin Kabir and Rahnuma Rifat Chowdhury for fabrication help and teaching me the current IGZO TFT process as well as the rest of the Hirschman Research Group who helped whenever they could. Corning Inc. for funding the research and depositing IGZO films. Patricia Meller and the rest of the SMFL staff for tool help and other assistance. Dr. Robert Pearson and Dr. Dale Ewbank for project guidance and organization. The Microelectronic Engineering Class of 2019 for reviewing the work and giving suggestions to improve the experiment and presentation.

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