CMOS TFTs allow for
- Devices fabricated using flash
- Next generation displays
- These devices are limited to
- Currently, most TFTs are

Thin film transistors (TFTs)
- This flash lamp system is
- Si solidifies resulting in a
- Glass substrate does not
- Si film absorbs light, rapidly

I. Project Objectives
- To investigate the addition of a fluorine implant to enhance the activation of boron in transistor source/drain regions during low temperature activation
- To develop a process that results in low resistance source/drain and is compatible with self-aligned CMOS thin film transistors

II. Motivation
- Thin film transistors (TFTs) are used in the backplanes of LED and OLED displays
- Currently, most TFTs are made of amorphous silicon (aSi:H)
- These devices are limited to NMOS, and have electron mobility less than 1 cm²/Vs
- Next generation displays require TFTs made from higher mobility materials
- Devices fabricated using flash lamp annealed polysilicon (FLAPS) are CMOS, high mobility, scalable, and compatible with existing manufacturing
- CMOS TFTs allow for incorporation of external control circuitry to be incorporated onto display

III. Overview of Flash Lamp Annealing
- Heated sample is exposed to a pulse of light from broad-spectrum Xe flashbulbs
- Si film absorbs light, rapidly heating and melting
- Glass substrate does not absorb light, staying below its thermal limit
- Si solidifies resulting in a polycrystalline film
- This flash lamp system is scalable allowing larger displays to be fabricated

IV. Device Fabrication
- Devices were fabricated using a previously developed FLAPS TFT process
- Source/drain implant was performed after FLA; fluorine followed by boron
- Fluorine dose of 1×10¹⁵ and 5×10¹⁵ cm⁻² were chosen
- Fluorine has shown to increase boron activation at low temperature (600°C) in crystalline silicon[4]
- Fabrication flow compatible with self-aligned devices

V. Results
- Id-Vgs Transfer Characteristic

<table>
<thead>
<tr>
<th>Fluorine Dose</th>
<th>None</th>
<th>1×10¹⁵ cm⁻²</th>
<th>5×10¹⁵ cm⁻²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear Vf</td>
<td>-3.5 V</td>
<td>-4 V</td>
<td>-2.8 V</td>
</tr>
<tr>
<td>ΔVf</td>
<td>0 V</td>
<td>0.3 V</td>
<td>2 V</td>
</tr>
<tr>
<td>μLin</td>
<td>24 cm²/Vs</td>
<td>13 cm²/Vs</td>
<td>28 cm²/Vs</td>
</tr>
<tr>
<td>μSat</td>
<td>140 cm²/Vs</td>
<td>70 cm²/Vs</td>
<td>220 cm²/Vs</td>
</tr>
<tr>
<td>ISATmax</td>
<td>131 μA</td>
<td>58 μA</td>
<td>280 μA</td>
</tr>
</tbody>
</table>

VI. Location Dependence
- Device characteristics change consistently depending on location on wafer
- Most likely cause is variation in crystallinity due to non-uniform exposure condition
- Direct comparison between treatments is difficult
- Improved system control can mitigate this issue

VII. Conclusions
- Van der Pauw measurements inconsistent with transistor performance due to differences in the influence of grain boundaries
- Direct comparison on impact of fluorine on boron activation inconclusive due to a portion of the fluorine implant entering the channel
- Devices with high fluorine dose showed increased current, indicating a lower source/drain series resistance
- High dose devices have less gate control, high off state leakage and threshold voltage shift, indicative of a conductive pathway
- Study is currently being replicated with thicker blocking oxide
- Non-uniformity in the exposure window complicates direct device comparisons and statistical analysis

VIII. References
1) https://www.flatpanelshd.com/ focus.php?subaction=showfull&fid=1474618766

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