Monolayer doping (MLD) for ultra-shallow junction MOSFET fabrication

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Doping is key for increasingly small semiconductor devices

- Integrated Circuits
- Photovoltaics
- Nanowires/Non-planar Devices
Doping is key for increasingly small semiconductor devices

But current industry techniques have limitations

Integrated Circuits
Photovoltaics
Nanowires/Non-planar Devices
Ion Implantation
Spin on dopant
MLD provides ultra-shallow, high concentration doping

**MLD Process Flow**

- **Phosphorus**
- **Carbon**
- **Oxygen**
- **Hydrogen**

![MLD Process Flow Diagram](image)

**X:** Diethyl vinylphosphonate

Vinyl group

- **Phosphorus**
- **Carbon**
- **Oxygen**
- **Hydrogen**

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Goal: Create MOSFETs with MLD doped source/drain

1. Develop a process to fabricate MOSFETs with MLD doped source/drain
2. Design MLD process chamber and characterize results
3. Fabricate and characterize devices
Process flow designed for MOSFETs with MLD doped S/D

1. Start with p-Si
2. Pattern field oxide
3. MLD n+ diffusion
4. Etch active area
5. NiSi anneal
6. Deposit Ni
7. Contact cuts
8. Deposit gate oxide
9. Etch Ni
10. Deposit Al
11. Pattern Al
Mask levels designed to fit processing constraints

• λ-based design rules
  - λ = 10 μm
  - Gate length was not controlled by λ, set to 0.5, 1, 2, 5, 10 μm

• Transistors with variable widths, inverter circuits, and resistors included in designs
MLD process chamber designed to be low-cost and functional
Patterned wafers doped via MLD are uniform and follow bulk trend

<table>
<thead>
<tr>
<th></th>
<th>Piece, $R_S$ ($\Omega/\square$)</th>
<th>6” wafer, $R_S$ ($\Omega/\square$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single MLD</td>
<td>1058.8</td>
<td>2189.0</td>
</tr>
<tr>
<td>Double MLD</td>
<td>769.6</td>
<td>1646.1</td>
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</tbody>
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Sheet Resistance vs. Position, After MLD Steps

Average $R_S$ decrease = 542.9 $\Omega/\square$
Decrease in $\sigma = 115.3$ $\Omega/\square$
Transfer characteristic shows field effect behavior

\[ I_D \text{ vs. } V_G, \ L = 10\mu m \]

- Subthreshold swing: \(~150mV/\text{dec}\)
- On/Off ratio: \(~10^6\)

\[ V_T = -0.3 \text{ V} \]
GIDL confirms dopant diffusion to gate edge and beyond

$I_D$ vs. $V_G$, $L = 10\mu$m

Gate-induced drain leakage

$V_{DD}$

inversion

$V_G < 0$

accumulation

$V_D = 5V$

$W = 110\mu$m

$W = 150\mu$m

depletion edge

GIDL

n+ drain
Current scales linearly with increasing $W$
Output characteristics reveal significant series resistance

Family of Curves, $L = 5\mu m$ $W = 110\mu m$

- $V_G = 2.0V$
- $V_G = 1.5V$
- $V_G = 1.0V$
- $V_G = 0.5V$
- $V_G = 0.0V$
- $V_G = -0.5V$
- $V_G = -1.0V$

$V_D$ vs $V_D$ (mA) $V_D$ (V)
Conclusions and future work

- MOSFETs with source/drain doped via MLD successfully fabricated and characterized
  - Devices demonstrated field effect behavior
  - Chamber design for MLD process was successfully tested
  - Proved that MLD can be patterned using SiO$_2$

- Future work:
  - Determine cause of high series resistance and revise process to minimize issue
  - Use a less isotropic etch for FOX or redesign masks to improve device yield
  - Use a better quality gate oxide – possibly hi-k
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References

Images:

Reference Papers: