Fabrication of MOSFETs on InGaAs with $\text{Al}_2\text{O}_3$ Gate Dielectric

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Overview

- Motivation
- Goal
- Mobility of III-V Materials
- Process Flow
- Mask Design
- Process Characterization
- Device Fabrication
- Electrical Results
- Conclusions
Motivation

- InGaAs high electron mobility compared to Silicon (10,000 cm²/V*s vs 1,400 cm²/V*s) this can lead to a boost in drive current at .5V power supply.

- Past fabrication of III-V MOSFETs used the University of Rochester’s ALD tool for the deposition of Al₂O₃ - Full fabrication process done at RIT.
Goal

• Fabrication of MOSFETs on InGaAs
  
  • Fabricate Capacitors on Si with Al$_2$O$_3$ dielectric using RIT’s ALD Tool and analyze CV.
  
  • Develop and characterize process for device fabrication.
Mobility of III-V Materials

- III-V Materials have higher electron mobilities than Si.
- Drive current is directly affected by mobility.
- Manufacturing costs of these materials much greater than that of Si, more defects, and higher stress and strain.

Process Flow
Starting Material Stack

N+ InGaAs
30nm

Intrinsic InGaAs
100nm

Buffer
Process Flow
Mesa Etch 20:20:1 Citric Acid:DI Water:H₂O₂

N+ InGaAs
30nm

Intrinsic InGaAs
100nm

Buffer

N+ InGaAs
30nm
Process Flow
Al₂O₃ Deposition by ALD – 100 Cycles

Intrinsic InGaAs
100nm
Buffer

N+ InGaAs
30nm

N+ InGaAs
30nm

Al₂O₃ ~10nm
Process Flow

$\text{Al}_2\text{O}_3$ Etch 100:1 HF:DI Water

- N+ InGaAs
  - 30nm

- Intrinsic InGaAs
  - 100nm

- Buffer

- $\text{Al}_2\text{O}_3 \sim 10\text{nm}$
Process Flow

Deposition of Mo and Patterning with Lift Off

- N+ InGaAs 30nm
- Intrinsic InGaAs 100nm
- Buffer
- Mo
- Al₂O₃ ~ 10nm
- Mo
- N+ InGaAs 30nm
Mask Design Layout

- Large MOSFET
- Transmission Lines for Contact Resistance Measurement
- 12 Pad Connection to Small MOSFET
- Capacitors for CV
Characterization of Al₂O₃ with MOS Capacitors on Si

MOS Capacitor with Al₂O₃ Dielectric

\[ T_{\text{ox}} : 12.8\text{nm} \]

Relative Dielectric Constant \( \varepsilon_r : 9.01 \)
20:20:1 Citric Acid:DI Water:H$_2$O$_2$
Etch Rate as a Function of Doping

Etch Rate vs Etch Depth of InGaAs Material Stack

Etched Mesa down to Intrinsic InGaAs

N+ InGaAs Etch Rate: ~1nm/sec
Lithography Challenges

- GCA Stepper was used for photolithography.
- Pieces were used for fabrication.
- Substrate is thicker than Silicon wafers. Requires different focus.
- Manual Alignment must be done for each lithography level.
Al₂O₃ Etch Characterization

Etch of Al₂O₃ can be seen down to InGaAs layer

Etch Rate: ~4Å/sec

100:1 HF:DI Water Etch of Al₂O₃
Characterization of Lift Off Process

Undercutting of LOR 5A can be seen underneath HPR504 Photoresist

Desired pattern achieved after Lift Off
Molybdenum Deposition

Small film thickness leaves film transparent.

Molybdenum Deposited with E-Beam Evaporation

Molybdenum Deposited with Sputtering
Finished Devices

W: 150µm  
L: 100µm  

W: 60µm  
L: 20µm  

W: 40µm  
L: 20µm  

W: 30µm  
L: 20µm  

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Electrical Results

- Testing of MOSFETs showed devices act like resistors.
- Fencing from lift off process paired with tight design rules lead to contact metal reaching down to the channel.
- Gate was found to be isolated from the Source/Drain.

Metal can be seen coming over the edge of the N+ InGaAs region
Conclusions

- Smaller features for the Source/Drain contacts should be used in the future to help prevent shorting.
- Depositing Mo using E-Beam Deposition requires further characterization. Decreasing the total mass of material inside the boat could provide better results.
- Sputtering Mo is viable for a lift-off process. Thick LOR is needed due to how conformal the film is from sputtering.
- Fabrication of an InGaAs MOSFET is achievable through the use of RIT’s SMFL tools alone.
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