Large Area Monolayer Doping Development

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Objective

Scale existing monolayer doping (MLD) process performed on Si pieces to full 6” wafers

- Design and implantation of an entire system

Investigate the doping characteristics

Fabricate diodes to electrically characterize the doping process
Motivation

Existing doping techniques such as ion implantation and spin on dopant have limitations

MLD offers a new method to solve these problems

<table>
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<tr>
<th>Doping</th>
<th>Strengths</th>
<th>Weakness</th>
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<tbody>
<tr>
<td>Ion Implantation</td>
<td>Widely Used Precise Dose Control Complex Doping Profiles</td>
<td>Damages Substrate Shallow Profiles are Difficult Hazardous Materials</td>
</tr>
<tr>
<td>Spin-on</td>
<td>No Damage Created Batch Fabrication</td>
<td>Hazardous Materials Forms Glassy Skin</td>
</tr>
<tr>
<td>MLD</td>
<td>No Damage Created Conformal Safer Chemistry</td>
<td>Low Dose</td>
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Theory

Process by which self-assembled monolayers of a dopant containing molecule are formed on crystalline silicon and driven in with a rapid thermal process.

Diethyl 1-propylphosphonate is phosphorus dopant containing chemistry -> mixed with Mesitylene solvent in 1:25 vol/vol ratio.
Apparatus for Pieces

1) Chemicals are measured out in glove bag
2) Solution in test tube is sparged (aerated with inert air) for 20 minutes
3) Wafer piece is added and connected to reflux condenser
4) Apparatus is lowered into 120°C Mineral Oil for 2 hours for reaction to occur
System Considerations

Withstand 120°C temperature and solvent
Needs to condense any vapors
Needs inlet/outlet for argon
Minimize chemical volume used
Low cost
Scaled Up Apparatus Design
Full 6” Wafers

Purchased container with tight fitting lid

3D Printed sleeve using Nylon
  ◦ Connects existing glassware to metal container
System Results

First run seal on lid did not hold – replaced with RTV seal -> Corrected
  ◦ However, results show similar sheet resistance measurements compared to pieces
  ◦ Speaks to robustness of the process

<table>
<thead>
<tr>
<th>Sheet Resistance Measurements</th>
<th>Pre-MLD</th>
<th>Post-MLD</th>
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</thead>
<tbody>
<tr>
<td>6” Wafer:</td>
<td>213 Ω/□</td>
<td>1126 Ω/□</td>
</tr>
<tr>
<td>Piece:</td>
<td>191 Ω/□</td>
<td>1031 Ω/□</td>
</tr>
</tbody>
</table>

CDE Resmap 3D plot of monolayer doped wafer
Doping Characterization
SIMS

Secondary Ion Mass Spectroscopy measured phosphorus concentration on wafer piece and on doped 6” wafer

Proves phosphorus was doped, matches historical data

- the shape of the profile is under investigation

$$\rho = \frac{1}{q(\mu_n n + \mu_p p)} \approx \frac{1}{q(1.3 \times 10^2 \times 5 \times 10^{18})} \approx 0.0096 \ \Omega \cdot \text{cm}$$

$$R_s = \frac{\rho}{t} \approx \frac{0.0096 \Omega \cdot \text{cm}}{100 \text{nm}} \approx 960 \ \Omega/\square$$

SIMS Courtesy of: NREL
Doping Characterization
Sheet Resistance

Varied anneal time and temperature and measured sheet resistance

At 900°C, phosphorus is not fully activated

At 1000° and 1100°C phosphorus activates and junction depths increase as anneal time is increased

Similar Trend Reported by Ho et. Al [1]
Electrical Characterization Diode

Fabricated and measured 118x120µm diodes
- Analyzed diode I-V characteristics taken on HP4145 in test lab
- First time diode with monolayer doped junction has been reported

\[
J = J_{\text{SCR}} + J_{\text{QNR}} = \frac{q n_x X_p}{2 \tau_n} \left( 1 - \frac{V}{V_{hi}} \right)^{1/2} \left( \exp \left( \frac{qV}{kT} \right) - 1 \right) + \frac{q n_x^2 D_n}{N_A L_n} \left( \exp \left( \frac{qV}{kT} \right) - 1 \right)
\]

At \( V_x \), \( J_{\text{SCR}} = J_{\text{QNR}} \) gives \( \tau_n \)

Carrier lifetime extracted: \( \tau \sim 0.23 \mu s \)
- Ideality Factor (QNR): 1.57
- Ideality Factor (SCR): 2.16

*Sid Grover TLM Senior Design Process Flow*
Electrical Characterization

Diode

Plugging in extracted values into diode equation to compare to I-V curve with no series resistance and only high level injection shows non-idealities are due to both series resistance and high level injection.

Equation courtesy of: Cristea, Miron. "Unified Model for P-n Junction Current-voltage Characteristics."
Conclusion

New system design dopes full 6” wafers with phosphorus– opens many research paths as process is now compatible with the RIT SMFL

Sheet resistance measurements are consistent with SIMS data

Diodes were fabricated with MLD junction and characterized, first time reported

Opens up a new doping capability for the SMFL
Future Work

Further characterization research

Modeling of doping profile

Monolayer doping process with Boron

Transistor Source/Drain Doping
  • Polysilicon Gate Doping

Conformal Doping Around FinFETs

Selective Emitter for Solar Cells

Through-Silicon Via Doping
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References

