Investigation of MIM Structures as Selector Devices for Crossbar Memory Arrays

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Introduction

- Big data keeps getting bigger
  - Today’s most profitable industries require unprecedented amounts of memory for data analytics
- To continue scaling, new types of non-volatile memories are needed
  - Resistive RAM (RRAM) and STT-MRAM both present promising results for the future of memory
- These new solutions require a different type of structure that allows for densely packed features
Crossbar Arrays

- The traditional NAND Flash structure can limit achievable densities

- Crossbar arrays are utilized by new non-volatile memories
- Simpler design allows for continued scalability
Selector Device

- As crossbar densities increase, leakage current becomes non-negligible.
- A selector device limits the leakage current from memory elements so that the current passing through a selected device significantly exceeds the residual leakage.
MIM Devices

- There are a few potential choices for selector devices
- Metal-Insulator-Metal (MIM) devices are particularly promising candidates
  - They have been previously shown to provide a large On/Off current ratio
  - MIM devices also allow for bipolar operation
    - This is a requirement for integration with many pre-existing crossbar technologies

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ideal Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Density</td>
<td>( \geq 10 \frac{\text{MA}}{\text{cm}^2} )</td>
</tr>
<tr>
<td>On/Off Ratio</td>
<td>( \geq 10^6 )</td>
</tr>
<tr>
<td>Operation Polarity</td>
<td>Bipolar</td>
</tr>
<tr>
<td>Scalability</td>
<td>Compatible with Memory Element</td>
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Ni/TiO₂/Ni

- This investigation focused on a Nickel-Titanium Dioxide-Nickel film stack.
- Using Nickel for both electrodes provides two main benefits:
  - Enables a simplified manufacturing process.
  - Allows for theoretical symmetry of I-V characteristics due to an equal work function difference regardless of the voltage polarity.
Work Functions & Band Gaps

- The I-V characteristics should be symmetric regardless of voltage polarity, due to equal differences between the oxide band gap and the metal work function on each side.

\[ \phi_1 = \phi_2 \]

\[ 5.1 \text{ eV} = \phi_1 \]

\[ \phi_2 = 5.1 \text{ eV} \]
Process Design

- Entire manufacturing process for selector is nine steps
- The designed process flow allows for ease of integration into pre-existing crossbar array processes
Process Flow

400 nm oxide growth

1st level lithography

60 nm oxide recess etch

60 nm Ni deposition

1st liftoff

2nd level lithography

15 nm TiO₂ deposition

60 nm Ni deposition

2nd liftoff
TiO$_2$ Processing Considerations

- The band gap of titanium dioxide varies widely with the degree of crystallinity of the film.
- This in turn leads to variation in the differences between the electrode and the insulator, which makes it hard to predict exact device behavior.
- Deposited below 200 degrees Celsius, the film should be amorphous.
- Above 240 degrees Celsius, there will be some degree of crystallinity in accordance to the anatase form of TiO$_2$.
- Above 700 degrees Celsius, there will be some degree of crystallinity in accordance to the rutile form of TiO$_2$ [1].
- Crystallization can potentially lead to better on/off current ratio in the oxide, but also lead to larger variations in the device functionality.
Investigation of MIM Structures as Selector Devices for Crossbar Memory Arrays

**Mask Design**

- **Features:**
  - Multiple 3X3 crossbar arrays
  - Single isolated cells
  - Van der Pauw structures
  - Lines of varying widths
Crossbar Arrays

- 3X3 Crossbar Arrays
  - Varying feature sizes from ½ micron to 16 micron
  - Allows for observations about the relationship between feature size and current density
Process Development

- Initially planned for Atomic Layer Deposition (ALD) of the TiO₂ film
  - Due to unforeseen tooling issues, only one run was attempted with the ALD tool
  - Nickel for the metal one layer was destroyed in the process
- Alternatively opted to deposit TiO₂ with an electron beam evaporation tool
  - This change in tooling changed the planned processing temperature
  - Deposited film is in a semi-crystalline rutile form, rather than the anticipated amorphous form
Nickel Stress Cracking

- Previously deposited nickel for the bottom electrode was rendered unusable.
- As soon as the wafer was placed in the chamber for TiO\textsubscript{2} ALD, the instant heat transfer stressed the nickel to the point of cracking.
  - Suggested fix: Initially set ALD hotplate to a low temperature, and then slowly bring it up to operating temperature while the piece is under vacuum.
**Completed Device**

- Smallest attempted features were resolved successfully
**I-V Characteristics**

- Clear non-linear characteristics
- Current densities of 10kA/cm² achieved with ½ micron features
- Current density increases with decreasing device area
- Asymmetric current response likely due to oxidation of the bottom nickel electrode
I-V Characteristics

- Center device yielded the most desirable I-V characteristics
I-V Characteristics

![I-V Curve for Selector Device 2-1 within Single 0.5 Micron Array, -8V to +8V](image-url)
I-V Characteristics

- Corner cases yield the worst performance
I-V Characteristics

- As cell density increases, selector device characteristics improve
**I-V Characteristics**

- Isolated cells have no discernable uniformity
Observations

- As cell density increases, device characteristics improve
  - Suspect this is linked to stress induced while performing liftoff
- An on/off ratio of six orders of magnitude was observed
- A maximum current density of 10kA/cm² was realized for a device with half micron features
- Current density increases with device scaling

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<th>MIM Compatibility</th>
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<tbody>
<tr>
<td>Current Density</td>
<td>( \geq 10 \frac{\text{MA}}{\text{cm}^2} )</td>
<td>Achievable with scaling</td>
</tr>
<tr>
<td>On/Off Ratio</td>
<td>( \geq 10^6 )</td>
<td>✓</td>
</tr>
<tr>
<td>Operation Polarity</td>
<td>Bipolar</td>
<td>✓ ✓</td>
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<td>Scalability</td>
<td>Compatible with Memory Element</td>
<td>✓ ✓</td>
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**Future Work**

- In-depth testing & results verification
- Investigate solution for asymmetric work functions
- Implementation of larger crossbar arrays containing both a selector device and a memory element
Acknowledgements

- Dr. Santosh Kurinec
- Dr. Robert Pearson, Dr. Dale Ewbank, and Dr. Lynn Fuller
- The SMFL staff
References


END
Appendix A: Selecting a Resist
Obstacles: Resist Availability

- The availability of nLOF 2020 was in question, so Sean and I had to find an alternative lift-off resist option
- AZ 1518 was the second choice
  - when tested, the current stock was ineffective due to age
  - The previously-used distributor no longer sold AZ products
- AZ 5214 was the third choice
  - Multiple experimental process runs led us to believe that this was a poor choice for our purposes
- The next option was to use the photo-inactive LOR5A resist in combination with OiR 620
  - This option yielded the needed liftoff profile, and is what will be implemented in the final device process
SEM Images

- All images were taken with the Leo SEM
- We over-developed, but with a 15-20 second reduction in development time it will work well
- You can see the undercut at 87 degree tilt of the stage
SEM Images

- Took measurements at 90 degree tilt
- The measured thickness of the LOR is 948.2nm
SEM Images

- The measured thickness of the OiR resist is 1098nm
- The measured undercut is 2944nm
- Measurements are within a couple percent of the thicknesses measured on the Spectramap
- Some error involved with lining up measurement lines in SEM tool
Appendix B: Growth of Isolation Oxide
Oxide Growth

- Target was 5000 Angstroms
- The thickest film achieved was 4090 Å, with an average across five wafers being ~3800 Å
  - Pretty far off from the target, but should still work just fine
- Fairly good uniformity, all had a thickness standard deviation of ~2 percent
Appendix C: Determination of Oxide Etch Rate
Trion Etch Rate

- The recipe that was available in the SMFL had last been confirmed in 2010, so I decided to determine the etch rate myself to make sure
  - Given recipe stated an etch rate of 366 Å per minute
- I determined an etch rate of 3.596 Å/sec, or ~216 Å/min
**Trion Etch Rate**

- Calculated average excludes the first data point

![Graph showing etch rate data with average rate of 3.596 Å]
Trion Etch Rate

- There is a mild negative effect on surface uniformity as etch time increases.

![Surface Uniformity with respect to Etch Time]