Surface Cleaning of III-V PIN Diodes to Reduce I_0 for TFET Applications

Ian R.T. Manwaring

Abstract—**The effect of surface cleaning and passivation techniques on the reverse bias saturation current I_0 of $In_{0.53}Ga_{0.47}As$ PIN diodes was investigated. The primary surface clean and passivation chemistries used were an HCl/D.I. H_20 solution, and an $(NH_4)_2S$ solution, respectively. The effect of a Benzocyclobutene (BCB) capping layer, along with the influence of the BCB adhesion promoter was also investigated. It was found that the use of the surface clean and sulfide passivation reduced I_0 by over an order of magnitude, while also drastically tightening the overall distribution of I_0 values over approximately 120 devices of different dimensions, when compared with devices without surface treatments. The use of BCB as a capping layer was seen to keep the distribution of I_0 values tight over time, implying that it can effectively cap a surface that has been passivated with sulfur.**

Index Terms—**III-V, TFET, PIN Diode, Sulfide Passivation, Surface Treatments, I_0, BCB.**

I. Introduction

With the proliferation of mobile devices, coupled with the inherent limitations of traditional Metal-Oxide-Semiconductor (MOS) technologies, the need to investigate novel devices that provide both low power consumption and superior switching capabilities is evident in order to drive future industry growth. A primary class of novel devices that are being considered for future implementations are Tunneling Field Effect Transistors (TFETs), due to the demonstrated improvement in switching capability [1]. This improvement is primarily due to the difference in current transport mechanism, as the TFET utilizes band-to-band quantum mechanical tunneling rather than thermionic emission, allowing the device to bypass the traditional 60 mV/decade swing limit. Apart from the TFET's ability to approach a near perfect switch, the device is also an attractive solution to the mobile industry due to its comparably low off-state current and large I_{ON} / I_{OFF} ratio. Given the requirements in both supply voltage and power consumption, the TFET is a promising candidate for the future of logic technologies [2], [3]. The optimization of the TFET fabrication process, along with device characterization and circuit implementation will be the limiting factors regarding the industry's future use of TFETs. The minimization of I_0 will have a direct impact on minimizing the subthreshold swing, which is usually at a minimum for the lowest currents.

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II. Background

Traditionally, TFETs are realized by depositing a high-κ dielectric material over the intrinsic region of a PIN diode and subsequently putting a gate metal down in order modulate the energy bands within the region. The modulation of this region, along with constant bias between the p and n regions of the diode, can allow for transistor like behavior when the conduction band of the intrinsic region falls below the valence band of the p region, inducing band-to-band-tunneling from the p to the n region of the device [6]. Often, III-V materials are utilized to fabricate TFETs due to the presence of smaller band gaps and higher tunneling probabilities when compared with silicon [4]. Mesa structures are commonly used as they are relatively simple to fabricate, and are easy to implement with an epitaxially grown PIN layered material. A basic schematic of a mesa structured TFET is shown in Fig. 1.

As off-state current is of great importance to the future implementation of TFETs in industry, minimizing reverse bias saturation current I_0 is crucial. Any significant leakage can vastly increase I_0, leading to a subsequent decrease in the I_{ON} / I_{OFF} ratio, rendering the device useless to industry. A common source of this off-state leakage, especially regarding the mesa structure used in TFET fabrication, is the presence of native oxides on the surface of the mesa. It is well documented that III-V oxides, especially those associated with Indium and Gallium, are conductive. The presence of conductive native oxides at the surface of the mesa structure can provide an undesirable conduction path that significantly reduces TFET performance [5]. A common method for removal of these native oxides is the use of an HCl based chemical surface clean, as III-V native oxides are soluble in this type of solution.

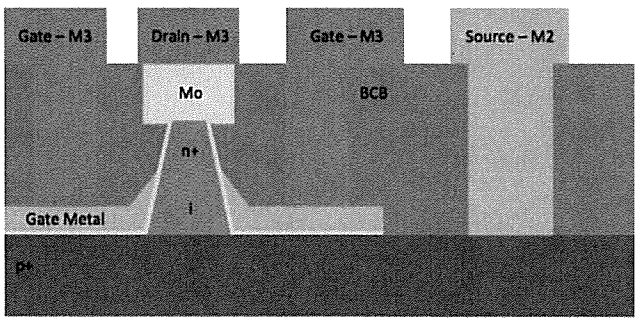

Fig. 1. Cross section of a basic III-V based mesa structured Tunneling FET.

In order to tie up the surface states on the surface of the PIN diode mesa, it is desirable to include a passivation step subsequent to native oxide removal in order to prevent the regrowth of native oxides. A common means of passivation includes a soak in an ammonium sulfide ($(NH_4)_2S$) solution [7]. Often a capping layer is then applied, as the positive effect of sulfide passivation generally deteriorates over time.

III. Experimental Setup

In order to understand the effect of an HCl/D.I. H_2O clean and subsequent sulfide passivation, along with the implications of using a BCB capping layer, multiple treatment combinations were implemented. Devices were constructed on $In_{0.53}Ga_{0.47}As$ substrates with a PIN structure on the surface of the wafer via molecular beam epitaxy at Texas State University. A basic process flow for each device is shown in Fig. 2. Note that the application of BCB was included in only select treatment combinations.

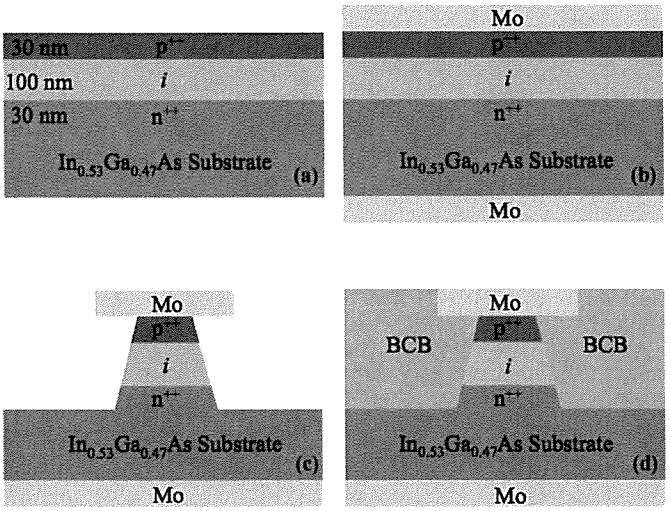

Fig. 2. (a) Starting Substrate. (b) Top side and back side Mo contact deposition. (c) Mo dry etch (SF_6) and InGaAs citric acid wet etch. (d) Surface clean, sulfide passivation, BCB application, cure and etch back.

Surface treatment combinations for the screening experiment were set up in order to have a control sample, a sample utilizing only the HCl/D.I. H_2O Clean and BCB, a sample utilizing both the HCl/D.I. H_2O clean and sulfide passivation, and a sample utilizing the HCl/D.I. H_2O clean, sulfide passivation, and the BCB.

A possible confounding factor in the screening experiment was the fact that the adhesion promoting chemistry (AP3000) used prior to the BCB application contains trace amounts of metallic ions, which could potentially have an effect on the reverse bias saturation current of the devices [8]. Given this confounding factor, another treatment combination was added to the proposed list in order to ensure that its effect could be brought into the analysis if needed. A full table summarizing all specific treatment combinations used in this screening experiment can be found in Table 1.

TABLE 1
Surface Treatment Combinations

Sample	HCl/D.I. H_2O Clean	$(NH_4)_2S$	AP3000	BCB
PIN 1	No	No	No	No
PIN 2	Yes	No	Yes	Yes
PIN 3	Yes	Yes	No	No
PIN 4	Yes	Yes	Yes	Yes
PIN 5	Yes	Yes	No	Yes

IV. Results and Discussion

The photo mask used to define the mesa structures consisted of numerous devices dimensions, with multiple perimeter and areas. A number of devices were long and narrow, were more square, and another set were serpentine in nature. There were approximately 120 testable devices on each sample, yielding over 1600 data points over the course of the entire study.

Early in the study it was found that sample PIN 2 was unintentionally over etched during the BCB etch back process, exposing the mesa surface to the oxygen plasma within the LAM 490 tool used for plasma etching. This oxygen plasma oxidized the surface of the mesa a considerable amount leading to very high reverse bias saturation currents. This sample was unable to be salvaged for usable data, and was not analyzed further.

It should be noted that all I_0 analysis was done in regard to current per unit perimeter length. It was initially surmised that since the principal leakage mechanism was due to undesired current flow through the conductive native oxides, a dependence on the perimeter of each device might be seen. However, this type of dependence was not experimentally observed for reverse bias analysis. Given the I-V characteristics of the diode, the dependence might actually lie in the forward bias region manifested by a change in diode ideality at lower applied biases. This deviation from ideality can be seen in Fig. 5.

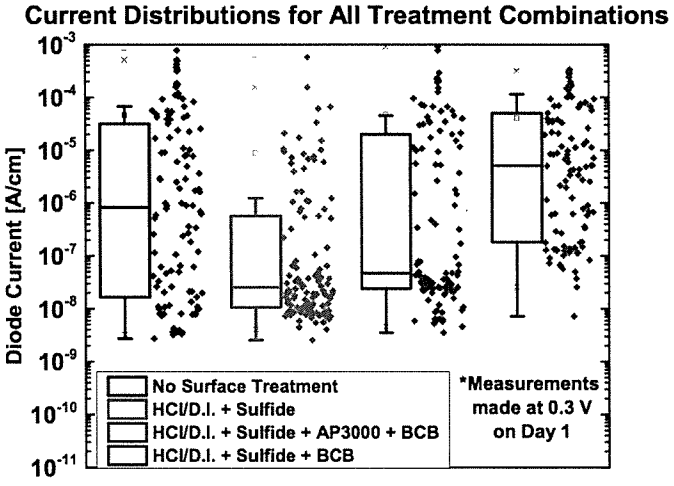

Fig. 3. I_0 distributions in Amperes per unit perimeter length for each analyzed treatment combination.

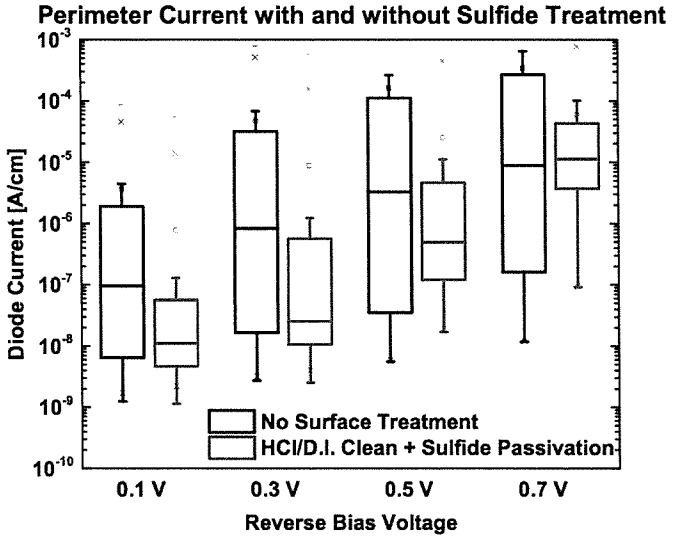

Fig. 4. Comparison of devices with and without HCl/D.I. H_20 Clean & Sulfide Passivation.

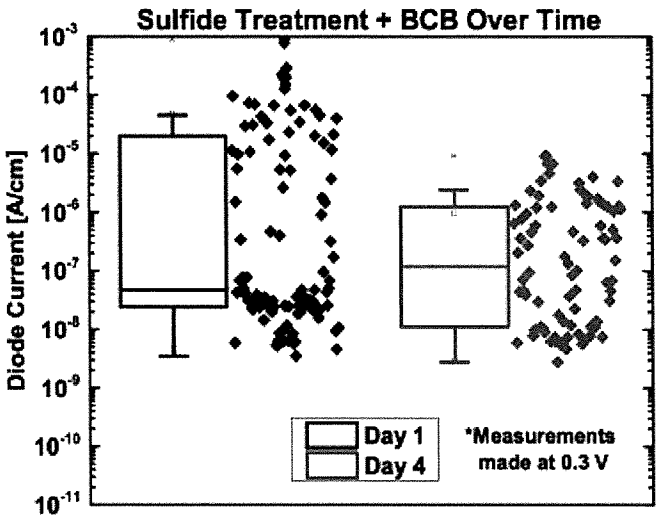

Fig. 6. PIN 4 I_0 measurements after day 1 and day 4, illustrating the ability for BCB capping.

Given the large amount of data points collected, it was appropriate to arrange each sample's data set into a box plot for simple visual comparison of I_0 distributions. A concise comparison of the I_0 distribution of each treatment combination directly after processing is shown in Fig. 3. All data points were taken at 0.3 V reverse bias.

Sample PIN 1 yielded a very large distribution in reverse bias saturation current, which was expected as it was not subject to any surface clean or passivation subsequent to the mesa definition. Sample PIN 3, which was treated with both the HCl/D.I. H_20 clean and Ammonium Sulfide passivation, produced a much tighter distribution in I_0 over numerous reverse bias voltage points, illustrated in Fig. 4. The I-V characteristics of an identical PIN diode tested on both PIN 1 and PIN 3 is shown in Fig. 5. The reverse bias current is approximately three orders of magnitude lower for PIN 3.

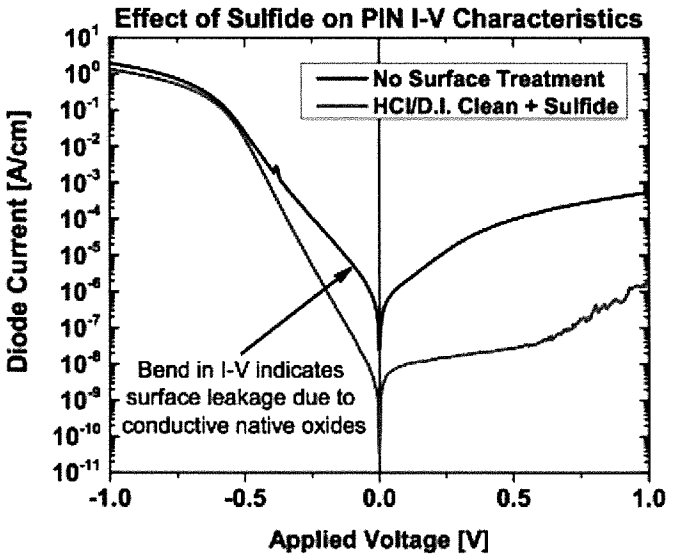

Fig. 5. I-V characteristics of a PIN diode treated with and without the HCl/D.I. H_20 clean.

Samples PIN 4 and PIN 5 were utilized to understand the effect of BCB as a capping layer. The only processing deviation between the two samples was in regard to the use of an adhesion promoter prior to the application of the BCB, as the adhesion promoter is known to contain trace amounts of metallic ions. Sample PIN 4 contained the adhesion promoter, which displayed much better capping properties that the sample without. Considering the results of PIN 4, it can be concluded that the metallic ions within AP 3000 have little effect on the reverse bias saturation current for these devices.

Overall, the use of BCB as a capping layer proved to be effective, as the average I_0 over the course of 4 days was approximately in equilibrium. In fact, the distribution was seen to tighten. This is illustrated in Fig. 6.

V. Conclusions

Given the substantial amount of data collected throughout the course of the screening experiment, a number of conclusions were drawn:

A very large distribution in I_0 was seen for the PIN diode devices that were not subjected to a surface clean or passivation after the mesa definition, which yielded a relatively high average current per unit perimeter length of approximately 9 x 10^{-7} A/cm. However, for devices that were subject to both the HCl/D.I. H_2O clean and sulfide surface passive after mesa etch showed a drastically tighter distribution in I_0 on Day 1, along with an over tenfold decrease in average I_0. This proves that an HCl clean to rid the mesa surface of conductive native oxides, coupled with the sulfide passivation to tie up any dangling bonds at the surface has a profound effect on I_0 reduction.

BCB as a capping layer was very effective, as over time, the positive effect of sulfide passivation continued to be evident. The capping layer was even seen to narrow the distribution in I_0 after 4 days. This trend was only seen, however, when an adhesion promoter was used prior to coating the BCB. It must also me noted that extreme care must be taken during the BCB

etch back process so as not to over etch and expose the mesa surface to the oxygen ambient.

Given the results of this data set, it is strongly advised that both an HCl/D.I. H_20 clean and Ammonium Sulfide passivation step be done after mesa definition. The inclusion of BCB as a capping layer is also advised, if done with care.

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