Improving sub-bandgap carrier collection in GaAs solar cells by optimizing InGaAs quantum wells using strain-balancing and distributed Bragg reflectors

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Improving sub-bandgap carrier collection in GaAs solar cells by optimizing InGaAs quantum wells using strain-balancing and distributed Bragg reflectors

by

Brandon Bogner

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Materials Science & Engineering

Materials Science & Engineering Program
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Rochester Institute of Technology
Rochester, New York
Date of Approval: 08/13/2021
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Committee Approval:

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ABSTRACT

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Dissertation Title: Improving sub-bandgap carrier collection in GaAs solar cells by optimizing InGaAs quantum wells using strain-balancing and distributed Bragg reflectors

Bulk carrier collection in GaAs solar cells is limited by the GaAs bandgap of 1.42eV, leaving low-energy photons below 1.42eV uncollected. The addition of low bandgap materials allows for the collection of these ‘unreachable’ photons in a GaAs solar cell. In_{x}Ga_{1-x}As can have bandgaps between 0.354-1.42eV based on indium composition, allowing for tunable collection at longer wavelengths. Including thin 9.2nm In_{x}Ga_{1-x}As quantum wells in the i-region of a GaAs n-i-p structure enhances photon collection past the 870nm GaAs band edge, increasing current production and potentially leading to higher efficiencies. Increased current production in GaAs solar cells is especially valuable since GaAs is used as a mid-junction cell in triple junction InGaP/GaAs/Ge structures, where current-matching between the three structures is vital for reaching efficiencies above 40% under solar concentration. To prevent accumulation of strain due to the differences in the GaAs and InGaAs lattice constants, tensile GaAs_{1-y}P_{y} barriers are added on either side of the InGaAs wells.

The effects of utilizing InGaAs-GaAsP superlattices in the i-region on device performance and material quality are investigated in this work. It was found that strain-balancing quickly became necessary in devices with as few as three wells. Distributed Bragg reflectors were incorporated in the structural design to allow a second pass of photons through the wells and are shown to
double the well current production without adversely affecting $V_{oc}$. Decreasing the local strain between the InGaAs wells and GaAsP barriers by dropping the phosphorus composition from 32% to 10%, along with optimizing the growth conditions of the superlattice, dramatically improved the interface quality of devices grown on 2° and 6° offcut substrates in addition to recovering $V_{oc}$ above 1.00V with a 12xSBQW superlattice. Current production of the superlattice was also shown to increase from $13 \frac{\mu A}{well}$ using 32%P barriers to over $30 \frac{\mu A}{well}$ using 10%P barriers.
To my family for the unconditional love and support as I ventured into the science world.
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Chapter 1

Introduction

The first satellites to include solar cells for power generation were the Sputnik 3 and Vanguard 1, both launched in 1958. The early cells on-board were 8% efficient n-type Si. Since semiconductor photovoltaic (PV) devices were developed only four years earlier at Bell Labs, the technology was not yet widely accepted as a reliable form of power generation, so chemical batteries were expected to act as the main power source. The batteries in Vanguard 1 were non-operational after a short 20 days, while the Si cells remained functional for over 6 years [1]. The longevity of the cells in orbit paved the way for PV to become the primary power source in satellites. Si cells remained the only available power source in space missions until 1970 [2]. With further advancement in photovoltaics, satellite power generation began transitioning to higher-efficiency, lightweight devices, mainly driven by a high cost per kilogram of space launches [3]. The emergence of epitaxially grown crystalline III-V alloys in the 1980’s led to the early development of III-V solar cells, offering more flexibility in terms of available material properties and layer structures, along with enhanced radiation tolerance critical to operational lifetime in space.

Terrestrial applications, however, are still dominated by Si, given its abundance on Earth,
established fabrication methods and the scalable capability to grow wafers larger than 300mm in diameter. Higher raw material cost and limited device size have prevented III-V’s from having a similar impact on the terrestrial market.

Si PV has been extensively investigated since the 1960’s but has not made significant advancements in efficiency since the late 1990’s. Pushing past 30% efficiency has proven difficult, mainly limited by Si being an indirect bandgap material. Promoting carriers across the bandgap in indirect materials requires a change in momentum in addition to overcoming the energy difference between the conduction ($E_c$) and valence ($E_v$) band. This momentum change is brought on by either the generation or absorption of phonons. Phonon assistance in indirect materials makes photon absorption relatively unlikely, which translates into two general trends; longer carrier lifetimes of $10^{-7}$-$10^{-3}$ sec compared to $10^{-9}$-$10^{-7}$ sec in direct bandgap materials, and lower absorption coefficients across a majority of the absorbing energy range [4]. Fig. 1.1 shows the absorption coefficient of Si and GaAs, revealing the order of magnitude difference between indirect and direct bandgap absorbance. The larger absorption coefficient of GaAs allows it to be grown thinner without sacrificing photon collection, bringing the typical active material thickness from 20-50\(\mu m\) in Si to less than 3\(\mu m\) in GaAs [4].

Another major advantage III-V’s have over Si is their ability to be grown epitaxially as alloys. Lattice-matching III-V’s allows for varying bandgaps between adjacent layers. A map of bandgap vs lattice constant of common semiconductor alloys can be seen in Fig. 1.2. III-V’s can be alloyed for lattice-matching, while Si is more difficult to lattice-match given its fixed lattice constant.

Carrier lifetimes are strongly affected by recombination center density in a material. Stacking crystalline layers of different lattice constants builds strain between the layers, leading to
Figure 1.1: Absorption Coefficients $\alpha$ of Si and GaAs. $\alpha_{GaAs}$ remains high up to the GaAs band-edge, while $\alpha_{Si}$ decreases as photon energy approaches the Si band-edge.

the formation of defects centralized around the interface. These crystalline defects act as recombination centers that trap carriers, which are highly deleterious to solar cell performance. Keeping strain between layers low, typically below a few hundred ppm, is imperative to maintaining high open-circuit voltage ($V_{oc}$) in devices. Section 1.1 will expand on how device performance is affected by material properties.

### 1.1 Photovoltaic Device Operation

Fundamentally, a photovoltaic device is a diode used to separate carriers after they are generated by the absorption of a photon. The junction can consist of one or more semiconductor materials. Si, for example, forms a homojunction through doping with boron (n-type) or phosphorus (p-type). III-V’s, however, can advantageously form heterojunctions by stacking
oppositely-doped epitaxial layers. These junction layers have different bandgaps, which can be tailored to a chosen spectrum. A photon incident on the device will create an electron-hole pair if its energy is larger than the bandgap ($E_g$) of the host material.

The electron-hole pair will then be separated by the junction’s electric field and collected if they do not recombine before successfully passing through the junction.

Building on their diode nature, PV devices can be modeled as two ‘leakage’ diodes with ideality factors $n=1$ and $n=2$, along with shunt and series resistances [5]. Fig. 1.3 depicts the two-diode model as a circuit element, which can be represented mathematically as [6]:

$$J = J_{01} \left( \exp \left( \frac{q(V - J R_s)}{kT} \right) - 1 \right) + J_{02} \left( \exp \left( \frac{q(V - J R_s)}{2kT} \right) - 1 \right) + \frac{V + J R_s}{R_{sh}} \quad (1.1)$$

where $V$ is the external bias to across the diode, $J_{01}$ is the $n=1$ dark, or saturation current density corresponding to recombination in the bulk, $J_{02}$ is the $n=2$ dark current density corresponding
to recombination in the depletion region, $T$ is the device temperature, $k$ is the Boltzmann constant, $R_s$ and $R_{sh}$ are the series and shunt resistances, respectively. When the device is illuminated, the diode curve shifts into the fourth quadrant by $J_L$, the current generated by the incident light on the surface of the device, visualized in Fig. 1.4. It is common practice to flip the illuminated diode curve over the voltage axis into the first quadrant when characterizing device performance. If shunt resistance is high, typically on the order of $10^6 \, \Omega$ and series resistance remains below $5 - 10 \, \Omega$, the linear dependence on voltage can be assumed negligible. Eq.1.1 then becomes:

$$J = J_{01} \left( \exp \left( \frac{q(V - J_R s)}{kT} \right) - 1 \right) + J_{02} \left( \exp \left( \frac{q(V - J_R s)}{2kT} \right) - 1 \right) - J_L \quad (1.2)$$

Setting $V = 0$ in Eq.1.2 gives the short-circuit current density, $J_{sc}$, which is the resulting current produced by the device under no external biases. $J_{sc}$ is a useful metric to compare performance across similar device structures and is related to the Quantum Efficiency of each layer in the device. The open-circuit voltage ($V_{oc}$) cannot be easily extracted directly from Eq.1.2 due to its position in both the n=1 and n=2 exponential terms. Simplifying the two-diode model into a single-diode model with a varying ideality factor allows for simpler extraction of
Figure 1.4: Left: Shifting of the dark diode curve by $J_L$ into the fourth quadrant under illumination. Right: Example AM0 LIV curve with labeled parameters.

$V_{oc}$:

$$J = J_{0n} \left( \exp(\frac{q(V - JR_s)}{nkT}) - 1 \right) - J_L + \frac{V - JR_s}{R_s h} \quad (1.3)$$

Setting $J = 0$ then solving for $V$ yields the open-circuit voltage:

$$V_{oc} = \frac{nkT}{q} \ln \left( \frac{J_{sc}}{J_{0n}} - 1 \right) \quad (1.4)$$

From Eq. 1.4 it is clear that to maintain a high open-circuit voltage, saturation current densities, and therefore recombination events, need to be limited. Breaking down the saturation current contribution in Eq. 1.2 reveals how material properties influence carrier recombination. The saturation currents are given as:

$$J_{01} = qn_t^2 \left( \frac{1}{N_a} \sqrt{\frac{D_n}{\tau_{0n}}} + \frac{1}{N_d} \sqrt{\frac{D_p}{\tau_{0p}}} \right) \quad (1.5)$$

$$J_{02} = qn_t W \frac{W}{2\tau_0} \quad (1.6)$$
where $q$ is the fundamental unit of charge, $D_n$ ($D_p$) is the diffusion coefficient of electrons in the p-type material (holes in the n-type material), $n_i$ is the intrinsic carrier concentration, $N_d$ ($N_a$) is the n-type (p-type) doping concentration, $\tau_{0n}$ ($\tau_{0p}$) is the the minority carrier lifetime of electrons in the p-type material (holes in the n-type material), $\tau_0 = (\tau_{0p} + \tau_{0n})/2$, and $W$ is the voltage-dependent depletion width. The intrinsic carrier concentration is exponentially related to the bandgap of the material:

$$n_i = \sqrt{N_c N_v \exp \left( \frac{-E_g}{2kT} \right)}$$  \hspace{1cm} (1.7)

where $N_c$ ($N_v$) is the effective density of states in the conduction (valence) band. Since $V_{oc}$ is inversely related to $n_i$, as bandgap increases, $V_{oc}$ increases.

This trend can be viewed more intuitively by considering Fermi level splitting due to carrier injection: [4]:

$$V_{oc} = \frac{E_{Fn} - E_{Fp}}{q}$$  \hspace{1cm} (1.8)

where $E_{Fn}$ and $E_{Fp}$ are the quasi-Fermi levels of electrons and holes in the p-type and n-type materials, respectively. The relation above assumes an ideal junction, where depletion region recombination is neglected [4]. Measured $V_{oc}$ is lower in devices where depletion recombination ($J_{02}$) is significant.

The *squareness* of the LIV curve in Fig.1.4 is described by the fill factor, which is the ratio of the maximum power point (mpp) vs. $I_{sc}V_{oc}$:

$$FF = \frac{P_{max}}{I_{sc}V_{oc}} = \frac{I_mV_m}{I_{sc}V_{oc}}$$  \hspace{1cm} (1.9)
The fill-factor is strongly dependent on resistive losses, where low shunt resistance is reflected in a negative slope at low bias and high series resistance in a slower current decay near $V_{oc}$. The overall efficiency is then described by the ratio of the max power point to the incident spectral power:

$$\eta = \frac{P_{max}}{P_{in}} = \frac{V_{oc}J_{sc}FF}{P_{in}}$$  \hspace{1cm} (1.10)

where $P_{in}$ is the incident spectral power on the device, discussed below in Section 1.2.

Optimizing device efficiency quickly becomes a balancing act between the various loss mechanisms limiting PV energy conversion. Assuming ideal material quality, a majority of these losses are a result of the relationship between effective bandgap and the incident spectrum.

### 1.2 Solar Spectrum

The solar spectrum can be approximated as a black body radiating at 6000K. Black body radiators ideally emit light isotropically, governed by Planck’s Law of black-body radiation [7]:

$$B_\nu(\nu, T) = \frac{2\hbar \nu^3}{c^2} \frac{1}{e^{\hbar \nu / kT} - 1}$$  \hspace{1cm} (1.11)

where $B_\nu$ is the spectral radiance, $c$ is the speed of light in a vacuum, $\hbar$ is Planck’s constant, $\nu$ is the frequency of radiation emitted, and $T$ is the temperature of the black body radiator. Temperature is the driving variable in black body radiation, which gives the Sun its characteristic spectrum as seen in Fig. 1.5. Deviations from an ideal black body come from temperature variations across the Sun’s surface, solar atmosphere effects, and Fraunhofer absorption lines.
The light incident on Earth’s surface is assumed to be traveling in parallel streams, since the solid angle from the Sun as seen from Earth is \(6.8 \times 10^{-5}\) steradians, or 0.53°. Earth’s atmosphere absorbs a portion of the incident solar radiation, with absorption depending on the path length light is taking to reach Earth’s surface. This path length is described by Air Mass, which is the angular deviation from normal incidence \((z)\) on Earth’s surface:

\[ AM = \sec(z) = \frac{1}{\cos(z)} \] (1.12)

The standards used for PV characterization are AM0, corresponding to conditions outside of the atmosphere, and AM1.5G, corresponding to a 48.1° deviation from normal incidence. The AM0 spectrum provides a power density of \(136.6 \frac{mW}{cm^2}\), while the AM1.5G spectrum is conveniently \(100.0 \frac{mW}{cm^2}\).
1.3 Multijunction Devices & Managing Efficiency Losses

Maximizing device efficiency begins with choosing a bandgap to balance various losses in the energy conversion process. The largest loss mechanisms are a direct result of material bandgap, with photons either having a larger energy than the bandgap, or not enough energy to promote carriers to the conduction band. Excess photon energy \((h\nu - E_g)\) in the first case is lost to lattice vibrations, termed *thermalization*. In the other case, photons with less energy than the bandgap do not generate carriers. These two loss mechanisms resulting from detailed-balance theory (discussed below), are visualized in Fig. 1.6 and can make up over 50% of the initial solar spectral energy incident on a PV device.

Other fundamental losses include a Carnot thermodynamic loss driven by the operating temperature of the device, angular effects of the incident light, and emission of photons generated from radiative recombination [8].
The relationship between bandgap and maximum efficiency was famously investigated in 1961 with Shockley & Quiesser’s detailed balance theory (SQ theory) of PV devices [9]. Their theory describes ideal device performance, and still provides a widely-accepted benchmark for device efficiency. The SQ theory limits recombination to radiative events, along with assuming that each photon with $E_\lambda \geq E_g$ produces an electron-hole pair. Since only radiative recombination events are considered, all carriers generated are eventually collected even if the radiative diffusion length ($\tau_{rad}$) in the material is shorter than the path length required for carriers to be collected [10]. The resulting short-circuit current can be described by integrating the material’s absorbance across the entire solar spectrum:

\[
J_{sc} = q \int_{E_g}^{\infty} \phi_{Sun} (E) a (E) dE = q \int_{E_g}^{\infty} \phi_{Sun} (E) a (E) dE
\]  

(1.13)

where $\phi_{Sun}$ is the solar photon flux, $a$ is the absorbance of the device (0 for $E_\lambda < E_g$ and 1 for $E_\lambda \geq E_g$) [11].

If the device is in thermal equilibrium with the surrounding environment, absorbed photon flux must equal the photon flux emitted by the device. Treating the PV device as a black body radiator, the emitted flux is given as:

\[
\phi_{emit} (E) = \frac{2\pi E^2}{h^3 c^2} \exp \left( -\frac{E - V}{kT} \right)
\]  

(1.14)

where $E$ is the emitted photon energy and $V$ is the device bias due to illumination [8].

The diode saturation current ($J_{0,rad}$) resulting from this emitted flux in the single diode
Table 1.1: SQ Theroetical Efficiency of an n-junction device [12]

<table>
<thead>
<tr>
<th>n</th>
<th>$E_1$ (eV)</th>
<th>$E_2$ (eV)</th>
<th>$E_3$ (eV)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.34</td>
<td>-</td>
<td>-</td>
<td>32.9</td>
</tr>
<tr>
<td>2</td>
<td>0.94</td>
<td>1.61</td>
<td>-</td>
<td>45.3</td>
</tr>
<tr>
<td>3</td>
<td>0.93</td>
<td>1.37</td>
<td>1.91</td>
<td>51.2</td>
</tr>
</tbody>
</table>

Equivalent of Eq. 1.2 can be expressed in a similar fashion to Eq. 1.13 as:

$$J_{0,rad} = q \int_{E_g}^{\infty} \phi_{\text{emit}}(E) a(E) \, dE$$  \hspace{1cm} (1.15)

This ideal saturation current influences device performance in exactly the same way as explained in Section 1.1.

The SQ theory can be expanded to include multiple bandgap devices, treated as separate absorbers connected in series. Adding multiple bandgaps allows for more efficient management of thermalization losses by splitting the incident spectrum between the layers, limiting the energy loss of photons with larger energies than the bandgap. Table 1.1 summarizes the bandgaps necessary for maximum efficiency under the solar spectrum [12].

A majority of communication satellites today rely upon a triple-junction (3J) structure for high-power production [13]. The structure of choice is $\text{In}_{0.51}\text{Ga}_{0.49}\text{P} - \text{GaAs} - \text{Ge}$, with bandgaps of 1.9eV, 1.42eV, and 0.7eV, respectively. This structure can be grown lattice-matched, connected by two highly-doped tunnel junctions. On account of a series connection between the sub-cells, the overall device current is limited by the lowest current-producing diode, which happens to be GaAs. Therefore, current-matching is essential in optimizing device efficiency. To increase current production in the GaAs sub-cell, its effective bandgap must be lowered near 1.2eV following Fig. 1.7, given the fixed Ge bottom sub-cell bandgap of 0.7eV.
Growing the device metamorphically is one option to tailor bandgaps closer to their optimal values, as reported by NREL in 2008, with an efficiency over 40% under concentrated illumination. Instead of focusing on the GaAs middle sub-cell, metamorphic devices target the low bandgap sub-cell using InGaAs alloys instead of the lattice-matched Ge. The bottom InGaAs alloy implemented by NREL had a 0.67eV bandgap, aligning much closer to the optimal bandgaps in Table 1.1. This technique utilizes (Al)InGaP grading layers to minimize threading dislocations in the high-power top junction, but remains far from the optimal bandgap combination while being considerably more difficult to grow than a lattice-matched structure [14]. Fig. 1.8 shows the thick, grading layers required accompanied by dislocation formation near the high-power InGaP top sub-cell.

The alternative is to include low-bandgap nano-structures in the GaAs sub-cell that will
Figure 1.8: Ion-beam and 220 dark field TEM images of the 2008 NREL metamorphically graded 3J structure with bandgaps of 0.67, 1.29 and 1.80eV [14]

absorb a small portion of the solar spectrum past the GaAs band edge, in effect ‘stealing’ photons from the Ge bottom cell. The impact on collection in shifting the effective bandgap of the GaAs sub-cell to 1.2eV is shown in Fig. 1.9, assuming only thermalization losses.

1.4 Introducing Nanostructures in GaAs

Bandgap engineering to extend the absorption range of GaAs solar cells can be achieved through the inclusion of thin, repeatable nanostructures. These nanostructures can be realized as either 2D (quantum well - QW) or 3D (quantum dot- QD) systems. Previous work utilizing quantum dots has shown improvements in multi-junction device efficiency, but maintaining proper quantum dot growth conditions is difficult to achieve [15].

In this work, the nanostructure of choice will be quantum wells, specifically shallow In$_x$Ga$_{1-x}$As
Figure 1.9: Effects on thermalization utilizing an $\text{InGaP – GaAs – Ge}$ structure, accounting for thermalization losses only. The increase in collection by lowering the GaAs effective bandgap is shown in yellow.

wells with compositions near $x = .10$. Inserting the wells in the i-region of a n-i-p solar cell takes advantage of the electric field across the junction. Carriers traveling in the depletion region will rely on a combination of tunneling and thermal energy to escape the wells, visualized in Fig. 1.10. Escape and recombination rates are described by the respective lifetimes of carriers before escape or recombination occurs. Inside quantum wells, the escape rate is given as:

$$
\tau_E^{-1} = \tau_{th}^{-1} + \tau_{tun}^{-1}
$$

(1.16)

where $\tau_E$, $\tau_{th}$ and $\tau_{tun}$ are the effective, thermal and tunneling escape lifetimes of carriers confined in a well [16]. Both thermal and tunneling escape rates are functions of well geometry
Figure 1.10: (left) Density of States changing from continuous function in bulk material to discrete levels in quantum well structures taken from a nextnano tutorial by S. Birner. (right) The band diagram of a QW superlattice with illustrated carrier escape mechanisms.

and depth:

\[
\tau_{th}^{-1} = \sqrt{\frac{kT}{2\pi m_w^* L_w^2}} \exp \left( \frac{-E_B}{kT} \right) \tag{1.17}
\]

\[
\tau_{tun}^{-1} = \frac{n \hbar \pi}{2L_w^2 m_w^*} \exp \left( -\frac{2}{\hbar} \int_0^{L_B} \sqrt{2m_b^*(E_B - Fz)} \, dz \right) \tag{1.18}
\]

where \( E_B \) is the field-dependent barrier height, \( m_w^* (m_b^*) \) is the effective mass of the carrier in the well (barrier), \( L_w (L_B) \) is the well (barrier) width, and \( F \) is the position-dependent electric field. From these two equations, common observed trends can be established: both escape rates will decrease if barrier height or well thickness increase, thermal escape is intuitively tied to temperature, and tunneling rates increase under larger electric fields. Typical radiative lifetimes in high-quality InGaAs-GaAsP QW systems fall within the nanosecond \((10^{-9} \text{ sec})\) range, so to successfully collect carriers escape rates must be at least an order of magnitude faster [17].

As more wells are added to the i-region, compressive strain between the InGaAs wells
and GaAs host material builds, leading to the generation of lattice defects, until the material eventually fully relaxes. To counteract the compressive strain, a thin barrier material with a smaller lattice constant than GaAs can be inserted to strain-balance (SB) the overall structure. With proper strain-balancing, a larger number of wells (50+) can be grown without relaxation in the i-region, as the Sugiyama group at the University of Tokyo have demonstrated over the last decade.

For InGaAs quantum wells, $\text{GaAs}_{1-y}\text{P}_y$ is typically used as the strain-compensating barrier material because it is a direct-bandgap material for compositions below $y = .5$ and has large enough bandgap that it does not absorb photons that may penetrate through the i-region. The thickness of the $\text{GaAs}_{1-y}\text{P}_y$ barrier can be adjusted by varying the composition of phosphorus. As phosphorus percentage increases, the required barrier thickness for SB decreases, but the barrier height carriers need to overcome grows. A trade-off quickly emerges - thinner barriers help maintain a thinner i-region which translates into a stronger electric field that assists in tunneling escape, but the accompanied increase in barrier height may limit thermal escape from the wells. Working with these basic trends, well and barrier properties can be chosen based on the desired carrier escape mechanisms, under the assumption that material quality is unaffected by changes to the periodic well-barrier structure, or superlattice (SL).

Looking ahead, the first well-barrier system utilized in this work is a strain-balanced 9.2nm $\text{In}_{0.08}\text{Ga}_{0.92}\text{As} - 3.2\text{nm} \text{GaAs}_{0.08}\text{P}_{0.32}$ superlattice. The band diagram simulated in nextnano, a 1-D simulation software geared towards nanostructures, of this strain-balanced QW structure is given in Fig. 1.11, with confined energy states $E_{c1}$ and $E_{c2}$ of 157.0, 108.9 meV respectively. Additional simulations in nextnano performed by Anastasiia Fedorenko of thermal and tunneling escape rates as barrier height (P-composition in the GaAsP barriers) is changed are shown
Figure 1.11: Nextnano simulation of a 3xSB In$_{0.08}$Ga$_{0.92}$As-GaAs$_{0.68}$P$_{0.32}$ QW system utilized in Chapter 2 with confined states $E_{e1}$, $E_{e2}$, $E_{lh1}$, $E_{lh2}$ and $E_{hh1}$. Bandgaps of the wells ($E_{g,\text{well}}$) and barriers ($E_{g,\text{bar}}$) were 1.305 and 1.670eV respectively.

Table:

<table>
<thead>
<tr>
<th>Energy State</th>
<th>Energy Level (meV)</th>
<th>Effective Mass ($m_0$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>e1</td>
<td>157.0</td>
<td>0.0631</td>
</tr>
<tr>
<td>e2</td>
<td>108.9</td>
<td>0.2244</td>
</tr>
<tr>
<td>lh1</td>
<td>161.5</td>
<td>0.1694</td>
</tr>
<tr>
<td>lh2</td>
<td>140.3</td>
<td>0.0760</td>
</tr>
<tr>
<td>hh1</td>
<td>101.0</td>
<td>0.5127</td>
</tr>
</tbody>
</table>

in Fig. 1.12. The thermal escape rates for this system are quite high, in the $10^{11} - 10^{12} \frac{1}{\text{sec}}$ range, while tunneling escape rates are $10^4 - 10^6 \frac{1}{\text{sec}}$. This early simulation result suggests that thermal escape dominates and tunneling escape will play little to no part in carrier escape from the InGaAs wells, regardless of barrier height, thickness or depletion region electric field.

Distributed Bragg reflectors (DBR) may also be added below the QWs to provide another pass of uncollected photons, effectively doubling the number of wells in the i-region. DBR’s are alternating layers of material with different indices of refraction ($n$). The values of $n$ can be tuned to reflect a specific range of wavelengths following Fresnel diffraction at adjacent interfaces, with reflectivity increasing as more DBR pairs are added. DBRs make a great addition to QW solar cells because they do not require additional fabrication steps and only reflect photons that the InGaAs wells can absorb, transmitting higher wavelength photons into...
Figure 1.12: InGaAs quantum well (left) strain-balance thickness as a function of barrier composition with thermal escape rates given for GaAs$_{0.9}$P$_{0.1}$ and GaAs$_{0.68}$P$_{0.32}$ barriers, (right) tunneling escape rate as a function of depletion region electric field. Simulation were done in nextnano by Anastasiia Fedorenko.

the bottom Ge sub-cell [18]. Results of implementing a DBR into QW devices will be shown later in Section 2.3.

1.5 Characterization Techniques

Throughout this work, a variety of characterization methods will be used to analyze material quality and device performance. Arguably the most important metric used to compare devices in the PV industry is power conversion efficiency under the solar spectrum, $\eta$, mentioned in detail in Section 1.1. The PV Characterization Lab at RIT has a TS Space Solar Simulator that produces an irradiance spectrum closely matched to $AM_0$, with a additional filters to emulate $AM1.5G$ conditions. The RIT AM0 spectrum is plotted against the ASTM standard in Fig. 1.13.
The RIT simulated spectrum is produced using a Hydrargyrum medium-arc iodide (HMI) lamp for the high-intensity, short wavelengths and a Quartz Tungsten Halogen (QTH) lamp for the longer wavelength tail. A schematic of the solar simulator’s operation is shown in Fig. 1.14. The simulated solar spectrum in Fig. 1.13 is calibrated using reference GaAs and InGaP 1-J solar cells measured at the NASA Glenn Research Center and the National Renewable Energy Laboratory (NREL) with known short-circuit current densities.

To characterize illuminated J-V performance, the current produced by the PV device is measured under a range of external biases until open-circuit conditions are met \((J = 0)\). After flipping the J-V into the first quadrant, \(R_{sh}, R_s, J_{sc}, V_{oc}, FF\), and \(\eta\) can be extracted. In combination with illuminated J-V analysis, dark J-V curves can be taken by removing all illumination sources. Both J-V curves can be used to extract saturation currents and their associated ideality factors, but the illumination-free J-V curves tend to offer more reliable diode-model fits.

Quantum Efficiency is another common measurement technique used in PV analysis. External Quantum Efficiency (EQE) is a function of wavelength, defined as the ratio of carriers
collected per photon incident on the device, with values ranging from 0 to 1. The power dependence of the incident photons can be taken into account through a similar parameter, Spectral Responsivity (SR), given in units of $A/W$. Since EQE and SR are representative of the same phenomenon, they are related through a simple unit conversion:

$$EQE(\lambda) = \frac{hc}{q} \frac{SR(\lambda)}{\lambda}$$  \hspace{1cm} (1.19)

and can be used interchangeably to extract the device short-circuit current in a similar fashion to Eq. 1.13:

$$J_{sc} = \frac{q}{hc} \int_0^\infty EQE(\lambda) F_{inc}(\lambda) \lambda d\lambda = \int_0^\infty SR(\lambda) F_{inc}(\lambda) d\lambda$$  \hspace{1cm} (1.20)

where $F_{inc}$ is the incident spectral irradiance, a term used to represent photon flux as a function of photon energy instead of number of photons.
In reality, SR is typically the measurement taken, which is then converted into an EQE spectrum using Eq. 1.19. Since SR depends on the ratio of current generated to the incident spectral power at a given wavelength, a broad-band illumination source may be used. At RIT, the illumination source is a QTH lamp. The broad QTH spectrum is then sent through a monochromator, which breaks the spectrum down into small wavelength ranges. This, in effect, is a measurement of collection efficiency as a function of the bandgaps present in the device, so each layer in the structure corresponds to a portion of the SR spectrum. The overall SR curve is then a sum of each layer’s contribution. To filter out external illumination sources, the RIT QE system includes a chopper wheel, tuned to the measurement frequency of a Stanford DSP Lock-In Amplifier. The current generated by the device is sent to a preamplifier that boosts the signal before being compared to the incident illumination power measured by photodetectors with known SR curves. An additional set of photodetectors is placed above the sample stage to measure the power of light reflected off the device, which can be used to measure a reflectivity spectrum. The reflectivity of the device \( (R) \) can be used to ‘filter out’ photons that were not absorbed, giving a new quantum efficiency that better reflects internal device characteristics. This new quantum efficiency is appropriately named Internal Quantum Efficiency, or IQE for short, defined as:

\[
IQE = \frac{EQE}{1 - R - T}
\]

(1.21)

where \( T \) is the transmission of photons through the device. Assuming the device is thick enough to fully absorb all photons with energy greater than its bandgap(s), transmission becomes negligible. A schematic of the RIT QE system is given in Fig. 1.15.

Biasing the device during an EQE measurement allows for characterization of the dominant
escape mechanism associated with a specific energy transition. This technique is known as Carrier Collection Efficiency (CCE). CCE is extremely helpful in probing escape mechanisms in regions affected by a strong electric field, especially for deciphering between thermal and tunneling-dominated escape in the QWs [19].

Moving away from PV-specific measurement techniques, material characterization is also a vital component of successful PV device design. Carrier injection, either through photoexcitation or passing a current through the device, can provide information on recombination lifetimes and material quality. Photoluminescence (PL) is carrier injection through photoexcitation, and is used extensively in this work to compare the material quality of various QW structures, typically measured in samples without p-n junctions to remove carrier drift. Unless stated otherwise, the samples measured are not connected to an external circuit, so carriers cannot escape. Instead, they are forced to recombine either radiatively, emitting a photon, or non-radiatively through Auger or SRH processes. Ideally, carriers generated in direct bandgap materials will recombine radiatively, emitting a photon that can be absorbed by photodetectors.
after passing through a monochromator. The monochromator filters the emitted photons by wavelength, resulting in a PL spectrum. PL peak intensity and width are related to the material quality of the wells through its dependence on radiative lifetimes. Higher intensity peaks can be associated to increased radiative recombination events, while thinner peaks are a sign of a more uniform well composition [20].

In combination with PL, High-Resolution X-ray Diffraction (HRXRD) can be used to assess relative material quality. The HRXRD used throughout this paper is a Bruker D8 Discover. A high-intensity, nearly monochromatic x-ray source is incident on the sample surface, where the beam penetrates the sample until it interacts with core electrons in the crystalline lattice. Scanning across the sample’s angular orientation with respect to the x-ray source, $\theta$, produces sharp peaks where constructive interference between successive (hkl) planes occurs. Bragg’s law, a simplified model of diffraction, can be used to determine where these peak $\theta$ values occur given lattice size ($a$), the x-ray wavelength ($\lambda$), and the (hkl) plane responsible for the diffraction event:

$$2d_{hkl}\sin(\theta) = n\lambda$$

(1.22)

where $n$ is the order of diffraction and $d_{hkl} = a/\sqrt{h^2 + k^2 + l^2}$. XRD plots are typically given as a function of $2\theta$, the angle between the detector and x-ray source. For GaAs, the targeted (hkl) plane for SL investigation is (004), where the GaAs Bragg peak is near 66.050°. Thin epitaxial layers in the sample will produce periodic interference fringes surrounding the sharp Bragg peak in addition to their own Bragg peaks, with compressively strained layers appearing at lower $2\theta$ angles and tensilely strained layers appearing at higher $2\theta$ angles according to the
differentiated Bragg’s law with respect to the Bragg angle:

$$\frac{\Delta d}{d} = \frac{\Delta a}{a} = \frac{a_{L, \text{perp}}}{a_S} = -\Delta \theta \cot \theta_B$$  \hspace{1cm} (1.23)

where $a_{L, \text{perp}}$ is the perpendicular composition-dependent lattice constant of the strained epitaxial layer, $a_S$ is the substrate lattice constant, $\Delta \theta$ is the difference in between the layer and substrate XRD peak in radians, and $\theta_B$ is the Bragg angle of the substrate [21]. The SL period thickness can also be extracted using:

$$t = \frac{\lambda}{2\Delta \theta_p \cos \theta_B}$$  \hspace{1cm} (1.24)

where $\lambda$ is still the x-ray source wavelength and $\Delta \theta_p$ is the spacing between adjacent SL fringes. Sharp SL peaks are desired and represent uniform composition and abrupt interfaces. An example XRD scan with labeled Bragg, superlattice and Pendellösung peaks can be seen in Fig. 1.16

1.6 Organization of Upcoming Chapters

The following chapters will focus on the device performance of single-junction GaAs solar cells designed for use as the middle cell in a 3J InGaP – GaAs – Ge device. Chapter 2 will briefly explain growth and fabrication methods used throughout this work. A majority of the chapter, however, will be directed towards the influence of In$_x$Ga$_{1-x}$As well/GaAs$_{1-y}$P$_y$ barrier superlattices on PV device performance and material quality, with compositions ranging from $x = .07 - .14$ and $y = .30 - .34$. The effects of adding a DBR to boost QW current
production will also be investigated. Chapter 3 will transition to lower \%P barriers, with compositions closer to $y = .10$. Chapter 4 will review the summarized conclusions from this study and present a short outline for future work.

Figure 1.16: XRD scan showing Bragg, SL and Pendellösung fringes
Chapter 2

Thin GaAsP Barrier QW Results

2.1 Growth & Fabrication Methods

All devices presented in this work were grown on 50mm diameter p-type GaAs (100) substrates at RIT in an Aixtron close-coupled showerhead metal organic vapor phase epitaxy (MOVPE) system at a pressure of 100mbar. The precursors used are trimethylgallium (TMGa), arsine (AsH₃), trimethylindium (TMIn), phosphine (PH₃), trimethylaluminium (TMAI), diethyl telluride (DETe), silane (Si₂H₆), diethylzinc (DEZn), and carbon tetrachloride (CCl₄). Sample material quality is monitored during growth through a variety of techniques, including 405nm, 632nm and 951nm reflectance, surface temperature through sample emissivity, and strain through substrate curvature. An integrated LayTec EpiCurveTT software is used to analyze the collected data to extract growth rates and layer thicknesses, shown in Fig. 2.1.

Once grown, devices are fabricated in the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT, a class 1000 cleanroom, using standard fabrication techniques.
Chemistries used are positive photoresists (PR) S1813 and AZ-1512, CD-26 photoresist developer, hydrochloric acid (HCl), phosphoric acid (H₃PO₄), hydrogen peroxide (H₂O₂), ammonium hydroxide (NH₄OH), hydrofluoric acid (HF), acetone, and isopropyl alcohol (IPA). All devices are designed to have top-bottom contacts, where metallization is done through electroplating in sulfite gold solution.

The sample frontside surface is first coated in photoresist using a CEE spincoater programmed to a max spin speed of 3000rpm. Then the sample backside is cleaned of residual III-V alloys using alternating etches in HCl and a 3:1:25 H₃PO₄:H₂O₂:H₂O mixture. The backside contact is then electroplated at 8-12mA for 13 minutes after a 30sec dip in zinc sulfate to increase backside doping, corresponding to Au thicknesses of 1.5-2µm. After electroplating, the photoresist is stripped using acetone and IPA, then the samples are annealed at 407°C for 6 min to assist in Zn diffusion.
Figure 2.2: Solar Cell Fabrication Process Flow.

The front-side of the sample is then re-coated in photoresist and goes through two lithography processes using an MJB4 mask aligner, where the exposed PR is developed in CD-26. Any potential GaOx on the front-side contacts are etched in HCl. After the GaOx etch the frontside contacts are electroplated at 6mA for 13.5 min, resulting in a contact thickness of 1.3 µm. The frontside photoresist is then removed and the samples are spincoated one last time. The next lithography step protects the active cell areas during a mesa etch used to isolate neighboring cells. The mesa etch is done using 3:1:25 H₃PO₄:H₂O₂:H₂O solution and concentrated HCl. The photoresist is then stripped and the active area contacts are etched using a stirred NH₄OH:H₂O₂:H₂O solution. A process flow of the fabrication procedure is given in Fig. 2.2.

The final device contains 12 1x1 cm², two 0.5x0.5 cm² QE pads, two 0.5x0.5 cm² EL pads and multiple TLM pads for the occasional sheet resistance measurement. An image of a fabricated device is given in Fig. 2.3.
2.2 Effects of Strain-Balancing on Device Performance

Before investigating the effects of quantum wells on device performance, a baseline sample (BL) was fabricated and used as a benchmark for future quantum well device comparison. The baseline structure is given in Fig. 2.4 using the layer structure described in detail below. Illuminated J-V under AM0, external quantum efficiency and dark J-V analysis were performed, with plots and extracted parameters of each given in Fig. 2.5.

The BL $V_{oc}$ is quite high given the 1.42eV bandgap of GaAs, translating into a $W_{oc}$ of 0.377V which is simply the difference between the material bandgap and open-circuit voltage and is used to compare device quality across various bandgap materials. A $W_{oc}$ below 0.4V is common for high-quality solar cell devices [22]. The discrepancy between the integrated short-circuit current from EQE and the measured value from AM0 illumination coincides with a grid-finger shadowing loss of roughly 3%, a factor common in all devices given the identical lithography mask set used in fabrication.
The first set of quantum well devices investigated in this work focused primarily on performance effects of strain-balancing in 3-period and 6-period QW samples. The structures were grown on p-GaAs (100) wafers with 2° offcuts toward <110> and included 9.2nm In_{0.07}Ga_{0.93}As wells separated by either 4nm GaAs strained or 3.2nm GaAs_{0.68}P_{0.32} strain-balanced barriers. The thickness of the GaAs_{0.68}P_{0.32} barrier was determined by matching the average lattice constant of a single In_{0.07}Ga_{0.93}As-GaAs_{0.68}P_{0.32} stack with the lattice constant of GaAs [23]:

$$<a> = \frac{2t_b a_{GaAsP} + t_{QW} a_{InGaAs}}{2t_b + t_{QW}} = a_{GaAs} = 5.653 \text{Å}$$  \hspace{1cm} (2.1)$$

where $t_b$ and $t_{QW}$ are the layer thicknesses corresponding to the GaAsP barrier and InGaAs well, respectively, and $a$ is the composition-dependent lattice constant of each layer. This, in
Figure 2.5: (left) Illuminated J-V performance under AM0, (right) Dark J-V analysis with a two-diode model fit and (bottom) External Quantum Efficiency from 300-1000nm of the initial baseline structure BL.

\[ \langle f \rangle = \frac{\langle a \rangle - a_{GaAs}}{a_{GaAs}} \quad (2.2) \]

Ideally, the average strain across the SL would be zero, allowing for multiple periods that contribute no net strain to the overall structure. There is, however, inherent localized strain between the alternating layers that may introduce defects at the well-barrier interface. As the wells get deeper (increased In-composition) or the barriers get thinner (increased P-composition), the
localized strain increases, making strain-balancing more sensitive to slight variations in composition and thickness in both the vertical and lateral direction with respect to growth.

Fig. 2.6 shows the layer design of the initial quantum well devices. The polarity of all devices in this study is n-i-p, meaning the junction consists of an n-type emitter, an unintentionally-doped i-region and a p-type base.

The device structures outside the i-region are nominally identical, allowing for a direct comparison between the strained vs SB QW superlattices. Working from the surface down, the top 150nm is an n-type GaAs contact layer, highly doped to provide an ohmic contact to the electroplated Au. Below the contact is a 50nm n-type InAlP : Si window, or front surface field (FSF), used to prevent hole recombination near the metal-semiconductor interface. The n-i-p junction then begins, made up of a 50nm n-type InGaP : Si emitter, a ∼200nm i-region which is nominally doped around 1e15 cm⁻³, and a 2.68µm p-type GaAs : C base. Similar to the FSF, a 50nm highly doped p-type InGaP : Zn back surface field (BSF) is added to prevent electron recombination near the bottom metal-semiconductor interface. The thicknesses were chosen based on minority carrier diffusion lengths in each respective layer. A good rule of thumb is to design layers to be no more than 3x thicker than the minority carrier diffusion length. The typical growth rate for GaAs in RIT’s MOVPE is 2.3µm/hr, with high V/III ratios of 45+ to allow for stable III-V bonds and to prevent group-III droplet formation on the epi-surface. Layer dopings and compositions are individually calibrated through Hall and HRXRD analysis of thick (200+nm) growth on GaAs substrates.

Characterization techniques used on these devices include AM0 LIV performance along with QE and CCE. LIV curves are given in Fig. 2.7 and statistics in Table 2.1. The most notable trend from Table 2.1 is the improved uniformity of $V_{oc}$ across the wafers once SB is
Figure 2.6: Initial structures investigating strain-balancing, utilizing 3x 9.2nm In$_{0.07}$Ga$_{0.93}$As wells. Device (A) contains 4nm strained GaAs barriers, (B) 3xSB 3.2nm GaAs$_{0.68}$P$_{0.32}$ barriers, (C) 6xSB 3.2nm GaAs$_{0.68}$P$_{0.32}$ barriers introduced. The $V_{oc}$ in samples B and C also remains within 10mV of the baseline, which was expected since the structures contain relatively few quantum wells. This recovery in $V_{oc}$ is a direct result of strain-balancing. As more wells are added to the i-region $V_{oc}$ is expected to decrease, but the impacts of SB were already apparent at these early stages.

Overall device $J_{sc}$ did not increase with 3x or 6xQWs, but the current production from the wells is visible in the EQE curves, given in Fig. 2.8. The current production per well was

<table>
<thead>
<tr>
<th>Sample</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>$V_{oc}$ (mV)</th>
<th>$FF$ (%)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A - 3xQW</td>
<td>25.9 ± 0.1</td>
<td>1020 ± 10</td>
<td>83 ± 1</td>
<td>15.9 ± 0.4</td>
</tr>
<tr>
<td>B - 3xSBQW</td>
<td>25.57 ± 0.09</td>
<td>1041 ± 3</td>
<td>84 ± 3</td>
<td>16.4 ± 0.5</td>
</tr>
<tr>
<td>C - 6xSBQW</td>
<td>25.86 ± 0.07</td>
<td>1035 ± 5</td>
<td>84.2 ± 0.6</td>
<td>16.4 ± 0.5</td>
</tr>
<tr>
<td>BL</td>
<td>25.8 ± 0.02</td>
<td>1043 ± 2</td>
<td>85.2 ± 0.6</td>
<td>16.8 ± 0.2</td>
</tr>
</tbody>
</table>
found to be 13.3\(\mu A\) for sample A and 10\(\mu A\) for samples B and C. The QW sub-band peaks of the SB wells do appear to follow a linear relationship with well number, given the doubling of peak height and steady current production per well going from 3 to 6xSBQW. The non-SB wells show two energy transitions at 935nm and 905nm, while the SB wells only show a single transition at 905nm. This could mean that indium incorporation inside the wells is lower in a strain-balanced SL structure relative to a non-strain-balanced SL structure, leading to a blueshift in the QW bandedge.

Carrier collection efficiency (CCE) was utilized to probe this shift going to SB wells. CCE results for the 3xQW and 3xSBQW devices are given in Fig. 2.9. As positive bias is applies to
Figure 2.8: EQE spectra of samples A, B and C taken on QE pads. The overall device spectrum is shown on the left, while sub-band collection is inset on the right with the BL sub-band EQE used for extraction of QW current production.

Sample A, effectively 'flattening the bands' and reducing the electric field across the i-region, the 935nm peak becomes attenuated, while the 905nm peak in both samples A and B remains fixed. From this it can be inferred that the low-energy carriers at 935nm rely on a strong electric field to escape the wells before recombining. Therefore, the increased barrier height due to strain-balancing using 32%P barriers is limiting the low-energy carriers generated in the wells from escaping thermally, hinting at strong non-radiative recombination in the i-region.
2.2.1 Updated QW Device Designs after MOVPE Repair

After emergency repairs were done on the MOVPE showerhead, three test devices were grown to gauge the health of the reactor. These structures, shown in Fig. 2.10, were grown on 6° < 110 > offcuts instead of the previously used 2° < 110 > offcuts in premature preparation of a multijunction device which has yet to come into fruition. The effects of substrate offcut, or misorientation, will be discussed in detail in section 2.6. The devices included slight variations in layer design from previous samples, most notably a thicker base layer to improve current collection in the base, moving from 2.68µm in samples A-C to 3.5µm, a thinner InAlP window of 25nm doped to \(-9.5 \times 10^{17} \text{cm}^{-3}\) with Te instead of Si, and a 200nm i-region. Sample D was used as a baseline, with no QWs. Sample E included 3xQWs without strain-balancing, still using a nominal 9.2nm 8%In well between 4nm GaAs barriers. Sample F had slightly deeper wells, using 10%In and SB 4.9nm 32%P barriers.

![Figure 2.9: CCE analysis of 3xQW investigating the sub-band collection of the wells with (B) and without (A) SB.](image-url)
Figure 2.10: Test structures grown after MOVPE showerhead repair. Sample (D) contains no QWs, (E) 3x strained 9.2nm In$_{0.08}$Ga$_{0.92}$As wells using 4nm GaAs barriers, (F) 3xSB 9.2nm In$_{0.1}$Ga$_{0.9}$As wells using 4.9nm GaAs$_{0.68}$P$_{0.32}$ barriers.

The LIV results, shown in Fig. 2.11 of devices D-F immediately reveals the impact of built-up compressive strain in the i-region. Without SB, $V_{oc}$ drops 41mV compared to the baseline. This $V_{oc}$ drop is nearly 2x larger than the previous non-strain-balanced device, A, because the GaAs base doping was lowered by a factor of three after MOVPE repairs. With SB of 3x 10%In wells, $V_{oc}$ remains above 1.040V. Dark J-V fitting results using Eq. 1.1 of samples D-F are given in Table 2.2. The fitted saturation current densities reveals that the recombination mechanism limiting $V_{oc}$ is in fact non-radiative recombination inside the n-i-p junction. This non-radiative recombination is expressed through the $J_{02}$ saturation current in the two-diode model. The $J_{02}$ component without SB increases an order of magnitude relative to both the
Table 2.2: Two-Diode Model Dark J-V Fitting Results: Samples D-F

<table>
<thead>
<tr>
<th>Sample</th>
<th>$J_{01}(A/cm^2)$</th>
<th>$J_{02}(A/cm^2)$</th>
<th>$V_{oc}(mV)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>D - Baseline</td>
<td>$7.9 \times 10^{-20}$</td>
<td>$3.6 \times 10^{-12}$</td>
<td>1043</td>
</tr>
<tr>
<td>E - 3xQW no SB</td>
<td>$3.5 \times 10^{-19}$</td>
<td>$4.0 \times 10^{-11}$</td>
<td>988</td>
</tr>
<tr>
<td>F - 3xSBQW</td>
<td>$6.0 \times 10^{-20}$</td>
<td>$8.0 \times 10^{-12}$</td>
<td>1040</td>
</tr>
</tbody>
</table>

Baseline and SB devices, leading to the loss in $V_{oc}$ following Eq. 1.4.

Figure 2.11: LIV results of samples D-F, showing the effects on $V_{oc}$ of excess strain buildup in the i-region.

Additionally, $J_{sc}$ increases in the 3xSBQW device by an average of 0.17mA/cm$^2$ compared to the baseline. A portion of the observed $J_{sc}$ boost is a result of the QWs. Interestingly, the 3xSBQW device is still showing a blueshift in sub-band collection even though the wells contain 2% more indium, which lowers the QW bandgap and should lead to a redshift in QW absorption. This is the same trend observed between devices A-C, where strain-balancing supresses QW current generation relative to its strained counterpart. This phenomenon will be
discussed in more detail in section 2.6.

Photoluminescence (PL) of samples E and F in Fig. 2.13 confirms the blueshift after introducing strain-balancing. The nominal 8%In QWs in sample E show a sharp QW emission peak at 930nm with a FWHM of 18nm (25meV). The nominal 10%In SBQWs in sample F show a suppressed QW emission peak blueshifted by 8nm with a larger FWHM of 31nm. Larger PL FWHM can be attributed to roughness at the well-barrier interface or compositional variation inside the well [24]. Between samples A-F, there is not yet enough data to determine which influence is driving the larger FWHM in the SB wells, but in either case the material quality of individual layers appears to degrade with the inclusion of GaAs$_{0.68}$P$_{0.32}$ barriers. This degradation may be causing the lower QW current production in SB wells, but does not yet translate into the dramatic $V_{oc}$ losses observed in the non-SB devices.
Figure 2.13: Photoluminescence spectra of samples E and F, normalized to the 973nm GaAs peak.

2.3 Addition of a Distributed Bragg reflectors

Distributed Bragg reflectors (DBRs) have been studied extensively in high-performance lasers since the 1990s to confine photons emitted from InGaAs wells, lowering the threshold, or turn-on, current for lasing [25]. The III-V PV community quickly adopted similar DBRs to improve photon absorption in thin-film devices [18]. In the PV field, however, DBRs are used to reflect light that was not collected by the QWs, acting as a selective mirror. This gives the wells another chance to absorb any transmitted photons and ideally doubles the current generation in the wells without extending the i-region. The DBR is especially valuable because it assists in more efficiently bringing the InGaAs wells to their optical thickness of roughly 1.0-1.5µm, the equivalent of 100-150 wells [22].

Alternating sub-100nm layers of Al$_{0.9}$Ga$_{0.1}$As and Al$_{0.1}$Ga$_{0.9}$As with refractive indices of
n=3.05 and n=3.52 targeting 900nm wavelength photons, respectively, were previously studied as the DBR pairs. Assuming normal incidence, reflectivity between two adjacent layer of different refractive indices can be calculated using:

\[ R(\lambda) = \left| \frac{n_1 - n_2}{n_1 + n_2} \right|^2 \]  

(2.3)

where \( n_1 \) and \( n_2 \) are wavelength-dependent refractive indices of the two layers. Simulations done in TFCalc, a simulation software designed for optical coating optimization, by Dr. Steve Polly shown in Fig. 2.14, reveal the spectral range the DBR can actively reflect, targeting the sub-band wavelengths only accessible by the InGaAs wells.

The reflectivity of the DBR increases as more pairs are added, until nearly all the photons between 900-950nm are reflected back through the device. For maximum reflection, 12 DBR pairs are used, corresponding to a thickness of 2\( \mu \)m. More than 14 pairs would require additional material without improving current collection in the wells. The increase in short-circuit current production is calculated by factoring in the change in reflectance by adding the DBR to a device:

\[ EQE_{\text{DBR}} = EQE \times \frac{1 - R}{1 - R_{DBR}} \]  

(2.4)

The DBR is inserted below the InGaP BSF, as shown in Fig. 2.15, where it is safely reflecting photons around 900nm without adversely affecting recombination in the active regions of the device. The first 12 pair DBR introduced in this study was included in a device with the same nominal structure as sample A, the device with non-SB 3xQW of 9.2nm 7%In wells surrounded by 4nm GaAs barriers. For simple comparison, this initial DBR device will be
Figure 2.14: DBR simulations done by Dr. Steve Polly showing (left) the selective reflection range of alternating 76.2nm Al$_{0.9}$Ga$_{0.1}$As /66.7nm Al$_{0.1}$Ga$_{0.9}$As layers, (right) short-circuit current density vs the number of DBR pairs used. Saturation of current density is denoted by the dashed line at 12-14 pairs, where DBR reflection is maximized.

referred to as $A_{\text{DBR}}$. Both sample A and $A_{\text{DBR}}$ were grown on 2° offcuts toward $<110>$. LIV results comparing samples A and $A_{\text{DBR}}$ are given in Table 2.3. The open-circuit voltage is identical between the two devices and the short-circuit current in the DBR sample does show a 320µA/cm$^2$ increase, resulting in an average efficiency gain of 0.8%. The replicated $V_{oc}$ is supported by LIV fits, returning $J_{02}$ values of $1.31 \times 10^{-11} A/cm^2$ and $1.57 \times 10^{-11} A/cm^2$ for samples A and $A_{\text{DBR}}$, respectively.

The boosted current in the DBR sample can be attributed to both an increase in current

<table>
<thead>
<tr>
<th>Sample</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>$V_{oc}$ (mV)</th>
<th>$FF$ (%)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A - 7%In 3xQW no DBR</td>
<td>25.9 ± 0.1</td>
<td>1020 ± 10</td>
<td>83 ± 1</td>
<td>15.9 ± 0.4</td>
</tr>
<tr>
<td>$A_{\text{DBR}}$ - 7%In 3xQW w/ DBR</td>
<td>26.22 ± 0.07</td>
<td>1020 ± 10</td>
<td>85 ± 1</td>
<td>16.7 ± 0.3</td>
</tr>
</tbody>
</table>
Figure 2.15: Updated layer structure after adding a 12-period AlGaAs DBR to sample A, a non-SB 3xQW device.

production from the wells and a slight overlap between the GaAs base bandedge and the DBR reflection range, shown in Fig. 2.16. The sub-band EQE results support the claim that a DBR, when implemented correctly, can double the current production per well without adversely affecting open-circuit voltage. The sharp sub-band peaks present in sample A_{DBR} are a result of multiple Fabry-Perot resonance cavities throughout the structure. At its most fundamental, a photon reflected off the DBR may be reflected again by one of the many interfaces in the device. This occurs if conditions for total internal reflection of the given photon energy is satisfied and the photon has traveled an integer number of wavelengths before interacting with
2.4 Effects of Deeper Wells

Increasing %In in InGaAs lowers the bandgap of the material and extends the collectable range of the wells. Increasing this collection range allows for a larger decrease in the effective bandgap of GaAs per QW added, which should translate into greater current production in the device. As was mentioned in section 1.4, adding more indium into the wells comes at the cost of increasing the local strain at the well-barrier interface. This makes strain-balancing more difficult and could lead to an increased number of non-radiative recombination centers, or traps, at the interface. The Sugiyama group at the Univ. of Tokyo summarized the effects of increased
strain due to deepening the InGaAs wells beautifully in [27]. Their conclusion, visualized in Fig. 2.17, was that if strain is not properly managed in the i-region, $V_{oc}$, carrier lifetime and potentially fill-factor will degrade. The degradation in $V_{oc}$ has already been observed in section 2.2 when comparing strained vs SB structures using relatively shallow InGaAs wells.

This section will focus on the device performance of moving from 10%In to 14%In wells, which deepens the QW from a bandgap of 1.279eV (970nm) to 1.223eV (1014nm). To calibrate growth conditions and measure strain, two calibration samples were grown targeting 10xSBQW of 9.2nm 10%In and 14%In wells, still SB using GaAs$_{0.68}$P$_{0.32}$ barriers. The zero strain thicknesses of the GaAsP barriers were calculated to be 5.0nm and 6.8nm, giving nominal SL periods of 14.1nm and 15.9nm, respectively. These two calibration structures will be referred to as SL-10 and SL-14, denoting the relative indium percentages of each superlattice.

X-ray diffraction and photoluminescence measurements were taken to characterize strain...
and relative material quality, shown in Fig. 2.18. The XRD SL peaks are heavily attenuated relative to their expected simulation curves created in Leptos, a Bruker dynamic diffraction simulation software that came with the RIT Bruker D8, but strain could still be extracted through angular differences between the zeroth order and Bragg peaks using Eq. 1.23. The XRD strain came out to 370 and 1100 ppm for samples SL-10 and SL-14, along with superlattice periods of 13 and 14.5 nm respectively. These strains and corresponding period thickness results are clear indicators that missing the target zero-strain SL periods by just 2 nm or less after moving to higher %In wells can manifest as nearly tripling the overall SL strain.

The material quality of the superlattices already appears far from ideal given the PL and XRD results. The lack of sharp SL peaks can be attributed to diffuse scattering off of rough well-barrier interfaces [28]. This observation is also supported by the loss of Pendellösung fringes present in the simulations, which are highly sensitive to diffuse scattering effects. The
PL results show low-intensity, wide QW peaks, agreeing with the XRD conclusions that interface roughness is prominent in these superlattices. The 14%In wells in SL-14 produce a brighter PL peak shifted by 18nm relative to the 10%In wells, resulting in a 4.5nm shift per 1% increase in indium composition. The brighter peak in SL-14 can be attributed to enhanced carrier generation and eventual radiative recombination in the wells, as expected from deepening the wells.

After calibrating the superlattices, devices were grown using the device design of sample F with 12 wells instead of 3. These devices will be referred to as G-10 and G-14, with labeling following the SL structure. Illuminated J-V curves and EQE are given in Fig. 2.19.

The LIV curves show a rather large drop in $V_{oc}$ of 40mV when increasing indium composition, while the expected overall $J_{sc}$ boost was not observed. To diagnose this $V_{oc}$ loss, dark J-V curves were taken to examine the effects of increased %In QWs on non-radiative recombination in the junction. The resulting saturation currents, given in Table 2.5, reveal a 2.5x increase
in $J_{02}$ going from 10% to 14%In. This increase corresponds to 48mV loss in $V_{oc}$ using Eq. 1.4. The $J_{02}$ increase is due to the larger local strain at the well-barrier interfaces in combination with already rough interfaces, potentially leading to a larger non-radiative recombination center density.

Table 2.4: Dark J-V Fitting Results of G-10 and G-14

<table>
<thead>
<tr>
<th>Sample</th>
<th>$J_{01} (A/cm^2)$</th>
<th>$J_{02} (A/cm^2)$</th>
<th>$V_{oc} (mV)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>G-10 - 10%In</td>
<td>$1.0 \times 10^{-19}$</td>
<td>$1.2 \times 10^{-9}$</td>
<td>881</td>
</tr>
<tr>
<td>12xSBQW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G-14 - 14%In</td>
<td>$5.0 \times 10^{-19}$</td>
<td>$3.0 \times 10^{-9}$</td>
<td>842</td>
</tr>
<tr>
<td>12xSBQW</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Integrated sub-band EQE does reveal the enhanced QW current production in G-14, where the 14 and 10%In wells produce $38.3 \mu A/cm^2$ and $13.3 \mu A/cm^2$ per well respectively. This nearly 3x increase in current production per well is desired for current-matching in a 3J device, but the $V_{oc}$ loss is too large to pursue deeper wells until interface roughness is better managed.

2.5 Including More Quantum Wells

Devices with differing well number have already been investigated in previous sections, but not directly compared. This section will examine the device performance effects of adding additional wells to the i-region.

As wells are added, the i-region becomes thicker, weakening the electric field used to separate charge carriers. Since simulation results in chapter 1 suggest that thermal escape is the dominant escape mechanism, as the i-region grows carrier escape from the wells should remain fairly constant.

The main concern that comes with a thicker i-region is the potential loss in $V_{oc}$. This $V_{oc}$
loss is driven by two complimentary processes; increasing the total InGaAs thickness in the i-region, and adding more interfaces for carriers to non-radiatively recombine. As total InGaAs thickness increases, the effective bandgap of the i-region begins to shrink, causing the quasi-Fermi level splitting to drop along with the bandgap change, which decreases $V_{oc}$ through Eq. 1.8 [29]. With a 12 well superlattice of 9.2nm InGaAs wells, as shown in previous sections, the total InGaAs thickness in the i-region is only 110.4nm, so this effects plays only a minor role in any observed $V_{oc}$ drop. Instead, the addition of well-barrier interfaces in the i-region would drive $V_{oc}$ losses. If interface recombination is managed through successful strain-balancing and abrupt transitions from well to barrier are realized, $V_{oc}$ can be maintained as well number increases, as shown by [30] in Fig. 2.20.

![Figure 2.20: Careful management of well-barrier interfaces leading to a stability in $V_{oc}$ as InGaAs wells are added. Image taken from [30]](image)

The observed effects of well number on $V_{oc}$ of samples investigated thus far are plotted in Fig. 2.21. Even with relatively few data points, $V_{oc}$ is seen to drop as wells are added for all InGaAs compositions. Devices with 6 or less well maintain a $V_{oc}$ above 1.030V, but rapid
The drop-off occurs when moving to 12 wells.

The loss in $V_{oc}$ was investigated through dark J-V fitting, as done in previous sections. The most notable $V_{oc}$ drop in Fig. 2.21 comes in devices with 10%In QWs, or samples F and G-10. Saturation current corresponding to the dark J-V fits, provided in Table 2.5, reveal over a 2 order of magnitude change in $J_{02}$ moving from 3 to 12xQWs. The $J_{01}$ saturation current corresponding to bulk and surface recombination increased by only 67%, suggesting that increasing the number of quantum wells does not adversely affect bulk carrier behavior unless strain propagates into the window and emitter regions under excessive strain accumulation. Therefore, it can still be safely assumed that $V_{oc}$ degradation is dominated by non-radiative recombination in the junction.

Fig. 2.22 shows the sub-band collection of samples F and G-10. Comparing sub-band EQE
Table 2.5: Dark J-V Fitting Results of F and G-10

<table>
<thead>
<tr>
<th>Sample</th>
<th>( J_{01} ) (A/cm(^2))</th>
<th>( J_{02} ) (A/cm(^2))</th>
<th>( V_{oc} ) (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>F - 10%In 3xSBQW</td>
<td>( 6.0 \times 10^{-20} )</td>
<td>( 8.0 \times 10^{-12} )</td>
<td>1034</td>
</tr>
<tr>
<td>G-10 - 10%In 12xSBQW</td>
<td>( 1.0 \times 10^{-19} )</td>
<td>( 1.2 \times 10^{-9} )</td>
<td>872</td>
</tr>
</tbody>
</table>

of these samples supports the claim that thermal escape is driving carrier collection from the i-region. Moving from 3 to 12xSBQWs integrated \( J_{sc} \) quadruples, meaning current production per well remains constant as more wells are added.

In section 2.3 it was found that including a DBR can double sub-band current production. Increasing carrier production through the employment of a DBR has no significant effect on non-radiative recombination, which in turn does not adversely affect \( V_{oc} \) like increasing the number of wells appears to do. To lower the effective device bandgap more wells will be needed, so the accompanied increase in non-radiative recombination will need to be addressed, however a DBR is currently shown to be a more promising avenue for increasing sub-band current production.

## 2.6 Influences of Substrate Offcut

With the long-term goal of current matching the GaAs middle cell of a 3J device, the effects of offcut on 3J structures carry over to this study of GaAs devices. The most important impact of growing the Ge-GaAs-InGaP 3J on a high offcut is effective management of antiphase domains that appear at the Ge-GaAs interface due to a transition from a non-polar to a polar semiconductor. Introducing a high offcut adds disorder to the atomic bonds, preventing dislocation propagation into the GaAs subcell from Ga-Ga or As-As bonds [31]. Fig. 2.23 shows
Figure 2.22: Sub-band EQE of Samples F and G-10 compared to a baseline for extraction of current production per well.

that misfit dislocations are held at the Ge-GaAs interface as offcut angle is increased.

Figure 2.23: [220] Bright-Field TEM images showing anti-phase domain management at the Ge-GaAs interface as substrate offcut angle is increased. Image taken from [31].

In addition, the InGaP bandgap can be tuned between 1.85-2.00eV through lattice ordering effects by growing on misoriented offcut substrates or rapid thermal annealing [32]. As InGaP becomes more disordered, its bandgap blueshifts. This effect allows the top InGaP sub-cell to better manage thermalization losses and may increase its \( V_{oc} \). Growing InGaP on a larger offcut substrate leads to more disorder, so 3J devices are preferentially grown on either 6°, 10°
Figure 2.24: Diagram of step edge development due to a misoriented substrate. The \( <100> \) plane defines the terrace normal and the \( <110> \) plane determines the offcut orientation for substrates used in this work.

or 15\(^\circ\) offcuts.

A misoriented substrate produces atomic step-edges with terrace widths that decrease with increasing offcut, following the geometric relationship of:

\[
l = d \cot \theta
\]  

(2.5)

where \( d \) is the distance between adjacent lattice planes normal to the surface and \( \theta \) is the misorientation angle. In the case of the GaAs substrates used in this work, the surface normal is \( <100> \), corresponding to a d-spacing of 5.653 Å. Fig. 2.24 provides a visualization of step edge formation from misorientation towards to \( <110> \) plane.

Atoms incident on the terraces during growth (adatoms) preferentially adhere at the step edges because the Ehrlich-Schwoebel barrier present from additional dangling bonds provides a minimum energy that adatoms are drawn towards. In the case of InGaAs and GaAsP growth, step bunching occurs as a result of differing incorporation rates from ascending and descending adatoms, leading to lateral, periodic variation in layer thickness [33]. Step bunching has also been shown to increase with local strain between the well and barrier layers as well as with
Figure 2.25: (left) XRD and (right) Photoluminescence of samples SL-0, SL-2 and SL-6. The broad red-shift GaAs PL peak in SL-0 is due to a Zn-doped substrate used on the 0° sample, which is not related to the quality of the epi-structure.

Calibration samples comparing the material quality of a 10xSB 9.2nm In\textsubscript{0.1}Ga\textsubscript{0.9}As- 6.7nm GaAs\textsubscript{0.68}P\textsubscript{0.32} superlattice were grown using the same growth conditions as previous samples on 0°, 2° and 6° offcuts towards <110>. The three calibration samples will be referred to as SL-0, SL-2 and SL-6, denoting their offcut angles. X-ray diffraction and photoluminescence measurements were taken to compare the material quality of the superlattices. The XRD results shown in Fig. 2.25 reveal high quality interfaces in SL-0, given the sharp SL peaks and preserved Pendellösung fringes. Samples SL-2 and SL-6 lose all SL fringes, suggesting that interface roughness emerges even at a rather low offcut angle of 2 degrees. The same trends are present in the PL results, where the quantum well peak FWHM grows from 18.6nm in SL-0 to 46.4nm in SL-6.

To further investigate the observed interface roughening as offcut angle increases, TEM images were taken of the superlattices, shown in Fig. 2.26. The undulating growth in both
Figure 2.26: [220] Dark-Field TEM images of (left) SL-0, (middle) SL-2, (right) SL-6 with increased variations in well and barrier thicknesses as step-bunching worsens. InGaAs - dark, GaAsP - bright. TEM data was provided by Nikhil Pokharel at the South Dakota School of Mines and Technology.

offcut samples shows strong step bunching effects while the InGaAs-GaAsP transitions are still visible, supporting XRD and PL findings that interface roughness is the cause of peak widening and attenuation. As offcut increases from $2^\circ$ to $6^\circ$ the undulations grow and begin to affect the GaAs layer above. If more wells are grown on a $6^\circ$ device, strain accumulation would begin to extend into the emitter and possibly to the top-most regions of the device, leading to degradation above the i-region.

Strain-balanced device performance has not been directly compared between offcuts using the superlattice structures presented in this chapter. However, devices analyzed in chapter 3 will compare $0^\circ$ to $2^\circ$ offcut samples.
2.7 Conclusions

Throughout this chapter the effects of strain-balancing, distributed Bragg reflectors, well depth and substrate offcut were investigated. Strain-balancing was shown to be necessary as accumulated strain builds with the addition of wells. $V_{oc}$ quickly degraded by 52mV in 3xQW devices as $J_{02}$ increased from 8e-12 with strain-balancing to 4e-11 $\frac{A}{cm^2}$ without strain-balancing. Quantum well current collection decreased as strain-balancing was introduced, along with a consistent blue-shift in the QW absorption peak relative to non-strain-balanced wells.

Distributed bragg reflectors provided promising results with regards to current production. The DBR design was chosen to be a 12-period stack of alternating $Al_{0.9}Ga_{0.1}As$ and $Al_{0.1}Ga_{0.9}As$ layers, which increased the reflection of QW accessible photons above 90%. Since the DBR is places outside the active region of the device it did not cause any significant changes to $J_{02}$ and gave an identical $V_{oc}$ to it non-DBR counterpart.

Deepening the wells through increasing the indium composition from 10% to 14% led to a 40mV drop in $V_{oc}$ but did increase the current production per well to 38.3 $\frac{\mu A}{cm^2}$ from 13.3 $\frac{\mu A}{cm^2}$. With the 32%P barriers, moving from 3 to 12xSBQW increased $J_{02}$ by three orders of magnitude, resulting in a severe 162mV drop in $V_{oc}$.

Section 2.6 showed that growing the superlattices on an offcut substrate caused dramatic degradation in material quality. XRD SL peaks became attenuated beyond recognition, suggesting that interface roughness is playing a major role in the superlattice growth. TEM images investigating growth on 2° and 6° offcuts confirmed that interface roughness begins distorting the superlattice once step-edges are available for indium adatoms to diffuse to.
Chapter 3

Lower Strain Barrier QW Results

3.1 Prior Work

A majority of the work on InGaAs-GaAsP superlattices for use in GaAs solar cells has been done using deep well layers of 20+%In strain-balanced using sub-10nm 30+%P GaAsP barriers [19]. Using thin barriers allows for more well material to be placed in the i-region, translating into greater current production and assisting in tunneling escape from the wells. However, the open-circuit voltages of such devices remains low [19].

Other groups such as Imperial College and more recently NREL have shown that lower bandgap, thicker GaAsP barriers can still lead to substantial QW current generation without sacrificing $V_{oc}$ as severely. The devices presented in Steiner et. al included 50+ 11%In InGaAs wells surrounded by 10%P GaAsP barriers, reaching a sub-band QW EQE of 60% [22].
3.2 Optimizing Growth Flow Sequences

Improving the well-barrier interface began with optimizing growth conditions. As shown in Fig. 2.26, the poor interfaces began once offcuts were introduced. The wavy growths observed in the $2^\circ$ and $6^\circ$ offcut samples can be attributed to a combination of effects driven by phosphorus and indium growth. When indium is grown on GaAs the lower binding energy of InAs (1.53eV) relative to GaAs (1.73eV) prevents indium from diffusing, leaving it to 'float' on the surface until InAs monolayers form or the surface indium atoms fully incorporate into the epi structure [35]. As growth temperature increases indium segregation effects become more pronounced. At higher temperatures the indium atoms have more energy to migrate along the growth surface, which allows them to more easily adhere to the step-edges. Local strain also increases indium surface segregation through the inclusion of an elastic energy contribution that promotes surface diffusion over lattice incorporation, as shown in [34] and [35]. Both effects described above lead to indium step-bunching.

The GaAsP barrier growth enhances step-bunching effects through the interplay between As and P. Arsenic has been known to desorb slowly from the epi surface, preventing phosphorus from adsorbing at the start of GaAsP growth [36]. This effect leads to the potential formation of an InGaAsP quaternary at the well-barrier interface along with non-uniform phosphorus incorporation in the barrier. Both of these effects can lead to deviations in local strain-balancing, which only further increases indium segregation.

To better manage indium surface segregation and slow phosphorus adsorption, 10xSBQW $\text{In}_{0.1}\text{Ga}_{0.9}\text{As-GaAs}_{0.68}\text{P}_{0.32}$ superlattice calibration samples were grown on $0^\circ$ offcut $< 100 >$
GaAs using three gas flow sequences, labelled SL-f0, SL-f1 and SL-f2. The calibration structure and flow sequences investigated are given in Fig. 3.2. Sample SL-f0 was grown using the same flow sequence present in all Chapter 2 QW samples, containing thin GaAs interlayers between the wells and barriers and additional flow steps to address As-P adsorption. Sample SL-f1 removes the GaAs interlayers while addressing InGaAsP formation through clearing the surface of phosphorus with an $H_2$ purge after barrier growth. Sample SL-f2 re-introduces the GaAs interlayers to prevent intermixing as well as three $H_2$ purge steps to remove indium and phosphorus from the epi surface after well and barrier growths. Samples SL-f0 and SL-f2 include $PH_3$ and $AsH_3$ preflows ahead of barrier growth to stabilize As and P exchange so the As and P surface compositions stabilize.

To compare the resulting superlattice material qualities of each flow sequence, photoluminescence and x-ray diffraction data were taken. The PL and XRD results are given in Fig. 3.2.
The superlattice peaks in SL-f2 have an average FWHM of 264sec relative to the respective 334sec and 321sec FWHMs for samples SL-f0 and SL-f1, along with more prominent Pendellösung fringes. PL results show identical QW peak positions, meaning that adjusting the flow sequences does not change well composition. However, removing the GaAs interlayers in SL-f1 resulted in a lower QW peak intensity. The GaAs interlayers appear to help minimize intermixing at the well-barrier interface, as was shown in [39].

Flushing the surface before switching between well and barrier growth along with keeping thin GaAs interlayers has shown improvements in SL material quality. Moving forward, the SL-f2 flow sequence will be used to grow the QW superlattice.
3.3 Investigating Lower Strain 10%P Barriers

As discussed in section 2.6, indium step-bunching effects increase as local strain between the well and barrier increases. The lattice mismatch between the nominal $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ well and $\text{GaAs}_{0.68}\text{P}_{0.32}$ barrier leads to a local strain of $1.86 \times 10^{-2}$. Moving to a shorter 10%P GaAsP barrier reduces the local strain to $1.07 \times 10^{-2}$, nearly half the strain present in the 32%P barriers. Maintaining the 9.2nm $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ wells, this new 10%P barrier requires that the GaAsP thickness must be increased from 6.7nm to 17nm following the strain-balancing conditions described in section 2.2.

To test the impact of lower %P barriers against previous superlattices three calibration samples were grown, this time on $< 100 > \text{GaAs}$ oriented 2° towards $< 110 >$. Samples SL-P1 and SL-P2 consist of nominally identical 32%P barriers but were grown at 670°C, 600mbar & 620°C, 100mbar respectively. Sample SL-P3 consisted of 17nm 10%P barriers grown at 650°C and 100mbar. These three structures will be compared to the 32%P 10xSBQW sample grown on a 2° $< 110 >$ substrates at °C and 100mbar discussed in section 2.6, SL-2.

Again, XRD and PL were used to compare the material quality of the calibration samples, given in Fig. 3.3. It is immediately clear that moving to offcut substrates quenches the superlattice peaks present in the section 3.2 0° samples. This peak attenuation was observed in section 2.4 and has been shown to be caused by interface roughness present in the Chapter 2 TEM image of sample SL-2. Raising the growth temperature from 650°C to 670°C and pressure from 100mbar to 600mbar led to a blueshift in the QW PL peak as well as providing GaAsP XRD SL peaks. The higher growth temperature may have reduced In-incorporation in the wells, which was previously observed in [35]. Extracting $\text{GaAs}_{1-x}\text{P}_x$ composition from the two SL
peaks revealed that the barriers were taller than expected, with a phosphorus composition of 38%. The increased %P was due to increased phosphorus adsorption from a higher growth temperature. Decreasing the growth temperature in SL-P2 to 620°C also brought on XRD SL peaks in both the wells and barriers. The improved material quality is evident in the bright PL peak as well, suggesting that non-radiative recombination in the wells becomes suppressed as growth temperature decreases.

Most notably, dropping the phosphorus composition to 10% in SL-P3 recovered the SL peaks with an average FWHM of 260sec, comparable to the 0° offcut samples with 32%P barriers. In addition to the high quality XRD scan, the QW PL peak in sample SL-P3 is significantly brighter than all 32%P barrier samples. The FWHM of the QW peak is 20.4nm, compared to 35nm in sample SL-P0, the original SL structure. Both observations suggest that
lowering the barrier phosphorus composition, effectively reducing the local strain at the well-barrier interface, dramatically restored interface sharpness as well as compositional uniformity in the wells.

Temperature-dependent PL (TDPL) was performed on samples SL-2 and SL-P3 to support the XRD and room-temperature PL results. The temperature dependence of photoluminescence can be modeled through the Arrhenius equation:

$$I(t) = \frac{I_0}{1 + \sum_i C_i \exp \left( -\frac{E_i}{kT} \right)}$$

(3.1)

where $C_i = \frac{\tau_{rad}}{\tau_{nr}}$ and $E_i$ is the activation energy associated with a single non-radiative recombination center [40]. As temperature increases in the calibration samples generated carriers in the wells gain thermal energy, which is used to escape into the barriers where the carriers will eventually recombine without an electric field to assist in tunneling. As was done in [24], two non-radiative recombination centers will be used in TDPL fitting; a low-temperature recombination at the well-barrier interface due to trap centers, and a higher-energy recombination center associated with successful thermal escape from the wells that ends with recombination in the barrier. The TDPL data and fitting results are given in Fig. 3.4.

From the fit results, the low-temperature non-radiative recombination centers lie at the same energy for both 10% and 32%P barrier samples but the density of these states ($C_1$) is an order of magnitude larger in SL-2. Since $E_1$ is the same between both samples, the non-radiative recombination mechanism is consistent regardless of phosphorus composition but is more prevalent in the 32%P barrier superlattice. As temperature increases, these interfacial trap states become saturated as more carriers are able to escape the wells. Moving from 32%P to
Figure 3.4: (left) TDPL raw data and fit curve and (right) fit results of samples SL-2 and SL-P3. 10\%P barriers the activation energy of thermal escape decreases, as was expected with moving to a shorter barrier.

3.4 Offcut Effects on Material Quality

The previous section revealed that decreasing strain at the well-barrier interface produced not only sharper interfaces but also an enhancement in radiative recombination in the wells. With the overarching goal of this work being to increase current-production in the GaAs sub-cell of a 3J device with minimal loss in $V_{oc}$, more calibration samples were grown to test the resilience against step-bunching in larger superlattices containing 25xSBQWs. These 25xSBQW calibration samples utilize the same nominal superlattice configuration in section 3.3 - 9.2nm In$_{0.1}$Ga$_{0.9}$As wells and 17nm GaAs$_{0.9}$P$_{0.1}$ barriers.

Extending the growth temperature investigation to this 25xSBQW study, each of the three 2° offcut substrate orientations investigated will be grown at 600°C and 650°C. The three 2° offcut substrates vary in their orientation, either towards $<110>$, $<111>A$ or $<111>B$. The A
Figure 3.5: (left) XRD and (right) PL of samples SL-H110, SL-H111A, SL-H111B, all grown at 650°C.

and B in the <111> orientations refer to gallium or arsenic terminated surfaces, respectively [41]. The samples will be referred to by growth temperature using SL-H for samples grown at 650°C and SL-L for samples grown at 600°C, followed by the orientation direction, 110, 111A or 111B. XRD and PL of the 650°C samples, SL-H110, SL-H111A and SL-H111B are shown in Fig. 3.5, while XRD of SL-L110 compared to SL-H110 is given in Fig. 3.7.

In all three XRD curves, bi-modal SL peaks are prevalent, suggesting that there is a transition to a second superlattice period as additional wells are grown. This transitional point can be observed in the sudden change in curvature between periods 7-11 in EpiTT data of the growth along with a cross-sectional TEM image of sample SL-H110, shown in Fig. 3.6. NREL has recently observed the same phenomena in their TEM image of an 80xSBQW solar cell grown on 2° <111>B GaAs where rippling growth appears in the upper 2/3 of the superlattice [22].

The rippling behavior in both superlattices is again caused by step-bunching, leading to a slow build-up of local strain near the step edges. This local strain eventually causes lateral
Figure 3.6: (left) EpiTT and (right) TEM of sample SL-H110 showing evidence for bi-modal growth of SL past the 7th SL period.

variation in layer thicknesses, manifesting as ripples instead of the extreme undulations present in Fig. 2.26. The extracted strain from XRD using SL peak positions of SL-H110 reveals a transition from 169ppm in the lower portion of the SL to 1700ppm in the upper portion. This transition matches the period where there is a change in slope of EpiTT curvature (green curve) of SL-H110. Fortunately for NREL, their rippling did not translate into significant dislocation formation or dramatic losses in device performance.

Although the XRD data in Fig. 3.5 shows a slight improvement in SL peak FWHM of 296sec for the $<111>A$ vs. 345sec for the $<110>$ orientation, the PL results reveal a 3x taller QW peak in the $<111>A$ offcut relative to $<110>$ and $<111>B$. This dramatic increase in QW luminescence suggests that SL growth on a $<111>A$ oriented substrate may be more impervious to non-radiative traps between the wells and barriers. The exact mechanisms for this increase in PL intensity are not fully understood, but may be related to change in arsenic step coverage moving from $<110>$ to $<111>A$, which has been shown to change growth rates and adatom surface diffusion [24]. Temperature-dependent photoluminescence would help
Figure 3.7: (left) XRD of SL-H110 and SL-L110. (right) PL of samples SL-L110, SL-L111A and SL-L111B.

analyze any recombination effects quantitatively, but has not been performed in this study.

Dropping the growth temperature to 600° appears to sharpen the interfaces and recover single period XRD superlattice fringes shown in Fig. 3.7. The average superlattice FWHM decreases from 388sec in SL-H110 to 163sec in SL-L110, corresponding to improvements in compositional uniformity and layer thickness in both InGaAs and GaAsP. The PL results for the 600° samples, also shown in Fig. 3.7, reveal that even with the improved uniformity, radiative recombination in the wells can decrease along with temperature possibly due to impurity incorporation in the superlattice [42]. All three offcut orientations produce PL spectra of similar intensities, suggesting that superlattice growth at 600°C may lead to additional non-radiative recombination centers even if interface quality is improved.
3.5 10%P Barrier Device Results

The superlattice analysis done in previous sections suggests that shifting to a 17nm 10%P GaAsP barrier dramatically improves the well-barrier interface quality. With the improved material quality, device performance is expected to also see improvements in current production from the wells along with a potential $V_{oc}$ recovery when wells are added to the i-region.

P-type $2^\circ <111>$ A offcut substrates were not available at the time of the upcoming experiment, but will provide an interesting study if they are investigated in future work. Instead, four samples were grown on $2^\circ <110>$ offcut p-type GaAs to examine the effects of well number and growth temperature on device performance. The samples were grown with either 6x or 12xSBQWs grown at 600°C or 650°C following the structures shown in Fig. 2.10 with superlattices grown using the optimized SL-f2 gas flow switching sequence outlined in Fig. 3.1. The samples with i-regions grown at 600°C will be referred to as H-L6 and H-L12 and the samples with i-regions grown at 650°C will be referred to as H-H6 and H-H12, with the 6 and 12 denoting the number of wells included. EpiTT curvature analysis reported compressive strains of 98, 127, 318 and 129ppm for samples H-L6, H-L12, H-H6 and H-H12 respectively, which are on target with the previous calibration samples and already 3x lower than the equivalent 32%P barrier devices.

AM0 illuminated J-V results are given in Table 3.1 and curves of the best cells on each wafer can be seen in Fig. 3.8. The $V_{oc}$ drop when adding wells is still present in this round but the 12xSBQW devices are already showing a 130mV recovery relative to their 32%P barrier counterparts. The anticipated boost in current production from decreasing local strain between the wells and barriers is not present in the LIV results but is reflected in the sub-band EQE
Table 3.1: AM0 LIV Statistics for 10%P Barrier Devices

<table>
<thead>
<tr>
<th>Sample</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>$V_{oc}$ (mV)</th>
<th>$FF$ (%)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>H-L6 - 600° 6xSBQW</td>
<td>26.0 ± 0.2</td>
<td>1012 ± 8</td>
<td>80 ± 4</td>
<td>15.5 ± 1.0</td>
</tr>
<tr>
<td>H-L12 - 600° 12xSBQW</td>
<td>26.1 ± 0.2</td>
<td>1005 ± 2</td>
<td>76 ± 2</td>
<td>14.2 ± 0.6</td>
</tr>
<tr>
<td>H-H6 - 650° 6xSBQW</td>
<td>25.6 ± 0.2</td>
<td>1019 ± 2</td>
<td>81 ± 3</td>
<td>15.6 ± 0.6</td>
</tr>
<tr>
<td>H-H12 - 650° 12xSBQW</td>
<td>25.5 ± 0.2</td>
<td>1006 ± 4</td>
<td>78 ± 2</td>
<td>14.7 ± 0.4</td>
</tr>
<tr>
<td>D- Baseline</td>
<td>25.8 ± 0.2</td>
<td>1043 ± 2</td>
<td>85.2 ± 0.6</td>
<td>16.8 ± 0.2</td>
</tr>
</tbody>
</table>

given in Fig. 3.9. The low fill-factors in this round are related to metallization issues during fabrication and are not a reflection of material quality.

The sharp QW peaks at 925nm reflect the improved superlattice material quality previously observed in XRD and PL, with the 12xSBQW samples reaching 10% QW EQE. The extracted sub-band current production corresponds to 37 and 32 $\mu$A $\text{well}^{-1}$ in H-L6 an H-L12 and 35 $\mu$A $\text{well}^{-1}$ in both H-H6 and H-H12. This increased current generation from the wells is more than double the 13 $\mu$A $\text{well}^{-1}$ production in sample G-10, a 12xSBQW device with 10%In wells and 32%P barriers. As well number increased from 6x to 12x, current production per well remained constant, confirming that these 17nm barrier devices are still thermal-escape dominated, as was suggested in section 2.2. Interestingly, the current production does not change moving between the 600°C and 650°C growth temperatures. There is, however, a slight 5-10mV drop $V_{oc}$ after decreasing the growth temperature but this difference is not large enough to draw any conclusions regarding the relationship well performance and growth temperature.

The relationship between $V_{oc}$ and $J_{02}$ in Fig. 3.10 from fitting the LIV curves shows that $J_{02}$ recovered nearly an order of magnitude relative to the last 12xSBQW device, sample G. As the well number increases from 6 to 12 in the 600°C samples, $J_{02}$ remains unchanged even
though $V_{oc}$ drops 10mV. The same increase in well number in the 650°C samples leads to a 4x increase in $J_{02}$ along with a similar 10mV decrease in $V_{oc}$. From this small sample set, the 10%P barrier devices appear more resilient to $J_{02}$, or non-radiative recombination, increases as more wells are added. Samples H-L6 and H-L12 show slight enhancement in this resilience, but are still reporting overall lower $V_{oc}$ than the samples with superlattices grown at 650°C, H-H6 and H-H12.

### 3.6 Conclusions

In this chapter it was shown that optimizing the gas flow sequences during superlattice growth improved material quality through flushing the surface of indium and phosphorus with $H2$ and
Figure 3.9: (left) Full EQE spectrum and (right) sub-band EQE of samples H-L6, H-L12, H-H6, H-H12.

re-introducing thin GaAs interlayers to prevent quaternary formation between the wells and barriers. Along with optimizing the flow sequence, dropping the phosphorus composition to 10% dramatically improved the interface sharpness. This improvement occurred because high local strain at the well-barrier interface causes an increase in indium segregation at the growth surface, allowing the surface indium atoms to more easily adhere to step-edges on misoriented substrates. When local strain is reduced the compositional uniformity of InGaAs improved, as shown in the sharp PL peak of SL-P3. Temperature-dependent photoluminescence and cross-sectional TEM confirmed the improvement in the well-barrier interface through a decrease in trap density and a delayed onset of lateral thickness variations.

Decreasing growth temperature from 650°C to 600°C was shown to further sharpen the superlattice interfaces. A lower growth temperature decreases the distance surface indium atoms can diffuse, limiting the indium step-bunching that is causing interface roughness. Decreasing
the growth temperature has been known to cause a potential increase in impurity concentration, creating additional non-radiative recombination centers as well as increasing the unintentional doping of the i-region.

Since the QW superlattice designs presented in this work are thermal-escape dominated, current extraction from the wells was shown to remain constant as growth temperature was adjusted. The lower growth temperature devices, however, began to show slight losses in \( V_{oc} \) relative to the 650\(^\circ\) devices. In all 10\%P barrier devices \( J_{02} \) recovered to below \( 1 \times 10^{-10} \ \frac{A}{cm^2} \), with \( V_{oc} \)’s remaining above 1.01V. This result is a massive improvement relative to the 12xSBQW 32\%P barrier device \( V_{oc} \) of 0.872V. Along with the \( V_{oc} \) recovery current
production per well was shown to be above $30\frac{\mu A}{cm^2}$, which is twice as large as the current production of equivalent wells surrounded by 32% P barriers.
Chapter 4

Conclusions

4.1 Summarizing Overall Trends

Successful current-matching of a 3J InGaP-GaAs-Ge requires that the bandgap of the middle GaAs cell be lowered closer to 1.2eV given by SQ detail-balanced theory. To lower the effective GaAs bandgap, low bandgap InGaAs quantum wells are added to the i-region. InGaAs has a larger lattice-constant that GaAs, so balancing the accumulated compressive strain caused by growth of InGaAs on GaAs is essential. Tensile GaAsP barrier layers are added on both sides of the InGaAs wells with thicknesses governed by the strain-balancing conditions of Eq. 2.1. The impact of strain-balancing was immediately apparent in a 3xQW device, where using 32%P barriers maintained a $V_{oc}$ of 1.040V but resorting to 4nm GaAs barriers led to a 21mV loss in $V_{oc}$. Strain-balancing was found to also affect current production in the wells. With strain-balancing the QW absorption peak was consistently blue-shifted relative to non-strain-balanced devices, resulting in lower current production per well.

Including a distributed Bragg reflector assists in increasing well current production by reflecting photons that can be re-absorbed by the wells. Optimization of the DBR revealed that
a 14 period $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$-$\text{Al}_{0.1}\text{Ga}_{0.9}\text{As}$ superlattice can reflect over 90% of the photons that the wells did not absorb in the first pass. The DBR proved extremely effective, doubling the well current production from $13.3 \frac{\mu A}{cm^2}$ to $26.7 \frac{\mu A}{cm^2}$ without increasing recombination in the i-region.

Another attempt at increasing QW current production was made by deepening the wells from 10% to 14% indium. Increasing the indium composition in the wells increases the local strain between $\text{InGaAs}$ and $\text{GaAsP}$, leading to further step-bunching effects that roughens the interfaces. With the shift from 10% to 14% indium, $J_{02}$ was increased by a factor of two, resulting in a $V_{oc}$ loss of 40mV. The wells, however, did see a boost in current production from $13.3 \frac{\mu A}{cm^2}$ to $38.3 \frac{\mu A}{cm^2}$. The effects of adding more wells to the i-region was also studied as a way to increase current production. In the three well compositions studied, $V_{oc}$ was shown to decrease as wells are added. With step-bunching leading to interface roughness, lateral thickness variations only increase with each additional well, as was reflected in the the $J_{02}$ increase from 3 to 12xSBQW.

Offcut angle was also shown to influence superlattice material quality using 32%P barriers. XRD analysis showed that the superlattice interfaces remained clean on a 0° offcut but the superlattice peaks were absent in the 2° and 6° offcut samples. TEM images confirmed the XRD results, showing a clear increase in interface roughness moving to higher offcut angles.

Chapter 3 began with optimizing the gas flow sequences during superlattice growth. The most successful flow sequence included thin GaAs interlayers between the well and barrier to prevent $\text{InGaAsP}$ formation and $H_2$ purges between layers to remove excess indium and phosphorus from the surface. Once the gas flow sequences were optimized 10%P barriers were compared to the previously used 32%P barriers. Superlattice peaks in XRD of the 10%P barrier
samples recovered alongside photoluminescence intensity, both signs of improved interfaces.

The 10%P barriers were found to recover $J_{02}$ values to levels consistent with 32%P 3xS-
BQW devices, resulting in open-circuit voltages approaching or above 1.010V. Sub-band EQE
showed sharp QW peaks at 10% EQE, providing consistently high current production per well
of 32-35 $\frac{\mu A}{cm^2}$ in devices with 6x and 12xSBQWs.

Put more consisely, utilizing 10%P barriers helped maintain $V_{oc}$’s above 1V and did not
limit collection of carriers generated in the wells due to the thermal-escape dominated nature
of the superlattice.

### 4.2 Future Directions of Research

Future work can be taken in multiple directions. The first and most pressing would be to
continue adding wells to the i-region while using 10%P barriers. $V_{oc}$ will continue to decrease
as wells are added, but will begin to degrade more quickly once interface roughness leads to
3-dimensional quantum structures. Once the maximum number of wells is determined, a DBR
would be added to double the well current generation.

Well depth was investigated using 32%P barriers, but not in the 10%P barrier superlattices.$V_{oc}$ may be less sensitive to increased well depth after local strain was reduced by moving
to shorter barriers. An alternative would be to grade the wells so the interfaces are at lower
%In than the centers, allowing for deeper wells without increasing local strain between at the
well-barrier interface.

All devices investigated in this work were single-junction GaAs. Growing two-junction
InGaP-GaAs devices with and without quantum wells would reveal how close the optimal
QW superlattice brings the InGaP and GaAs sub-cells to current-matching conditions.
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