Optimization and Characterization of Low-Cost Substrates for III-V Photovoltaics

by

Elisabeth L. McClure

This dissertation is submitted in partial fulfillment of the requirements for the degree of Doctorate of Philosophy in Microsystems Engineering

Microsystems Engineering Program
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ABSTRACT

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The highest achieved photovoltaic power conversion efficiency (approximately 47% under concentration) is available from III-V multijunction solar cells made from subcells of descending bandgap that optimize light collection from the solar spectrum. Unfortunately, both III-V multijunction and single-junction solar cells are expensive, limiting their use to niche concentration or space power applications and precluding their competitiveness in the terrestrial flat-plate market. The majority of the III-V solar cell cost is attributed to the thick, monocrystalline substrates that are used as a platform for epitaxial growth, and to the throughput, precursors, and utilization of those precursors associated with traditional growth reactors. Significant cost reduction to approach $1/W for total photovoltaic system cost is imperative to realize III-V solar cells that are cost-competitive with incumbent silicon solar cells, and can include techniques to develop inexpensive substrates directly; enable multiple reuses of a pristine, expensive substrate without the need for polishing; and enhance the throughput by increasing the semiconductor growth rate during epitaxy. This dissertation explores two main techniques to achieve low-cost substrates for III-V photovoltaics: aluminum-induced crystallization to create polycrystalline germanium thin films, and remote epitaxy through graphene to enable monocrystalline substrate reuse without polishing. This dissertation also demonstrates record III-V growth rates exceeding 0.5 mm/h using a potentially lower-cost III-V growth technique, which would increase throughput in production reactors. The ability to reduce the costs associated with both substrates and epitaxy will be imperative to decreasing the total system cost of III-V PV.
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Chapter 1

Introduction

1.1 Motivation

The earth receives as much energy in a single hour from sunlight as the global population consumes in an entire year [1]. This presents a profound opportunity for solar panels (arrays of semiconductor devices that generate current when exposed to light) to replace or alleviate the usage of fossil fuels for electricity production. According to the U.S. Energy Information Administration, the maximum power consumed worldwide is currently 12.5 TW and projected to increase to 16.9 TW by 2030 [2]. Several projections have indicated that with a continuation of current policies and line-of-sight technology, 3 TW of photovoltaic (PV) energy generation is possible by 2030 [3] [4]. These projections also suggest that an increase in PV deployment up to 10-11.5 TW is possible for a continued reduction of module cost while simultaneously improving the solar cell efficiency compared to standard silicon (Si) modules with 25% efficiency.

One pathway to improve efficiency is the use of III-V materials, which are compounds from elements in groups III and V on the periodic table that have high absorption coefficients, direct bandgap, and long
minority carrier lifetimes. An additional benefit of III-V solar cells is the ability to grow junctions in tandem that have similar lattice constants but different energy bandgaps, which allows each junction to be tailored to absorb a specific region of the solar spectrum. These solar cells are called multijunction solar cells. Fig. 1.1 shows a comparison of the maximum power conversion efficiency reached by different PV technologies from 1976 to 2018 [5]. The purple data points indicate record efficiencies by III-V single- and multijunction solar cells, while the blue data points are record efficiencies by Si solar cells, which dominate current terrestrial solar markets. From this plot, the highest efficiency is achieved by a III-V multijunction solar cell composed of six junctions, which reaches an efficiency of 47.1% under concentrated light of 143 suns. At conditions that simulate 1-sun air-mass 1.5 global (AM1.5G) conditions corresponding to a zenith angle of the sun of 48.19° and representing the average terrestrial solar radiation resources across the contiguous United States [6], the efficiency for that same solar cell reaches 39.2%. The record efficiency for one single-junction gallium arsenide (GaAs) solar cell is 29.1% at AM1.5G. And in comparison, the best laboratory efficiency for a Si solar cell is 26.7% at AM1.5G.

While III-V solar cells are very efficient, they often entail expensive growth techniques and depend upon thick, monocrystalline semiconductor substrates such as GaAs, indium phosphide (InP), or germanium (Ge) as platforms for the epitaxial growth process. Typical III-V substrates are an estimated $100 per 6-inch diameter GaAs wafer and $130 per 6-inch diameter Ge wafer [7], while in comparison, a 6-inch diameter Si wafer costs roughly $0.42 for an unpolished solar grade wafer [8]. The low cost of Si wafers compared to GaAs and Ge wafers is both because Si is the second most abundant element in the earth’s crust apart from oxygen [9], and due to the success of the microelectronic industry at manufacturing Si for applications ranging from thin-film transistors to photonics. The cost associated with GaAs and Ge substrates limit the utility of III-V PV to concentration applications that couple small solar cells with optics that concentrate the incident sunlight, or space power applications where the importance of
Figure 1.1: Best research-cell efficiencies over time for solar cells categorized by material system [5]. This plot is courtesy of the National Renewable Energy Laboratory, Golden, CO.

Low mass favors thin, high-efficiency III-V PV.

In order to make III-V PV competitive in the terrestrial flat-plate market, techniques to reuse the substrate for multiple solar cell growths have been proposed. This is advantageous both for the ability to reduce substrate costs as well as to remove solar cells from the substrate in order to reduce the weight and thickness of the device. Furthermore, light trapping techniques that deposit dielectric layers in between the last semiconductor layer and the back gold allow thinned solar cells to reach higher efficiency through photon recycling. However, the cost attributed to the substrate still dominates the overall device cost even after transferring the device to another platform, polishing the original substrate, and reusing it for growth 20 times [10], shown in Fig. 1.2. The analysis behind this figure takes into account the cost associated with making a standard single-junction III-V solar cell for a terrestrial flat-plate module, including the cost of a monocrystalline, epi-ready GaAs substrate, growth of a single-junction GaAs solar cell with an aluminum arsenide (AlAs) release layer to separate the solar cell from
the substrate for reuse, lithography and deposition of back and front contact metals, dissolution of the release layer, and deposition of an antireflection coating. When the cost is divided into categories of required margin, depreciation, electricity, labor and maintenance, semiconductor growth by metal-organic chemical vapor deposition (MOCVD), and substrate cost, it becomes apparent that the substrate is still the most expensive aspect of the solar cell, even after 20 reuses of the substrate.

![Figure 1.2: Projected cost of installing a planar III-V solar cell with 25% power conversion efficiency and 20 reuses of the substrate, adapted from Ref. [10].](image)

The technoeconomic analysis also proposed a roadmap for the reduction of III-V single-junction solar cell costs that emphasized the importance of both reducing the cost of the substrate as well as developing less expensive growth techniques that include cheaper precursors and higher deposition rates [10]. The latter can be solved either by finding ways to utilize growth regimes in conventional MOCVD reactors at higher growth rates such as those demonstrated at 120 $\mu$m/hr while maintaining 24.5% efficiency for a single-junction GaAs solar cell [11], or by using hydride vapor phase epitaxy (HVPE) which has shown growth rates above 300 $\mu$m/hr and uses less expensive elemental metal precursors than organometallic compounds [12].

The development of low-cost substrates for III-V solar cells offers a wealth of diverse research perspectives, which typically fall into one of two categories: replacement of the epi-ready substrate with
low-cost virtual substrates, or reuse of the epi-ready substrate multiple times. Figure 1.3 illustrates the two different techniques and highlights in bold the ones investigated in this thesis. Many research avenues exist to create low-cost virtual substrates, including roll-to-roll ion-beam assisted deposition that creates Ge films on flexible polycrystalline metal alloy foils [13] [14]; growth of InP on molybdenum foil substrates by reacting indium films with phosphine (PH$_3$) through a vapor-liquid-solid reaction [15] [16]; III-V top cells on a Si bottom cell/substrate [17] [18]; direct growth of Ge on Si with low threading dislocation density for III-V PV [19] [20]; and crystallization of amorphous semiconductor films using either flash lamp annealing [21] or aluminum-induced crystallization (AIC) to achieve polycrystalline Si or Ge seed layers [22] [23] [24]. This thesis examines the various parameters that can be controlled for the AIC process, and since the final Ge films are polycrystalline, the goal of this research is to maximize grain size, uniformity of the films, and preferential crystal orientation.

<table>
<thead>
<tr>
<th>Low-Cost Substrates</th>
<th>Monocrystalline Substrate Reuse</th>
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<tbody>
<tr>
<td>• Roll-to-roll IBAD foils</td>
<td>• Epitaxial lift off</td>
</tr>
<tr>
<td>• InP VLS growth</td>
<td>• Laser ablation</td>
</tr>
<tr>
<td>• III-V on Si tandems</td>
<td>• Transfer printing</td>
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<tr>
<td>• Ge/Si virtual substrates</td>
<td>• Porous Ge</td>
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<tr>
<td>• Flash-Lamp Annealing</td>
<td>• Spalling</td>
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<tr>
<td>• Metal-induced crystallization</td>
<td>• Remote epitaxy</td>
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Figure 1.3: Schematic of various low-cost substrate technologies that fall into one of two categories: developing a low-cost virtual substrate, or reusing a monocrystalline substrate.

From the substrate reuse perspective on the other side of Fig. 1.3, one of the most common techniques and the one considered in the technoeconomic analysis of Fig. 1.2 is epitaxial lift-off (ELO). This process separates the device layers from a GaAs substrate using hydrofluoric acid to selectively remove an aluminum-containing release layer such as AlAs or AlGaAs, first proposed by Konagai et al.
The device is then typically bonded to a low-cost material such as glass [26] [27], a polymer [28] [29], metal [30], or Si for handling. Other variations on the ELO process can include the use of phosphide-containing release layers etched by HCl instead of aluminum-containing release layers etched by HF [31]; however, the general principle of chemically removing a release layer remains the same. The advantages of ELO include substrate reuse to decrease the substrate cost per cell, the ability to transfer devices to thin and flexible substrates, and the potential to exceed the efficiency of a solar cell with its original rigid substrate since a thin device with a backside reflector can enhance light trapping. While the cost per wafer reduces as the number of substrate reuses increases, this asymptotically reaches a limit. Before growing on a substrate after ELO, chemical-mechanical polishing (CMP) is required to make the substrate epi-ready again. Therefore, the price of the solar cell with theoretical hundreds of reuses asymptotically approaches the cost of CMP, which is a flat rate of $8/wafer or $3.4/Watt [10]. This cost for the solar cell is still above grid parity and too expensive to be competitive on a terrestrial market.

Alternative techniques to reuse a monocrystalline substrate in order to reduce the solar cell cost typically center around the concept of using a sacrificial layer to promote separation of device layers from the original substrate. Laser liftoff is one approach which uses a buried release layer to selectively absorb light and separate the device layers from the substrate through ablation, as demonstrated for both GaAs [32] and InP [33]. While this technique can achieve relatively fast separation of films, the area of the device to be lifted off is limited by the size of the laser. Another method uses transfer printing and regrowth to achieve solar cells on virtual substrates by growing stacks of release layers [34]. This has demonstrated excellent results when transferred to non-native GaAs wafers as proof of concept, albeit currently limited to devices with dimensions below 730 µm due to the side lengths of the membrane. Another promising substrate reuse technique creates pores in a Ge substrate through chemical treatment, followed by an anneal to create a smooth surface for epitaxy while leaving an embedded porous layer.
as a fracture plane for liftoff from the substrate [35]. Alternatively, nickel can be deposited as a stressor layer on top of a GaAs solar cell for a technique called spalling, where the thickness of the nickel determines the depth of the fracture plane and can be used to separate a device from a substrate while maintaining nearly identical cell performance to the baseline [36]. The technique this thesis focuses on, however, is remote epitaxy through graphene. Remote epitaxy can achieve high device performance using a 2D release layer that leaves behind a pristine III-V interface when a metal stressor is used to exfoliate the monolayer of epitaxial graphene [37]. This work will explore nucleation conditions on graphene using the remote epitaxy process.

This thesis describes the process optimization and results from two methods to potentially reduce the cost associated with substrates for III-V solar cells, where the specific objectives and approach are listed below. In particular, chapters are devoted to Ge crystallization on SiO$_2$-coated Si, nucleation studies on polycrystalline and monocrystalline Ge substrates, and growth of GaAs solar cells on graphene that use the weak van der Waals bonds of graphene as a release layer to reuse a GaAs substrate without the need for chemical mechanical polishing.

1.2 Objectives

The research objectives will be split into two parts. The first involves the development of the process and techniques to create III-V solar cells on a polycrystalline Ge solar cell. This work will be performed at the Rochester Institute of Technology (RIT) and those research objectives include:

1. Process development for aluminum-induced crystallization of Ge at RIT
2. Optimization of process conditions for aluminum-induced crystallization of Ge
3. Synthesis and characterization of polycrystalline Ge films
4. Analysis of nucleation conditions for growth on polycrystalline and monocrystalline Ge films
5. Demonstration of a solar cell on polycrystalline Ge by aluminum-induced crystallization
The second set of objectives involves ways to decrease the cost of monocrystalline GaAs and Ge substrates, and were performed at the National Renewable Energy Laboratory (NREL). These research objectives include:

1. Exploration of growth conditions necessary to nucleate GaAs epilayers on a graphene-coated GaAs substrate

2. Growth of GaAs solar cells on a graphene template for epitaxial liftoff

### 1.3 Approach

The goals of this thesis are achievable by pursuing research at both RIT and NREL. For the RIT component, a recrystallization process will first need to be established. A variety of parameters — including deposition technique, anneal temperature, anneal time, carrier gas, pressure, temperature ramp rate, and substrate thickness — will be studied to yield the desired crystal orientation and grain size. The Ge layers resulting from the process optimization will then be characterized by techniques such as optical microscopy, scanning electron microscopy, x-ray diffraction, *in-situ* reflectance, *in-situ* curvature, and electron backscattered diffraction. Test structures will then be grown on the best polycrystalline Ge substrates to evaluate the effect of nucleation conditions compared to commercial monocrystalline and polycrystalline Ge substrates. Finally, solar cells with optimal growth conditions will be grown, fabricated, and characterized on these substrates.

The work at NREL represents a parallel approach to low-cost III-V PV. Techniques such as epitaxial liftoff are used commercially to allow high-quality growth on epi-ready substrates, after which the solar cell or other device is removed, and the substrate is polished and prepared for the next growth. 2D materials allow remote epitaxial registry between the substrate and layers grown during epitaxy (epi-layers) through a gap up to 9 angstroms, and can then act as a release layer with minimal impact to the interface. Developing both the nucleation and growth conditions at NREL to achieve high-efficiency
solar cells on 2D materials would allow for substrate reuse while avoiding polishing costs associated with conventional techniques.

1.4 Organization of Thesis

Chapter 1 provides the motivation, objectives, and approach to develop low-cost substrates for III-V photovoltaics. Of particular interest is the development of poly-Ge substrates through aluminum-induced crystallization, and the reuse of GaAs substrates through remote epitaxy.

Chapter 2 gives an introduction to the theory of solar cells, analysis of theoretical polycrystalline solar cell performance, challenges to growth on Ge substrates, and summary of the remote epitaxy process. The background provided here will guide the discussion in the subsequent chapters.

Chapter 3 discusses the development of the aluminum-induced crystallization process used to create poly-Ge substrates. Optimization of several parameters are discussed, with particular focus to how temperature ramp rate and substrate thickness affect the crystallization process.

Chapter 4 examines three distinct experiments to optimize growth on polycrystalline substrates using the MOCVD at RIT. The fist experiment evaluates solar cell growth on commercial polycrystalline and monocrystalline GaAs and Ge substrates to better understand the effect of antiphase domains and grain boundaries. The second experiment evaluates the performance of low-temperature GaAs nucleation layers and high-temperature indium gallium phosphide (InGaP) nucleation layers for various temperatures. The third study investigates the solar cell performance from samples produced via aluminum-induced crystallization.

Chapter 5 explores a parallel approach to low-cost III-V PV substrates beyond the synthesis of polycrystalline substrates. Nucleation conditions for remote epitaxy are investigated with the goal of enabling high-efficiency solar cells with the capability of multiple reuses. This chapter summarizes computational fluid dynamics modeling of how reactant gases and GaAs growth rate are expected to
change with carrier gas, as well as annealing results and preliminary GaAs growth on graphene.

Chapter 6 gives a conclusion to the dissertation as well as a summary of awards and products by the
time the degree was completed.
Chapter 2

Background

2.1 Solar Cell Operation and Device Physics

A solar cell is a p-n junction diode where electron-hole pairs are generated by excitation from photons with energy greater than the bandgap of the semiconductor material. In 1960, a landmark paper by Shockley and Queisser used detailed balance - a technique that balances carrier generation, extraction, and radiative recombination - to predict the upper limit of single junction solar cell efficiency. Figure 2.1 shows the maximum limit of power-conversion efficiency $\eta$ plotted as a function of bandgap $(qV_g)$ on the top x-axis and $x_g=V_g/kT$ on the bottom axis, where $q$ is the magnitude of charge for an electron, $k$ is the Boltzmann constant, and $T$ is the temperature of the solar cell [38].

The detailed balance limit assumes that the incident light is unconcentrated, all recombination is radiative, and all photons with energy greater than the bandgap energy create one electron-hole pair each. Under these assumptions, the maximum theoretical efficiency of 30% corresponds to a semiconductor with a bandgap around 1.1 eV. The shape of the curve accounts for the fact that semiconductors with a bandgap larger than 1.1 eV suffer transmission losses, since a significant number of photons have
Figure 2.1: Power conversion efficiency plotted as a function of band gap for a single-junction solar cell. The maximum efficiency $\eta$ from a single junction solar cell occurs at a band gap around 1.1 eV. This figure was adapted from Ref. [38] with the permission of AIP Publishing.

insufficient energy to excite an electron-hole pair across the bandgap. Meanwhile, semiconductors with a bandgap less than 1.1 eV encounter thermalization losses due to phonon emission when minority carriers quickly decay to the band edge. A single-junction solar cell can be modeled by the ideal diode equations for a p-n junction diode, where the device current under illumination is given by

$$I = I_0\left(e^{\frac{qV}{kT}} - 1\right) - I_L \tag{2.1}$$

where $q$ is the elementary charge, $V$ is the applied voltage, $k$ is the Boltzmann constant, $T$ is the temperature of the cell, $I_0$ is the reverse saturation or dark current, and $I_L$ is the current due to light [39]. The negative sign for $I_L$ indicates the generation of current by the device. The $I_0$ and $I_L$ terms can then be described fundamentally. Since solar cells operate under forward bias, the dark current is dominated by minority carrier diffusion, and written as

$$I_0 = \frac{qD_p n_i^2}{L_p N_D} + \frac{qD_n n_i^2}{L_n N_A} \tag{2.2}$$
where $D_p$ and $D_n$ are diffusion coefficients of minority holes and electrons respectively, $L_p$ and $L_n$ are minority carrier diffusion lengths, $n_i$ is the intrinsic carrier concentration of the semiconductor, and $N_D$ and $N_A$ are donor and acceptor concentrations $^{[39]}$. The light current from Eq. 2.1 is defined as the number of photons per second per unit area (photon flux) incident on the solar cell surface that are collected,

$$I_L = Aq \int_{E_g}^{\infty} \frac{d\phi_{ph}}{dE} dE \quad (2.3)$$

where $A$ is the cell area, $q$ is the elementary charge, $d\phi_{ph}$ is the derivative of the photon flux density, and the integral accounts for the light above the bandgap absorbed by the solar cell $^{[39]}$.

By solving Eq. 2.1 over a range of voltages, theoretical current-voltage (I-V) curves can be generated. From these, the maximum power and power conversion efficiency can be determined by

$$\eta = \frac{P_{max}}{P_{in}} = \frac{I_{max}V_{max}}{P_{in}} = \frac{I_{SC}V_{OC}FF}{P_{in}} \quad (2.4)$$

where $I_{max}$ and $V_{max}$ correspond to the current and voltage at the point of maximum power, $I_{SC}$ is the short-circuit current when no voltage is applied, $V_{OC}$ is the open circuit voltage when there is no current, and FF is the fill factor or sharpness of the I-V curve.

### 2.1.1 Effect of Antiphase Domain Formation

In addition to the detailed balance limits defined above, some further loss mechanisms need to be considered that can pose potential challenges when nucleating a polar compound such as GaAs on a nonpolar compound such as Ge. In this case, Ge is a good candidate for substrate material for III-V solar cell applications due both to its similar lattice constant to GaAs and its narrow bandgap that makes Ge suitable for a bottom junction in a multijunction solar cell. One potential loss mechanism of growing
a polar compound on a nonpolar substrate is the formation of antiphase domains (APDs), which are regions of antisite defects at the interface between a polar compound and a nonpolar substrate, shown in Fig. 2.2. Adapted from Ref. [40], Fig. 2.2a shows a schematic cross section of a GaAs epilayer nucleated on a Ge substrate, where Ge atoms are represented in green, Ga in purple, and As in blue. These APDs occur since As preferentially bonds to the Ge surface, and any steps that form which are an odd number of atomic layers in height will then create rows of Ga or As that are out of phase with the layer at the previous step height. APDs have a characteristically triangular shape and continue until the out-of-phase regions eventually self-annihilate. Figure 2.2b shows a dark-field transmission electron microscope (TEM) image of a cross-section of a GaAs solar cell grown on a Ge substrate. The image depicts APDs that appear at the interface between the Ge substrate and the GaAs buffer layer.

Figure 2.2: a. Schematic of APDs that form due to a difference in step height of the substrate by an odd number of monolayers. b. Dark-field TEM image of APDs at the interface between GaAs epilayers and a Ge substrate, taken at NREL.

APDs can lead to ordering faults in the subsequent polar growth. Since APDs act as extended one-dimensional scattering centers that propagate out-of-plane, they can be treated similarly to threading dislocations, degrading lifetime in a material as a function of the aerial density using the following equation

\[ \tau_{TDD} = \frac{4}{\pi^3 D_{\rho_{APD}}} \]  

(2.5)
where \( D \) is the diffusion length and \( \rho_{APD} \) is the APD density [41]. However, there are several methods to suppress or eliminate the formation of APDs. One technique is to anneal the Ge substrate prior to growth in order to convert the tetrahedral bonds at the surface to trigonal planar bonds, which creates a double atomic step that eliminates APDs [42]. Another technique is to nucleate on substrates with crystal orientations on which it is energetically unfavorable for APDs to form, such as a (211) surface [42]. If APD formation cannot be eliminated, the effects can be suppressed by the growth of thick buffer layers to allow APDs to self-annihilate before reaching the active layers of the device.

2.1.2 Effect of Grain Boundaries on Solar Cell Performance

Grain boundary recombination can also cause losses in solar cell efficiency. Grain boundaries occur when multiple nucleation points develop, grow, and eventually converge. The boundary between crystals can cause two detrimental effects: high interfacial recombination velocity and a high sheet conductance along the grain boundary interface [43]. Several techniques exist to suppress the effect of grain boundary recombination in GaAs solar cells, including selectively anodizing the grains [44] or passivating the grain boundaries with selenium [45] [46].

In order to fit the minority carrier diffusion length (MCDL) and to predict grain boundary-induced degradation in GaAs solar cells, a minority carrier drift-diffusion model was developed based on the work by Hovel and Woodall [47]. The polycrystalline MCDLs are predicted by combining the bulk MCDL with the grain boundary influenced MCDL calculated using Eq. 2.6 below,

\[
L_g = \sqrt{\frac{D d_g}{4S_g}}
\]

(2.6)

where \( D \) is the minority carrier diffusion constant, \( S_g \) is the interface recombination velocity (assumed to be 5x10^6 \( \text{cm}^2/\text{s} \)), and \( d_g \) is the grain size [48].

MCDLs were also used to calculate reverse saturation currents of an ideal n=1 diode (\( I_{01} \)) in order
to generate current density-voltage (J-V) curves. The $V_{OC}$ of a GaAs control cell was used to fit a nonradiative $n=2$ term and to determine the space charge region reverse saturation current component ($I_{02}$). The system of equations can be written as:

\[
J_s = \begin{cases} 
\frac{qn_iS_gW_g}{d_g/4}, & d_g >> W_g \\
\frac{qn_iS_gW_g(d_g - W_g)}{d_g^2/4}, & d_g > 2W_g \\
qn_iS_g, & d_g < 2W_g 
\end{cases}
\]  

(2.7)

where $n_i$ is the intrinsic carrier concentration of GaAs and $W_g$ is the depletion width between grains and is a function of the barrier height from grain boundary traps and background doping [48]. Thus, $W_g$ can be calculated as

\[
W_g = \frac{2\epsilon V_d}{qN} 
\]  

(2.8)

where $N$ is the region doping and $V_d$ is the barrier between grains which is assumed to be 0.2 V [48]. Reverse saturation current due to recombination in the space-charge region, which is also impacted from APDs can be modeled as

\[
J_{0,SCR} = q \frac{n_iw_{emitter+base}}{(\tau_p\tau_n)^{1/2}} 
\]  

(2.9)

where $\tau$ are the final minority carrier lifetimes, including all recombination mechanisms, and $w$ is the depletion width calculated from the built-in potential and growth structure in the case of inclusion of a uid region. Finally, the total diode current in the solar cell is given by
\[ J = -J_{SC} + J_{0,Diff}(e^{\frac{V-JRs}{k_BT}} - 1) + (J_{0,SCR} + J_S)(e^{\frac{V-JRs}{2k_BT}} - 1) + \frac{V + JR_S}{R_{SH}} \] (2.10)

These equations can then predict spectral responsivity (SR) and J-V characteristics for monocrystalline and polycrystalline GaAs solar cells grown on GaAs and Ge substrates, accounting for intragrain material quality as well as the effects of grain size, grain boundary recombination velocities, and nucleation induced defects [49]. Figure 2.3 shows the range of efficiencies predicted as a function of grain size on the x-axis ranging from 100 nm to 100 mm, and grain boundary recombination velocity on the y-axis from 100 cm/s to $10^8$ cm/s, where $10^6$-$10^7$ cm/s is an average recombination velocity for unpassivated grain boundaries in GaAs [48].

![Figure 2.3: One-sun AM1.5G contour plot showing expected device efficiency across a range of grain sizes from 100 nm to 100 mm and grain boundary recombination velocities from 100-$10^8$ cm/s. The two horizontal bands in the plot are the expected range of unpassivated grain boundary recombination velocities for GaAs.](image)

These calculations predict the achievable efficiency of an In$_{0.01}$Ga$_{0.99}$As solar cell on recrystallized...
Ge. The results from the contour plot indicate that for polycrystalline grain size between 100 µm to 1 mm, a 20% solar cell could be achieved without surface passivation, and with surface passivation, the solar cell could approximate a monocrystalline GaAs solar cell.

### 2.1.3 Demonstration of Polycrystalline Solar Cells

While polycrystallinity and APD formation can influence the device performance of a solar cell, both effects can be suppressed. This provides an opportunity to create large-grain polycrystalline solar cells that have high device efficiency approaching those grown on monocrystalline substrates, as shown previously in Fig. 2.3. Successful growth on polycrystalline substrates requires simultaneous optimization of several parameters, including enhancement of polycrystalline grain size to minimize grain boundary recombination, passivating the grain boundaries to minimize grain boundary recombination velocity, and minimizing the formation and effects of antiphase domains. Techniques to accomplish these various aspects have been demonstrated for III-V solar cells in the work below.

GaAs solar cells grown on polycrystalline Ge have been demonstrated with 19.7% efficiency under AM1.5G illumination for a 4 cm$^2$ cell and 21.2% for a 0.25 cm$^2$ cell [50]. The higher solar cell efficiency for a smaller device size indicates that the smaller device was able to encompass fewer grain boundaries. One of the enabling factors for these high efficiencies was the grain size of the substrates, which were commercial cast optical-grade polycrystalline Ge with grain size between 0.04-1 cm [51]. The other key component was the ability to use Se to passivate the grain boundaries [45]. After achieving high efficiency on sub-mm poly-Ge substrates, the next step was to use the acquired knowledge to transition to high-efficiency GaAs solar cells on glass or molybdenum platforms using Ge as a seed layer [52].

Moving towards that goal, state-of-the-art low-cost templates have been able to reach increasingly high efficiency over the years. InP solar cells made by the vapor-liquid-solid phosphorization of liquid indium have demonstrated 12.3% efficiency on a molybdenum-sputtered glass substrate [53]. A GaAs
solar cell on Hastelloy metal foils with 11.5% efficiency was obtained using a roll-to-roll sputter process with ion-beam assisted deposition to create a buffer layer stack and Ge seed layer, chemical vapor deposition to create the Ge nucleation layer, and MOCVD to grow the solar cell [54]. And as an alternative approach, GaAs efficiencies of 9.2% have been observed on solar cells grown on poly-Ge crystallized by rapid thermal annealing on a molybdenum disc [55].

While these techniques all demonstrate the capability of solar cells grown on low-cost substrates to reach promising device efficiencies, work to create polycrystalline Si layers can also yield insight to the development of low-cost Ge substrates. The following section describes aluminum-induced crystallization (AIC), a technique that has been shown to create large Si or Ge grain size with the ability to create preferential crystal orientations based on the anneal conditions. Record Si solar cell efficiency from AIC have reached 8% efficiency on p-type substrates and 2.9% on n-type substrates [56] [57]. For AIC of Ge substrates, grain size exceeding 100 µm has been achieved with an internal quantum efficiency (IQE) of 70% under 1 V bias [58]. These results are promising and the process is described in further detail below.

2.2 Aluminum-Induced Crystallization

In order for a process to be thermodynamically permissible, its Gibbs free energy must be less than zero. Most processes will tend towards the minimum Gibbs free energy, but if an energy barrier exists, additional energy is needed to overcome the barrier and truly minimize the total Gibbs free energy. Figure 2.4 shows the Gibbs free energy diagram as a function of atomic bond length, which achieves a local minimum for an amorphous material, and an absolute minimum for polycrystalline material. Due to attractive forces between atoms, it is energetically unfavorable for two individual atoms to be isolated at a distance infinitely far away from one another. As the atoms move closer, they reach a local minimum of Gibbs free energy where some atoms reach the ideal bond length, but others are
either closer or further away. This structure is called amorphous, where little order exists in the atomic arrangement. In order to arrange all of the atoms in a crystal such that each atom has the energetically ideal bond length, energy must be added into the system to surmount the energy barrier. Under this condition, the atomic arrangement will move from an amorphous state to a crystalline one, which is the absolute minimum energy of the system. If the atoms are pushed increasingly close together, the Gibbs free energy increases until it approaches an infinite energy state in a hypothetical case of two atoms that are so close that they begin to occupy the same space. This drive to minimize Gibbs free energy and achieve a crystalline bond length is a driving force to create polycrystalline substrates from amorphous layer deposition.

![Gibbs free energy diagram for the crystallization of amorphous germanium](image)

Figure 2.4: Gibbs free energy diagram for the crystallization of amorphous germanium, modified from Ref. [59] under the terms of the Creative Commons CC BY license.

One technique to achieve low-cost and large-grain polycrystalline silicon or germanium substrates for solar cells is called metal-induced crystallization (MIC). In this process, a layer of either eutectic or compound-forming metal is deposited adjacent to an amorphous semiconductor layer in order to induce nucleation points at temperatures below that of the standard semiconductor crystallization temperature. The amorphous semiconductor bonds are weakened at the metal interface if the metal is above a critical thickness to provide sufficient mobile free electrons that disrupt the covalent bonds [60]. This leads
to rapid metal-semiconductor intermixing at the interface, which causes crystallization to initiate at sub-eutectic temperature due to the weakened bonds [61].

For III-V applications, Ge is often a suitable substrate candidate because it is nearly lattice-matched to GaAs and is therefore relatively easy to grow lattice-matched epilayers. While MIC of Si can only occur during the layer transfer process, studies indicate that Ge is able to crystallize both at the polycrystalline metal grain boundaries and at the metal/semiconductor interface [62]. Hence, MIC of Ge can occur in one of thee ways, shown in Figure 2.5: (i) a metal layer is deposited below an amorphous semiconductor layer, followed by a low-temperature anneal that allows the metal to diffuse to the surface while the amorphous semiconductor crystallizes around the metal [63] [23]; (ii) the metal layer is deposited above the amorphous semiconductor layer, and an anneal allows the layer exchange to occur [64] [65]; or (iii) a thin metal capping layer is deposited above the thick amorphous semiconductor layer, and an anneal allows the amorphous semiconductor to crystallize starting from the metal/semiconductor interface, after which point the metal capping layer can be removed [66].

Studies have investigated the crystallization properties of 20 transition metals in contact with either amorphous Si or amorphous Ge, and in both cases aluminum and gold are the two metals that lower the crystallization temperature the most [67] [68]. Since aluminum is cheaper than gold, aluminum is often the preferred metal for the crystallization of amorphous semiconductors, yielding the subsidiary of MIC called aluminum-induced crystallization (AIC). In AIC, the presence of aluminum (Al) decreases the temperature needed to crystallize amorphous Ge well below both the Ge crystallization temperature without Al around 500 °C and the Al-Ge eutectic temperature of 423 °C [69], with temperatures as low as 180 °C reported in literature [70]. The rate of diffusion of Al through Ge depends on the temperature of the process, while the diffusion length is determined by both temperature and time. Table 2.1 shows the diffusion coefficients at each interface of the Al, Ge, Si, and SiO$_2$ stack at a temperature of 300 °C. The reported diffusion length is equal to the square root of the diffusion coefficient multiplied
by the anneal time. It should be noted that diffusion data for silicon dioxide into silicon at such low temperature is difficult to find. Instead, the data in Table 2.1 is reported from work that derived the diffusion coefficient from an Arrhenius fit of data within a temperature range of 1150-1300 °C. An upper limit of the diffusion at 1200 °C would yield a diffusion coefficient of 9.8e-19 cm²/s, which corresponds to diffusion lengths of 1.8 to 2.6 nm for 10 or 20 hour anneals, respectively [71]. At 300 °C, the extrapolated diffusion lengths are so small that it can be assumed that SiO₂ doesn’t diffuse into Si.

A schematic of the AIC process used in this work is shown in Fig. 2.6. Many options exist for the choice of substrate material, including glass [75], ceramics [66], polymers [76], or silicon [63]. A layer of Al is then deposited on the substrate by either electron-beam [77], sputtering [69], or thermal evaporation [78]. In most cases, the sample is removed from vacuum to allow the Al surface to oxidize,
Table 2.1: Diffusion coefficients at the relevant interfaces for Al and Ge bilayers on an SiO$_2$-coated Si substrate at an anneal temperature of 300 °C.

<table>
<thead>
<tr>
<th>Materials</th>
<th>Diffusion Coefficient at 300 °C (cm$^2$/s)</th>
<th>Diffusion length for 10 hours (nm)</th>
<th>Diffusion length for 20 hours (nm)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al into Ge</td>
<td>4.7e-13</td>
<td>1301</td>
<td>1840</td>
<td>[72]</td>
</tr>
<tr>
<td>Al into SiO$_2$</td>
<td>1.65e-16</td>
<td>24</td>
<td>35</td>
<td>[71], [73]</td>
</tr>
<tr>
<td>Si into SiO$_2$</td>
<td>1.5e-46</td>
<td>2e-14</td>
<td>3.3e-14</td>
<td>[74]</td>
</tr>
</tbody>
</table>

where AlO$_x$ acts as a permeable barrier that slows the interdiffusion of Al and Ge during annealing and leads to both larger grains and preferential crystal orientation [68]. Ge is then deposited on top of the Al layer, and the sample is annealed near or below the Al-Ge eutectic point [79] [80]. As was studied in AIC of Si, Al catalyzes the crystallization process by diffusing through and weakening the bonds in the amorphous semiconductor layer during the anneal, driven by the concentration gradient and higher chemical potential of maintaining amorphous bonds compared to the crystalline ideal bond length [81]. The resulting energy released from this process enables the nucleation and growth of c-Ge grains at the semiconductor/metal interface and around the diffused Al [82]. The result of this process is complete layer exchange between the initial Ge and Al layers, at which point the Al layer on top of the remaining poly-Ge film is selectively etched hydrochloric acid (HCl).

![Figure 2.6](image.png)

**Figure 2.6:** Schematic of the AIC process used at RIT, where Al and Ge were successively deposited on hundreds of nanometers of thermally-grown oxide on a Si substrate. When annealed, Al diffuses through the Ge leaving a polycrystalline Ge film underneath a layer of Al, where Al can be selectively etched in a 5-hour concentrated HCl bath [24].

State-of-the-art AIC techniques are able to achieve grain size larger than 1 mm when recrystallizing Ge with an Al capping layer, but reported detrimental cracking, peeling, or dewetting for all substrates...
investigated except alumina [66]. By depositing the Al layer underneath the Ge layer, stress can be released during annealing as aluminum diffuses to the surface and layer transfer occurs [65]. Another important consideration for stress is the Al thickness during initial deposition, where tensile stress is observed for thin Al layers and becomes more compressive with increasing Al thickness for AIC of a-Si films [83]. Ge substrates with large grain size, preferential crystal orientation, uniform coverage across wafer-scale areas, and low stress are critical to successfully creating low-cost substrates for III-V growth. The work presented in Chapter 3 explores a variety of parameters to try to enhance this process.

2.3 Remote Epitaxy

Incumbent substrate reuse techniques such as epitaxial liftoff have been employed to allow high-quality growth on epi-ready substrates, after which a solar cell or other device can be removed and the substrate can be polished and prepared for the next growth. However, cost estimates from Woodhouse et al. show that wafer polishing attributes to roughly $8/polish or $3.4/W, which alone is above the SunShot price goal for PV systems that targets $1/W [10]. Since conventional epitaxy involves covalent bonding between the substrate and epilayers, those bonds are often difficult to break when trying to reuse the crystalline substrate for subsequent growths. Growth on 2D materials, however, involves weaker van der Waals bonding between the 2D material and the epilayers, which would then enable smooth separation between the epilayers and the substrate without the need for repolishing. A critical component of this technique is the demonstration that the substrate below the 2D material can still interact with the epilayers through a <9 angstroms thickness, thus allowing the epilayers to have the same crystal orientation as the substrate [84]. This process is called remote epitaxy, as it involves remote epitaxial registry with a substrate through a 2D material.

Figure 2.7 shows a schematic of the remote epitaxy process. An epi-ready GaAs substrate initially undergoes an etch to remove the oxide, followed by either graphene transfer from a SiC substrate or
direct chemical vapor deposition (CVD) growth on either the substrate or a nucleation layer on the substrate. An inverted solar cell can then be grown on top of the graphene-coated GaAs substrate, after which a nickel exfoliation process separates the substrate from the epilayers at the graphene interface.

![Figure 2.7: Schematic of the remote epitaxy process, demonstrating either graphene growth or transfer onto a cleaned GaAs substrate, inverted solar cell growth, nickel exfoliation, and the resulting solar cell and GaAs substrate.](image)

Using this technique, Kim et al. grew GaAs LEDs on both a graphene-coated GaAs substrate and a standard epi-ready GaAs substrate as a baseline [84]. Both the current-voltage characteristics and electroluminescence appeared nearly identical between the two devices, indicating the success of their process. Furthermore, GaAs growth on GaAs substrates via remote epitaxy through graphene shows identical zinc-blende (001) orientations between the substrate and epilayer compared to the baseline without graphene, and no defects could be identified at the interface [37]. The work presented in Chapter 5 explores the anneal and growth conditions to nucleate GaAs on graphene for solar cell applications in a dynamic-hydride vapor phase epitaxy reactor.
Chapter 3

Aluminum-Induced Crystallization

3.1 Introduction

AIC is a low-temperature process where the presence of aluminum (Al) decreases the temperature required to crystallize amorphous germanium (a-Ge) well below both its standard crystallization temperature of 500 °C and the Al-Ge eutectic temperature of 423 °C [69]. The typical parameters explored in literature to optimize this process include total anneal time [85] [63] [64], time that vacuum was broken between the Al and Ge depositions to form a native AlOₓ layer [63], anneal temperature [86] [87] [68] [70], and layer order for Al and Ge [65]. However, many other parameters affect this process, including the effect of different deposition techniques, ambient gas and pressure during the anneal, absolute and relative Al and Ge thicknesses, temperature ramps to and from the anneal temperature, and substrate thickness. The following sections discuss how those parameters were chosen in order to optimize both grain size and surface coverage of Ge on Si/SiO₂ substrates, with a table of all experiments summarized in Appendix A.
3.2 Initial Experimental Setup

3.2.1 Aluminum Oxidation

One technique to obtain large-grain poly-Ge samples by AIC is to break vacuum between the deposition of the Al and Ge layers [58]. This creates a thin, native oxide meant to slow Al diffusion during the AIC process, which leads to a compact layer of large-grain Ge underneath Ge islands that have smaller grain size which can then be etched away with H\textsubscript{2}O\textsubscript{2} by using the AlO\textsubscript{x} layer as an etch stop [22] [23]. Prior work by Toko et al. explored the effect of breaking vacuum between the deposition of the Al layer and Ge layer for 1 minute, 5 minutes, and 30 minutes, where they found that oxidizing the Al layer in air for a longer time enabled large polycrystalline grain growth on the order of 100 \( \mu \)m after annealing for 30-400 hours at temperatures between 325-350 °C [63].

To reproduce this work as a baseline, Si(111) substrates with a thickness of 280 \( \mu \)m were cleaned with a standard RCA procedure of dipping the Si wafers in a volumetric ratio of 1:1:5 ammonium hydroxide : hydrogen peroxide : deionized water for 10 minutes, a 5x rinse in deionized water, a 1-minute dip in 49% hydrofluoric acid, a 5x rinse in deionized water, a 10-minute rinse in 1:1:6 hydrochloric acid : hydrogen peroxide : deionized water, and a final 5x rinse in deionized water. These wafers were then placed in a Bruce diffusion furnace at 1000 °C to grow 1 \( \mu \)m of SiO\textsubscript{2} to act as a diffusion barrier between the Si substrate and the layer of Al to be deposited in the next step. A CVC 601 DC sputter system was used to deposit a 50 nm Al layer and a 50 nm Ge layer on the oxide-coated Si substrates. The layer thicknesses were verified by inserting a glass slide with Kapton tape before each deposition, where the tape was removed after the completed deposition for profilometry measurements. To explore the effect that oxidizing the Al layer had on Ge diffusion and crystallization, one sample was removed from vacuum and exposed to air for 30 minutes before reloading into the chamber, and the other sample
experienced immediate Ge deposition after the Al deposition without breaking vacuum. The two samples were annealed together in a Lindbergh Blue M tube furnace for 10 hours at a pressure of 30 Torr and a temperature set point of 260 °C, where Appendix B shows the relationship between the furnace set point and the true temperature. The temperature set point was chosen from literature that showed crystallization at 250 °C for anneal times as low as 3 hours [78], and the suggestion that lower anneal temperature may lead to larger grain size [70] [63]. Figure 3.1 shows x-ray diffraction (XRD) and optical microscope comparisons of the samples with and without breaking vacuum to achieve the native AlOₓ layer.

Figure 3.1: a. XRD and b. optical microscopy of samples when vacuum was broken between Al and Ge deposition for 30 minutes compared to c. optical microscopy of samples when vacuum was maintained and the two layers were deposited one right after the other. The magnification for both samples was 1,000x.

The XRD measurements shown above were performed in a Rigaku D/Max-B with a copper Kα x-ray source using a 2θ range of 25-40°. Beneath the XRD spectra are lines that indicate the peak position associated with Ge, Si, and Al standards from the International Centre for Diffraction Data (ICDD) database as a visual aid for peak identification. After depositing the films and before annealing,
XRD shows the Si(111) peak of the substrate and an Al(111) peak of the polycrystalline Al layer deposited underneath the amorphous Ge layer, shown in blue. The sample annealed without allowing the native aluminum oxide layer to form (red XRD spectrum) shows a strong Ge(111) peak and the optical microscope image shows a roughened surface morphology, indicating that layer transfer was initiated. However, the Ge(111) peak is absent for the sample where a native oxide was allowed to form, shown as the turquoise XRD spectrum. The Al(111) peak is enhanced, suggesting that the crystal shown in Fig. 3.1 is Al. Unfortunately, the Al crystals are infrequent and dendritic, despite being large. The long, dendritic branches of the crystal lead to a higher perimeter of each crystal and hence greater opportunity for grain-boundary recombination, which would be detrimental to solar cell performance. These results suggested that depositing the Al and Ge layers without breaking vacuum was preferable to breaking vacuum, since the former showed a large Ge(111) peak and the latter did not after the 10 hour anneal.

After continued optimization of the parameters described in Sections 3.2-3.4, the effect of Al oxidation was revisited for further analysis. Figure 3.2a shows optical microscopy with a Nomarski prism of a sample with 50 nm Al and 50 nm Ge layers deposited on a Si substrate with 1 μm SiO₂, where vacuum was broken for 5 minutes between the two depositions. The sample was then annealed for 100 hours at 300 °C set point and etched for 1 second in 1.5% HF to remove the Al layer above the Ge. The sample shown in Fig. 3.2b and c had layer thicknesses of 200 nm Al and 200 nm Ge layers deposited on a Si substrate with 500 nm SiO₂, where vacuum was again broken for 5 minutes between the two depositions. This sample was annealed for 100 hours at 325 °C true temperature and etched for 5 hours in concentrated HCl. While this sample appears smooth in large areas, particularly compared to first sample described, it becomes clear when looking at a large area that the sample suffers from delamination down to the SiO₂ layer in other areas, as shown in the lower magnification of the sample in Fig. 3.2c.

In each case, breaking vacuum between the Al and Ge layers seemed to lead to large voids in
Figure 3.2: Optical microscopy of a.) a sample with 50 nm Al and 50 nm Ge layers deposited on a Si substrate with 1 µm SiO$_2$, where vacuum was broken for 5 minutes between the two depositions. The substrate was then annealed for 100 hours at 300 °C set point and etched for 1 minute in 1.5% HF, compared to b.) a sample annealed with 200 nm Al and 200 nm Ge layers deposited on a Si substrate with 500 nm SiO$_2$, where vacuum was again broken for 5 minutes between the two depositions. The substrate was annealed for 100 hours at 325 °C true temperature and etched for 5 hours in concentrarted HCl. This sample looked smooth in large areas, but delaminated from the oxide in other areas, as shown in c.) a lower magnification image of the same sample.

the film, likely because the AlO$_x$ layer is allowed to form by leaving the sample in air, rather than by a controlled deposition technique. This hypothesis is supported by MIC studies that examined RF sputtering and atomic layer deposition of an Al$_2$O$_3$ barrier that yielded large Ge grain size in excess of 600 µm and reasonable uniformity as suggested by both optical micrographs and pictures of the sample [88]. However, breaking vacuum between layers would be nonideal for industry: it creates an extra step in the process, requires time to vent the chamber and then reach the required base pressure again, and would require an additional deposition step to achieve high-purity Al$_2$O$_3$ at the crystallization interface. Oxidation in air between the Al and Ge layers was attempted several more times before eventually deciding that maintaining vacuum between layers seemed to show promising c-Ge films that avoided these pitfalls, after which this became standard practice.

3.2.2 Sputtering vs. Thermal Evaporation

Sputtering and thermal evaporation are both types of physical vapor deposition methods, where physical vapor deposition is characterized by solid or molten sources that enter the gas phase through a physical mechanism, typically in a reduced pressure environment [89]. For sputtering, high energy inert particles
strike a target of the desired material to be deposited, allowing atoms from the target to enter the gas phase and deposit on a substrate. For thermal evaporation, a boat containing pellets or wires of the source material is heated, which then allows the desired material to either evaporate or sublime onto a substrate. AIC literature reports a variety of techniques to deposit Al on the substrate, including sputtering [69], thermal evaporation [78], or electron-beam deposition [77], with no clear preference for one technique over the other. In order for different deposition techniques to be rigorously compared, the tools would need to have the same height between source and sample, the same platen rotation or planetary configuration, and the same deposition rate. However, the comparison between the in-house sputtering and thermal evaporation tools were compared roughly as a decision for which technique to use to deposit the films for the remainder of our process.

Two 280 µm-thick Si samples with 1 µm of SiO$_2$ were prepared with 50 nm Al and 50 nm Ge interrupted by a 30 minute vacuum break between layers, where one sample was prepared in a Kurt J. Lesker PVD 75C thermal evaporator and the other was prepared in the CVD601 sputter system. These samples were then annealed together for 20 hours at a temperature set point of 260 °C and a pressure of 30 Torr in a Lindbergh Blue M tube furnace. Figure 3.3 shows optical micrographs and powder XRD in the Rigaku D/Max-B of the two samples. Neither method showed the expected Ge(111) peak indicating Ge crystallization, possibly because of the challenges with breaking vacuum between layers as described in the previous section. The scanning electron microscope (SEM) images shown in Fig. 3.3b and c compare how Al (light) diffused through the Ge layer (dark). For the sputtered sample, the Al showed random patterns of crystallization on the surface, often elongated or with large perimeter which could be detrimental to solar cell performance due to a greater chance of grain-boundary recombination. The sample that was thermally evaporated showed more spherical grains, so thermal evaporation was chosen as the deposition method of choice moving forward.

The disparity between the XRD peaks of the two samples shown in Fig. 3.3 was surprising due
to the significant difference in both height and full-width at half-maximum (FWHM) of the Si(111) substrate peak, which should have been identical since the same substrate was used between samples. Furthermore, the total thickness of the Ge and Al layers was only 100 nm, which should have prevented significant penetration losses in general, let alone such significant changes in peak intensity from one sample compared to the other. One limitation of the Rigaku D/Max-B was that the stage was at a fixed $90^\circ$ angle and could not be adjusted for alignment to either the Si(111) substrate or the deposited layers. It was later revealed that without the ability to align to a layer before the measurement, the absolute and relative intensity of the substrate and layer peaks depended significantly on how the substrate was mounted, and was not giving reproducible data. This issue was eventually resolved by switching to a Bruker D2 Phaser XRD system. Even though the substrate angle was also fixed, the D2 Phaser enabled substrate rotation, which scanned a variety of angles in the phi direction despite limitations in chi. This provided reproducible measurements scan-to-scan, and was the XRD system used for the remainder of this work.
3.2.3 Carrier Gas and Pressure

Up to this point, all anneals were performed in the Lindburgh Blue M tube furnace with a N\textsubscript{2} flow of 0.5 L/min and held at a pressure of 30 Torr. One of the limitations of the tube furnace was the lack of \textit{in-situ} diagnostics to evaluate crystallization behavior at various times throughout the anneal. Meanwhile, a new MOCVD reactor was installed, which besides its conventional III-V growth capabilities, was able to anneal the substrates while measuring \textit{in-situ} curvature (and subsequently stress) of the films during the anneal, as well as \textit{in-situ} reflectance at three different wavelengths penetrating different depths into the layer stack. Furthermore, the MOCVD had the ability to flow either N\textsubscript{2} or H\textsubscript{2} gas during the anneal, where H\textsubscript{2} was never plumbed to the tube furnace for safety concerns. To study the effects of ambient gas on crystallization, layers of 300 nm Al / 200 nm Ge films were deposited by thermal evaporation without breaking vacuum between layers, using a SiO\textsubscript{2}-coated Si substrate. The reason for the thicker Al and Ge films is explored in detail in the next section, but had started to show improved crystallization compared to the 50 nm Al / 50 nm Ge films. The sample was cleaved in half and annealed for 10 hours at a 500 °C set point (estimated around 415 °C true temperature) at a temperature ramp-rate of 1 °C/s and a pressure of 40 mbar (30 Torr) to be comparable to prior work.

![H\textsubscript{2} anneal pre-etch](image1.png) ![N\textsubscript{2} anneal pre-etch](image2.png)

Figure 3.4: Optical micrographs of identical samples annealed with either H\textsubscript{2} (left) or N\textsubscript{2} (right) gas during a 10-hour ~ 415 °C anneal. The magnification for both samples is 200x.
Figure 3.4 shows optical microscopy of the two samples annealed with otherwise identical conditions, one in a H\(_2\) ambient and one in an N\(_2\) ambient. The sample annealed in H\(_2\) showed two types of crystals: round Al spheres and snowflake-like Ge crystals, where composition was determined using energy-dispersive x-ray spectroscopy (EDS) in an SEM. The sample annealed in N\(_2\) showed large, dendritic crystals for both Al (dense crystals shown in blue) and Ge (shown in orange). Figure 3.5 shows in-situ reflectance at a wavelength of 405 nm, which provides insight to how reflectance near the surface changes as a function of anneal time. The reflectance for the sample annealed in H\(_2\) is constant once temperature and pressure are stabilized, and remains constant until the anneal has finished at which point temperature and pressure are returned to ambient conditions. When this sample was removed, it was fairly specular, which is consistent with the results from the reflectance measurement. The sample annealed in N\(_2\), however, showed changes in reflectance at various points that was indicative of the extensive crystal formation and growth across the sample surface.

![Figure 3.5](image)

Figure 3.5: 405 nm reflectance during a 10-hour ~ 415 °C anneal of identical samples annealed in either H\(_2\) or N\(_2\).

Since these 300 nm Al / 200 nm Ge sample showed interesting features, but not films ready for epitaxial growth, the Al thickness was decreased to 100 nm Al while maintaining the 200 nm Ge layer thickness and annealed for 10 hours in either an H\(_2\) or N\(_2\) ambient under the same conditions as the
previous samples. Figure 3.6a and b show SEM with an EDS map overlay of the two samples after etching the Al, as well as the reflectance during the anneal in Fig. 3.6c. In the EDS maps, the red background corresponds to Si, the green islands correspond to Ge, and the blue shows trace amounts of Al that remained in the Ge layer at high dopant levels. In both cases, Ge islands can be seen, but the Ge islands are larger for the sample annealed in H$_2$. The reflectance in both cases was low, and neither sample was specular after the anneal, instead demonstrating Ge islands and Al decorating the perimeter of the islands.

Figure 3.6: SEM with an EDS overlay of a. the samples annealed in H$_2$ and b. the samples annealed in N$_2$ as well as c. 405 nm reflectance from the two samples. The scale bar for both SEM images is 3 µm.

The role that pressure plays during the anneal was also evaluated. Two samples were annealed in the MOCVD at a 480°C set point (estimated 400 °C true temperature) for 10 hours at a pressure of either 40 mbar (30 Torr) or 980 mbar (735 Torr). Figure 3.7 shows optical microscope images of the two samples, where the samples annealed closer to atmospheric pressure showed larger grain size than the sample annealed at 40 mbar. This gave us reason to pursue atmospheric pressure in subsequent experiments.
3.2.4 Thickness of Aluminum and Ge Films

The Al and Ge layers reported in literature are often both 50 nm in thickness [63] [65] [70] [90], which were the thicknesses used in the initial experiments to examine the effect of deposition technique and breaking vacuum between the Al and Ge films. However, since those films were not yielding the desired quality for solar cell applications, thicker Al and Ge films were explored. The upper limit of Ge layer thicknesses reported in literature are as high as 1 µm [78] up to 2-5 µm [91] [66]. As a starting point for the study of layer thickness optimization, the Al layer was fixed to 50 nm, and Ge was varied from 200 nm, 400 nm, and 600 nm to see which sample demonstrated the best Ge recrystallization. The Al and Ge layers were deposited by thermal evaporation in a Kurt J. Lesker PVD 75C thermal evaporator on a Si/SiO$_2$ substrate, then annealed for 10 hours at a set point between 480-500 °C (≈ 400-415 °C true temperature) at a temperature ramp rate of 0.1 or 1 °C/s, shown in Fig. 3.8. In order to gain additional insight into the crystallization process, the following annealing experiments were performed in the MOCVD, which provided in-situ measurements of curvature and reflectance. Since the pyrometer cannot accurately read temperatures below a true temperature of 450 °C, both the temperature set points

![Image of optical microscope images of two samples annealed for 10 hours at approximately 400 °C, one with a pressure of 40 mbar (left) and the other with a pressure of 980 mbar (right). The magnification for both samples is 500x.](image)

Figure 3.7: Optical microscope images of two samples annealed for 10 hours at approximately 400 °C, one with a pressure of 40 mbar (left) and the other with a pressure of 980 mbar (right). The magnification for both samples is 500x.

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and estimations of the true temperature are provided for the discussion.

<table>
<thead>
<tr>
<th>Sample Configuration</th>
<th>Optical Microscopy Image</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 nm Al, 200 nm Ge</td>
<td><img src="image1.png" alt="Image" /></td>
</tr>
<tr>
<td>50 nm Al, 400 nm Ge</td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
<tr>
<td>50 nm Al, 600 nm Ge</td>
<td><img src="image3.png" alt="Image" /></td>
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Figure 3.8: Optical microscopy of samples with 50 nm of Al and varying thicknesses of Ge from 200-600 nm, annealed at temperatures between 480-500 °C set point (estimated 400-415 °C true temperature) and ramp rates of either 1 °C/s or 0.1 °C/s.

The top left image of Fig. 3.8 shows the 50 nm Al / 200 nm Ge sample annealed for 10 hours at 480 °C set point (estimated 400 °C true temperature) at a temperature ramp rate of 1 °C/s, where the beginning of layer transfer can be observed as demonstrated by the development and growth of nucleation points. Conversely, the 50 nm Al / 400 nm Ge film annealed with the same conditions showed no change in surface morphology, and the 50 nm Al / 600 nm Ge showed cracks. Since the surface features of the 50 nm Al / 200 nm Ge sample seemed promising, the temperature was increased to a 500 °C set point (estimated 415 °C true temperature) for a 10 hour anneal with the same 1 °C/s
temperature ramp rate from the previous sample set. Both cracks and crystals were observed in the 50 nm Al / 200 nm Ge case, the development of nucleation points were observed in the 50 nm Al / 400 nm Ge sample, and cracks were observed in the 50 nm Al / 600 nm Ge sample as well as voids down to the Si/SiO$_2$ substrate. The temperature ramp rate was decreased from 1 °C/s to 0.1 °C/s at the 500 °C set point 10-hour anneal to see what effect the temperature ramp may have on crack formation and propagation. Interestingly, crack formation in the center of the 50 nm Al / 600 nm Ge sample was suppressed, while cracks can still be observed along the edges. The crystallization and surface texturing in the 50 nm Al / 200 nm Ge increased with a slower temperature ramp-up rate.

Figure 3.9: EpiTT reflectance data of the three anneals for the three samples with 50 nm of Al and 200-600 nm of Ge. The red curves indicate the 480 °C set point anneal at a 1 °C/s ramp rate, the green curves indicate the 500 °C set point anneal at a 1 °C/s ramp rate, and the blue curves indicate the 500 °C set point anneal at a 0.1 °C/s ramp rate.

Since the samples were annealed inside the MOCVD, reflectance could be recorded in-situ during the anneal, shown in Fig. 3.9. As was observed above, the two 50 nm Al / 200 nm Ge samples that were annealed near a 415 °C true temperature exhibited cracks in the film that were not observed at the lower temperature of 400 °C. Mirroring the visual observation, sudden drops in reflectance could also be observed in the samples with cracks, which would later be understood as an indication for the point at which the cracks occurred during the anneal. For the 50 nm Al / 400 nm Ge samples, each curve had the same shape (and correspondingly, very little change could be seen visually between
the different samples), and high reflectance that is correlated with the specular surface we observed by optical microscopy. For the 50 nm Al / 600 nm Ge sample, large changes in reflectance can be observed, and it is likely that cracks formed very early in the anneal due to stress caused by the large difference in film thickness between the Al and Ge.

The 200 nm Ge film seemed to show the best visual signs of crystallization, while the 600 nm Ge film showed severe cracks in the film in every case. Based on these results, the thickness of the Ge layer was then fixed to 200 nm, and the Al layer was varied between 50 nm, 100 nm, and 200 nm. The optical microscope images are shown in Fig. 3.10. Cracks were observed for both of the 50 nm Al / 200 nm Ge samples, and very little crystallization was observed after the 10 hour anneal for the 100 nm Al / 200 nm Ge sample. However, the 200 nm Al / 200 nm Ge sample showed many nucleation points without cracks, which appeared to be the best nucleation behavior from the sample set.

Figure 3.10: Optical microscope images at 200x magnification of samples with fixed Ge thickness of 200 nm and varying Al thickness between 50 nm and 200 nm, annealed at a 500 °C set point for 10 hours.

The ramp rate was then increased to 1 °C/s at the same anneal temperature and time of a 500 °C
set point for 10 hours, with samples that had 200 nm Ge and Al layer thickness ranging from 100-300 nm Al centered around the 200 nm Al thickness. Those results are shown in Fig. 3.11 both before and after etching the Al layer. It was found that the 1.5% HF solution reported in literature is not selective to germanium. After exploring various etch chemistries, concentrated HCl was found to selectively etch Al at a rate of 0.96 nm/min without affecting the Ge layer. This HCl etch became standard practice for removing the Al layer.

![Pre-etch](image1.jpg) ![Post-etch](image2.jpg)

Figure 3.11: Optical microscope images at 200x magnification of samples with a fixed Ge thickness of 200 nm and varying Al thickness between 100 nm and 300 nm, annealed at 500 °C for 10 hours with a 1 °C/s temperature ramp rate from room temperature to anneal temperature.

The samples with 200 nm Ge and either 100 nm or 200 nm of Al showed promising Ge crystallization after the etch, which was the first step towards the development of Ge templates suitable for III-V growth. The 200 nm Ge and 300 nm Al layer proved useful for studies that required the observation of individual nucleation points and early stages of grain growth, and are featured in the studies in the following section.
3.3 Ramp Rate Study

A study of the effects of stress observed in-situ during aluminum-induced crystallization is presented, focusing on the effects of temperature ramp-up and ramp-down rates of the anneal that appear to play a vital role in initial grain formation and termination, respectively. The absolute Al and Ge thickness, as well as the ratio between them, were also varied in an attempt to minimize both the initial stress in the film as well as the stress induced while the anneal progressed. This study evaluates the role that temperature ramps (both up and down) have on stress, taking into consideration films with different thicknesses of Al and Ge deposited on a Si/SiO$_2$ substrate.

3.3.1 Theory

S. Hu and P. McIntyre studied nucleation of Ge during AIC as a function of anneal time, and developed a model to predict the density of islands, average area, and surface coverage of the Ge [92]. Since all three characteristics can be measured experimentally, parameters that are more difficult to measure - such as nucleation rate and nucleation saturation time, since Ge nucleation occurs underneath the layer stack at the Si/SiO$_2$ interface - can be extracted from those equations and correlated to studies such as temperature ramp rate. To start, the equation for area fraction of Ge on the substrate at time $t$ can be described as

$$f(t) = 1 - e^{-A^c/A}$$  \hspace{1cm} (3.1)

where $A$ is the area of the sample and $A^c$ is the extended area of the grains, or the sum of the area of individual grains. Taking into account that $A^c$ depends on nucleation density and grain size, we can then rewrite the equation as
\( f(t) = 1 - e^{-\int_0^t \dot{N}_N(\tau)Y(\tau,t)\,d\tau} \)  

(3.2)

where \( \dot{N}_N \) is the nucleation rate and \( Y \) is the area of a Ge crystal island nucleated at time \( \tau \) with growth until time \( t \). Testing the limits of this equation, we can confirm that this is a good approximation for the system. As grain size approaches infinity, perfect surface coverage can again be achieved. For an infinite nucleation rate corresponding to a surface covered with nucleation points, 100% surface coverage would again be achieved as infinitely many nucleation points cover the entire surface. If either grain size or nucleation points approach zero, the system didn’t crystallize, and the surface coverage approaches zero. The nucleation rate is given by

\[
\dot{N}_N = N_0 \frac{1}{\tau_N} e^{-\frac{t}{\tau_N}}
\]  

(3.3)

and depends upon a maximum nuclei density \( N_0 \), the nucleation saturation time \( \tau_N \) (which is inversely proportional to the nucleation rate at a given site). The final form of Eq. 3.1 can thus be written as

\[
f(t) = 1 - e^{-\int_0^t N_0 \frac{1}{\tau_N} e^{-\frac{\tau}{\tau_N}} Y(\tau,t)\,d\tau}
\]  

(3.4)

where the area fraction can be evaluated from 0% surface coverage to 100% surface coverage. In the following section, we experimentally measured the maximum nucleation density \( N_0 \), average area of the crystals \( Y \), and surface coverage \( f(t) \). Using these equations, we can derive the nucleation saturation time and the nucleation rate as a function of ramp rate by using these equations and the experimental measurements.
3.3.2 Experimental Details

500 nm of SiO$_2$ was thermally grown on a 2-inch n-type 280 µm thick Si(111) substrate from Wacker-Chemitronic (now Siltronic AG) using a Bruce Diffusion Furnace. Al and Ge were successively deposited from thicknesses ranging from 50-300 nm and 200-600 nm, respectively, using a Kurt J. Lesker PVD 75C thermal evaporator. The samples were annealed in an Aixtron MOCVD reactor at 500 °C set point (estimated 400 °C surface temperature) for 10 hours at a pressure of 40 mbar and H$_2$ flow of 4 L/min. Wafer curvature and reflectivity were measured in-situ using a LayTec EpiTTCurve monitor. After annealing, Al was etched using a 1.5% dilute solution of hydrofluoric acid.

Samples were characterized with a differential interference optical microscope with a Nomarski prism, as well as field emission scanning electron microscope (FESEM) using a Bruker EDS detector to understand the sample surface morphology and material diffusion. XRD was performed with a Bruker D2 Phaser powder XRD system to verify the relative peak intensity of the Al and Ge layers and verify the crystal orientations present. Finally, the curvature was analyzed to reveal relative stress in the films during the course of the anneal.

3.3.3 Results and Discussion

Recall from Fig. 3.8 that many of the samples prepared with 50 nm of Al and 200-600 nm of Ge exhibited cracks due to stress, which was likely caused by an insufficiently thick Al layer for uniform layer transfer. Figure 3.12 shows SEM and optical microscope images of two samples with 50 nm of Al and 200 nm of Ge, annealed to a 500 °C set point for 10 hours at rampup rates of either 1 °C/s or 0.1 °C/s. In each case, both large cracks and µm-sized crystallization were observed. The SEM image in Fig. 3.12b illustrates how stress propagates from a center, surrounded by a ring of material that crystallized around it. The SEM image has overlayed EDS mapping of Al (red), Ge (green), and Si (blue) to indicate the elemental composition of the surface features. Both Al and Ge surround the crack.
Figure 3.12: a. Optical microscopy and b. SEM of a sample with 50 nm of Al and 200 nm of Ge, annealed to a 500 °C set point for 10 hours at a ramp-up rate of 1 °C/s. c. Optical microcopy of the same sample annealed at a ramp-up rate of 0.1 °C/s. In both cases, the surface features include crystallized Ge and cracks. © IEEE 2016

propagation centers, and delamination ensues as the substrate is increasingly exposed. The extent of delamination continues to worsen as the Ge layer thickness is increased while the Al thickness remained constant at 50 nm.

By using thicker Al layers and keeping the Ge thickness constant, the stress observed in Fig. 3.12 could be alleviated, and no cracks were observed in the 300 nm Al / 200 nm Ge samples. Figure 3.13 shows SEM and corresponding EDS mapping of this sample annealed at different ramp-up and ramp-down conditions. For the 300 nm Al / 200 nm Ge sample, the EDS mapping represents Al in red and Ge in gold. The SEM indicates that Ge grain nucleation and termination are affected by anneal ramp rates. This data is quantified in Table 3.1 by analyzing the SEM images of the 0.1 °C/s samples as shown, and the 1 °C/s samples at lower magnification in order to have a more representative sample size of nucleation points. The faster ramp-up rate was correlated to fewer Ge nucleation points, which led to a lower density of larger sized grains observed in the samples. The slower ramp-down rate seemed to yield larger grain size, but that may be attributed to an increased effective anneal of 1 hour, or 10% of the total anneal time. Had optimal conditions been used that allowed for full layer transfer and complete grain growth, the nucleation and termination processes could not have been observed.
Figure 3.13: Plan-view SEM images with corresponding EDS mapping of samples with 300 nm of Al and 200 nm of Ge after a 500 °C set point anneal for 10 hours. The corresponding ramp conditions for the anneal were: (a) 1 °C/s ramp-up rate, 1 °C/s ramp-down rate. (b) 1 °C/s ramp-up rate, 0.1 °C/s ramp-down rate. (c) 0.1 °C/s ramp-up rate, 1 °C/s ramp-down rate. (d) 0.1 °C/s ramp-up rate, 0.1 °C/s ramp-down rate. © IEEE 2016
Figure 3.14 shows log-scale XRD of the 300 nm Al / 200 nm Ge samples annealed with different ramp rates, where a scan speed of 2 seconds/step was used as the stage rotated at 30 rpm to survey the various grain orientations. Several Ge orientations were observed, dominated by a preferential (111) orientation. The Al peak remained relatively constant since a post-anneal Al etch was not performed, and the Si peaks were constant in intensity and position between each sample since they were all prepared from the same substrate. The most notable change between XRD plots is the increase in the Ge(311) peak and decrease in the Ge(220) peak for both samples that experienced the 0.1 °C/s ramp-up rate compared to the 1 °C/s ramp-up rate. The Ge(311) peak was nearly identical for the fast ramp-up rates, but increased by 53% for the 0.1 °C/s ramp-up rate, 1 °C/s ramp-down rate, and increased by 115% for the 1 °C/s ramp-up rate, 1 °C/s ramp-down rate relative to the Ge(311) peaks for the fast ramp-up rates. Meanwhile, the Ge(220) peak was 4% lower for the 0.1 °C/s ramp-up rate, 1 °C/s ramp-down rate, and 30% lower for the 1 °C/s ramp-up rate, 1 °C/s ramp-down rate relative to the slower ramp-up rates.

Figure 3.14: XRD of the samples with four temperature ramp rate combinations shown in Fig. 3.13.

The relationship between stress and ramp-up rate was then investigated for the 200 nm Al and 200 nm Ge sample. The curvature of each sample set was measured in-situ, and stress was calculated for the different samples, using the Stoney equation.
\[
\sigma_f = \frac{\kappa \cdot M_s \cdot h_s^2}{6h_f}
\]  

(3.5)

where \(\sigma_f\) is the film stress, \(\kappa\) is the substrate curvature, \(M_s\) is the substrate biaxial modulus, \(h_f\) is the film thickness, and \(h_s\) is the substrate thickness \([93]\). Figure 3.15 shows the stress over time observed \textit{in-situ} for the various ramp rate combinations.

![Figure 3.15: In-situ stress curves as a function of ramp rate for samples prepared with 300 nm of Al and 200 nm of Ge. Time = 0 indicates at which point the sample reached the 500 °C set point. © IEEE 2016](image)

In each case, the stress started at -39 MPa for the 300 nm Al, 200 nm Ge sample at room temperature. As temperature increased during the initial ramp-up, compressive stress was observed (indicated by a negative slope) due to the mismatch in thermal expansion coefficients between the substrate and Al/Ge bilayer \([90]\). The compressive stress was then reduced by nearly 0.1 GPa, still before the anneal reached 500 °C, but occurred more gradually for the slower 0.1 °C/s ramp-up rate than it did for the 1 °C/s ramp. Since no cracks were observed in any of the films post-anneal, this reduction in compressive stress was attributed to atomic diffusion of Al or nucleation of Ge grains \([90]\). For both samples with the ramp-up rate of 1 °C/s, the absolute stress during the 10-hour anneal stabilized at the same intensity as the initial
film stress pre-anneal. For the ramp-up rate of 0.1 °C/s, the absolute stress at the 500 °C set point was lower than the initial stress in the films. During cooling, tensile stress was observed in each case, but the change in tensile stress over time was more abrupt for the samples with faster, more abrupt ramp-down rate.

Table 3.1 shows the average grain size, density, and surface coverage as measured by Scanning Probe Image Processor (SPIP) software from SEM data, as well as the root mean square roughness as measured by atomic force microscopy (AFM). This study indicates that the ramp-up rate to the anneal set point temperature has a significant effect on grain nucleation for crystallization of Ge using AIC. SEM and EDS images from the sample set with 300 nm of Al and 200 nm of Ge indicated that larger grains formed for the faster ramp-up time, indicating a lower density of Ge nucleation points. The relative order of magnitude of grain size, the extent of Ge coverage, and the grain area all increased for the faster ramp-up rate. On average, the grain size was also larger for slower ramp-down times, but this was attributed to a longer effective anneal by 10%. XRD indicated the presence of multiple Ge peaks, where the Ge(111) peak was the strongest in each case.

Table 3.1: Summary of grain size, density, surface coverage, and average roughness as a function of ramp rate for samples annealed for 10 hours at 400 °C.

<table>
<thead>
<tr>
<th>Ramp Rate</th>
<th>Average Grain Area (µm²)</th>
<th>Average Grain Density (mm⁻²)</th>
<th>Surface Coverage (%)</th>
<th>RMS Roughness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 °C/s up, 1 °C/s down</td>
<td>410</td>
<td>614</td>
<td>25.2</td>
<td>7.6</td>
</tr>
<tr>
<td>1 °C/s up, 0.1 °C/s down</td>
<td>842</td>
<td>229</td>
<td>19.3</td>
<td>8.9</td>
</tr>
<tr>
<td>0.1 °C/s up, 1 °C/s down</td>
<td>6.7</td>
<td>5.5e4</td>
<td>36.8</td>
<td>7.2</td>
</tr>
<tr>
<td>0.1 °C/s up, 0.1 °C/s down</td>
<td>6.8</td>
<td>5.7e4</td>
<td>37.8</td>
<td>8.5</td>
</tr>
</tbody>
</table>

Table 3.2 shows the calculated nucleation rate and nucleation saturation time, using the method described in Section 3.3.1. Since the surface coverage measured experimentally only varied from 19.3% to 37.8%, the values for nucleation conditions across the different ramp rates are calculated to be fairly close. As expected, the faster nucleation rates correspond to shorter time required to create
nucleation points. Using this understanding that the faster temperature ramp rates gave larger grains, similar nucleation rates compared to the lower ramp rate samples, and that these conditions were not ideal for ultimately creating polycrystalline Ge templates, the ramp rate experiment was performed on samples that showed more promising Ge surface coverage.

Table 3.2: Summary of nucleation rate and nucleation saturation time as a function of ramp rate for samples annealed for 10 hours at 400 °C.

<table>
<thead>
<tr>
<th>Temperature Ramp Rate</th>
<th>Nucleation Rate (nuclei/hour)</th>
<th>Nucleation Saturation Time (hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 °C/s up, 1 °C/s down</td>
<td>0.35</td>
<td>2.9</td>
</tr>
<tr>
<td>1 °C/s up, 0.1 °C/s down</td>
<td>0.33</td>
<td>3.0</td>
</tr>
<tr>
<td>0.1 °C/s up, 1 °C/s down</td>
<td>0.37</td>
<td>2.7</td>
</tr>
<tr>
<td>0.1 °C/s up, 0.1 °C/s down</td>
<td>0.37</td>
<td>2.7</td>
</tr>
</tbody>
</table>

Figure 3.16 shows the continuation of this study for 200 nm Al and 200 nm Ge films annealed at 375 °C for 50 hours with a temperature ramp-up rate of 1 °C/s, which had showed larger grain size and surface coverage in Fig. 3.11 of Section 3.2.4 for the same time compared to the 300 mm Al / 200 nm Ge samples explored above. The 1 °C/s temperature ramp rate became the standard for all further studies because of its ability to yield larger crystals and compact Ge films. Increasingly higher temperature ramps (5-100 °C/s) were explored via rapid thermal annealing to initiate nucleation, and then moved to the tube furnace to complete the layer transfer. However, no significant benefit was observed at higher ramp rate, and the film quality appeared worse when the anneal was started in one tool and then moved to another than when the anneal was performed in one furnace continuously.

### 3.4 Substrate Thickness study

AIC has been shown to create poly-Ge substrates on a variety of platforms, including glass [75], ceramics [66], polymers [76], and Si [63] [69] [65]. Although there is great versatility in substrate choice,
optimal conditions are necessary to minimize stress that can occur in the poly-Ge films. Signs of delamination and dewetting [66], stress [87], and hillock formation [65] have been observed on various platforms, as well as the deposition and anneal conditions that can suppress those effects. Additional considerations that affect the resulting film quality include the rate of Ge diffusion, where slow Ge diffusion has been shown to promote large-grain Ge crystal growth, and rapid Ge diffusion has been shown to yield small-grain Ge islands [22] [23]. A thicker initial a-Ge layer of 150 nm compared to a 50 nm layer was shown to improve surface coverage of the Ge film post-anneal, but also created many small-grain Ge islands above those large-grain Ge films as a result of supplying more Ge atoms for diffusion, where the small-grain islands could later be removed [23]. Exploring additional conditions that may also affect the diffusion rate will be critical to enabling large-grain Ge films with high surface coverage.

Substrate thickness is one factor that can affect stress and resulting grain size in poly-Ge films. Oya
et al. explored the effect of polyimide substrates with thickness ranging from 12 µm to 125 µm on the grain size and (111) orientation fraction of poly-Ge films. The 125 µm thick polyamide films showed higher (111)-oriented grains compared to the 12 µm or 25 µm polyamide films explored in the study, due to the larger curvature and therefore stress associated with the thinner films [10]. However, rigid substrates are often reported in literature for the AIC process - including Si, glass, and ceramics – which have greater thicknesses in the range of 200-525 µm and substantially less curvature than the polyamide films. Investigating the effect of substrate thickness on thicker, rigid substrates could inform how grain size, orientation, and surface coverage are affected.

The following study explores the effect of five Si substrate thickness from 200-525 µm, including (100) and (111) crystal orientations at similar substrate thickness, as a function of temperature on the resulting poly-Ge films. The results indicate that substrate thickness impacts both grain size and surface coverage. This work has implications for scalability since thicker substrates are often used for larger wafers. This study also provides insight for achieving uniform films with high surface coverage and minimal stress, which is critical for utility in industry.

3.4.1 Experimental Details

The commercial Si substrates used in this experiment had thicknesses of 200 µm, 250 µm, 280 µm, 375 µm, and 525 µm. Four of these Si substrates were (100) oriented: the 200 µm substrate from SiMPore Inc., the 250 µm and 375 µm substrates from Virginia Semiconductor Inc., and the 525 µm substrate from Wafer Works Corporation. A 280 µm thick Si(111) substrate was also evaluated in this study from Wacker Chemitronic (now Siltronic AG). This allowed for evaluation of both the effects of substrate thickness and substrate orientation for commercially available Si substrates.

A standard RCA clean was performed for all of the Si substrates at the same time, followed immediately by transferring them to a Bruce diffusion furnace at 1000 ºC for 500 nm of thermally grown
SiO$_2$, where the primary function of the oxide was to prevent Al from gettering the Si. Layers of 200 nm polycrystalline Al and 200 nm amorphous Ge were subsequently deposited using a Kurt J. Lesker PVD 75C thermal evaporator on all of the oxide-coated Si substrates at the same time. Once deposited, the samples were placed in a Lindbergh Blue M tube furnace with a 4” quartz tube, a Eurotherm 2704 temperature controller, and a General Electric 5KCR 47UG26T vacuum pump. For each anneal temperature, all 5 substrate thicknesses were placed in the tube furnace to be annealed together. The temperature reported was verified using a 52-2 60HZ Fluke thermometer with a thermocouple placed in the center of the tube where the samples sit during theanneals and allowed to stabilize for at least 10 minutes at each temperature reading.

Once the samples were loaded into the tube furnace, the quartz tube was pump-purged from 10 Torr to 760 Torr twice at room temperature under a nitrogen flow of 500 sccm. After the pump-purge was complete, the temperature was ramped to the anneal temperature (365 °C, 375 °C, or 385 °C) at a rate of 1 °C/s, annealed for 50 hours, and then ramped down to room temperature at a 1 °C/s set point. After the anneal, the samples were characterized with a Nomarski optical microscope then etched for 5 hours in a concentrated HCl bath with a selective etch rate of Al compared to Ge at 0.96 nm/min. Finally, the remaining poly-Ge films were analyzed with a Nomarski optical microscope, TESCAN field emission scanning electron microscope (FESEM) with a Bruker EDS detector, and electron backscatter diffraction (EBSD) with a Hikari Detector from EDAX Inc.

3.4.2 Results and Discussion

This study evaluated a sample set of 200 nm Al / 200 nm Ge bilayers deposited on SiO$_2$ grown on five unique Si substrate thicknesses between 200 µm to 525 µm, annealed for 50 hours at one of three different temperatures between 365-385 °C, and etched for 5 hours in concentrated HCl to remove
residual Al. Optical micrographs of the sample set are displayed in Fig. 3.17. The resulting poly-
Ge films can be classified into three nucleation regimes: large yet discrete islands observed at either
high temperature or the 200 \( \mu m \) substrate thickness, continuous films with \( \mu m \)-sized pores which were
observed in the Ge films with substrates between 250-375 \( \mu m \) and anneal temperature between 365-375
\( ^\circ C \), and films with cracks which were observed in films at 525 \( \mu m \) at 365-375 \( ^\circ C \).

<table>
<thead>
<tr>
<th></th>
<th>200 ( \mu m ) Si(100)</th>
<th>250 ( \mu m ) Si(100)</th>
<th>280 ( \mu m ) Si(111)</th>
<th>375 ( \mu m ) Si(100)</th>
<th>525 ( \mu m ) Si(100)</th>
</tr>
</thead>
<tbody>
<tr>
<td>385 ( ^\circ C )</td>
<td>a.</td>
<td>b.</td>
<td>c.</td>
<td>d.</td>
<td>e.</td>
</tr>
<tr>
<td>375 ( ^\circ C )</td>
<td>f.</td>
<td>g.</td>
<td>h.</td>
<td>i.</td>
<td>j.</td>
</tr>
<tr>
<td>365 ( ^\circ C )</td>
<td>k.</td>
<td>l.</td>
<td>m.</td>
<td>n.</td>
<td>o.</td>
</tr>
<tr>
<td>325 ( ^\circ C )</td>
<td>p.</td>
<td>q.</td>
<td>r.</td>
<td>s.</td>
<td>t.</td>
</tr>
</tbody>
</table>

Figure 3.17: Optical microscopy with a Nomarski prism of the Ge films after etching the Al in concen-
trated HCl on the 5 different Si substrates annealed at temperatures of (a-e.) 385 \( ^\circ C \), (f-j) 375 \( ^\circ C \), and
(k-o) 365 \( ^\circ C \) for a 50 hours. All images were taken at 1,000x magnification with an optical microscope
[24].

Discrete Ge islands were realized at 385 \( ^\circ C \) across all 200-525 \( \mu m \) substrate thicknesses, and for the
200 \( \mu m \) substrate thickness across the 365-385 \( ^\circ C \) anneal temperatures. Scanning Probe Image Proc-
essor software was used to find the feature size and percent surface coverage of poly-Ge compared to the
Si/SiO\textsubscript{2} substrate, where the results are quantified in Table A. Figure 3.17a-e shows optical microscope
images at 1,000x magnification of the samples annealed at 385 \( ^\circ C \) after removing the Al layer, where
Ge islands occurred regardless of substrate thickness, with surface coverage between 43.4% - 52.3%.
Figure 3.17 a, f, and k shows the Ge islands that formed on the 200 µm substrate with surface coverage between 50.8% - 60.5%. The a-Ge films deposited on the 200 µm substrate or annealed at 385 °C both experienced a greater amount of thermal energy than the other samples explored in this study, either due to increased anneal temperature or a thinner substrate that allowed the films to reach the anneal temperature more quickly. Hsu et al explored the effects of temperature and other parameters on stress for AIC of Si films, and found that higher temperatures seemed to be associated with a lower activation energy for crystallization, and ability to release the film stress in a shorter time [94]. Similarly, Ge island nucleation may have been favored for the 200 µm substrate or 385 °C anneal due to rapid atomic migration that occurred to quickly relieve stress.

By dropping the temperature from 385 °C to 375 °C, substantial changes in the films were realized, as indicated in Figure 3.17 f-j. Among them were the presence of cracks that occurred in the poly-Ge films deposited on the 525 µm substrates at both 365 and 375 °C, which is a mechanism to relieve stress in films during the AIC process [90] [95]. Cracks in the film may have occurred to compensate for the thickness and rigidity of the 525 µm substrate. Figure 3.17 g-j and 1-n demonstrate compact poly-Ge films with µm-sized pores. Since these films represented the highest surface coverage without cracks, SEM of these six best samples was performed and analyzed with Scanning Probe Image Processing software to quantify the surface coverage and pore size. Figure 3.18 shows SEM taken of the Ge films on the 250-375 µm substrates that had been annealed at 365 °C and 375 °C.

Scanning Probe Image Processor software was used to measure the surface coverage and feature size of the samples evaluated in this study, where the results are displayed in Table 3.3. For large, discrete poly-Ge islands and poly-Ge films with cracks, the optical micrographs shown in Fig. 3.17 provided the most representative perspective from which to draw statistics. However, the exact pore size and surface coverage for the compact poly-Ge films with µm-sized pores demanded analysis from the SEM images shown in Fig. 3.20.
Figure 3.18: SEM of the samples shown in Fig. 3.20g-j and Fig. 3.20l-n that demonstrated the highest, most uniform surface coverage [24].

Figure 3.19 graphically displays the surface coverage reported in Table 1 as a function of temperature and substrate thickness, where each of the 15 samples investigated in this study are represented by the black data points. The poor surface coverage observed for all samples with 200 \( \mu \text{m} \) substrates or were annealed at 385 °C is easily observed, where lowering the anneal temperature to 365-375 °C or increasing substrate thickness improves surface coverage. There is a bimodal distribution in highest surface coverage; however, the poly-Ge films on the 525 \( \mu \text{m} \) Si(100) substrate exhibited cracks while the poly-Ge films on the 280 \( \mu \text{m} \) Si(111) substrate did not.

While high surface coverage is imperative for solar cell growth and fabrication, large grain size is necessary in order to minimize grain boundary recombination [48]. SEM, EDS, and EBSD measurements were taken to better understand the effects that substrate thickness may have on surface coverage, residual Al content, and grain size, respectively, for the three nucleation conditions observed in this study. Figure 3.20 shows these results for the samples with 200 \( \mu \text{m} \) Si(100), 280 \( \mu \text{m} \) Si(111), and 525 \( \mu \text{m} \) Si(100) substrates annealed at 375 °C. The top row shows the EBSD inverse pole figures for the

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>250 ( \mu \text{m} ) Si(100)</th>
<th>280 ( \mu \text{m} ) Si(111)</th>
<th>375 ( \mu \text{m} ) Si(100)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.65</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
<td><img src="image3.png" alt="Image" /></td>
</tr>
<tr>
<td>3.75</td>
<td><img src="image4.png" alt="Image" /></td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
</tbody>
</table>
Table 3.3: Surface coverage and feature size reported using Scanning Probe Image Processor software as a function of substrate thickness, substrate orientation, and anneal temperature [24].

<table>
<thead>
<tr>
<th>Substrate Thickness ($\mu$m)</th>
<th>Substrate Orientation</th>
<th>Temperature ($^\circ$C)</th>
<th>Surface Coverage (%)</th>
<th>Mean Feature Diameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>365</td>
<td>58.9</td>
<td>0.48 $\mu$m islands</td>
</tr>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>375</td>
<td>60.5</td>
<td>0.54 $\mu$m islands</td>
</tr>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>385</td>
<td>50.8</td>
<td>1.2 $\mu$m islands</td>
</tr>
<tr>
<td>250</td>
<td>Si(100)</td>
<td>365</td>
<td>80.8</td>
<td>0.33 $\mu$m pores</td>
</tr>
<tr>
<td>250</td>
<td>Si(100)</td>
<td>375</td>
<td>89.5</td>
<td>0.34 $\mu$m pores</td>
</tr>
<tr>
<td>250</td>
<td>Si(100)</td>
<td>385</td>
<td>47.7</td>
<td>2.3 $\mu$m islands</td>
</tr>
<tr>
<td>200</td>
<td>Si(111)</td>
<td>365</td>
<td>95.6</td>
<td>0.25 $\mu$m pores</td>
</tr>
<tr>
<td>200</td>
<td>Si(111)</td>
<td>375</td>
<td>96.9</td>
<td>0.31 $\mu$m pores</td>
</tr>
<tr>
<td>200</td>
<td>Si(111)</td>
<td>385</td>
<td>43.4</td>
<td>1.4 $\mu$m islands</td>
</tr>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>365</td>
<td>92.7</td>
<td>0.34 $\mu$m pores</td>
</tr>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>375</td>
<td>91.2</td>
<td>0.33 $\mu$m pores</td>
</tr>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>385</td>
<td>51.2</td>
<td>1.5 $\mu$m islands</td>
</tr>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>365</td>
<td>92</td>
<td>Cracks</td>
</tr>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>375</td>
<td>95.7</td>
<td>Cracks</td>
</tr>
<tr>
<td>200</td>
<td>Si(100)</td>
<td>385</td>
<td>52.3</td>
<td>0.76 $\mu$m islands</td>
</tr>
</tbody>
</table>

three samples, where the triangle in the top left corner maps the color of the images to (100), (111), or (101) crystal orientations. Comparing the EBSD inverse pole figure for the three samples, the average grain sizes were 10.76 $\mu$m for the 200 $\mu$m Si(100) substrate, 0.3 $\mu$m for the 280 $\mu$m Si(111) substrate, and 1.32 $\mu$m for the 525 $\mu$m Si(100) substrate. The second row of Fig. 3.20 shows the SEM image of the samples with a box where EBSD was performed. The third row of Fig. 3.20 shows SEM with an EDS map of the three samples at a lower magnification than the SEM image in the second row, where the green corresponds to Ge, blue corresponds to Si, and red corresponds to Al.

The SEM image with an EDS overlay of the 200 $\mu$m Si(100) sample confirms the presence of large Ge islands on a Si/SiO$_2$ substrate. The EBSD shows 10.76 $\mu$m-sized poly-Ge grains, which are approximately the size of the features measured. This result is notable because although the discrete island formation observed on the 200 $\mu$m Si(100) substrate is detrimental for device fabrication, the individual islands appear to be single crystal orientations.
Figure 3.19: Contour maps showing surface coverage as a function of temperature and substrate thicknesses for all Si(100) samples and the Si(111) sample. The dots indicate the data points from the sample set [24].

The Ge films on the 280 $\mu$m Si(111) substrate, which had high surface coverage without any cracks, demonstrated grain sizes above 300 nm with no preferential crystal orientation as seen from EBSD. It has been reported that a higher (111) crystal orientation fraction can be observed if a short exposure to atmosphere is introduced between depositions of the the Al and Ge layers [63]. However, a compact Ge film could not be achieved across a full 2-inch wafer when that procedure was attempted in-house, whereas that level of uniformity could be observed when vacuum was not broken between the two layers. The sample with cracks on the 525 $\mu$m substrate did not appear to complete layer transfer according to the high Al content observed in the EDS map. Since crystallization, Al diffusion to the surface of the film stack, and cracks are all mechanisms to relieve stress [90], it is likely that cracks formed in these samples in lieu of the expected layer transfer.

To better understand the effects of substrate thickness on the crystallization process, COMSOL Multiphysics modeling software was used to simulate the effects of various substrate thicknesses. The layer
stack was created to simulate the real layer thicknesses and materials used in the study. Other simulation parameters included convective heating, an initial temperature of 293 K, an anneal temperature of 653 K, and a 1 °C/s temperature ramp rate. The software output the temperature of the Al/Ge interface where crystallization has been shown to initiate [69] and then calculated how the interface temperature changes during the anneal. Figure 3.21 shows the results of the COMSOL simulation for the first 10 minutes of the anneal.

While each of the layers deposited on the 200-525 µm thick substrates reached the same temperature after 10 minutes, there is a noticeable difference in the temperature of the Al/Ge interface during the temperature ramp up, despite the simulated furnace ramp being set to a constant 1 °C/s ramp in each case. This indicates that thicker substrates act as a heat sink to the Al and Ge layers, lowering the effective temperature ramp rate proportional to the substrate thickness. Temperature ramp rate has been shown to influence the density of nucleation points and grain size for both Ge [96] as well as other
Figure 3.21: COMSOL Multiphysics simulation of the 1 °C/s temperature ramp up rate set point used in the experiment (dashed black line) as well as the temperature at the Al-Ge interface as a function of time for different substrate thicknesses [24].

material systems [97] [98]. Since the first 10 minutes of the anneal are critical to the development of nucleation points according to XRD measurements [65] as well as stress in the film according to SEM images [87], different Ge films can result from otherwise identical Al/Ge bilayers deposited on substrates with varying thickness.

The simulation indicates that the 200 µm substrate reaches temperatures during the first 10 minutes of the anneal that the 525 µm substrate reaches nearly 50 seconds to several minutes later. This higher effective anneal temperature may explain the formation of Ge islands, which were most similar to the substrates that were annealed at or above 385 °C. Island formation was likely due to a combination of higher thermal energy during the temperature ramp as well as substrate curvature that allowed the substrate to compensate for some of the film stress. On the other extreme, cracks may have formed on the 525 µm substrate due to a combination of lower thermal energy during the initiation of nucleation points, coupled with the rigidity and lack of mechanical flexibility provided by the thick substrate. The combination of a lower effective temperature ramp-rate with increased substrate thickness as well as a
lack of mechanical flexibility in the thicker substrate that could cause the films to experience greater stress and therefore crack (or thinner substrates that could cause the films to curve and create islands) are credited with the diverse Ge film morphology as a function of Si substrate thickness.

3.5 Conclusions

This chapter evaluated the methods for creating substrates with high surface coverage and greater than 10 $\mu$m grain size required for growing solar cells. A variety of parameters were considered, including the effects of Al oxidation, different deposition techniques, ambient gas and pressure during the anneal, absolute and relative Al and Ge thicknesses, total annealing time, anneal temperature, temperature ramps to and from the anneal temperature, and substrate thickness.

To summarize the experiments, breaking vacuum after Al deposition to form a native oxide was found to be detrimental to surface coverage, and was omitted for most experiments. Thermal evaporation was shown to create rounder, more uniform Ge crystals, and was pursued instead of the sputtering tool at RIT. Where possible, a hydrogen ambient appears to be conducive to larger grain size; however, that was not an option for the Lindburgh Blue M tube furnace due to safety concerns. 980 mbar (735 Torr) showed larger Ge crystals than the 40 mbar (30 Torr) pressure, and was employed after a pump-purge process from 10 Torr to 760 Torr twice at room temperature to remove residual oxygen in the chamber. The layer thicknesses chosen for the samples were 200 nm Al / 200 nm Ge at an optimal temperature around 375 °C for those film thicknesses. Finally, a survey of Si substrate thicknesses and their effect on grain size and surface coverage indicated that the 280 $\mu$m Si(111) gave the best surface coverage, but the films deposited on the 200 $\mu$m Si(100) substrate showed the largest grain size according to EBSD.

These studies illuminated the effect that temperature ramp rate and substrate thickness have on surface coverage, indicating that both an optimal temperature ramp rate and substrate thickness exist for
a given set of AIC conditions. After optimizing our substrates, solar cells were grown as discussed in the next chapter.
Chapter 4

MOCVD Growth on Germanium Substrates

4.1 Introduction

In order to grow high-efficiency solar cells on low-cost polycrystalline substrates, an understanding of the impact of nucleation conditions on the quality of the subsequent epitaxial layers is required. First, solar cells were grown on commercial monocrystalline and polycrystalline GaAs and Ge substrates to experimentally validate a model developed in-house of how solar cell performance is affected by polycrystallinity and antiphase domain (APD) formation. Next, double heterostructures were grown on commercial substrates to determine the optimal nucleation layer material and temperature for growth of GaAs on poly-Ge. These test structures were grown on both the commercial Ge substrates and the AIC substrates from the previous chapter. To finish this study, solar cells were grown on AIC Ge as well as commercial monocrystalline and polycrystalline Ge as baselines.
4.2 Solar Cells on Commercial Monocrystalline and Polycrystalline Germanium Substrates

The experiments detailed in this section explore the effect of grain size and APD formation on minority carrier diffusion length (MCDL) and lifetime. Substrates were purchased from several companies, including AXT Inc. for c-GaAs substrates used as the baseline, CMK Ltd. for poly-GaAs substrates used to distill the effects of grain size, and Umicore for c-Ge and poly-Ge substrates used to examine the effect of APDs both individually and with the compounded effect of polycrystallinity. The poly-GaAs substrates were unpolished when ordered and had large randomly oriented grains with an average diameter of 400 $\mu$m. The unpolished poly-GaAs substrates were sent for polishing through III/V Reclaim, which is a company that specializes in reclaiming used, crystalline III-V substrates by removing the top few microns of material, polishing the substrate to a roughness less than 1 nm, and vacuum-sealing the samples for return. The poly-Ge substrate were polished as-received and had randomly oriented grains with an average diameter of 200 $\mu$m.

![Figure 4.1: Electroluminescence images taken of the surface of GaAs solar cells grown on both poly-GaAs and poly-Ge substrates.](image)

In order to quantify the grain size, electroluminescence was performed, which is a technique that sources current to the solar cell and measures the resulting luminescence. Figure 4.1 shows images of
the poly-GaAs and poly-Ge solar cells that were taken with an infrared camera attached to an optical microscope. Since grain boundaries act as recombination centers, they can be observed as dark boundaries that can then allow an average grain size to be measured.

To determine the orientation of the poly-GaAs substrate, Figure 4.2 shows XRD that was performed on two of the grains that exhibited a difference in external quantum efficiency (EQE), one of which appeared light when viewed optically compared to the other, which appeared darker. The light grain on the poly-GaAs substrate showed many points of low-intensity mosaic crystals, while the dark grain exhibited relatively little mosaicality with only a few high-intensity peaks. Both shared a 15° offset in the (111) direction from the surface normal, but are rotated far from each other in-plane.

![Figure 4.2: XRD of the light and dark dark grains on the commercial poly-GaAs substrate.](Image)

P-i-n GaAs solar cells were grown by MOCVD on a (100) c-GaAs substrate from AXT, Inc. and a poly-GaAs substrate from CMK Ltd., while p-i-n In_{0.01}Ga_{0.99}As solar cells were grown on a (100) c-Ge substrate with a 6° offcut from Umicore and a poly-Ge substrate from Umicore. The c-GaAs and c-Ge substrates were polished, standard epi-ready n-type substrates. The layer structure of the solar cells grown on these substrates is shown in Fig. 4.3. Standard precursors were used for solar cell growth, including trimethylgallium (TMGa), trimethylindium (TMIn), arsine (AsH\textsubscript{3}) and PH\textsubscript{3} for
alkyl and hydride sources. Doping was accomplished using disilane for n-type materials and diethylzinc (DEZn) for p-type materials. Both samples were annealed at 700 °C prior to initiating growth in order to minimize APDs, then temperature was lowered to 500 °C for the buffer layer and 620 °C for the remainder of the growth. The c-GaAs and poly-GaAs substrates were both grown together, while the c-Ge and poly-Ge substrates were also grown together in a subsequent run. In order to grow high-quality III-V solar cells on Ge, a 25 nm nucleation layer was grown at a low temperature to minimize the effects of polycrystallinity followed by a thicker buffer to minimize the effect of APDs and allow them to self-annihilate [99]. Above the buffer layer, the growth was analogous for both the GaAs and Ge runs.

Standard fabrication processes were then used to fabricate the solar cells. These include starting with a solvent rinse that submerges the samples for 2 minutes in acetone followed by 2 minutes in isopropyl alcohol, then drying the samples with a nitrogen gun. The samples were then taken to an SCS spin coater for photoresist application in preparation for lithography of the front contacts. Once
the sample was placed on the spin coater and a strong vacuum connection was secured, one drop of hexamethyldisilazane (HDMS P-20) was applied per inch diameter using a pipette, then left for 10 seconds in order to turn the wafer surface hydrophobic and promote better adhesion to the photoresist. The spin coater was then set to a 3 step procedure: 500 rotations per minute (RPM) with a 3 second ramp and 10 second application, then 3,000 RPM with a 3 second ramp and 40 second application, and finally 5,000 RPM with a 3 second ramp for a duration of 5 seconds. This is our typical recipe for the spin coater and will be used for the duration of this fabrication process and for subsequent ones mentioned in this work. Next, half a pipette of lift-off resist (LOR 10A) was applied during the 500 RPM spin, then baked on a hotplate at 180 °C for 6 minutes. This ensures that excess gold can be lifted off away from the developed pattern. Finally, a photoresist called S1813 was applied during the 500 rpm spin and heated at 115 °C for 1 minute. Front lithography was then performed using Karl Seuss Mask Aligner 55 with 10 mW/cm² intensity for an exposure time of 12.5 seconds, giving an energy density of 125 mJ/cm². The samples were developed in CD26 for 2.5 minutes, wafted back and forth in a wafer wand to ensure development even in between small features. The samples were then rinsed for 5 minutes in deionized water, oxide etched in 1:10 HCl:H₂O, rinsed again in water, and loaded in the Nano38 PVD evaporator for Au/Zn/Au (20 nm/20 nm/500 nm) front contacts. Excess metal was lifted off in Remover PG overnight, after which the samples were washed with deionized water and inspected under an optical microscope.

Lithography was then performed to isolate the devices, using HMDS applied as it was above, followed by S1827 applied during the 500 RPM spin and baked for 1 minute at 115 °C. The samples were taken to the Karl Seuss Mask Aligner again, this time with a 10 mW/cm² exposure for 18 seconds, or ran energy density of 180 mJ/cm². The samples were again developed in CD26 for 2 minutes, then rinsed in deionized water. Afterwards, the samples were dipped in 3:4:1 H₃PO₄:H₂O₂:H₂O to etch the GaAs contact, concentrated HCl to etch the InGaP window, 3:4:1 again to etch the GaAs p-i-n junction,
and concentrated HCl to remove the back etch stop. The sample was then submerged for 2 minutes in acetone, 2 minutes in another beaker of acetone, and 2 minutes in isopropyl alcohol in order to strip the resist and clean the wafers. The contact etch was then performed, using 2:1:50 of NH₄OH:H₂O₂:H₂O, followed by a rinse in deionized water. The front surface of the wafers were coated in S1827 to protect the wafer surface and baked on a hotplate at 130 °C for 1 minute. The back of the wafer was dipped in 1:10 HCl:H₂O to remove oxide, then loaded in a Kurt J. Lesker PVD 75C thermal evaporator for Au/Ge/Ni/Au (25 nm/50 nm/35 nm/500 nm). After deposition, the photoresist was stripped in 2 minutes each of acetone/acetone/isopropyl alcohol. Then the samples were annealed at 407 °C (50 second soak at rim, 10 second push to heater zone of tube furnace, 6 minute bake, 10 second return to rim. 50 second soak at rim) for a total time of 8 minutes.

Figure 4.4 shows experimental best-cell J-V measurements without antireflection coatings, performed at AM1.5G using a TS Space Systems dual source solar simulator. The lamps were calibrated using InGaP and GaAs reference solar cells calibrated by NREL. The c-GaAs and poly-GaAs solar cells were compared to determine the effects of polycrystallinity on device performance, while the c-Ge and poly-Ge solar cells were compared to determine the effects of polycrystallinity and the effectiveness of a buffer layer on APD suppression. Quantified in Table 4.1, the GaAs solar cell grown on a c-GaAs substrate had a short-circuit current density (J_SC) of 19.3 mA/cm² and an open-circuit voltage (V_OC) of 1.04 V, consistent with historic baseline GaAs solar cells under AM1.5G. The solar cell grown on the poly-GaAs substrate had a comparable J_SC of 18.9 mA/cm², but exhibited a 100 mV drop in V_OC compared to the c-GaAs baseline. This drop in V_OC correlated with the fit for grain boundary recombination at 400 µm grain diameter, which is consistent with the grain size measured with electroluminescence and an IR camera. The solar cell grown on c-Ge exhibited the lowest J_SC and V_OC. While the low temperature GaAs buffer layer is supposed to provide good nucleation on arbitrary grain orientations,
Figure 4.4: Experimental J-V and modeled fit for the solar cells grown on the commercial c- and poly-GaAs and Ge substrates.

it did not work well on the (100) surface of the crystalline Ge substrate, resulting in a high APD density. Transmission electron microscopy performed at NREL was used to confirm the APD density at the buffer layer, indicating an APD density between 1.3-3x10^9 cm^-2 for growth on c-Ge. The APD density was sufficiently low for the growth on poly-Ge, which indicates that the combination of nucleation and buffer layers was successful for the polycrystalline substrate.

Table 4.1: AM1.5G J-V characteristics of the solar cells grown on c- and poly- GaAs and Ge substrates.

<table>
<thead>
<tr>
<th>Device</th>
<th>$J_{SC}$ (mA/cm²)</th>
<th>$V_{OC}$ (V)</th>
<th>$FF$</th>
<th>$\eta$ (exp)</th>
<th>$\eta$ (model)</th>
<th>$\eta$ (ARC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>c-GaAs</td>
<td>19.3</td>
<td>1.04</td>
<td>77.9%</td>
<td>15.6%</td>
<td>15.8%</td>
<td>21.5%</td>
</tr>
<tr>
<td>poly-GaAs</td>
<td>18.9</td>
<td>0.94</td>
<td>69.7%</td>
<td>12.4%</td>
<td>12.5%</td>
<td>16.5%</td>
</tr>
<tr>
<td>c-Ge</td>
<td>17.3</td>
<td>0.86</td>
<td>74.1%</td>
<td>11.0%</td>
<td>11.0%</td>
<td>14.8%</td>
</tr>
<tr>
<td>poly-Ge</td>
<td>19.4</td>
<td>0.89</td>
<td>68.8%</td>
<td>11.9%</td>
<td>12.5%</td>
<td>16.6%</td>
</tr>
</tbody>
</table>

These devices were measured with spectral responsivity (SR) over a wavelength range of 400-1,000 nm in order to calculate EQE. Figure 4.5 shows the best-cell EQE measurements of the four devices. All devices show slight loss in EQE near 650 nm due to the InGaP window. The (In)GaAs cells also show a slight absorption edge red-shift compared to GaAs due to the decrease in bandgap when 1% In was incorporated to lattice match epilayers to the poly-Ge substrate. The GaAs solar cell grown on a c-GaAs substrate had the highest EQE due to high material quality and an optimized design. The GaAs solar cell
grown on a poly-GaAs substrate showed similarly high EQE since grain boundaries affect $V_{OC}$ more than $J_{SC}$. The (In)GaAs solar cell grown on the poly-Ge substrate showed higher EQE than the cell on the c-Ge substrate, indicating suppressed APD formation over a greater number of crystal orientations using the low temperature nucleation layer and thick buffer layer. However, the EQE for (In)GaAs grown on c-Ge would have closely approached that of GaAs grown on c-GaAs had the design instead been optimized for the (100) orientation and $6^\circ$ offcut of the specific monocrystalline Ge substrate.

![Experimental QE and modeled fit for the solar cells grown on the commercial c- and poly-GaAs and Ge substrates.](image)

Figure 4.5: Experimental QE and modeled fit for the solar cells grown on the commercial c- and poly-GaAs and Ge substrates.

Table 4.2 quantifies the grain size, effective emitter and base MCDLs, and saturation current density $J_{01}$ that reflects recombination in the emitter and base, extracted from the fit. For the growths on GaAs, the effective emitter MCDL and base MCDL appear to be the same, indicating good material quality throughout the growth. However, the $J_{01}$ term is larger for the solar cell on poly-GaAs, which is reflected in the lower $V_{OC}$. For the growths on Ge, however, the emitter MCDL is larger in both cases in the emitter than in the base, which indicates that there is a presence of APDs in the base of both cases that self-annihilate before reaching the emitter. The $J_{01}$ term for the growths on Ge are also larger than the $J_{01}$ for the growths on GaAs, which is confirmed by the lower $V_{OC}$ exhibited by both cells compared to the GaAs baselines.
Table 4.2: Material parameters for the modeled fit and diode characteristics of the solar cells grown on c- and poly-GaAs and Ge substrates.

<table>
<thead>
<tr>
<th>Device</th>
<th>Grain Size (μm)</th>
<th>Effective Emitter MCDL(μm)</th>
<th>Effective Base MCDL(μm)</th>
<th>J₀₁ (mA/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>c-GaAs</td>
<td>-</td>
<td>1.6</td>
<td>1.6</td>
<td>9.5 × 10⁻²¹</td>
</tr>
<tr>
<td>poly-GaAs</td>
<td>400</td>
<td>1.4</td>
<td>1.4</td>
<td>1.2 × 10⁻²⁰</td>
</tr>
<tr>
<td>c-Ge</td>
<td>-</td>
<td>0.9</td>
<td>0.1</td>
<td>8.2 × 10⁻²⁰</td>
</tr>
<tr>
<td>poly-Ge</td>
<td>200</td>
<td>1.3</td>
<td>0.6</td>
<td>2.2 × 10⁻²⁰</td>
</tr>
</tbody>
</table>

4.3 Photoluminescence Test Structures on Polycrystalline and Monocrystalline Substrates

The solar cell results on commercial c-Ge and poly-Ge substrates indicated the necessity for optimal nucleation layer conditions in order for the power conversion efficiency and quantum efficiency to more closely approach those of the c-GaAs solar cells. Two nucleation layer materials are explored in the following sections: a 25 nm high-temperature InGaP layer and a 25 nm low-temperature GaAs layer. Photoluminescence of these two nucleation layers over a variety of temperatures is then directly compared to inform the nucleation layer conditions for solar cell growth in Section 4.4.

4.3.1 High Temperature InGaP Nucleation Layers

Figure 4.6a shows the double heterostructures grown for this study on c-Ge substrates, as well as a c-GaAs substrate for a baseline comparison. The two test structures are analogous, where the main differences include a 25 nm InGaP nucleation layer, thicker buffer layer, and 1% In to lattice match (In)GaAs for the Ge substrate compared to the GaAs substrate. Alₐ₀.₃₂Ga₀.₆₈As/In₀.₀₁Ga₀.₉₉As/Al₀.₃₂Ga₀.₆₈As double heterostructures were grown on the three substrates in an Aixtron 3x2” MOCVD system. Prior
to growth, the samples were annealed in hydrogen at 700 °C for 10 minutes inside the chamber. Standard precursors were used for growth, including TMGa, TMIn, trimethylaluminum (TMAI), and AsH₃, and the (In)GaAs emission layer was lightly p-type doped with DEZn to enhance photoemission. Three nucleation layer temperatures (630 °C, 650 °C, and 670 °C) were analyzed, after which the growth proceeded at the same temperatures as the c-GaAs baseline (685 °C for the Alₐ₀.₃Ga₁₀.₆As layers and 650 °C for the remainder of the growth). Figure 4.6b shows photoluminescence from the GaAs baseline and the three temperatures (630 °C, 650 °C, and 670 °C) for the 25 nm InGaP nucleation layer. The GaAs baseline shows a 3.5x increase of photoluminescence (PL) intensity compared to the highest PL intensity from the double heterostructures on Ge.

Figure 4.6: a. Layer structure of analogous double heterostructures on c-GaAs or c-Ge substrates. b. Photoluminescence signal from the GaAs baseline and the three temperatures (630 °C, 650 °C, and 670 °C) for the 25 nm InGaP nucleation layer.

In order to analyze the discrepancy of the high GaAs PL intensity compared to the lower PL intensity on Ge substrates, in-situ temperature and stress measurements were analyzed, shown in Fig. 4.7 as a function of growth time. The colors correspond with the color scheme of the layers shown in Fig. 4.6. The Al₀₃Ga₀₆As barriers seem to introduce stress that continues into the In₀.₀₁Ga₀.₉₉As active region for samples on c-Ge substrates, which can be seen by an increase in curvature after the first AlGaAs barrier. While 100 nm of Al₀₃Ga₀₆As is well below the critical thickness of the material, these layers were decreased from 100 nm to 50 nm for the following low-temperature GaAs nucleation layer study.
4.3.2 Low-Temperature GaAs Nucleation Layer

Double heterostructures with a low-temperature GaAs nucleation layer were then grown to compare the material quality of the double heterostructures to those of the prior study. The substrates considered included commercial Ge(001), commercial polycrystalline Ge with 200 μm sized grains, and Ge substrates prepared through AIC. A temperature study was performed from 500 °C to 600 °C of a low-temperature GaAs nucleation layer, where this layer was expected to improve performance of growth on polycrystalline Ge substrates [99].

To prepare the AIC samples, the best conditions from Chapter 3 were recreated. 500 nm of SiO$_2$ was thermally grown on a 2 inch n-type Si(111) substrate from Wacker-Chemitronic using a Bruce diffusion furnace. Al and Ge were successively deposited with a thickness of 200 nm each, using a Kurt J. Lesker PVD 75C thermal evaporator. The samples were annealed in a Lindbergh Blue M tube furnace at a temperature of 380 °C for 50 hours at atmospheric pressure and a N$_2$ flow of 500 sccm. The temperature ramps to and from ambient temperature were controlled using a Eurotherm 2704 temperature controller at 1 °C/s. Post-anneal Al etching was then performed in a solution of concentrated HCl for 6 hours to remove the residual Al.
\( \text{Al}_{0.32}\text{Ga}_{0.68}\text{As/In}_{0.01}\text{Ga}_{0.99}\text{As/Al}_{0.32}\text{Ga}_{0.68}\text{As} \) double heterostructures were grown on the three substrates in an Aixtron 3x2” MOCVD system. Prior to growth, the samples were annealed in hydrogen at 700 °C for 10 minutes inside the chamber. Four temperatures were explored for the initial GaAs nucleation layer: 500 °C, 520 °C, 550 °C, and 600 °C, which were verified with in-situ thermocouple measurements. The subsequent \( \text{In}_{0.01}\text{Ga}_{0.99}\text{As} \) layers were grown at 650 °C, while the \( \text{Al}_{0.32}\text{Ga}_{0.68}\text{As} \) layers were grown at 685 °C. Baseline comparisons were grown on (100) p-type crystalline Ge (c-Ge) substrates with a 6° offcut towards <111> as well as a commercial polycrystalline Ge (poly-Ge) substrate with preferential (111) orientation and approximately 200 \( \mu \text{m} \) average grain size. The AIC samples were characterized with a field emission scanning electron microscope (FESEM) using a Bruker EDS detector to understand the sample surface morphology and material diffusion. EBSD was performed using the Hikari detector from EDAX at operating conditions of 15 kV, 1.4 nA, and a 10 mm working distance. PL measurements were taken on all samples using a 532 nm laser with a power density of 14.4 W/cm\(^2\) and a Princeton Acton SpectraPro SP-2300 monochromator with 2 \( \mu \text{m} \) front slit size and 1.42 \( \mu \text{m} \) back slit size, equipped with a thermoelectrically cooled Si photodiode.

Figure 4.8 shows a secondary electron SEM image of the polycrystalline Ge samples prepared by AIC after Al removal, and Fig. 2b shows the same image with an EDS map overlay. As can been seen, the film has a high Ge content with only trace amounts of Al. As well, a compact Ge film was observed with 91.6% coverage on the surface, where the 1 \( \mu \text{m} \) sized pores down to the Si/SiO\(_2\) substrate are a result of residual Al that remained from the initial deposition. Figure 4.8c shows EBSD results, where an average grain diameter was found to be approximately 620 nm, and the inverse pole figure indicate no preferential crystal orientation. The grain size and orientation from these AIC Ge substrates is consistent with similar annealing conditions reported by other groups, where improved grain size and crystal orientation uniformity can be achieved in future work with lower annealing temperature, longer annealing time, and breaking vacuum between the Al and Ge depositions [63].
Figure 4.8: Characterization of the 200 nm polycrystalline Ge samples using a.) SEM that revealed a compact film with $\sim 1 \mu m$ sized pores, b.) EDS mapping that indicated that the film is Ge with minimal Al remaining post-etch., and c.) EBSD measurements indicating an average of 620 nm sized randomly oriented grains. © IEEE 2018

Figure 4.9 shows the layer structure for the $\text{Al}_{0.32}\text{Ga}_{0.68}\text{As/In}_{0.01}\text{Ga}_{0.99}\text{As/Al}_{0.32}\text{Ga}_{0.68}\text{As}$ double heterostructure grown on all substrates in this study, where the temperature of the 25 nm GaAs nucleation layer was varied to observe the effects on the material quality of the active region. The combination of the low-temperature nucleation layer and thick buffer layer are intended to both suppress the effects of polycrystallinity and allow APDs to self-annihilate [99]. Each run contained one Ge(001) wafer, one commercial poly-Ge wafer, and one AIC poly-Ge wafer.

Figure 4.9: Layer structure of the double heterostructure with 25 nm low-temperature GaAs nucleation layer grown on all Ge substrates.

Figure 4.10 shows images of the surface of each of the samples post-growth using an optical microscope with a Nomarski prism. From the growth on Ge(001), triangular surface defects can be observed.
at 500 °C, which decrease in density as the temperature increases up to 550 °C. For a 600 °C nucleation layer, however, the surface becomes very rough and there is a clear degradation in material quality as observed by photoluminescence. The double heterostructures grown on AIC poly-Ge showed uniform surface morphology both across the wafer as well as run-to-run, suggesting a level of insensitivity to nucleation layer temperature. The double heterostructures grown on commercial poly-Ge showed drastically different surface morphology depending on the orientation of the grains.

![Figure 4.10: Optical microscopy taken with a Nomarski prism of the surface of the Al_{0.32}Ga_{0.68}As/In_{0.01}Ga_{0.99}As/Al_{0.32}Ga_{0.68}As double heterostructures grown on monocrystalline Ge, commercial polycrystalline Ge, and polycrystalline Ge made through the AIC process. The temperatures listed indicate the temperature of the GaAs nucleation layer, where all other growth conditions were identical run-to-run. © IEEE 2018](image)

Figure 4.11 shows the photoluminescence from the Al_{0.32}Ga_{0.68}As/In_{0.01}Ga_{0.99}As/Al_{0.32}Ga_{0.68}As double heterostructure grown on the Ge(001), commercial poly-Ge, and AIC poly-Ge substrates, where all samples were measured at the same time and under the same conditions. The PL intensity from the double heterostructure grown on Ge(001) in Fig. 4.11a shows a high dependence on nucleation layer temperature. The highest peak intensity was observed from the samples with nucleation layers grown at 500 °C and 550 °C. It should be noted that of the four samples, only the 500 °C sample was a full 2 inch
wafer, where the others wafers were half of a 2 inch wafer, meaning that a larger region without edge effects may have artificially raised the PL intensity of the 500 °C nucleation layer sample. As expected from the rough surface morphology observed in Fig. 4.10, the sample with the 600 °C nucleation layer demonstrated the lowest PL intensity.

Figure 4.11: Photoluminescence of the Al$_{0.32}$Ga$_{0.68}$As/In$_{0.02}$Ga$_{0.99}$As/Al$_{0.32}$Ga$_{0.68}$As double heterostructures with GaAs nucleation layers grown at different temperatures on a. Umicore Ge(001) and b. Umicore poly-Ge substrates, where three regions on each sample were surveyed to determine a range of PL intensities across different crystal orientations, and c. AIC poly-Ge substrates. The samples were all measured at the same time, under the same conditions. © IEEE 2018

Figure 4.11b shows the PL from the double heterostructures grown on commercial poly-Ge, where three regions were chosen on each sample to survey a wider array of grain orientations. For these samples, a trend in growth conditions may still be observed, particularly since the samples with the 600 °C nucleation layer are clustered with consistently low PL intensity; however, the more dominant effect is the range of PL intensity from different grain orientations. This result is attributed the ability of specific grain orientations or offcuts to suppress APDs [42], where a high density of these defects would reduce the minority carrier lifetime and subsequently the photoluminescence intensity. Figure 4.11c shows the PL intensity from the AIC poly-Ge substrate, where each sample is nearly identical both across the wafer and from run-to-run, indicating that changes in nucleation layer temperature within a range of 100 °C play a minor role in a sample with grain size below 1 µm. This implies that the substrates are a larger barrier to high PL intensity than the growth, where larger grain size and more
uniform grain orientation are expected to improve PL intensity.

AIC substrates were developed with 620 nm average grain size and arbitrary grain orientation. Double heterostructures were grown on these substrates as well as baselines consisting of commercial poly-Ge and monocrystalline Ge(001) substrates. The temperature of the initial GaAs nucleation layer was varied between 500 °C and 600 °C to determine which growth conditions gave the best material quality. The growths on Ge(001) substrates with a 6° offcut towards <111> showed high PL intensity, particularly at nucleation layer temperatures of 500 °C (the only full 2 inch wafer) and 550 °C (the smoothest surface morphology). The photoemission on the Ge(001) substrates was very dependent on the nucleation layer. However, the more dominant variable for the commercial poly-Ge samples was the orientation of the grains, where large variations in both surface morphology and PL can be observed in different regions of the sample. The uniformity was very consistent in the AIC poly-Ge samples, both across different points on the wafer and between samples. This indicates that the photoemission is limited by grain size, which will need to be enhanced in future work.

4.3.3 Comparison of GaAs and InGaP Nucleation Layers

The PL emission from the above InGaP and GaAs nucleation layer studies are compared directly in Fig. 4.12, where the double heterostructure layer structures are shown in Figs. 4.6a and 4.9. The double heterostructure with a GaAs nucleation layer that were grown in a temperature range between 500-550 °C demonstrates stronger PL emission that those with the InGaP nucleation layers grown between 630-670 °C.

While the PL emission increases for the GaAs nucleation layers at increasingly low temperatures, the PL emission conversely increases for the InGaP nucleation layers at increasingly high temperatures. The low-temperature GaAs nucleation layers appeared to give the highest PL signal, and temperatures much lower than 500 °C are expected to have negative consequences on the growth. These effects may
manifest as rough surfaces in the regime where Ga atoms have insufficient kinetic energy to move to the correct spot on the lattice. To further optimize the InGaP nucleation layer, higher temperatures may continue improving the PL emission based on the results between the nucleation layer grown at 670 °C compared to 650 °C.

### 4.4 Solar Cells Grown on Commercial Monocrystalline, Commercial Polycrystalline, and AIC Polycrystalline Substrates

After the development of the substrates described in Chapter 3 and the development of nucleation layers described above, the next step was to grow solar cells on these templates. Many research groups have studied AIC for both Ge and Si photovoltaic applications, where Si solar cell efficiency records on AIC substrates have reached 8% efficiency on p-type substrates and 2.9% on n-type substrates [57] [56]. For AIC of Ge, grain size greater than 100 µm has been achieved with an IQE of 70% under 1 V bias [58].
This section explores the one-sun and concentrated performance of GaAs solar cells grown on AIC Ge, poly-Ge from Umicore with 400 $\mu$m grain size, and c-Ge from Umicore with a (100) orientation and a 6° offcut to the (111) plane.

For preparation of the AIC Ge substrates, 2” Si wafers with a thickness of 280 $\mu$m were RCA cleaned and then transferred to a Bruce diffusion furnace for 500 nm thermally grown SiO$_2$ at 1000 °C. Subsequent layers of 200 nm Al and 200 nm amorphous Ge were deposited using a Kurt J Lesker PVD 75C thermal evaporator. The samples were then placed in a Lindbergh Blue M tube furnace with a 4” quartz tube, a Eurotherm 2704 temperature controller, and a General Electric 5KCR 47UG26T vacuum pump. After pump-purging the chamber from 10 Torr to 760 Torr twice at room temperature with a nitrogen flow of 500 sccm, the samples were annealed for 50 hours at 760 Torr and a temperature of 375 °C using the same 500 sccm nitrogen flow as the pump-purge and a 1 °C/s ramp rate to and from the anneal temperature. After annealing, the samples were placed in a 5-hour HCl bath, which selectively etches the Al that has diffused to the top of the Ge layer at a rate of 0.96 nm/min. Characterization of the substrate was performed using a TESCAN-MIRA SEM at 10 kV, a working distance of 13.78 mm, and a magnification of 5 kx. Complimentary EDS mapping was performed in the same area as the secondary electron SEM image using a Bruker EDS attachment. Figure 4.13 shows both the secondary electron SEM image and the overlaid EDS map of the surface of the Ge samples after the 50 hour anneal and 5-hour concentrated HCl bath. In the EDS map, red indicates the presence of Al, green indicates Ge, and blue indicates Si. Some Al signal is still observed in the EDS map due to residual Al from diffusion that creates a p-type Ge film with doping around $10^{21}$ cm$^{-3}$. The Ge film is compact, but $\mu$m-sized islands and pores can be noted in the film as a result of the diffusion process. Substrate quality may be enhanced in future work by using an H$_2$O$_2$ etch to remove Ge islands prior to the etch that removes the Al layer [23].

Figure 4.14 shows $2\theta$-$\omega$ XRD scans from 20°-100°, both before and after etching the Al layer, in
order to better understand the crystallinity of the substrates. XRD of these samples was performed using a Rigaku SmartLab with a Cu Kα source, a Ni filter, and a 5° incident and receiving Soller slit. A rocking curve was performed prior to the scan to ensure alignment with respect to the film, which was oriented slightly off of the Si(111) substrate. The presence of Ge (111), (220), (311), and (224) peaks confirm that the Ge layer is polycrystalline. The pre-etch sample showed Al (111) and (222) peaks, indicating strong preferential crystal orientation in the Al layer, and the disappearance of those peaks after the HCl bath confirms that the Al was removed.

Two epi-ready substrates were also used in this work as baselines: a p-type (100) c-Ge substrate with a 6° offcut to the (111) plane from Umicore, and a p-type poly-Ge substrate with around 400 µm average grain size. Solar cells were grown on all substrates with an AIXTRON close-coupled showerhead MOCVD reactor and standard precursors were used in the growth including TMGa, TMIn, AsH₃, and PH₃ for alkyl and hydride sources. Doping was accomplished using disilane (Si₂H₆) for n-type materials and either DEZn or carbon tetrachloride (CCl₄) for p-type materials. Figure 4.15 shows the layer structure of the solar cell that was then grown on these substrates. A top-top contact solar cell structure was necessary because of the insulting 500 nm SiO₂ layer between the recrystallized Ge film.
Figure 4.14: 2θ-ω XRD scans of the AIC Ge samples after the 50 hour anneal, both before and after the HCl etch to confirm completeness of the etch and crystallinity of the Ge substrate prior to growth. © IEEE 2019

and the Si substrate. The substrates were annealed in H₂ at 700 °C prior to initiating growth, after which the temperature was adjusted to 550 °C for the GaAs nucleation layer grown 2 µm thick to minimize the effects of APDs. The growth temperature was then increased to 575 °C for the In₀.₀₁Ga₀.₉₉As:C lateral conduction layer, which was used for lateral electrical transport to the back contacts. The rest of the n-i-p In₀.₀₁Ga₀.₉₉As solar cell was grown at 650 °C.

The mask design for the 2” AIC solar cells is shown in Fig. 4.16. The largest five cells on the mask are 1x1 cm² cells with 0.04 cm² grid shadowing, which yields an active area 0.96 cm². The next largest cells had an active area of 0.21 cm². Within the same unit as the two 0.21 cm² cells, there are six cells with an active area of 0.0062 cm², two cells with an active area of 0.0025 cm², and two cells with an active area of 0.0023 cm². Finally, the mask contains circle and square diodes with equivalent lateral diameter of 1,000 µm, 800 µm, and 600 µm. The square diodes had active areas of 0.0090 cm², 0.0055 cm², and 0.0028 cm². The circle diodes had active areas of 0.0066 cm², 0.0040 cm², and 0.0020 cm². The top-top contact GaAs solar cells on AIC Ge substrates were fabricated using standard III-V processing and lithographic techniques. Both the front and back contacts were created with a gold
Figure 4.15: Layer structure of the \textit{n-i-p} top-top contact In$_{0.01}$Ga$_{0.99}$As solar cell grown on an AIC substrate.

electroplating solution.

Current-density vs. voltage (J-V) measurements were performed using an XT-10 solar simulator for AM1.5G measurements and a High Intensity Pulsed Solar Simulator (HIPSS) for concentration measurements. Figure 4.17 shows 1-sun J-V curves at AM1.5G for the solar cells grown on Umicore c-Ge, Umicore poly-Ge, and AIC Ge substrates. The solar cells on Umicore c-Ge and poly-Ge had active areas of 0.1 cm$^2$, while the solar cells on AIC Ge had solar cell active areas ranging from 0.28 mm$^2$ to 0.96 cm$^2$. The AIC solar cells between 0.02-0.21 cm$^2$ showed both higher J$_{SC}$ and V$_{OC}$ for smaller device size. The maximum V$_{OC}$ of these cells is 0.17 V, which approaches the V$_{OC}$ range of 0.2-0.4 V for the Umicore poly-Ge cells with grain size around 400 µm. The AIC solar cells between 0.28-0.9 mm$^2$ also showed higher J$_{SC}$ and V$_{OC}$ for smaller device size with respect to others within that set. Between the two sets of different solar cell size, higher J$_{SC}$ is observed in the 0.28-0.9 mm$^2$ cells because the grids are closer together, which allows more carriers to be collected. However, the higher V$_{OC}$ is observed in the 0.02-0.21 cm$^2$ devices since the smaller 0.28-0.9 mm$^2$ cells experience a larger
perimeter/area ratio. Considering the baseline poly-Ge solar cells fabricated on large-grain Umicore substrates, much higher $J_{SC}$ is observed in the range of 13.6 to 17.1 mA/cm$^2$ than the AIC Ge solar cells since the latter experiences more grain boundary recombination due to the smaller grain size by several orders of magnitude. The $V_{OC}$ for the poly-Ge solar cells shows a wide distribution depending on the number of grain boundaries in each cell and the roughness of the growth on each grain. The $V_{OC}$ is also low due to degradation of Ge substrates with time, where higher $V_{OC}$ (0.89 V) was achieved on these substrates in prior work [100]. The J-V characteristics of the solar cell grown on the c-Ge substrate approach the efficiency of a standard GaAs solar cell.

Figure 4.18 shows quantum efficiency measurements for the solar cells grown on Umicore c-Ge, Umicore poly-Ge, and AIC Ge substrates. The extracted AM1.5G $J_{SC}$ of the AIC cell is 0.14 mA/cm$^2$, which falls within the range of measured data. The jump in the data at 550 nm indicates the point at which the grating on the monochromator changed. The EQE of the c-Ge is shown in black, while the EQE of the poly-Ge cells is shown in color. All of the poly-Ge EQE looks similar for shorter
Figure 4.17: 1-sun J-V curves for the solar cell on a Umicore c-Ge substrate (top graph, black), Umicore poly-Ge substrate (top graph, colored), and AIC Ge (bottom two graphs, correlated to the color of the boxes surrounding the perimeter of the cells on the schematic to the right). © IEEE 2019

wavelengths, but shows substantial degradation in the base for some of the cells correlating with the number of grain boundaries and orientation. This highlights the importance of minimizing APDs or other defects that can occur near the base, but then recover towards the top of the cell.

Figure 4.19 shows concentration measurements for the best solar cells from Fig. 4.17 grown on Umicore c-Ge, Umicore poly-Ge, and AIC Ge substrates. While the c-Ge solar cell shows higher current with increasing concentration, the solar cell efficiency decreases with increased concentration due to decreasing fill factor attributed to series resistance. The Umicore poly-Ge efficiency increases at first due to enhancements in fill factor, but then decreases near 136 suns due to series resistance. The AIC Ge cell constantly increases in all metrics with concentration, with a $V_{OC}$ range of 0.17-0.4 V, $J_{SC}$ range of 0.12-7.9 mA/cm$^2$, and efficiency range of 0.0063-0.023%. The recovery in $J_{SC}$ can be attributed to state-filling of defects since the higher concentration saturates non-radiative recombination centers in the device [101]. The $V_{OC}$, FF, and efficiency are plotted for all three cells in Fig. 4.19 as a function of concentration.
4.5 Conclusions

In this chapter, we first evaluated ideal cases of polycrystalline GaAs and Ge substrates with 200-400 \( \mu \)m grain size to better understand how polycrystallinity and APD density affect \( J_{SC} \), \( V_{OC} \), \( J_{01} \), and MCDLs. This study indicated the need to further develop the nucleation layer for growth on polycrystalline and monocristalline Ge, since the quality of the first layer nucleated on the substrate can determine the quality of the subsequent layers. Both nucleation layer temperature and material (InGaP or GaAs) were investigated. This study indicated that a low-temperature GaAs layer yielded better material quality than a high-temperature InGaP layer for growth on c-Ge, but that InGaP nucleation layers at higher temperatures should be explored in future work since the PL intensity continued to increase up to 670 \( ^\circ \)C. Meanwhile, the low-temperature GaAs nucleation conditions had minimal effect on the AIC samples since grain size was the major limitation. Finally, solar cells were grown on the AIC Ge substrates along with Umicore poly-Ge and c-Ge substrates as baselines. The solar cells on AIC Ge substrates showed
Figure 4.19: Concentrated J-V curves of the solar cells on AIC Ge (top left), Umicore poly-Ge (top right), and Umicore c-Ge (bottom left), as well as suns-$V_{OC}$ data (bottom right). © IEEE 2019

$V_{OC}$ up to 0.17 V, which is comparable to the lower end of the range of $V_{OC}$ for the Umicore poly-Ge baselines. The $J_{SC}$ of the solar cells on AIC Ge was low, but likely due to limitations from the grain size. Future AIC templates that are able to exhibit larger grain size and more uniform crystal orientation are projected to have better solar cell performance as demonstrated by those on the Umicore poly-Ge substrates.
Chapter 5

Remote Epitaxy Through 2D Graphene

5.1 Introduction

The previous sections have discussed in detail methods to create polycrystalline Ge films and optimize MOCVD growth on polycrystalline and monocrystalline Ge. In contrast, this chapter focuses on remote epitaxy, a technique to reuse epi-ready monocrystalline GaAs substrates by exploiting the weak van der Waals bond between graphene and the semiconductor in order to act as a release layer for substrate reuse. This substrate reuse technique is then coupled with dynamic-hydride vapor phase epitaxy (D-HVPE), which is a potentially lower-cost growth technique for III-V materials. These two techniques offer an attractive combination to collectively lower both the substrate and epitaxy costs. The growth conditions using nitrogen carrier gas in the D-HVPE first needed to be studied, since hydrogen carrier gas has been seen to etch graphene. Record GaAs growth rates were observed as a result of this optimization, approaching 530 \( \mu \text{m/hour} \) using nitrogen carrier gas and 400 \( \mu \text{m/hour} \) using hydrogen carrier gas and otherwise equivalent growth conditions. After calibrating the growth rate and material quality of GaAs and InGaP layers grown with the nitrogen carrier gas, annealing and initial growth experiments were
performed on graphene.

5.2 Growth Conditions Using Nitrogen Carrier Gas

D-HVPE has attracted significant attention for its potential as a lower-cost III-V growth technique due to the use of elemental group III precursors, high utilization of metals and hydrides, and ultrafast growth rates that would enable high throughput in production-line reactors [102] [7]. D-HVPE enables high-quality heterointerfaces due to its distinguishing ability to rapidly transfer substrates between multiple growth chambers, as demonstrated by the growth of Esaki diodes [103] [102] and multijunction solar cells [104] [105]. In addition to demonstrating device performance on par with traditional epitaxy techniques, D-HVPE has produced high III-V material growth rates exceeding 300 µm/hour while maintaining solar cell open-circuit voltage above 1.04 V [12].

HVPE of III-V arsenide/phosphide materials is most commonly conducted using H\(_2\) carrier gas, but there are potential benefits to the utilization of a less reactive carrier gas such as N\(_2\) or Ar since H\(_2\) is both highly flammable and comparatively more expensive. Additionally, H\(_2\) has been shown to etch graphene if there is any oxygen present [106], which makes H\(_2\) potentially incompatible as a carrier gas for remote epitaxy. Several groups have demonstrated HVPE growth with inert carrier gases such as N\(_2\) or Ar [107] [108] [109] [110] [111]; however, using an inert carrier gas in a regime where arsenic vapor (As\(_x\)) is the dominant group V species was shown to lower the growth rate compared to H\(_2\) [110] [111]. These lower growth rates would negatively affect throughput in production and are attributed to the different reaction mechanisms leading to GaCl reduction, which is the rate-limiting step to GaAs growth by HVPE [112] [113]. Specifically, the mechanism typically attributed to GaAs growth in an As\(_x\) regime, is

\[
GaCl + \frac{1}{4}As_4 + \frac{1}{2}H_2 \rightarrow GaAs + HCl, \tag{5.1}
\]
where \( H_2 \) participates as a reactant to reduce GaCl to form the byproduct HCl \[107][110][111]\. In the absence of \( H_2 \) in the \( As_x \) regime, GaCl reduction must occur through an alternative mechanism. The proposed mechanism for GaAs growth in this case is

\[
3\text{GaCl} + \frac{1}{2}\text{As}_4 \rightarrow 2\text{GaAs} + \text{GaCl}_3,
\] (5.2)

in which GaCl is reduced by a slower mechanism that converts three GaCl into volatile GaCl\(_3\) \[107][114]\. The carrier gas plays no direct role in the reaction in this mechanism. For disproportionately large amounts of group III precursors, this reaction mechanism can yield higher GaAs growth rates with N\(_2\) compared to the case of H\(_2\) carrier gas \[114]\. Otherwise, it becomes statistically improbable to assemble three GaCl molecules to create GaCl\(_3\), leading to the observed lower growth rate with N\(_2\) due to these kinetic limitations.

Recent HVPE work has demonstrated a “hydride-enhanced” regime in which a significant amount of uncracked AsH\(_3\) reaches the wafer surface, resulting in much higher growth rates compared to the As\(_x\) regime due to a lower kinetic barrier to growth \[107]\. Surface GaCl must again be reduced in the hydride-enhanced regime, but hydrogen from decomposing AsH\(_3\) is presumed to be more reactive than molecular H\(_2\), thereby driving enhancement of the growth rate. While the reaction equation Eq. 5.1 employs H\(_2\) as a reactant in an arsenic-rich growth regime, the hydride-enhanced growth mechanism features H\(_2\) as a product,

\[
\text{GaCl} + \text{AsH}_3 \rightarrow \text{GaAs} + \text{HCl} + \text{H}_2.
\] (5.3)

The hydride-enhanced regime enables deposition of GaAs through a mechanism that does not depend on the carrier gas as a reactant \[115]\, which has the potential to overcome previous limitations on the growth rate using inert carriers observed in the As\(_x\) regime.
In this work, we compare the growth of GaAs in the hydride-enhanced regime using H₂ and N₂ carrier gases. We find that the growth rate is in fact higher under N₂ compared to H₂ using conditions that limit the decomposition of AsH₃. Under conditions favoring a high degree of AsH₃ decomposition, however, lower growth rates are observed in N₂ compared to H₂, in agreement with the prior literature. We demonstrate growth rates up to 528 µm/h using N₂ carrier gas, and up to 400 µm/h using H₂ carrier gas. We used computational fluid dynamics (CFD) modeling to understand the effect of carrier gas on the thermal profile and the resulting extent of AsH₃ decomposition inside a simplified reactor geometry. Our modeling suggests that the lower thermal conductivity of the N₂ decreases the internal reactor temperature compared to H₂, thus reducing the likelihood of AsH₃ decomposition before reaching the substrate and enhancing the GaAs growth rate.

All materials were grown in a dual-chamber D-HVPE reactor, where complete details can be found in Ref. [116]. GaCl and InCl were formed in-situ by the reaction of anhydrous HCl over elemental Ga and In for the group III sources, and hydride gases were used for the group V source. The gas plumbing design is such that the carrier gas species can be either H₂ or N₂, but not a combination of both. We varied the extent of AsH₃ decomposition by varying the AsH₃ carrier flow rate, as in Ref [115]. Changes in the AsH₃ carrier flow rate (Q_{N₂}^{AsH₃} or Q_{H₂}^{AsH₃}) were offset by changes to carrier gas flows through other parts of the system to maintain constant partial pressures of reactant species. The reactor is heated in four independently controlled temperature zones: the two source zones in each growth chamber where the metal chlorides are formed were held at 800 °C for all experiments, while the two deposition zones where the substrate is located were held at 650 °C. All substrates used in this work were (100) GaAs substrates miscut 6° towards the (111)A plane. Growth rates were determined by either a contact profilometer to measure the height difference between the GaAs epilayers and a InGaP etch stop, or by cross-sectional SEM of an n-type GaAs epilayer doped with hydrogen selenide, grown directly on an undoped GaAs substrate.
The modeling shown in this work was performed with the commercially available computational fluid dynamics package CFD-ACE+ [117]. The 3D geometry used for these simulations is a simplified version of our reactor, consisting of a single growth chamber, shown in Fig. 5.1. Carrier gas flows through either a center tube as the carrier for AsH$_3$ or through an inlet that approximates the flows through the other parts of the reactor. The temperature was fixed at the reactor walls in the simulation to values of 800 °C at the source zone and 650 °C in the deposition zone, as in the deposition experiments. AsH$_3$ decomposition was modeled using data from Ref. [118] assuming the following irreversible, first order reaction:

$$AsH_3 \rightarrow \frac{1}{4}As_4 + \frac{3}{2}H_2$$ (5.4)

AsH$_3$ decomposition was assumed to occur only on the reactor surfaces, which was considered to be the dominant effect compared to gas phase decomposition.

We first performed a series of experiments to compare the GaAs growth rate under the hydride-enhanced mechanism using either H$_2$ or N$_2$ carrier gas. Previously, we demonstrated that a high Q$^{AsH_3}_{H_2}$ unlocks the hydride-enhanced regime by decreasing the amount of time that the AsH$_3$ spends at high temperature as it is injected into the reactor, which minimizes the likelihood of decomposition into As$_x$ [115]. In this study, we varied the GaCl partial pressure (P$_{GaCl}$) for both types of carrier gas while using the mass-flow controller maximum of 5000 sccm for either Q$^{AsH_3}_{N_2}$ or Q$^{AsH_3}_{H_2}$ in order to limit AsH$_3$ decomposition [12]. Figure 5.2a shows that the growth rates using both carrier gases linearly increase with increasing P$_{GaCl}$, resulting in GaAs growth rates up to 528 µm/h using N$_2$ carrier gas and 400 µm/h using H$_2$ carrier gas and otherwise equivalent growth conditions, as listed in the figure. GaAs growth rates for the samples grown with N$_2$ are significantly higher than those grown with H$_2$ under these hydride-enhanced conditions, in contrast to previous literature in the As$_x$ regime. Figure 5.2b shows the root mean square surface roughness ($R_q$) of this series. These samples were n-type GaAs grown.
Figure 5.1: Cross-sectional schematic of the single growth chamber modeled with CFD-ACE+. The temperature boundary conditions for the reactor walls were 800 °C applied to the walls at the source zone and 650 °C applied to the walls of the deposition zone. AsH₃ and the AsH₃ carrier gas were input through the center tube, while all other gases were input through the top inlet.

on nominally undoped GaAs substrates to ensure that any roughness could be directly attributed to the GaAs growth. R₉ for these samples stays below 1 nm as calculated from a 1 μm x 1 μm AFM scan, except for the highest growth rate 528 μm/h where R₉ is 2.08 nm, even though there was no attempt to optimize the growth conditions such as V/III ratio on our part. We suspect that the increase in R₉ at the higher growth rates is due to the decreasing V/III ratio as the P₆GaCl increases and the AsH₃ flow remains constant at the mass-flow controller maximum, shown in Fig. 5.2c. The surface morphology may become smoother at these high growth rates if more group V precursor were available. We also expect that these growth rates would continue to increase if the availability of AsH₃ did not become limiting, but these data represent the maximum growth rates we can achieve given our current mass-flow controllers for AsH₃ and AsH₃ carrier flow, which preclude our ability to adjust V/III ratio as we further increase GaCl.
Figure 5.2: a) GaAs growth rate as a function of GaCl partial pressure for both N₂ and H₂ carrier gasses, b) root mean square roughness $R_q$ as a function of growth rate, and c) V/III ratio as a function of growth rate, where GaCl was increased in this study while the AsH₃ and AsH₃ carrier flow mass-flow controller were at their maximum values. The black squares indicate data using a N₂ carrier gas and the red circles indicate data using H₂ carrier gas.

Next, we studied the effect of varying $Q_{N_2}^{AsH_3}$ and $Q_{H_2}^{AsH_3}$ to understand how the degree of AsH₃ decomposition affects the growth rate. In this experiment, we offset increases in $Q_{N_2}^{AsH_3}$ and $Q_{H_2}^{AsH_3}$ by decreasing carrier gas flow by an equal amount through other parts of the system to maintain constant reactant dilution for each data point. Figure 5.3 shows that at 500 sccm for $Q_{N_2}^{AsH_3}$ and $Q_{H_2}^{AsH_3}$, which is correlated to greater AsH₃ decomposition due to the longer dwell time in the reactor [115], that the growth rate of nitrogen is in fact lower than hydrogen (1.68 μm/hr compared to 5.4 μm/hr), in line with previous reports of growth in an inert carrier [111]. However, as $Q_{N_2}^{AsH_3}$ or $Q_{H_2}^{AsH_3}$ increase, the growth rate of the samples grown with N₂ becomes significantly higher than those grown with H₂, indicating
that \( \text{N}_2 \) is more effective at preventing \( \text{AsH}_3 \) decoposition than \( \text{H}_2 \).

We then performed CFD modeling to better understand the influence of the carrier gas on the extent of \( \text{AsH}_3 \) decomposition. In these simulations, we input carrier gas through a center tube to simulate \( \text{AsH}_3 \) flow, \( \text{Q}_{\text{N}_2}^{\text{AsH}_3} \), and \( \text{Q}_{\text{H}_2}^{\text{AsH}_3} \); and through a top inlet that approximates the flows through the rest of our reactor. The flow rates through the center tube in CFD-ACE+ were 65 sccm for \( \text{AsH}_3 \) and 2500 sccm for the carrier gas, while the flows through the top inlet were 7500 sccm for the carrier gas, 10 sccm for \( \text{GaCl} \), and 4 sccm for \( \text{HCl} \). These flows correspond to the actual flows used for the data points in Fig. 5.3 at 2500 sccm for \( \text{Q}_{\text{N}_2}^{\text{AsH}_3} \) and \( \text{Q}_{\text{H}_2}^{\text{AsH}_3} \). Figure 5.4 shows the modeled temperature distribution inside the growth chamber when using \( \text{H}_2 \) (left) or \( \text{N}_2 \) (right). In the \( \text{H}_2 \) case, the internal reactor temperature is initially low near both the top inlet and the first half of the center tube within the source zone, but eventually approaches the reactor wall boundary conditions of 800 \( ^\circ \text{C} \) in the source zone and is uniformly 650 \( ^\circ \text{C} \) throughout the deposition zone. In contrast, the temperature profile in the \( \text{N}_2 \) case is much cooler near the center of the reactor in the source zone, which allows the gas to remain cool as it enters the deposition zone. At 800 \( ^\circ \text{C} \), the thermal conductivity is 0.480 W/m·K for \( \text{H}_2 \), compared to 0.0694 W/m·K for \( \text{N}_2 \) [119], which greatly reduces heat transfer from the hot reactor walls in the
N₂ case. This effect decreases the temperature of the AsH₃ that flows through the center of the reactor, subsequently decreasing the likelihood of thermal decomposition.

Figure 5.4: CFD modeling of the temperature inside the simplified growth chamber using H₂ (left) or N₂ (right) carrier gas, where the lower thermal conductivity gas insulates the center tube from the hot reactor walls, thus keeping the gas at a lower temperature and minimizing the likelihood of thermal decomposition.

Figure 5.5 shows the partial pressures of As₄ and AsH₃ both as the species evolve down the length of the reaction chamber and as they appear at the plane of the substrate for the same simulation conditions used in Fig. 5.4. The higher effective reactor temperatures when using the H₂ carrier gas (as shown in Fig. 5.4) facilitate an increase in AsH₃ decomposition beginning in the source zone, which then leads to a greater partial pressure of As₄ in the deposition zone, shown in Fig. 5.5a (left). Figure 5.5b (left) displays a correspondingly high initial AsH₃ partial pressure in the H₂ case that decomposes significantly by the time it leaves the source zone. The remaining AsH₃ likely continues to decompose in the deposition zone due to the 4 cm²/s diffusion coefficient of AsH₃ in H₂ at 650 °C. In the N₂ case, a significant amount of AsH₃ reaches the substrate in the simulation shown in Fig. 5.5b (right), along with a much lower partial pressure of As₄ shown in Fig. 5.5a (right). AsH₃ only begins to decompose
as the reactor diameter expands, which may result from a corresponding decrease in gas velocity that increases the AsH$_3$ residence time in the reactor. Compared to H$_2$, the low thermal conductivity of N$_2$ likely prevents premature AsH$_3$ decomposition in the deposition zone, and the diffusion coefficient of 0.6 cm$^2$/s in the cooler 480 °C region in the center prevents AsH$_3$ from reaching the reactor walls to decompose except where the walls begin to expand. The diffusion coefficient of AsH$_3$ in the deposition zone increases to 1.1 cm$^2$/s near the 650 °C reactor walls, corresponding to the increase in temperature away from the center of the reactor. These simulations indicate that the low thermal conductivity of N$_2$ thermally insulates AsH$_3$ from the hot reactor walls to minimize thermal decomposition compared to H$_2$, and the lower diffusion of AsH$_3$ in N$_2$ decreases the likelihood that AsH$_3$ will decompose at the hot reactor walls.

The simulations above indicate that a higher concentration of AsH$_3$ reaches the wafer surface in a hydride-enhanced regime with N$_2$ than with H$_2$, for otherwise equivalent growth parameters, which enables the higher growth rates with N$_2$. The forward reaction mechanism in a hydride-enhanced regime is independent of the carrier gas species as shown in Eq. 5.3, which permits the achievement of high growth rates with either H$_2$ or N$_2$ as we observe. We also note that the presence of H$_2$ could drive the reverse of this reaction, which could suppress growth rate, although the large equilibrium constant for this reaction means that the reverse reaction is unlikely [120]. More likely, the growth rate using N$_2$ is higher due to enhanced preservation of AsH$_3$ as long as there is a sufficient GaCl supply. GaAs has a lower kinetic barrier to growth with AsH$_3$ than As$_x$ [115], and less AsH$_3$ decomposition occurs with the low thermal conductivity carrier gas, resulting in higher growth rates for a N$_2$ carrier gas compared to H$_2$.

However, for low $Q_{\text{AsH}_3}^{\text{N}_2}$, significant AsH$_3$ decomposition into As$_x$ occurs. In this case, As$_x$ is the predominant group V reactant, and H$_2$ participates as a reactant to enable higher growth rates compared to GaAs growth using conditions where this H$_2$ is absent. This explains both the decrease in growth
Figure 5.5: CFD modeling of a) As$_4$ partial pressure inside the growth chamber for H$_2$ (left) and N$_2$ (right), where more As$_4$ is generated with H$_2$ carrier gas, and b) AsH$_3$ partial pressure inside the growth chamber showing that more AsH$_3$ is delivered to the substrate with N$_2$. Cross-sectional views of the plane of the substrate are shown below, depicting the partial pressure of each species at the substrate position.

rate observed in Fig. 5.3 for decreasing Q$_{N_2}^{AsH_3}$ and Q$_{H_2}^{AsH_3}$, as well as the comparatively lower growth rate of 1.7 µm/h with N$_2$ and 5.4 µm/h with H$_2$ at the lowest carrier gas flows. As a result of these experiments, several conditions were explored for GaAs growth with N$_2$ carrier gas. Experiments were then performed on graphene to ensure that no etching or wrinkling occurred during anneals at growth temperature, and that the graphene was intact after growth of a GaAs nucleation layer.
5.3 Growth on Graphene-Coated GaAs

Graphene samples were prepared by the graphitization of silicon carbide (SiC) and dry transferred to a GaAs substrate. These graphene-coated GaAs samples were then annealed in the HVPE at our standard growth temperature of 650 °C in an environment with N₂ carrier gas and AsH₃ to determine if these conditions would etch or wrinkle the graphene. Two graphene-coated GaAs samples were annealed with either 2500 sccm or 500 sccm AsH₃ carrier gas flow, where carrier gas flow was adjusted in other parts of the reactor so the total carrier gas flow through the system was the same in both cases. As described above, the 2500 sccm AsH₃ carrier gas flow was meant to enhance AsH₃ delivery to the substrate, while the 500 sccm AsH₃ carrier gas flow was more likely to generate Asₓ and hydrogen species, which might have deleterious effects on the graphene.

Figure 5.6 shows SEM of the two graphene samples pre- and post-anneal. Graphene sample G1 was annealed with the 2500 sccm AsH₃ carrier gas flow, and G2 was annealed with the 500 sccm AsH₃ carrier gas flow. The SEM images before the anneal show that the two graphene films were not identical. The G2 graphene was smoother, where the two dark spots in both pre-anneal images are an artifact from the SEM electron beam and not features of the samples. The SEM post-anneal images of the two samples reveals no wrinkling of the graphene in either case. However, sample G1 showed deposition that EDS identified as In-rich, which was initially surprising since only AsH₃ and nitrogen were flowing through the reactor. This deposition is attributed to the lower kinetic barrier to growth with AsH₃, and can be effectively prevented by allowing the AsH₃ to decompose into Asₓ, as seen in sample G2. However, since G2 showed neither deposition nor etching, Raman spectroscopy was necessary to determine if the graphene was still intact.

Figure 5.7 shows Raman spectroscopy of the two samples before and after the anneal to ensure the integrity of the graphene. A microscope was used to locate specific areas on the sample, and then a
Figure 5.6: SEM of the graphene-coated GaAs substrates G1 (2500 sccm AsH$_3$ carrier gas flow) and G2 (500 sccm AsH$_3$ carrier gas flow) before and after annealing at 650 $^\circ$C with AsH$_3$ and nitrogen carrier gas.

532 nm laser was used to excite phonons in the graphene to get the resulting signature. We find three characteristic peaks associated with the Raman spectroscopy of graphene: the 2D peak at 2700 cm$^{-1}$, the G peak at 1582 cm$^{-1}$, and the D peak at 1350 cm$^{-1}$ [121] [122]. The G and 2D peaks occur from a single resonance and double resonance Raman process, respectively, while the D peak occurs due to disorder in the sample [121]. For both graphene samples, a broadening and decrease in intensity of the D peak can be observed, which may be attributed to thermal etching of the residue that remained from the transfer of graphene from SiC to the GaAs substrates. This would decrease the intensity of the D peak since less residue remained after the anneal; however, heating may also cause contamination of the graphene as the residue thermally decomposes, which has been shown to then broaden the Raman peaks associated with graphene [123]. The relative change in intensity between the G and 2D peaks is potentially due to the enhanced adhesion between the graphene and GaAs substrate after annealing,
where the closer spacing can lead to more interaction and distortion of the Raman peaks. The most significant finding is that in both cases, the graphene remains intact after the anneal.

![Raman spectroscopy of the graphene-coated GaAs samples G1 and G2 pre- and post-anneal with AsH$_3$ and N$_2$.](image)

The next step was to grow a thin GaAs nucleation layer with low AsH$_3$ carrier gas flow and perform Raman to ensure that the D, G, and 2D peaks could still be observed. Since the penetration of the laser for Raman spectroscopy is assumed to be approximately half of the wavelength, the GaAs layer grown for this study needed to have a thickness less than or equal to 266 nm. A 150 nm GaAs layer was grown on the graphene sample G2, since no pre-deposition had occurred on this sample during the previous anneal. Figure 5.8 shows Nomarski optical microscope images and Raman spectroscopy of this sample before and after growth. Since the GaAs surface was rough after growth, additional studies of appropriate nucleation conditions beyond those used for the anneal are necessary. One critical point, however, was ensuring that the graphene remained intact after growth. The bottom row of Fig. 5.8 shows Raman spectroscopy as-received, after the anneal as shown in Fig. 5.7, and after GaAs growth. These results show that the G, 2D, and D peaks are observed in all cases, and that the graphene peaks appear nearly identical before and after growth, which is a promising result.
Figure 5.8: Top row: Nomarski optical micrographs of the graphene sample after annealing (left) and after growth of a 150 nm thick GaAs layer (right). Bottom row: Raman spectroscopy of the graphene-coated GaAs sample G2 as-received, after annealing at growth temperature for 10 minutes, and after 150 nm of GaAs growth.

5.4 Conclusions

In summary, growth rates up to 400 µm/h using H₂ carrier gas and 528 µm/h using N₂ carrier gas have been demonstrated in a D-HVPE reactor. The samples displayed smooth surfaces for growth rates up to 400 µm/h and 483 µm/h for the respective carrier gases, with the surface morphology of higher growth rate samples likely hampered by the lack of sufficient group V flows. CFD modeling showed enhanced AsH₃ delivery to the wafer surface enabled by a lower internal reactor temperature using N₂ carrier gas, whereas more AsH₃ decomposes into the less reactive Asₓ with H₂ in a hydride-enhanced regime. The high throughput, lower cost, and safety benefits of using N₂ compared to the incumbent H₂ used
in III-V arsenide/phosphide HVPE systems make N₂ a potentially attractive alternative carrier gas in a hydride-enhanced regime.

After characterizing the growth rate for various conditions, initial anneal and growth experiments were performed on the graphene templates. Two anneal conditions were considered: one in an AsH₃-rich environment with 2500 sccm AsH₃ carrier gas flow, and one in an Asₓ-rich environment with 500 sccm AsH₃ carrier gas flow. High AsH₃ carrier gas flow rates that allow more AsH₃ to reach the graphene surface appear more likely to cause unintentional pre-deposition on the graphene surface. However, this pre-deposition can be mitigated by allowing more of the AsH₃ to decompose into Asₓ, which has a higher kinetic barrier to growth. While no significant damage to the graphene could be observed for either annealing condition, further nucleation studies are required to produce smooth surface morphology of the GaAs epilayers.
Chapter 6

Conclusions

6.1 Summary and Outlook

6.1.1 AIC

The work described in Chapter 3 explored a variety of parameters that can be controlled for the AIC process, including the effects of Al oxidation, different deposition techniques, ambient gas and pressure during the anneal, absolute and relative Al and Ge thicknesses, layer order, total anneal time, anneal temperature, temperature ramps to and from the anneal temperature, and substrate thickness. Among the more interesting findings from these studies was the observation that the number of nucleation points and grain size correlate strongly with temperature ramp rate. The slower the temperature ramp rate, the more nucleation points were observed. However, for very fast ramp rates exceeding 50 °C/s, the Ge films appeared to degrade. The 1 °C/s ramp rate to an anneal temperature of 375 °C for 50 hours with 200 nm Al and 200 nm Ge films on a 280 μm thick Si substrate provided the highest Ge surface coverage of the conditions explored in this dissertation.

Another finding was the effect that substrate thickness has on the grain size, grain orientation, and
surface coverage of the samples, where thicker substrates are often used when scaling to larger-area devices. In this case, the motivation for the study was the onset of cracks that formed in a Ge film annealed on a 4-inch diameter 525 \( \mu \text{m} \) thick substrate, while a Ge film that was deposited and annealed at the same time, but on a 2-inch diameter 280 \( \mu \text{m} \) thick wafer, exhibited no cracks, 600 nm grain size, and high surface coverage. Additionally, we found that the use of a 200 \( \mu \text{m} \) thick Si substrate could produce predominantly (100)-oriented 10 \( \mu \text{m} \) Ge grains through AIC. Since GaAs solar cells are often grown on (100)-oriented substrates, future work that was able to demonstrate these (100)-oriented Ge substrates with large grain size, albeit better surface uniformity, could be extremely valuable to the field. Since Comsol simulations seem to confirm that substrate thickness influences the effective temperature ramp-rate, and the potential exists for additional mechanical effects from the flexibility of thin substrates and rigidity of thick substrates, further optimization considering a simultaneous design of experiments of ramp rate and substrate thickness could be fruitful.

There are likely additional parameters remaining to be explored that affect the initial number of nucleation points, final grain size, and preferential crystal orientation. It is imperative that future work strive to both optimize these parameters and do so in reasonably short time at low cost in order for this technique to be adopted in industry.

### 6.1.2 Solar Cell Growth on Polycrystalline Substrates

Monocrystalline and polycrystalline GaAs and Ge substrates with 200-400 \( \mu \text{m} \) grain size from Umicore were evaluated to better understand how polycrystallinity and APD density affect solar cell characteristics such as \( J_{\text{SC}} \), \( V_{\text{OC}} \), \( J_{\text{01}} \), and MCDLs. The results from this study indicated the need to further develop the nucleation layer for growth on polycrystalline and monocrystalline Ge. Both temperature and material (InGaP vs. GaAs) of the nucleation layer were then investigated. This study indicated that a low-temperature GaAs nucleation layer yielded better material quality than a high-temperature InGaP
layer grown on c-Ge for the temperature range studied, and that the low-temperature GaAs nucleation conditions had minimal effect on the AIC samples since grain size was instead the major limitation.

Polycrystalline Ge substrates were then developed by AIC to create Ge films with greater than 95% surface coverage uniformly across a half of a 2-inch wafer. A top-top contact n-i-p GaAs solar cell was grown and fabricated on an AIC Ge substrate as well as c-Ge and poly-Ge substrates from Umicore as baselines. The solar cells on AIC Ge show 1-sun $V_{OC}$ up to 0.17 V, which is comparable to the range of $V_{OC}$ for the poly-Ge baseline with 400 µm grain size. The AIC cells also exhibited an enhancement in $J_{SC}$ up to 8 mA/cm$^2$ under concentration. With continued efforts to enhance the grain size and orientation of the AIC Ge films, $J_{SC}$ similar to those of the c-Ge solar cells could be achieved, as shown by the performance of the Umicore poly-Ge solar cells.

6.1.3 Remote Epitaxy Through 2D Graphene

GaAs growth rates up to 528 µm/h were achieved with N$_2$ carrier gas compared to 400 µm/h with H$_2$ under the same conditions. While it was already known that enhanced AsH$_3$ delivery to the substrate was critical to unlocking ultrafast growth rates in HVPE, it was previously unknown the role in which carrier gas species could further enable this effect. Due to the lower thermal conductivity of N$_2$ compared to H$_2$, CFD simulations indicate that high AsH$_3$ carrier gas flow using N$_2$ is able to lower the temperature of AsH$_3$ and decrease the extent of thermal decomposition before reaching the substrate.

Using this knowledge of the effects that AsH$_3$ carrier gas flow has on the group V species, anneal conditions varying AsH$_3$ carrier gas flow were then explored in order to determine suitable conditions for GaAs growth on graphene. Two anneal conditions were considered, one in an AsH$_3$-rich environment with 2500 sccm AsH$_3$ carrier gas flow, and one in an As$_x$-rich environment with 500 sccm AsH$_3$ carrier gas flow. The graphene layers remained smooth and intact in both cases as confirmed by SEM and Raman spectroscopy. However, pre-deposition occurred for the 2500 sccm AsH$_3$ carrier gas flow,
which seems to indicate reaction with material in the boats or chamber walls enabled by the lower kinetic barrier to growth by $\text{AsH}_3$. Further nucleation studies are required to produce smooth surface morphology of the GaAs epilayers, which will continued to be explored in future work from this group.

6.2 Accomplishments

The awards won and products delivered by the student from August 2014 to January 2020 are listed below.

6.2.1 Awards

46th IEEE Photovoltaic Specialists Conference Lead Graduate Student Assistantship (2019)

7th World Conference on Photovoltaic Energy Conversion Graduate Student Assistantship (2018)

IEEE Rochester Section Travel Scholarship (2018)

National Renewable Energy Laboratory graduate student research internship (Summer 2017)

Hands-On PV Experience participant at the National Renewable Energy Laboratory (Summer 2016)

National Science Foundation Graduate Research Fellowship Program Honorable Mention (2016)

6.2.2 Products

The work from this dissertation was disseminated in the following places:


Appendices
Appendix A

Summary of AIC Experiments

The following table summarizes the experiments performed in Chapter 3 of this dissertation. Changes made from one sample to another are highlighted in bold. The sample nomenclature is the year (20)15, 16, 17, or 18, followed by either E or PE if the sample was annealed in the tube furnace compared to R if it was annealed in the MOCVD reactor, the three-digit sample number, and then a -1, 2, 3, or 4 depending on the position in which the sample sat in the susceptor for MOCVD anneals. Often temperature set point for the anneal was recorded, where a conversion between the tube furnace temperature set point and true temperature is displayed in Appendix B.
Table A.1: Summary of AIC experiments performed in this work from 2015-2018.

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<thead>
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<th>Ge Thickness (nm)</th>
<th>Layer Order</th>
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<th>Deposition Method</th>
<th>Substrate</th>
<th>Anneal Apparatus</th>
<th>Anneal Time (hours)</th>
<th>Anneal Temperature (C)</th>
<th>Gas Pressure (Torr)</th>
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<td>Layer Transfer</td>
<td>0</td>
<td>Thermal Evaporation</td>
<td>Si(111)</td>
<td>Tube Furnace</td>
<td>50</td>
<td>380</td>
<td>N₂</td>
<td>760</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Appendix B

Tube Furnace Temperature Calibrations

The following figure and table summarize the relationship between the Lindbergh Blue M tube furnace heating element set point and the true temperature as measured with a thermocouple. The thermocouple was inserted in a quartz boat and inserted into the center of the tube, pointed towards the air (instead of making contact with the surface of the quartz tube), and allowed to stabilize for at least 10 minutes between measurements.

Table B.1: Summary of the relationship between the temperature set point and the true temperature at the sample location inside the quartz tube.

<table>
<thead>
<tr>
<th>Temperature Set Point (°C)</th>
<th>True Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>41</td>
</tr>
<tr>
<td>100</td>
<td>69</td>
</tr>
<tr>
<td>150</td>
<td>118</td>
</tr>
<tr>
<td>200</td>
<td>167</td>
</tr>
<tr>
<td>250</td>
<td>207</td>
</tr>
<tr>
<td>300</td>
<td>258</td>
</tr>
<tr>
<td>350</td>
<td>307</td>
</tr>
<tr>
<td>400</td>
<td>363</td>
</tr>
<tr>
<td>436</td>
<td>400</td>
</tr>
<tr>
<td>450</td>
<td>413</td>
</tr>
</tbody>
</table>
Figure B.1: True temperature as measured in the center of the quartz tube as a function of temperature set point.
Glossary

AFM  atomic force microscopy. 48, 92


Al  aluminum. 21–24, 26–41, 43, 44, 46–49, 52, 53, 55–60, 72, 73, 79, 80

AlAs  aluminum arsenide. 3, 5

AM1.5G  air-mass 1.5 global. 2, 18, 67, 82, 83

APD  antiphase domain. 62, 63, 65, 67–69, 74, 76, 81, 84, 85

As  arsenic vapor. 88–92, 96, 98, 101

AsH₃  arsine. 64, 71, 80, 89–96, 98, 101, 105

CFD  computational fluid dynamics. 90, 91, 94, 101

CMP  chemical-mechanical polishing. 6

DEZn  diethylzinc. 65, 71, 80

EBSD  electron backscatter diffraction. 52, 55–57, 60, 73

EDS  energy-dispersive x-ray spectroscopy. 34, 35, 43, 44, 48, 52, 55–57, 73, 79, 98

ELO  epitaxial lift-off. 5, 6

EQE  external quantum efficiency. 64, 68, 69, 83

GaAs  gallium arsenide. 2–7, 9, 10, 13–19, 21, 24, 25, 62–74, 77, 79, 81, 83, 85, 87–92, 96–102

Ge  germanium. 2, 5–9, 18, 19, 21, 23, 24, 26–44, 46–60, 62–65, 67–87, 103–105

HVPE  hydride vapor phase epitaxy. 4, 87–90, 98, 101, 105

InGaP  indium gallium phosphide. 9, 66–68, 70, 71, 77, 78, 85, 87, 91, 104
InP  indium phosphide. 2, 5, 6, 18
IQE  internal quantum efficiency. 19, 78
J-V  current density-voltage. 16, 17, 67, 82
J_{SC}  short-circuit current density. 67, 69, 82–86, 104, 105
MCDL  minority carrier diffusion length. 15, 69, 85
MIC  metal-induced crystallization. 20, 21
MOCVD  metal-organic chemical vapor deposition. 4, 9, 19, 33, 35, 36, 38, 43, 64, 70, 73, 80, 87
NREL  National Renewable Energy Laboratory. 8, 67, 68
PH_{3}  phosphine. 5, 64, 80
PL  photoluminescence. 71, 73, 75–78, 85
PV  photovoltaic. 1–3, 5, 8, 9, 24
RIT  Rochester Institute of Technology. 7–9, 60
Si  silicon. 1, 2, 5–7, 19, 21, 24, 27–29, 31, 33, 43, 46, 49, 51, 52, 54, 60, 73, 78, 79, 81
SPIP  Scanning Probe Image Processor. 48
TEM  transmission electron microscope. 14
TMAl  trimethylaluminum. 71
TMGa  trimethylgallium. 64, 71, 80
TMIn  trimethylindium. 64, 71, 80
V_{OC}  open-circuit voltage. 67, 69, 82–86, 104, 105
XRD  x-ray diffraction. 28, 29, 31, 32, 43, 46, 48, 59, 64, 79, 80
References


