MULTILEVEL METALLIZATION

Michael J. Bailey
Senior Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

A bilevel metallization process using aluminum with 1% silicon for the Metal 1 layer, pure aluminum for the Metal 2 layer, and Accuglass X-11 311 Series spin-on glass for the interlevel dielectric was investigated. Problems encountered in via etching with previous bilevel work were eliminated by using a modified buffered HF etchant. Vias down to 6x6um in size were found to conduct and have resistances less than 1 Ohm. Spin-on glass coating processes, however, were still in need of refinement, as numerous pinholes were observed over the aluminum regions.

INTRODUCTION

Multiple layers of metal interconnects [1] have become the norm in industry for the back end processing of semiconductor wafers as device geometries have shrunk to submicron dimensions and increasingly faster devices are sought. Multiple interconnect layers allow devices to be packed more densely on a chip, since less area is required to route interconnect lines. Additionally, these shorter lines have a lower capacitance, thus reducing time delay restrictions on operating speed.

Interconnect metals and interlevel dielectrics must be chosen such that the necessary processing will not interfere with device characteristics. For most back end processing, high temperature steps must either be eliminated or minimized to prevent the outdiffusion of doped regions in the substrate. Interconnect and interlevel dielectric materials can, therefore, only be applied at low to moderate temperatures. Additionally, these materials must produce low defect films and adhere well to the underlying substrates. Interconnect metals must have low sheet resistance values. Metals having such characteristics include aluminum, molybdenum, tungsten, and various silicides. In some schemes, a silicide forms the lower metal layer, as it is resistant to the temperatures required to cure or reflow the dielectric film, and aluminum forms the upper metal layer, since it has better step coverage. Interlevel dielectrics, on the other hand, must have low dielectric constants(to keep capacitance between metal layers low), and be capable of producing films thick enough(without cracking due to film stress)

to provide good step coverage [1]. Materials such as polyimides, spin-on glass, and BPSG films(such as TEOS) lend themselves well for this purpose. BPSG offers the advantage that it will reflow at moderate temperatures after the via etch to produce a profile more favorable to aluminum deposition. For conventional processes, a sloped via profile as shown in Figure 1.(a) is generally preferable since it allows for better step coverage of the Metal 2 layer. Fabrication techniques utilizing a vertical via sidewall, however, are are becoming more widely used as less surface area is required for the via [1]. With this scheme, tungsten is selectively deposited and used to form a plug as shown in Figure 1.(b). A planarization process, however, may be necessary to achieve a profile over which the upper metal layer may be deposited.

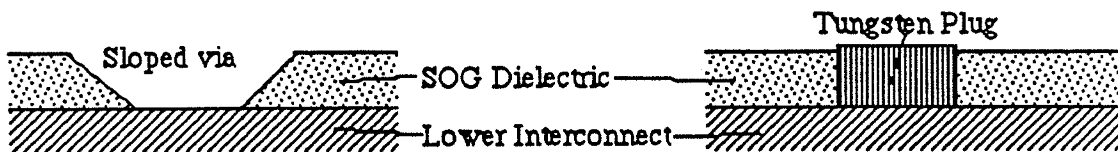

Figure 1.(a): Conventional via. (b): Vertical via.

Previous attempts have been made at R.I.T. [2-7] to develop a process for bilevel metallization using available materials. Aluminum was used for both metal layers, and deposited by evaporation. For an interlevel dielectric, materials such as polyimides, pyrolized photoresists, and spin-on glass had been evaluated. Of all the materials examined, spin-on glass(SOG) seemed to be the best candidate for a dielectric [4]. Adhesion to the metal layers and substrate was superior to that of the other materials and adequately high dielectric breakdown voltages were measured. Good ohmic contact at the vias between interconnect layers, however, could not be achieved due to suspected problems with the via etching process. Either the vias were underetched, an unknown film(possibly organic) remaining at the Metal 1 surface prevented electrical contact between layers, or the underlying Metal 1 layer was somehow attacked by the buffered HF used to etch the vias.

In this experiment, a bilevel metal process using aluminum with 1% silicon for the Metal 1 level, pure aluminum for the Metal 2 level, and Accuglass X-11 311 series SOG [8] for the interlevel dielectric was was investigated. Efforts focused on overcoming the theorized via etching problems.

EXPERIMENT

Experiments to characterize SOG processing were performed using bare and aluminum coated silicon monitor wafers. A spin speed of 3000 RPM was used for coating the SOG. For curing the SOG, a prebake step of either 100'C for 15 minutes in a convection oven or 150'C for one minute on a hotplate, followed by a 425'C cure in N2 was recommended [8]. Since the hotplate

bake caused large bubbles to appear in the film, the convection oven bake was used for most wafers. Film thickness was measured using an Alpha Step profilometer and found to be 2800A over silicon and 2300A over aluminum. After the final cure, films on the aluminum wafers were found to be relatively free of defects.

The SOG on aluminum was etched using a stock buffered HF(7% HF, 36% NH4F) solution. Vigorous attacking of the aluminum was observed both visually and in the Alpha Step profile, after the SOG had been cleared. A 5:2 volumetric mixture of the stock HF solution and glycerine was then used to etch the SOG. This mixture had sucessfully been used to etch CVD oxides over aluminum at IBM [9]. It was theorized that the glycerine molecules formed a protective coating over any exposed aluminum. With the glycerine added, attacking of the aluminum surface was completely eliminated. Over the course of a few minutes, however, selectivity of the etchant deteriorated, and the aluminum layer was attacked. For this reason, the etchant mixture had to be replaced after a few wafers were etched.

Ellipsometry was used to monitor the SOG interfaces after various processing steps. The aluminum films on silicon were analysed to yield a complex refractive index. After coating, curing, and etching the SOG, remeasurement of the surface yielded an almost identical refractive index, indicating no damage or residue on the aluminum film. The application and removal of photoresist from the SOG film was similarly studied. Again, no changes in ellipsometric parameters were observed, indicating no damage to the SOG resulting from the resist processing.

Electrical test structures for the evaluation of vias and the interlevel dielectric were fabricated on 3 inch wafers using three masking levels: Metal 1, Via, and Metal 2. The Metal 1 layer was deposited over a 2200A thick thermal oxide and patterned. The SOG was coated over this layer, the Via level exposed, and the modified buffered HF mixture described earlier used to etch the vias. Etch time was increased by 66%(15 seconds were required to etch the monitors bare of SOG) to insure that the vias would clear. Finally, the Metal 2 layer was deposited over the SOG and patterned. A 20 minute sinter in forming gas was performed at 425 'C to insure contact between layers. A cross section of the via test structure is shown in Figure 2, and a complete list of processing steps is found in Appendix C.

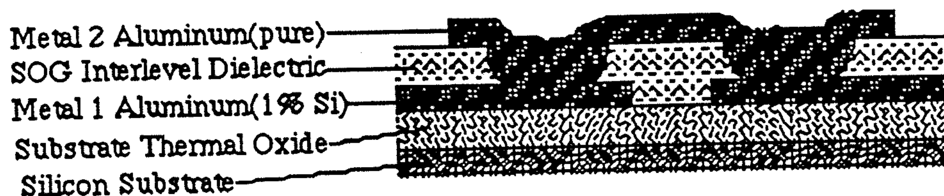

Figure 2: Cross section of via electrical test structure.

For patterning the wafers, a testchip(see Appendix A for layout) was designed on ICE, an in-house CAD tool, and emulsion masks made which could be used on a contact aligner. To test for shorting within and between layers, overlapping(Metal 1 and Metal 2) serpentine-comb structures, previously designed [7], were retained in the design. Contact test structures having the following via dimensions were designed: 6x6um, 10x10um, 20x20um, and 30x30um. These structures included via chains(40 vias in length) which could be tested over different lengths(Figure 3), and cross bridge Kelvin structures(Figure 4). Additionally, structures for alpha stepping the SOG, and interlevel capacitors(to test for shorting and dielectric breakdown) were incorporated into the testchip design.

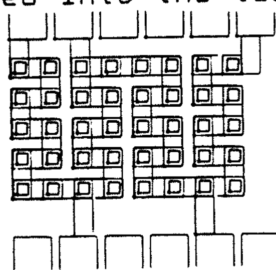

Figure 3: Via chain

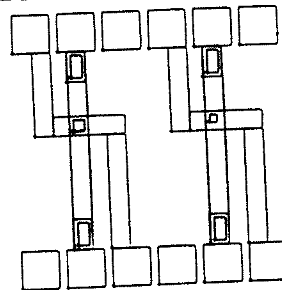

Figure 4: Kelvin structure

RESULTS/DISCUSSION

Electrical testing of the via chain and Kelvin structures before sintering revealed no electrical contact at the vias. After the sintering, however, electrical conduction was observed at via structures down to 6x6um in size at some die. Contact was consistently achieved for the 20x20um and larger vias. Contact resistance was determined using the chains of 40 vias, and these measurements are given in Appendix B. The total resistance of the chain was divided by 40 to obtain an approximate average resistance per via. For all the measurable vias, resistances were on the order of 1 Ohm, but varied within a range of +/-1 Ohm.

The interlevel capacitors and overlapping serpentine-comb structures were used to test for shorting between layers. At most of the capacitors and serpentines, shorting between the layers was observed. At other structures, dielectric breakdown was found to occur at only 4 volts. This interlevel shorting is believed to have been caused by pinholes in the SOG. After the coating and curing of the SOG, numerous pinholes were observed in areas over the aluminum on patterned wafers. This was not found to occur on the unpatterned aluminum monitors.

It is suspected that these pinholes were the result of an excessively thin dielectric layer over the Metal 1 regions. This was probably due to the fact the Metal 1 was 4000A thick. The SOG, by contrast, was only 2300-2800A thick. This problem might be solved by depositing a thinner Metal 1 layer. Metal 1, however, must be thick enough to provide adequate step coverage and sufficiently low sheet resistance.

Another solution to the pinhole problem might be a thicker coat of SOG. On three wafers, a second coat of SOG was added after the completed wafers were found to have these problems. Slight cracking, however, was observed in the film over aluminum regions. In this case, cracking may be due to the fact that the second coat was applied after a full cure of the first coat. Allied recommends that a second coat be applied only after partial cure(standard softbake followed by a 1 minute hotplate bake at 250'C) of the first layer [8]. Future work with SOG should investigate the use of a partial cure after the first coat.

CONCLUSION

After seven senior projects by students, interlevel contact at the vias has finally been achieved for a bilevel metal process at R.I.T. A wet etchant consisting of buffered HF and glycerine made it possible to etch a silicon oxide film over aluminum without attacking the underlying metal. It is not known if use of aluminum with 1% silicon for the Metal 1 layer, and pure aluminum for the Metal 2 layer also played a role in improving via electrical characteristics. Before this process can be implemented, however, work is needed to optimize the processing of SOG over a patterned aluminum surface to decrease pinhole density, and improve dielectric breakdown voltages. In subsequent work, a thinner Metal 1 layer and possibly multiple coats of SOG should be used for fabricating bilevel metal structures.

ACKNOWLEDGMENTS

I would like to thank the following people for their assistance with the multilevel metal project: Mike Jackson, Renan Turkman, and Bruce Smith.

REFERENCES

[1] Wolf, S., Silicon Processing for the VLSI Era: Volume 2, Chapter 4,1990.

[2] Knaus, C., unpublished senior research paper at Rochester Institute of Technology, 1985.

[3] Westerhoff, E., unpublished senior research paper at Rochester Institute of Technology, 1986.

[4] Newcomb, R., unpublished senior research paper, Rochester Institute of Technology, 1987.

[5] Carniero, M., unpublished senior research paper at Rochester Institute of Technology, 1988.

[6] Patterson, Ross., unpublished senior research paper, Rochester Institute of Technology, 1989.

[7] Quinn. M., unpublished senior research paper at Rochester Institute of Technology, 1990.

[8] Author not given, Accuglass Siloxane Spin-on-glasses,

Allied Chemicals.
[9] Gajda, J.; <u>Techniques in Failure Analysis of MOS Devices</u>
[10] Manos, D.; Flamm, D.; <u>Plasma Etching: An Introduction</u>, 1989.

APPENDIX A: TESTCHIP DESIGN

1. Alpha step structure
2. 30x30,20x20 Kelvin
3. 30x30 via chain
4. 20x20 via chain
5. 10x10 via chain
6. 6x6 via chain
7. 10x10,6x6 Kelvin
8. Metal 1 capacitor
9. Bilevel serpentine
10. Metal 2 serpentine
11. Metal 2 capacitor
12. Interlevel capacitors