PRELIMINARY FORMATION OF DEEP TRENCH CAPACITORS

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ABSTRACT

A Tegal 700 plasma etcher was used to etch trenches in (100) p-type silicon wafers using a SF6/O2 plasma. Silicon etch rates of approximately 1.17 microns/minute and a Si:SiO2 selectivity ratio of 22.0 were obtained. Scanning Electron Micrographs show the etch was isotropic in nature with an aspect ratio of approximately 2:1.

INTRODUCTION

The development of VLSI technology into the ULSI realm follows a path that is inversely proportional to, among other things, cell area. Figure 1 shows the progress of decreasing cell size in relation to memory on a single chip. "Any further increase in complexity of VLSI devices must spring from either a decrease in device feature size, increase in 'available' semiconductor area or volume, or better use of the material in terms of novel device structures and circuit architectures" [1]. Device size continues to decrease with the use of better photolithographic systems, and in recent years, the "one micron barrier", has been surpassed and even the "half micron barrier" has been broken in the laboratory environment, but "further decreases in minimum feature size [have] become slow and very expensive"[1]. Breakthroughs into the ULSI era will have to be accompanied not only by decreases in feature size, but also by the use of "novel device structures".

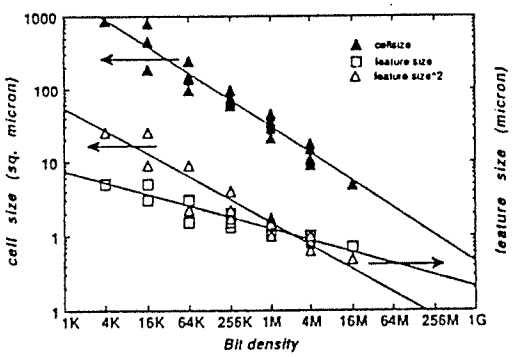


Figure 1: DRAM cell size evolution versus bit density [2].

One such "device" is the deep trench. Figure 2 shows the chronological progression of isolation techniques leading up to the use of trench isolation as a method of separating devices. Historically, devices on a chip were isolated by placing them sufficiently far away from other devices on the chip so that they did not interfere with each other. Several diffusion techniques followed to allow devices to be packed more densely on a chip. Single diffused areas were the first type of isolation, but they required the same amount of space laterally as vertically and were soon replaced by double diffused junctions. Double diffusions offered the same amount of vertical diffusion, but with less lateral diffusion due to two shorter diffusions instead of a single long one. The next generation of diffusion techniques involved the use of an oxide layer above a single diffusion. However, this process produced the "bird's beak" profile, seen in the figure, making it difficult to place devices at the edges of one another. Diffusion techniques for isolation were then replaced by etching techniques in the form of deep trenches. Trench isolation increases device density by providing (with very little chip area) electrical isolation of devices by blocking the lateral flow of diffusion currents between neighboring devices.

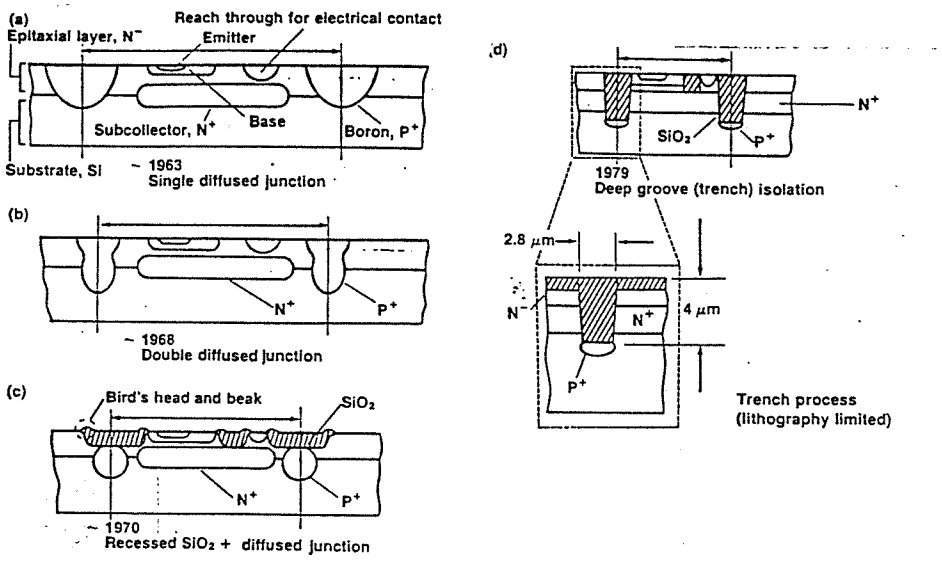


Figure 2: Progression of isolation techniques [3].

Trenches are ideal for isolating neighboring devices because they are built down into the wafer as opposed to taking up large amounts of surface area. In addition, they do not exhibit a "bird's beak" profile which makes it possible to position devices at the edge of the trench. The minimum size of the trenches is limited only by the lithography and etch of the system.

Trenches are now utilized in actual devices. As shown in Figure 3, a storage capacitor was made by modifying the deep trench isolation process. Conventional trench capacitors consist of an n+ layer formed on the trench surface over which a thin gate oxide is grown [4,5,6] and then a polysilicon layer is deposited. Since the storage capacitance is largely controlled

by the capacitor area, which in a trench capacitor is related to the depth of the trench, the deeper the trench, the higher the storage capacitance. In this manner, trench capacitor cells have provided a way to keep storage capacity high, and at the same time reduce cell area, thus making megabit DRAM memories (which require a large charge capacity) possible.

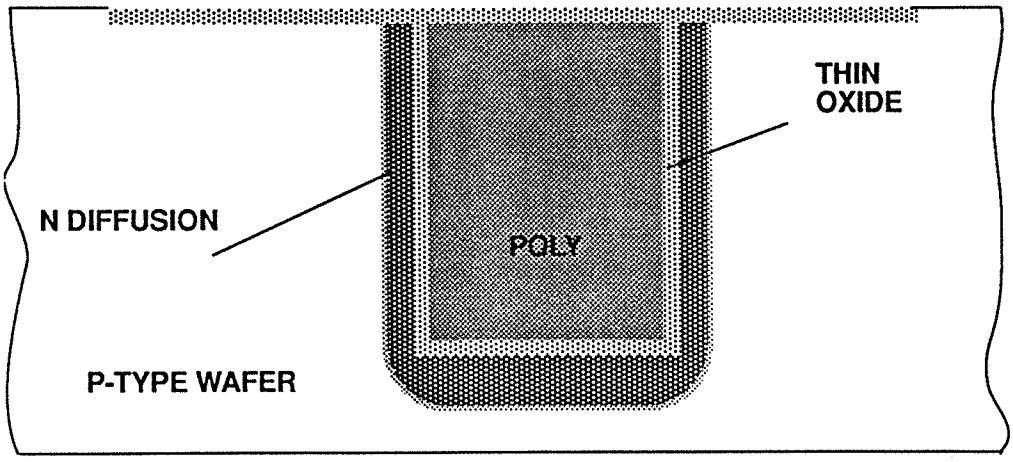


Figure 3: Cross section of a simple trench capacitor.

This experiment was performed as the first step towards the fabrication of trench capacitors or trench isolation devices. A plasma etch tool employing SF6/02 gases was uses to form trenches in silicon substrates.

EXPERIMENT

Ten (100) p-type wafers were obtained and cleaned using a standard RCA clean. A 2500 angstrom oxide layer was thermally grown at 1100 degrees Celsius for twelve minutes in a wet oxygen ambient. The wafers were then coated with 1.2 microns of KTI820 positive photoresist and patterned with a mask consisting of line/space pairs ranging from 0.1 to 10.0 microns.

The wafers were exposed using a GCA stepper and then developed on a GCA Wafertrac after which a wet chemical etch of the oxide was performed for three minutes in buffered HF. After the windows were etched in the oxide, the actual trenches in the single crystal silicon were etched. This was performed using a Tegal 700 plasma etcher and a 3:1 mixture (10 sccm: 3.3 sccm) of SF6/02[7]. The etcher was tuned to minimize the reflected power (<5Watts), while a pressure of 550 mtorr and a forward power of approximately 125 Watts was maintained. Measurements of the etched trenches were made using the Alpha-step profilometer after the thickness of the remaining oxide layer was measured using the Nanospec. Following the measurement of the trench depth, the etch profile was analyzed using the scanning electron microscope and micrographs were taken.

Similar trenches were also etched using the Reactive Ion Etch tool and a known polysilicon etch process[8] was applied. The RIE etch consisted of a low power, low pressure etch. The plasma was made up of a 10:3 (20 sccm: 6 sccm) SF6/02 ambient using 80 Watts of forward power with a pressure of 80 mtorr.

RESULTS/DISCUSSION

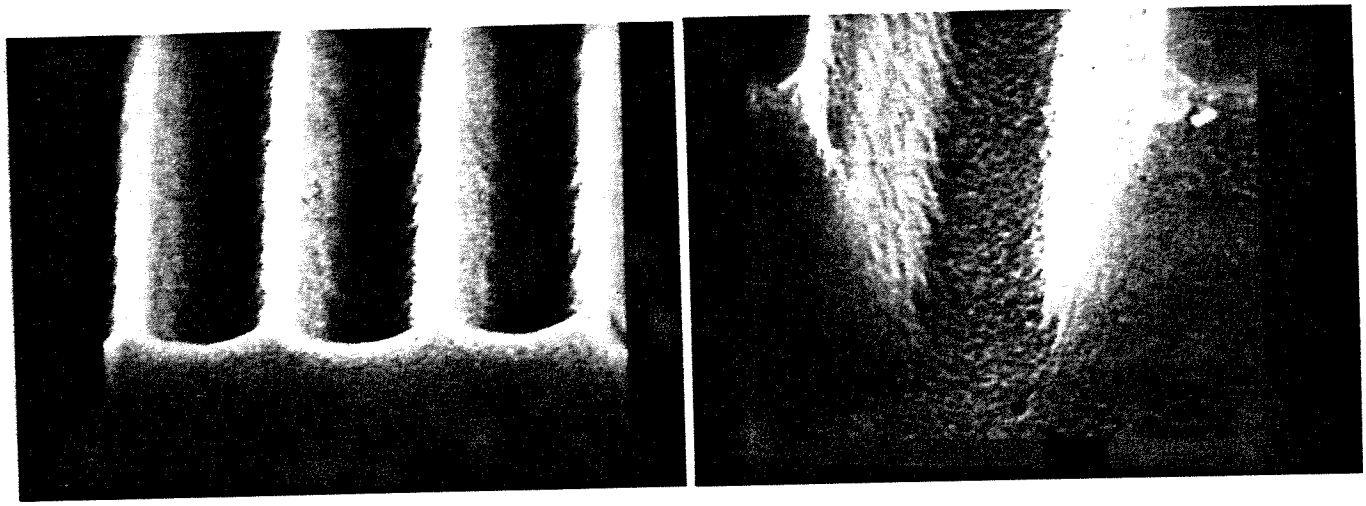
The results of the Alpha-step measurements, seen in Table 1, show the etch rates of the single crystalline silicon and the masking oxide layer. The average etch rate was 1.17 um/min for silicon and 0.50 for the oxide. The oxide etch rate for several of the trials were not determined because the oxide was etched away prior to the measurement of the deep trench.

Scanning Electron Micrographs of the various etches are seen in Figure 4. The first photo shows the initial attempts at etching single crystal silicon trenches. The original oxide windows were five microns apart and approximately three microns wide. After a five micron deep etch, the gap between trench areas has narrowed so that they are nearly touching. Photo two shows the profile of a five micron deep etch. The slope of the remaining silicon is approximately 60 degrees which represents a vertical to horizontal aspect ratio of approximately two (a completely isotropic etch would have exhibited a 45 degree slope). Photographs three through five are examples of undercutting due to the isotropic nature of the etch. Notice, in photo five, how the silicon has been completely undercut and the oxide is dangling. Photo six shows the remains of two micron line/space pairs after a three micron etch.

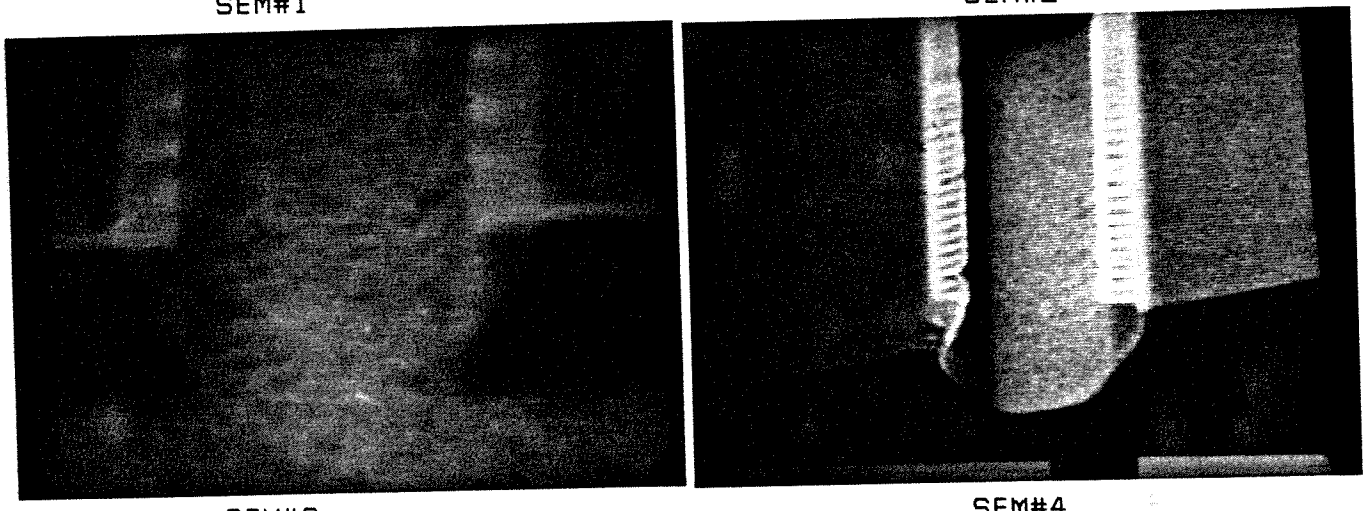
wafer #	Trench Depth (um)	Oxide Etched (Angs)	Etch Time (min)	Si Etch Rate (Ang/min)	SiO2 Etch Rate	Ratio Si: SiO2
2A	5.3	NA	4.66	11,400	NA	NA
2D	11.6	NA	9.32	12,400	NA	NA
4B	3.4	1434	3.0	11,400	478	23.8
4C	1.9	963	2.0	9,600	482	19.9
5B	3.7	1611	3.0	12,400	537	23.1
5C	2.2	1043	2.0	11,100	522	21.3
8A	2.7	NA	2.0	13,300	NA	NA
avg.	----	----	----	11,700	505	22.0

Table 1: Etch Rates in Tegal 700 With 3:1 SF6/02 Plasma

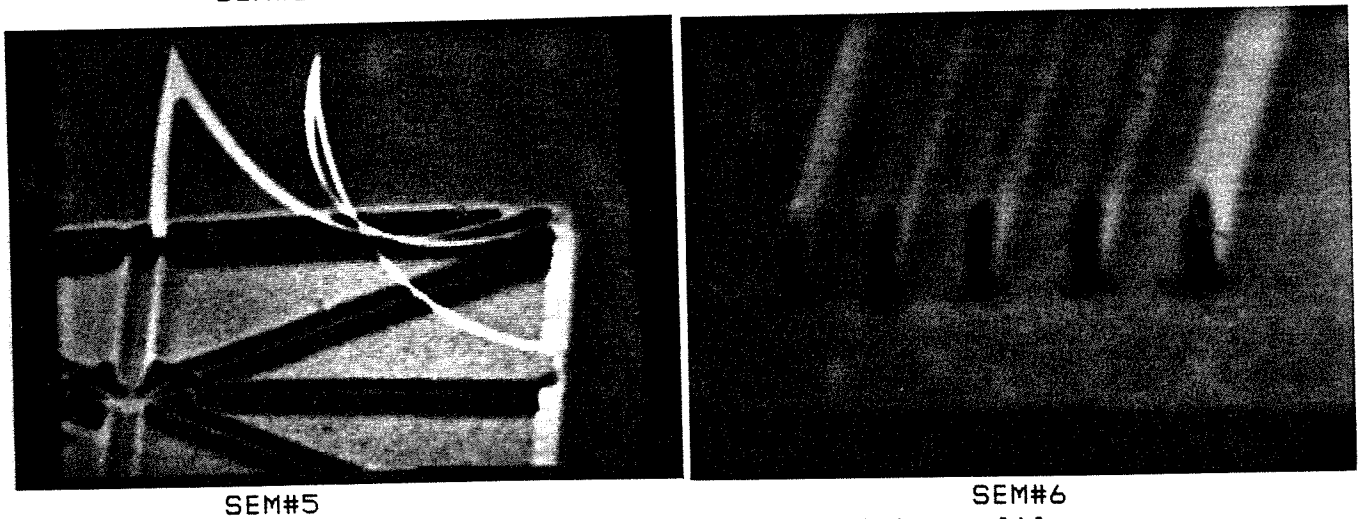
The results of the RIE etch were not quite as expected. A five minute etch in the 10:3 SF6/02 plasma yielded a 2.9 micron trench to give an etch rate of approximately 5800 angstroms/minute. Micrographs showed that the etch was not anisotropic as expected from the decrease of 02 in the system and ability to control the power and pressure settings. In fact, the profiles appeared worse than those obtained using the Tegal.



SEM#1 SEM#2



SEM#3 SEM#4



SEM#5 SEM#6

Figure 4. SEM Photos of silicon etch profiles.

CONCLUSION

The etching of deep trenches in single crystal silicon was performed using both the Tegal 700 and RIE etch tools, however, both tools produced etches lacking in the degree of anisotropy needed to produce three to five micron deep trenches with one to two micron wide openings at the surface.

Since the Tegal is limited by the inability to adjust the forward power and pressure, future experiments in silicon trench etching should concentrate on the RIE tool where the pressure can be increased to help decrease the lateral etching [9]. There is also the possibility of investigating other gases including chlorine based gases to perform single crystal silicon etching [10].

ACKNOWLEDGMENTS

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