MULTILEVEL METALIZATION

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ABSTRACT

A multilevel metal testchip which analyzes a first level metal, interlevel dielectric, and second level metal has been designed. The test structures will be used to detect opens or shorts in conducting lines, measure via resistance, measure sheet resistance, and determine linewidth or linespace.

INTRODUCTION

Metalization is most important in determining chip size, speed performance, and yield of all VLSI circuits [1]. The two key factors which affect the overall performance of today's VLSI circuits are the length and resistivity of the interconnect line[2]. This is evident by examining the expression for the RC time delay of an interconnect placed on a dielectric, shown in Equation (1):

$$RC = (\rho \times L^2 \times k)/t \qquad (1)$$

where rho is sheet resistivity, L is interconnect length, t is thickness of the interconnect, and k is dielectric constant of the interconnect. The use of multilevel metalization can drastically reduce the overall length of interconnect lines and therefore reduce the RC time delay. A single level metal would involve routing of metal traces through long stretches in order to make all connections without crossing paths.

This project developed a 4000 um by 4000 um multilevel metalization testchip. Each structure was designed with a specific purpose for analyzing a multilevel interconnect system.

The Interdigitated Meander shown in Figure 1 is merely a combination of a serpentine and two combs. The structure electrically detects opens or voids in conducting lines and shorts or bridging between the conducting lines. The leakage current is measured between the two sets of interdigitated fingers and the serpentine conductor to detect the existence of bridging. Measurements of the resistance of the serpentine are made to detect opens in the metal. To detect interlevel dielectric shorts, the test structure is fabricated over a first level metal and the voltage is applied between metal layers.

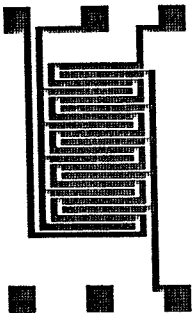


Figure 1: Interdigitated Meander

The Via Chain with a cross section, shown in Figure 2, is used to measure open contacts and via resistance. This is done by applying a voltage between the probe pads and measuring the current to determine if there is an open contact in the chain.

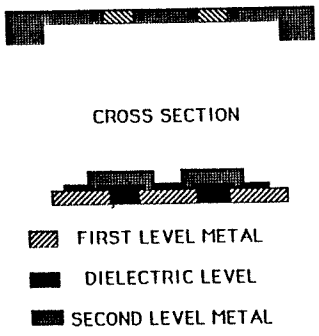
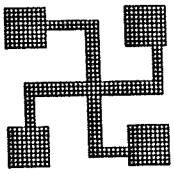


Figure 2: Via Chain

The Greek Cross, shown in Figure 3 is used to measure sheet resistance. A DC current is forced between two pads and the voltage is measured between the other two pads. The sheet resistance of the area where the two conducting lines intersect to form a cross can then be measured.

The next structure, shown in Figure 4, is the Contact Resistance Greek Cross. The Contact Resistance Greek Cross is used to measure the specific contact resistance of a single contact. This is done by the same procedure used to measure the sheet resistance with the Greek Cross. A DC current is forced between the two pads and the voltage is measured between the other two pads. The resistance is then calculated with this information using Ohm's law.



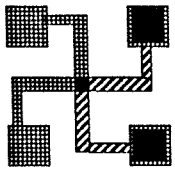


Figure 3:Greek Cross Figure 4:Contact Resistance Greek Cross

The Cross Bridge Sheet Resistor, shown in Figure 5 is a useful structure to measure linewidth of conducting layers. The sheet resistance is again obtained from the Greek Cross. The arm of the cross extending upward is tapped in two places constituting a bridge resistor. The resistance of this bridge may be determined by measuring the voltage between the taps when a known DC current is forced through the bridge. Given the sheet resistance of the bridge, the width of the bridge may be calculated. Both horizontal and vertical bridge widths are found using this structure.

The last structure which was designed is the Split Cross Bridge, shown in Figure 6. This structure is used to measure sheet resistance, linewidth, and linespace. The sheet resistance is determined from voltage and current measurements obtained from the Greek Cross built into the structure. Linewidth and linespace are determined from current and voltage measurements on the bridge structure.

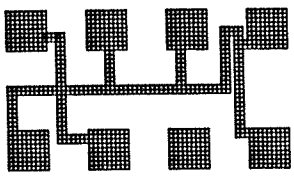


Figure 5: Cross Bridge Sheet Resistor

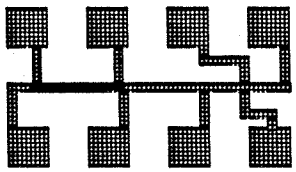


Figure 6: Split Cross Bridge

EXPERIMENT

After completing the needed research to determine the type of structures needed on the testchip, a circuit layout was designed using the Integrated Circuit Editor (ICE). ICE, an in-house CAD tool, is a program on the RIT VAX. The ICE editor was used to create a MAN files of the testchip. This MANN file was then used by the MANN 3000 Pattern Generator to create reticle of each layer of the testchip. The reticles were used by the Photorepeater to create a mask set of the multilevel metal testchip. Three layers are used in this testchip; they are metal one, metal two, and contact cuts. The metal one mask may also be used to pattern polysilicon.

Subsequent processing involved the use of ACCUGLASS 104, a spin on glass, which had previously been characterized at RIT [3]. The substrates used were three inch, (111), silicon wafers. Several wafers had about 1800 angstroms of oxide grown on them prior to aluminum deposition. Following a clean, aluminum was deposited using the evaporator to give a layer of about 2600 angstroms. The first level metal was then patterned using the created mask. The SOG was applied, cured, patterned using the designed contact cut mask, and etched. The second level metal was then deposited, patterned, and etched.

The critical steps of the above process are the SOG application, SOG cure, and SOG etching. Referring to past work done with ACCUGLASS 104, a spin speed of 2000 RPM for 20 seconds was used. This was done three times with a cure of ten minutes at 600 degrees C after the first and second spins. A cure of 60 minutes at 600 degrees C was done after the third and final spin. The SOG etching was completed in a 10:1 HF dip [3].

The last step in this experiment would consist of testing and making observations of the structures of the testchip by following the instructions described in the introduction.

RESULTS/DISCUSSION

The testchip layout can be found in the Appendix I and each cell plot is in Appendix II. Each cell is identified by a row and column number. The following list provides the location and identification of each structure. Processing of the multilevel metalization testchip stopped during the spin on of SOG. This project precludes the testing of the testchip structures. The testchip masks and testchip CIF file, can be located by contacting Mike Jackson at RIT.

Structure	Cell Position Row	Column
Contact Resistance Greek Cross with a 4 by 4 micron via.	1	1
Contact Resistance Greek Cross with a 2 by 2 micron via.	1	2
Contact Resistance Greek Cross with a 10 by 10 micron via.	2	1
Contact Resistance Greek Cross with a 6 by 6 micron via.	2	2
Greek Cross with 10 micron lines (metal one).	3	1
Greek Cross with 10 micron lines (metal one).	4	1
Greek Cross with 10 micron lines (metal two).	3	2
Greek Cross with 10 micron lines (metal two).	4	2
Cross Bridge with 10 micron lines (metal two).	5	1, 2
Cross Bridge with 30 micron lines (metal two).	6	1, 2
Cross Bridge with 10 micron lines and optical loading (metal two).	7	1, 2
Cross Bridge with 30 micron lines and optical loading (metal two).	8	1, 2
Split Cross Bridge with a 6 by 200 micron tap (metal two).	1	3, 4
Split Cross Bridge with a 10 by 200 micron tap (metal two).	2	3, 4
Split Cross Bridge with a 4 by 200 micron tap (metal two).	3	3, 4
Split Cross Bridge with a 2 by 200 micron tap (metal two).	4	3, 4
Split Cross Bridge with a 6 by 200 micron tap (metal one).	5	3, 4
Split Cross Bridge with a 10 by 200 micron tap (metal one).	6	3, 4

Cross Bridge with 10 micron lines (metal one).	7	3, 4
Cross Bridge with 30 micron lines (metal one).	8	3, 4
Via Chain with 4 by 4 micron vias.	1, 2, 3, 4	5
Via Chain with 2 by 2 micron vias.	1, 2, 3, 4	6
Via Chain with 10 by 10 micron vias.	5, 6, 7, 8	5
Via Chain with 6 by 6 micron vias.	5, 6, 7, 8	6
Interdigitated Meander with 10 micron lines and 10 micron spaces (metal two).	All	7
Interdigitated Meander with 10 micron lines and 5 micron spaces (metal two).	All	8
Interdigitated Meander with 10 micron lines and 10 micron spaces (metal two) on top of a 10 micron line and 10 micron space meander (metal one).	All	9
Interdigitated Meander with 10 micron lines and 5 micron spaces (metal two) on top of a 10 micron line and 10 micron space meander (metal one).	All	10

CONCLUSIONS

The testchip which was created will be of further use in the development of successful multilevel metalization at RIT.

ACKNOWLEDGEMENTS

I would like to thank Mike Jackson for his help throughout the project.

REFERENCES

[1] Saxena, A. N., Solid State Technology, Volume 27, p 93, 1984.

[2] Newcomb, Robert M., unpublished paper at Rochester Institute of Technology.

[3] Roberts, William., unpublished paper at Rochester Institute of Technology.

APPENDIX I:

TESTCHIP LAYOUT