# STANDARD CELL REALIZATION FOR THE MENTOR GRAPHICS CAD ENVIRONMENT

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## ABSTRACT

A common way of designing microelectronic circuits is by the use of standard cells. In advance systems the circuit can be read from a schematic diagram and the computer will select and place the cells and layout the signal paths automatically. In order to do so the computer needs a representation of these cells and a description of the routing design rules. The format and content of these descriptions were investigated for the Mentor Graphics IDEA system and a procedure for building libraries of standard cells was developed. The related data files were then developed to allow the creation of a library of standard cells for the RIT NMOS process.

## INTRODUCTION

Standard Cells are a method of Computer Aided Design where small, pre-designed subcircuits are selected from a library and connected together to produce layouts for microchips. This allows the designing of custom circuitry without the need to know the internals of the cells. The Mentor Graphics IDEA System, like the one on the Apollo computers in the CAE laboratory at RIT, has the ability to capture the design of a circuit from a schematic and do the placement and connection of the cells itself. However, the cells provided with the system are merely descriptions of the connection points with no internal transistor level layout. The Mentor Graphics System does provide utilities for building custom libraries when supplied with layouts for the cell and files containing associated data. A glossary of the terms used by the IDEA system is provided for reference.

The components involved in building a cell library are illustrated in Figure 1. The first part defines the over all rules for the chip. A file named CHIP.TDF, which is written in Mentor Graphics' Technology Definition Format (TDF) [1], must be constructed and placed in a directory where the library will eventually be kept. The CHIP.TDF file itself is made up of two sections, the RULES section, and the CHIP section. The RULES section is, as it sounds, concerned with the design rules of the technology. That is, it defines the size and spacing of the connecting wires and the size of the vias between routing layers.

It also contains data on the resistivity and capacitance of these wares and vias. The CHIP section lays out the "grid" on which the routing will be laid and defines the direction the routing on a plane will take. The CHIP.TDF file must be compiled with the TDFCHIPINPUT program generating the CADI.CHP file which is used by the CELLSTATION programs [2,3].

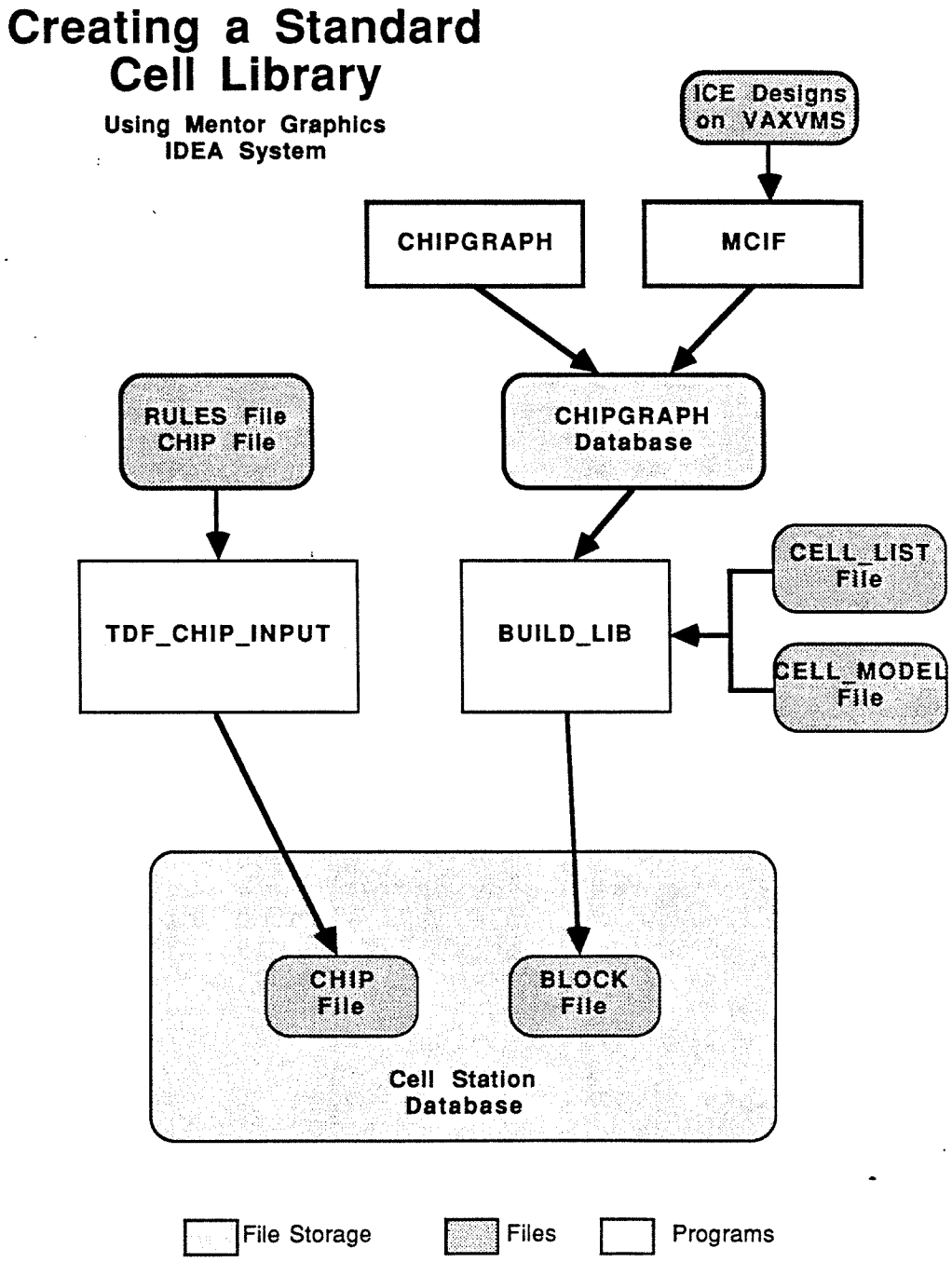


Figure 1: Elements of creating a Standard Cell Library

The other part to the library is the descriptions of the individual cells. These descriptions can be entered in two ways. The direct method is to write a data file in TDF and compile it using the TDFBLOCKINPUT program. This requires knowing the layout of the cells with respect to an origin point. The other method requires more set-up in the beginning but becomes simpler than the first method. It makes use of the BUILDLIB program that reads the geometric data of a standard cell drawn with the CHIPGRAPH program and generates the CADI.BLC file which is used by the CELLSTATION programs or a BLOCK.TDF file so that validation can be done. The BUILDLIB requires data on what to look for and where to look when defining signal and power pins. This is done with another TDF file called CELLMODEL which describes the assignment of graphics layer to routing level and the property names of the shapes to use as pins.

## LIBRARY DEVELOPMENT

To discover the requirements of the CELLSTATION software a ring oscillator, shown in Figure 2, was designed on the NETED schematic drawing program using the existing MOSIS CMOS standard cells. The design was analyzed with EXPANDCOMP and LOGICENTRY programs and then CELLFLOOR, CELLPLACE, and CELLPOWER were executed to create a chip floor plan, place the cells on the floor plan, and route the power, respectively. The design was then examined with CELLGRAPH and the CELLGRAPH batch signal routing option was used to make the signal connections as shown in Figure 3.

The next step was to make a prototype standard cell library. The CHIP.TDF file was adapted to be compatible with the design rules of the RIT NMOS process. A CELLMODEL file was also written that matched the existing definitions for the NMOS technology in CHIPGRAPH.

A CHIPGRAPH design of a NMOS inverter, shown in Figure 4, was used as an example. So that the BUILDLIB program could find and name the contact pins, CHIPGRAPH was used to attach properties to the appropriate boxes in the design.

The BUILDLIB program was run twice, once to build the library, again to generate a BLOCK.TDF file of the inverter. The TDF file was checked to see if BUILDLIB was interpreting the CHIPGRAPH design correctly.

For a more specific description of the parameters used in the TDF files and examples of the TDF files that were written, see the document "Building a Standard Cell Library" in appendix A.

## DISCUSSION

When the BLOCK.TDF file that was generated with BUILDLIB from the CHIPGRAPH design was compared to the initial design the file showed that all the pins were found and assigned to the correct place, but the direction (input or output) came up as "in" for all the pins. This is because the property PINTYPE was over looked when attaching properties to the pin shapes. This can be corrected in CHIPGRAPH on the design and BUILDLIB run again.

Even though it is now possible to build standard cell libraries like the one for NMOS, there is at present no way to access these cells. To do so symbols for each cell must be created with the SYMED design program and a menu choice made in NETED that will call these symbols. Some work has been done on this but it requires further investigation.

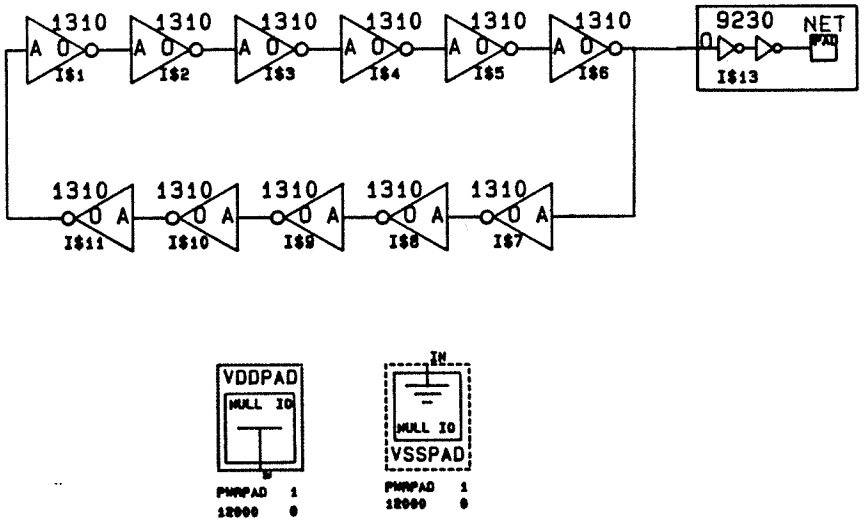


Figure 2: Schematic of Ring Ocilator in NETED

## CONCLUSION

Some standard cells have been designed on the Mentor Graphics System design tool CHIPGRAPH for the RIT NMOS process and it is hoped that others can be brought in from the ICE design tool on RIT's VAX VMS cluster. These designs must be checked to see that they have the proper attributes contained in them so that BUILDLIB can identify Io pins, power busses, and routing blockages.

When this project is completed both Microelectronic and Computer Engineering will have procedures and, as importantly, explanations of how to add to the NMOS library, as well as build new ones for other processes. It will also provide the ability to actually manufacture circuits designed with these cell in the fabrication facilities at RIT.

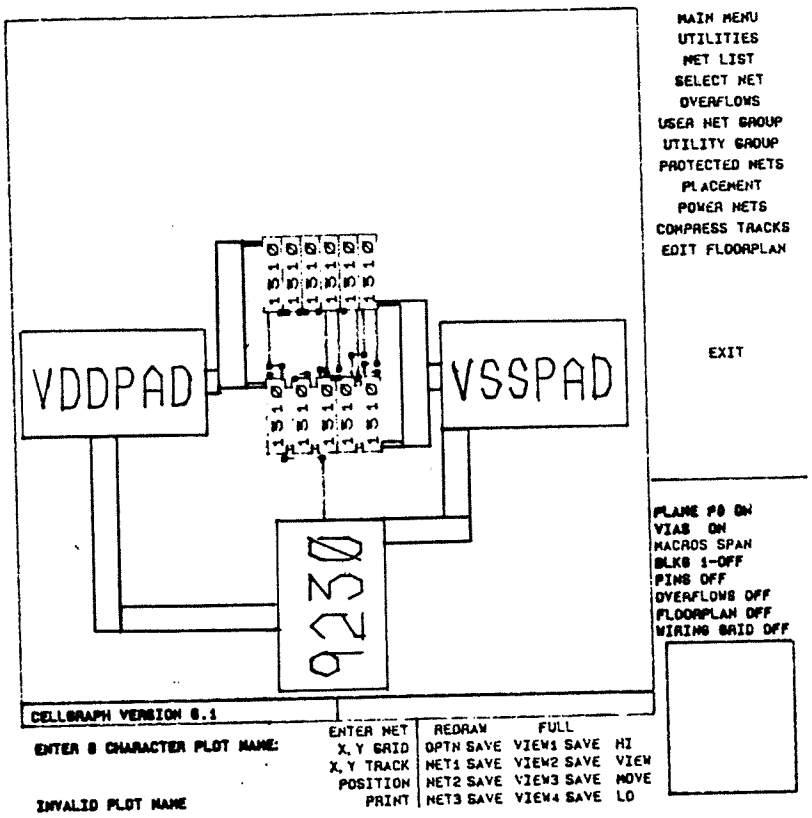


Figure 3: Ring Ocilator Chip in CELLGRAPH

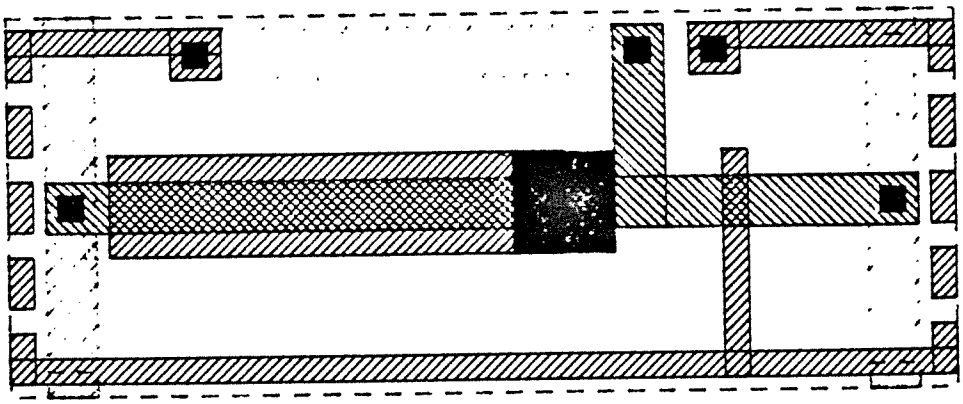

Figure 4: Design of Inverter Standard Cell in CHIPGRAPH

## ACKNOWLEDGMENTS

Thanks to Rob Pearson who directed me on this project and will have to find someone who will continue where I left off; to Shishir Ghate for help in getting the ball rolling; Dave Koeller for providing the CHIPGRAPH design of the inverter along with help in using CHIPGRAPH; and to Les, the lab assistant that had to field my repeated questions about the Apollos.

## REFERENCES

[1] Mentor Graphics, Technology Definition Format Manual software version 7.0 (March 1989), pp. 2-4 to 2-19

[2] Mentor Graphics, Cell Station User's Manual software version 6.1 (May 1988), pp. 4-84 to 4-96

[3] Mentor Graphics, Cell Station Reference Manual software version 6.1 (May 1988), pp. 2-46 to 2-61, pp. 5-11 to 5-30

## GLOSSARY

NETED: Schematic design utility for symbolic circuit layout.

CELLSTATION: Program for placement and routing of standard cells. Is able to place and route automatically from schematic designed in NETED, drawing on specific standard cell libraries.

CHIPGRAPH: Used to layout the physical geometries of a chip. (i.e. diffusions, poly, metal)

BUILDLIB: Translates physical designs from CHIPGRAPH into form used by CELLSTATION and groups these into libraries.

TDFCHIPINPUT: Compiles RULES and CHIP information into the cell library for use by CELLSTATION.

CHIP.TDF file: Data file in Technology Definition Format (TDF) containing RULE and CHIP data used by TDFCHIPINPUT to determine routing size, level, and direction.

BLOCK.TDF file: Data file in Technology Definition Format (TDF) containing MACRO definitions of the standard cells.

CELLMODEL file: Used by BUILDLIB to define how to determine power and signal pins in a physical design from CHIPGRAPH.